General Description

The MAX705-MAX708/MAX813L microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX705/MAX706/MAX813L provide four functions:

1)A reset output during power-up, power-down, and brownout conditions.

2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.

3)A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.

4) An active-low manual-reset input.

The MAX707/MAX708 are the same as the MAX705/MAX706, except an active-high reset is substituted for the watchdog timer. The MAX813L is the same as the MAX705, except RESET is provided instead of RESET.

Two supply-voltage monitor levels are available: The MAX705/MAX707/MAX813L generate a reset pulse when the supply voltage drops below 4.65V, while the MAX706/MAX708 generate a reset pulse below 4.40V. All four parts are available in 8-pin DIP, SO and µMAX packages.

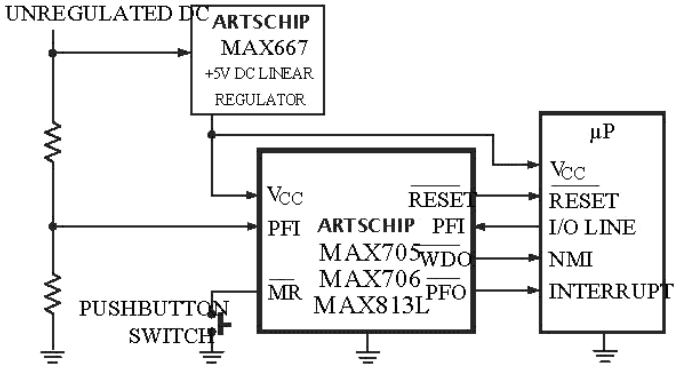
Applications

- Computers
- Controllers
- Intelligent Istruments
- Automotive Systems
- Critical µP Power Monitoring

Features

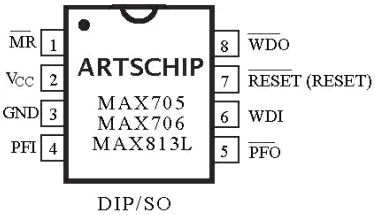
- µMAX Package: Smallest 8-Pin SO
- Guaranteed RESET Valid at Vcc=1V
- Precision Supply-Voltage Monitor
  4.65V in MAX705/MAX707/MAX813L
  4.40V in MAX706/MAX708
- 200ms Reset Pulse Width
- Debounced TTL/CMOS-Compatible Manual-Reset Input
- Independent Watchdog Timer – 1.6sec Timeout (MAX705/MAX706)
- Active-high Reset Output (MAX707/MAX708/MAX813L)
- Voltage Monitor for Power-Fail or Low-Battery Warning

Typical Operating Circuit

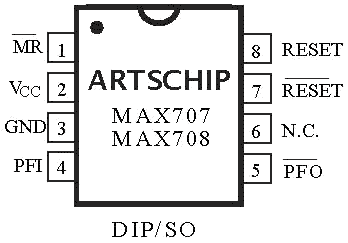


Pin Configurations

TOP VIEW



DIP/SO



DIP/SO

()ARE FOR MAX813L ONLY.

Pin Configurations continued at end of data sheet.

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX705CPA	0°C to +70°C	8 Plastic DIP
MAX705CSA	0°C to +70°C	8 SO
MAX705CUA	0°C to +70°C	8µMAX
MAX705C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

*Dice are specified at T_A=+25°C.

**Contact factory for availability and processing to MIL-STD-883.

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
Vcc……..-0.3V to 6.0V
All Other Inputs (Note 1)……-0.3V to (Vcc+0.3V)
Input Current
Vcc……20mA
GND……...20mA
Output Current (all outputs)……20mA
Continuous Power Dissipation
Plastic DIP (derate 9.09 mW/°C above +70°C)…727mW
SO (derate 5.88mW/°C above +70°C)……471mW
µMAX (derate 4.10mW/°C above +70°C)……..…..330mW
CERDIP (derate 8.00mW/°C above +70°C)……640mW

Operating Temperature Ranges

MAX70_C_, MAX813LC_.....0°C to +70°C
MAX70_E_, MAX813LE_……..……..-40°C to +85°C
MAX70_MJA……..……-55°C to +125°C
Storage Temperature Range……-65°C to +160°C
Lead Temperature (soldering, 10sec)…….……+300°C

Note 1: The input voltage limits on PFI and MR can be exceeded if the input current is less than 10mA.
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

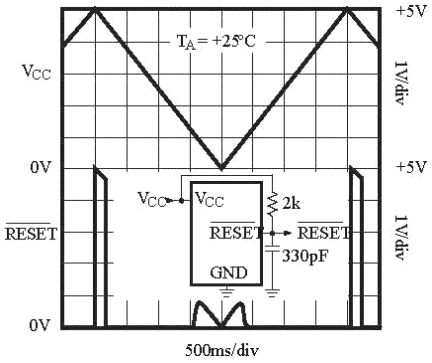
(Vcc=4.75V to 5.5V for MAX705/MAX707/MAX813L, Vcc=4.5V to 5.5V for MAX706/MAX708, T_A=T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	Vcc	MAX70_C	1.0		5.5	V
		MAX813LC	1.1		5.5	
		MAX70_E/M,MAX813LE/M	1.2		5.5	
Supply Current	I_{SUPPLY}	MAX705C,MAX706C,MAX813LC		150	350	µA
		MAX705E/M,MAX706E/M,MAX813LE/M		150	500	
		MAX707C,MAX708C		50	350	
		MAX707E/M,MAX708E/M		50	500	
Reset Threshold (Note 2)	V_{RT}	MAX705,MAX707,MAX813L	4.50	4.65	4.75	V
		MAX706,MAX708	4.25	4.40	4.50	
Reset Threshold Hysteresis (Note2)				40		mV
Reset Pulse Width (Note 2)	t_{RS}		140	200	280	ms
RESET Output Voltage		I_{SOURCE} =800µA	Vcc-1.5			V
		I_{SINK}=3.2mA			0.4	
		MAX70_C, Vcc=1V, I_{SINK}=50µA			0.3	
		MAX70_E/M, Vcc=1.2V, I_{SINK}=100µA			0.3	
RESET Output Voltage		MAX707, MAX708,I_{SOURCE}=800µA	Vcc-1.5			V
		MAX707,MAX708,I_{SINK}=1.2mA			0.4	
		MAX813LC, I_{SOURCE}=4µA, Vcc=1.1V	0.8			
		MAX813LE/M, I_{SOURCE}=4µA, Vcc=1.2V	0.9			
		MAX813L I_{SOURCE}=800µA	Vcc-1.5			
		MAX813L I_{SINK}=3.2mA			0.4	
Watchdog Timeout Period	t_{WD}	MAX705, MAX706,MAX813L	1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	VIL=0.4V, VIH – (Vcc)(0.8)	50			ns
WDI Input Threshold Low		MAX705, MAX706, MAX813L, Vcc=5V			0.8	V
WDI Input Threshold High			3.5			
WDI Input Current		MAX705, MAX706,MAX813L ,WDI=Vcc		50	150	µA
		MAX705, MAX706,MAX813L,WDI=0V	-150	-50		
WDO Output Voltage		MAX705,MAX706,MAX813L, I_{SOURCE}=800µA	Vcc-1.5			V
		MAX705,MAX706,MAX813L, I_{SINK}=1.2mA			0.4	
MR Pull-Up Current		MR=0V	100	250	600	µA
MR Pulse Width	t_{MR}		150			ns
MR Input Threshold Low					0.8	V
MR Input Threshold High			2.0			
MR to Reset Out Delay (Note 2)	t_{MD}				250	ns
PFI Input Threshold		Vcc=5V	1.20	1.25	1.30	V
PFI Input Current			-25.00	0.01	25.00	nA
PFO Output Voltage		I_{SOURCE} =800µA	Vcc-1.5			V
		I_{SINK}=3.2mA			0.4	

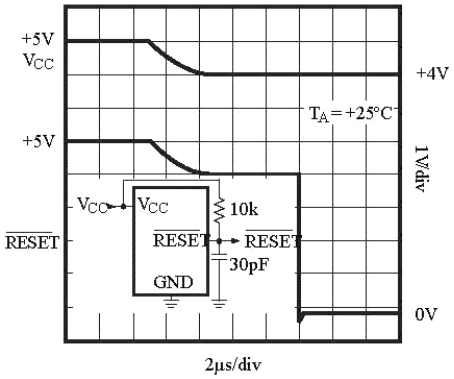
Note 2: Applies to both RESET in the MAX705-MAX708 and RESET in the MAX707/MAX708/MAX813L.

Typical Operating Characteristics

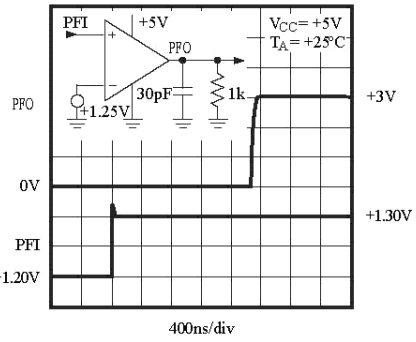
MAX705/MAX707
$\overline{RESET}$ OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



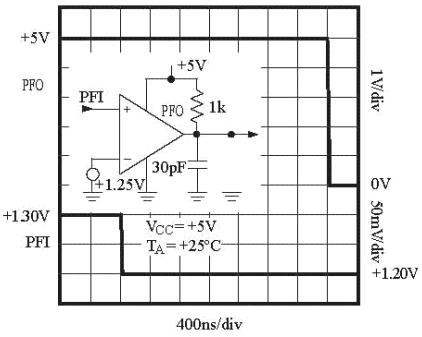
MAX705/MAX707
$\overline{RESET}$ RESPONSE TIME



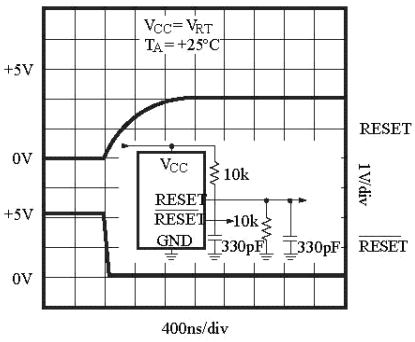
POWER-FAIL COMPARATOR
DE-ASSERTION RESPONSE TIME



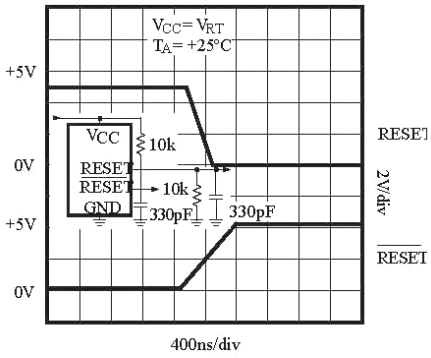
POWER-FAIL COMPARATOR
ASSERTION RESPONSE TIME



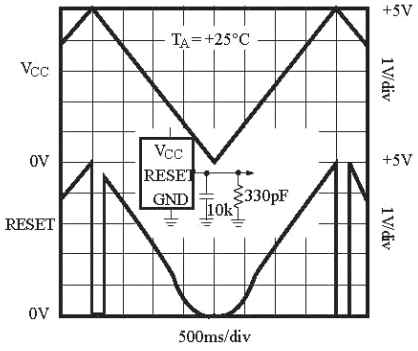
MAX707
RESET, $\overline{RESET}$ ASSERTION



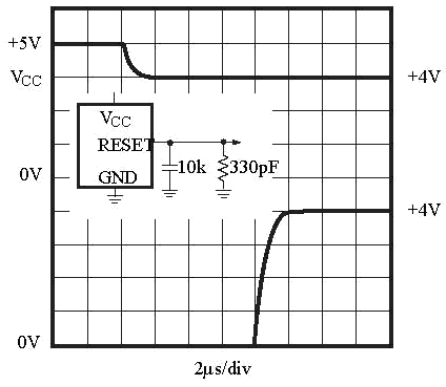
MAX707
RESET, $\overline{RESET}$ DE-ASSERTION



MAX707/MAX708/MAX813L
RESET OUTPUT VOLTAGE
Vs. SUPPLY VOLTAGE



MAX813L
RESET RESPONSE TIME



Pin Description

PIN						NAME	FUNCTION
MAX705/MAX706		MAX707/MAX708		MAX813L			
DIP/SO	µMAX	DIP/SO	µMAX	DIP/SO	µMAX		
1	3	1	3	1	3	MR	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250µA pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	4	2	4	2	4	Vcc	+5V Supply Input
3	5	3	5	3	5	GND	0V Ground Reference for all signals
4	6	4	6	4	6	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or Vcc when not nsed.
5	7	5	7	5	7	PFO	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise PFO stays high.
6	8	-	-	6	8	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three stated, or WDI sees a rising or falling edge.
-	-	6	-	-	-	N.C.	No Connect
7	1	7	1	-	-	RESET	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever Vcc is below the reset threshold (4.65V in the MAX705 and 4.40 V in the MAX706). It remains low for 200ms after Vcc rises above the reset threshold or MR goes from low to high (Figure 3). A watchdog timeout will not trigger RESET unless WDO is connected to MR.
8	2	-	-	8	2	WDO	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. WDO also goes low during low-line conditions. Whenever Vcc is below the reset threshold, WDO stays low; however, unlike RESET, WDO does not have a minimum pulse width. As soon as Vcc rise above the reset threshold, WDO goes high with no delay.
-	-	8	2	7	1	RESET	Active-High Reset Output is the inverse of RESET. Whenever RESET is high, RESET is low, and vice versa (Figure 2). The MAX813L has a RESET output only.

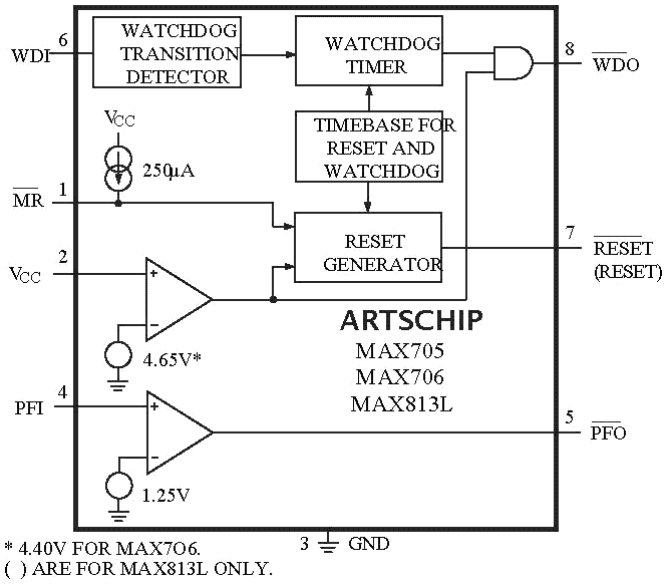


Figure 1. MAX705/MAX706/MAX813L Block Diagram

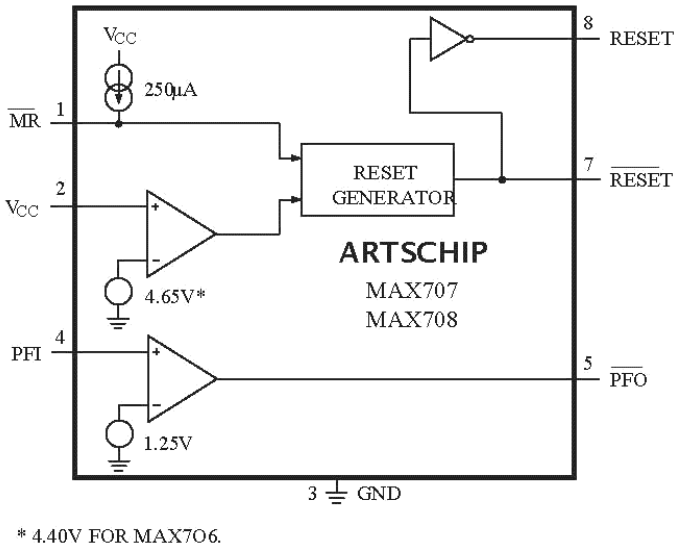


Figure 2. MAX707/MAX708 Block Diagram

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state, whenever the µP is in an unknown state. it should be held in reset. The MAX705-MAX708/MAX813L assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once Vcc reaches 1V, RESET is a guaranteed logic low of 0.4V or less. AS Vcc rises, RESET stays low. When Vcc rises above the reset threshold, an internal timer releases RESET after about 200ms. RESET pulses low whenever Vcc dips below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, Once Vcc falls below the reset threshold, RESET stays low and is guaranteed to be 0.4V or less until Vcc drops below 1V.

The MAX707/MAX708/MAX813L active-high RESET output is simply the complement of the RESET output, and is guaranteed to be valid with Vcc down to 1.1V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The MAX705/MAX706/MAX813L watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not three-stated, WDO goes low. As long as RESET is asserted or the WDI input is three-stated, the watchdog time will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulse as short as 50ns can be detected.

Typically, WDO will be connected to the non-maskable interrupt input (NMI) of a µP. When Vcc drops below the reset threshold, WDO will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but RESET goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, WDO can be used as a low line output. Since floating WDI disables the internal timer, WDO goes low only when Vcc falls below the reset threshold, thus functioning as a low-line output.

The MAX705/MAX706 have a watchdog timer and a RESET output. The MAX707/MAX708 have both active high and active-low reset outputs. The MAX813L has both an active-high reset output and a watchdog timer.

Manual Reset

The manual-reset input (MR) allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. MR is TTL/CMOS logic compatible, so it can be driven by an external logic line. MR can be used to force a watchdog timeout to generate a reset pulse in the MAX705/MAX706/MAX813L. Simply connect WDO to MR.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

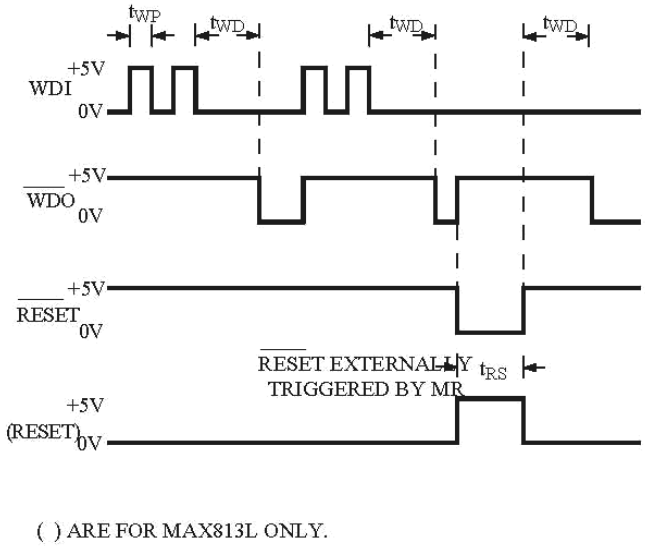


Figure 3. MAX705/MAX706/MAX813L Watchdog Timing.

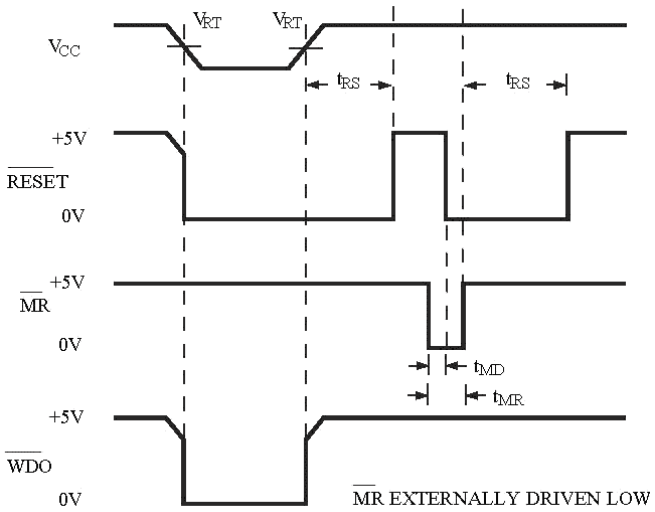


Figure 4. MAX705/MAX706 RESET, MR, and WDO Timing with WDI Three-Stated. The MAX707/MAX708/MAX813L RESET output is the inverse of RESET shown.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see Typical Operating Circuit). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

Applications Information

Ensuring a Valid RESET

Output Down to Vcc=0V When Vcc falls below 1V, the MAX705-MAX708 RESET output no longer sinks current – it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R1) is not critical. It should be about 100KΩ, large enough not to load RESET and small enough to pull RESET to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sun of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on other voltages in addition to the +5V Vcc line. Connect PFO to MR to initiate a RESET pulse when PFI drops below 1.25V. Figure 6 shows the MAX705-MAX708S configured to assert RESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), PFO is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers reset. As long as PFO remains high, the MAX705-MAX708/MAX813L will keep reset asserted (RESET=low, RESET =high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the Vcc line, and the resistors.

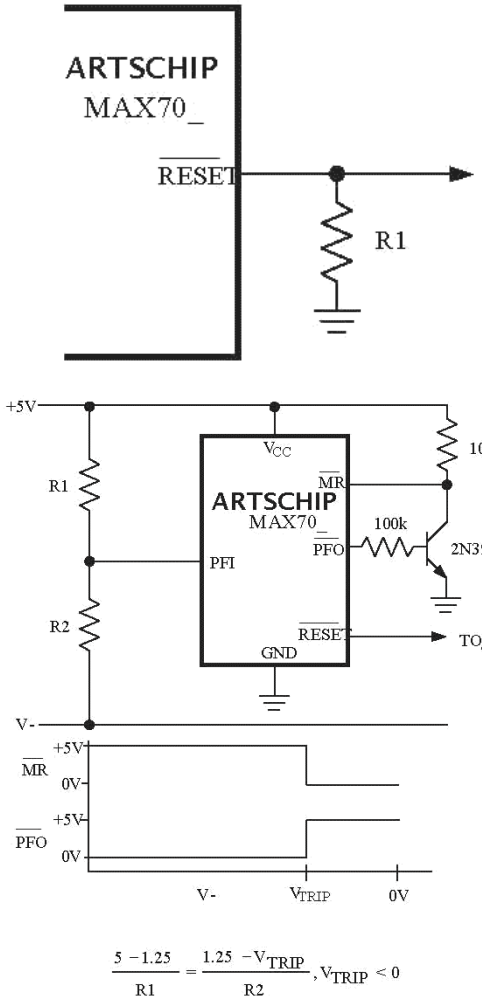
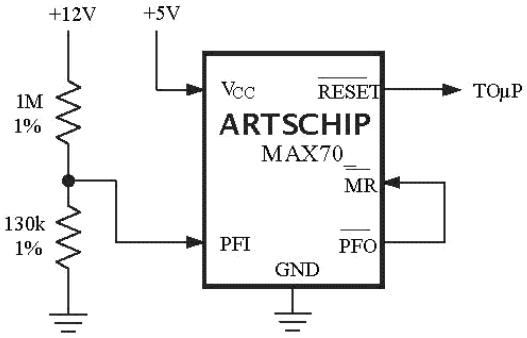


Figure 7. Monitoring a Negative Voltage



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25 °C	10.67	10.87	11.50	V

Figure 6. Monitoring Both +5V and +12V

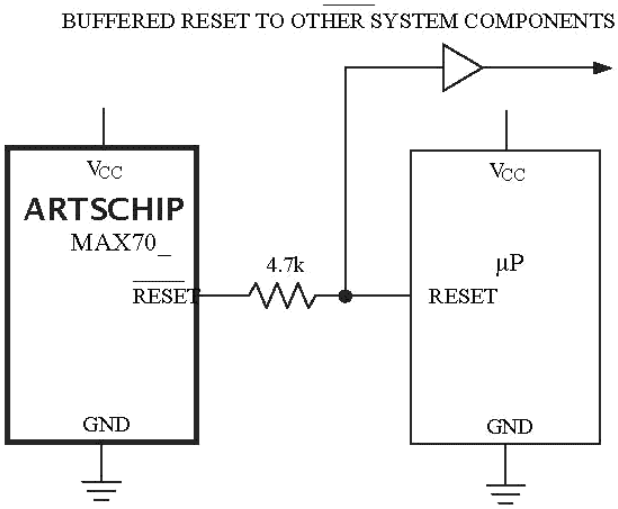


Figure 8. Interfacing to µPs with Bidirectional Reset I/O

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX705-MAX708 RESET output. If, for example, the RESET output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O, as in Figure 8. Buffer the RESET output to other system components.

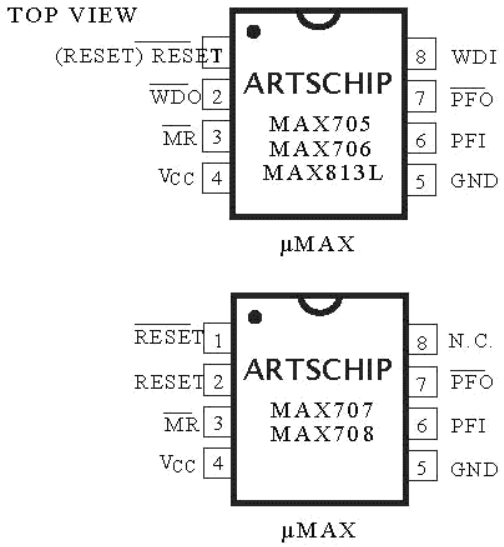
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX705EPA	-40°C to +85°C	8 Plastic DIP
MAX705ESA	-40°C to +85°C	8 SO
MAX705EUA	-40°C to +85°C	8 µMAX
MAX705MJA	-55°C to +125°C	8 CERDIP**
MAX706CPA	0°C to +70°C	8 Plastic DIP
MAX706CSA	0°C to +70°C	8 SO
MAX706CUA	0°C to +70°C	8 µMAX
MAX706C/D	0°C to +70°C	Dice *
MAX706EPA	-40°C to +85°C	8 Plastic DIP
MAX706ESA	-40°C to +85°C	8 SO
MAX706EUA	-40°C to +85°C	8 µMAX
MAX706MJA	-55°C to +125°C	8 CERDIP**
MAX707CPA	0°C to +70°C	8 Plastic DIP
MAX707CSA	0°C to +70°C	8 SO
MAX707CUA	0°C to +70°C	8 µMAX
MAX707C/D	0°C to +70°C	Dice *
MAX707EPA	-40°C to +85°C	8 Plastic DIP
MAX707ESA	-40°C to +85°C	8 SO
MAX707EUA	-40°C to +85°C	8 µMAX
MAX707MJA	-55°C to +125°C	8 CERDIP**
MAX708CPA	0°C to +70°C	8 Plastic DIP
MAX708CSA	0°C to +70°C	8 SO
MAX708CUA	0°C to +70°C	8 µMAX
MAX708C/D	0°C to +70°C	Dice*
MAX708EPA	-40°C to +85°C	8 Plastic DIP
MAX708ESA	-40°C to +85°C	8 SO
MAX708EUA	-40°C to +85°C	8 µMAX
MAX708MJA	-55°C to +125°C	8 CERDIP**
MAX813LCPA	0°C to +70°C	8 Plastic DIP
MAX813LCSA	0°C to +70°C	8 SO
MAX813LCUA	0°C to +70°C	8 µMAX
MAX813LC/D	0°C to +70°C	Dice*
MAX813LEPA	-40°C to +85°C	8 Plastic DIP
MAX813LESA	-40°C to +85°C	8 SO
MAX813LMUA	-40°C to +85°C	8 µMAX
MAX813LMJA	-55°C to +125°C	8 CERDIP**

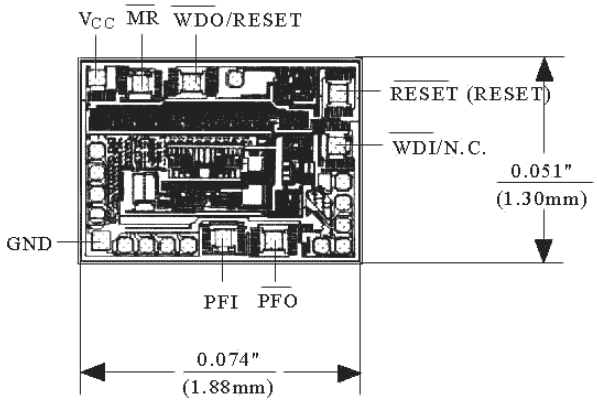
*Dice are specified at TA=+25°C.

**Contact factory for availability and processing to MIL-STD-883.

Pin Configuration (continued)



Chip Topography

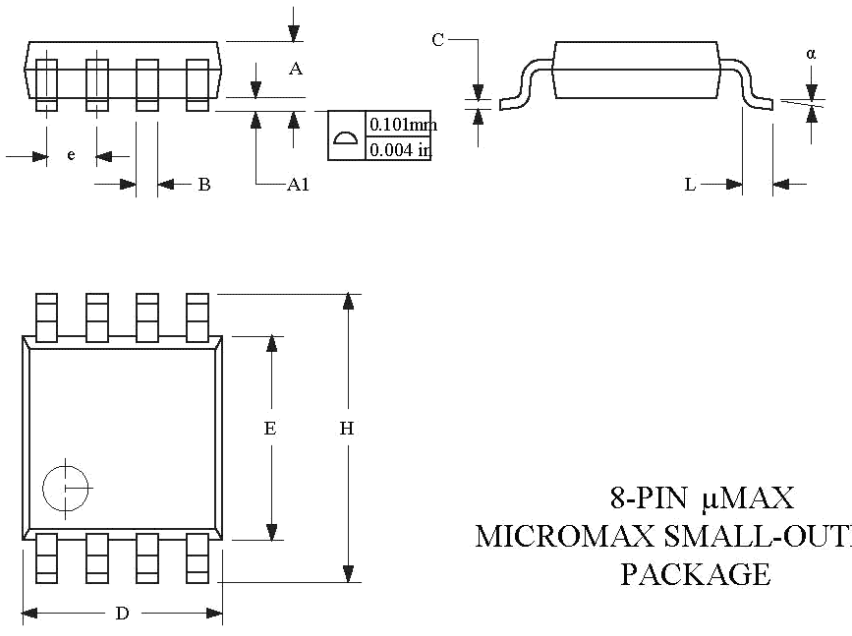


()ARE FOR MAX813L ONLY.

TRANSISTOR COUNT: 572

SUBSTRATE MUST BE LEFT UNCONNECTED.

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

21-0036D

8-PIN µMAX
MICROMAX SMALL-OUTLINE
PACKAGE