

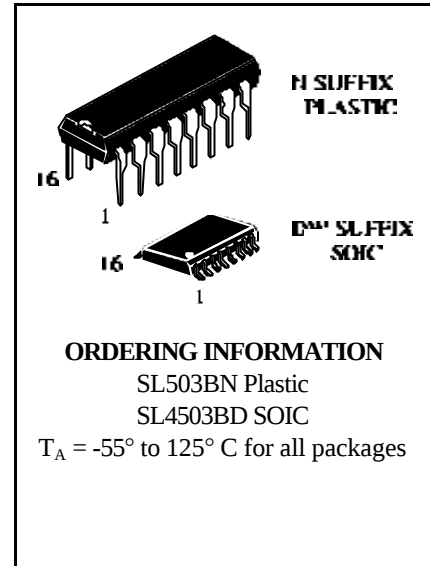
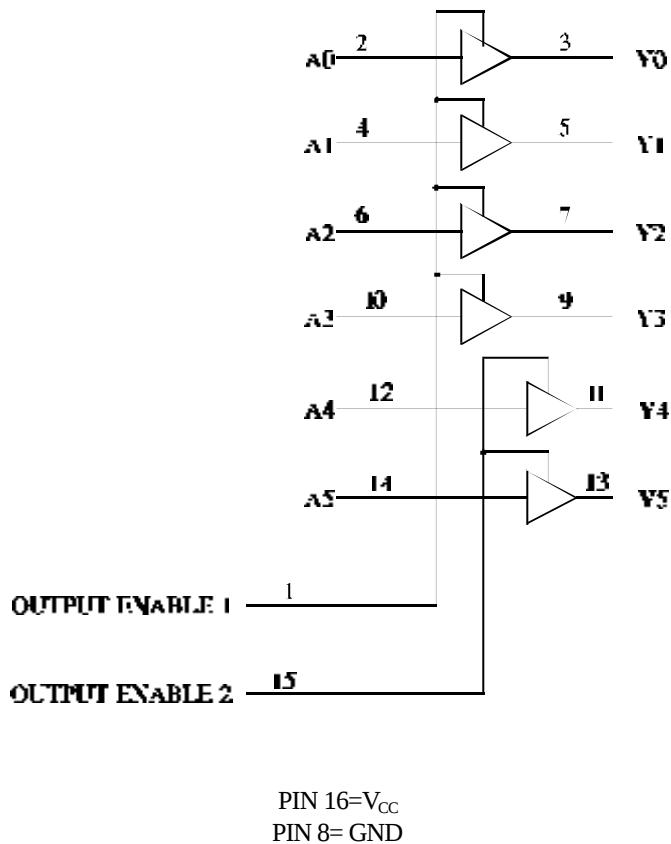
Hex Buffer

High-Voltage Silicon-Gate CMOS

The SL4503B is a hex noninverting buffer with 3state outputs having high sink- and source-current capability. Two output ENABLE controls are provided, one of which controls four buffers and the other controls the remaining two buffers.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 - 1.0 V min @ 5.0 V supply
 - 2.0 V min @ 10.0 V supply
 - 2.5 V min @ 15.0 V supply

LOGIC DIAGRAM



PIN ASSIGNMENT

OUTPUT ENABLE 1	1	16	V _{CC}
A0	2	15	OUTPUT ENABLE 2
Y0	3	14	A5
A1	4	13	Y5
Y1	5	12	A4
A2	6	11	Y4
Y2	7	10	A3
GND	8	9	Y3

FUNCTION TABLE

Inputs		Output
Enable 1, Enable 2	A	Y
L	L	L
L	H	H
H	X	Z

Z = high impedance
X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.



DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = V _{CC} - 0.5V V _{OUT} = V _{CC} - 1.0 V V _{OUT} = V _{CC} - 1.5V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low -Level Input Voltage	V _{OUT} =0.5 V V _{OUT} =1 V V _{OUT} =1.5	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} U _{OL} =0.4 V U _{OL} =0.5 V U _{OL} =1.5 V	5.0	2.6	2.1	1.3	mA
			10	6.5	5.5	3.8	
			15	19.2	16.1	11.2	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} U _{OH} =2.5 V U _{OH} =4.6 V U _{OH} =9.5 V U _{OH} =13.5 V	5.0	-1.2	-1.02	-0.7	mA
			5.0	-5.8	-4.8	-3	
			10	-3.1	-2.6	-1.8	
			15	-8.2	-6.8	-4.8	
I _{OZ}	Maximum Tree-State Leakage Current	Output in High-Impedance State V _{IN} = GND or V _{CC} V _{OUT} = GND or V _{CC}	18	±0.4	±0.4	±12	μA

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, $R_L=200\text{k}\Omega$ unless otherwise specified, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$\geq -55^\circ\text{C}$	25°C	$\leq 125^\circ\text{C}$	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5.0	150	150	300	ns
		10	70	70	140	
		15	50	50	100	
t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figure 1)	5.0	110	110	220	ns
		10	50	50	100	
		15	35	35	70	
t_{PHZ} , t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) $R_L = 1\text{ k}\Omega$	5.0	140	140	280	ns
		10	60	60	120	
		15	50	50	100	
t_{PZL} , t_{PLZ}	Maximum Propagation Delay, Output Enable to Output Y (Figure 2) $R_L = 1\text{ k}\Omega$	5.0	180	180	360	ns
		10	80	80	160	
		15	70	70	140	
t_{TLH}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	90	90	180	ns
		10	45	45	90	
		15	35	35	70	
t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	70	70	140	ns
		10	40	40	80	
		15	25	25	50	
C_{IN}	Maximum Input Capacitance	-		7.5		pF
C_{OUT}	Maximum Tree-State Output Capacitance (Output in High-Impedance State)	-		15		pF

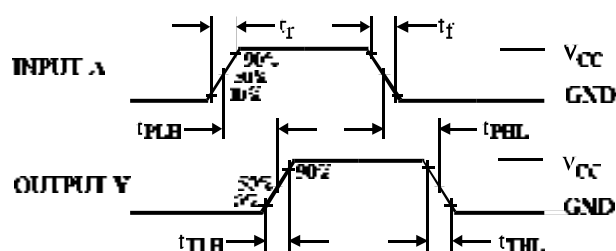


Figure 1. Switching Waveforms

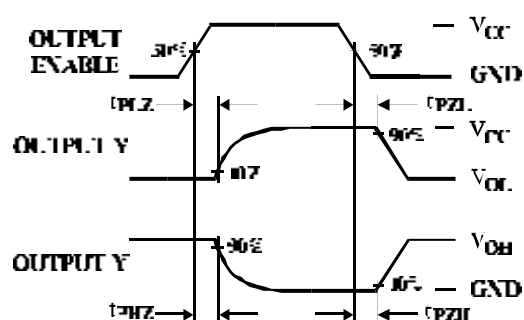


Figure 2. Switching Waveforms



EXPANDED LOGIC DIAGRAM (1/6 of the Device)

