Texas Instruments

TMP1075 Temperature Sensor With I²C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout

1 Features

- Accuracy:
  - ±1.5°C (Maximum) From −25°C to +100°C
  - ±2°C (Maximum) From −55°C to +125°C
- Low Power Consumption:
  - 2.7-µA Average Current
  - 0.37-µA Shutdown Current
- Wide Supply Range: 1.7 V to 5.5 V
- Temperature Independent of Supply
- Digital Interface: SMBus, I²C
- Can Coexist in I³C Mixed Fast Mode Bus
- Resolution: 12 Bits
- Supports up to 32 Device Addresses
- Alert Pin Function
- NIST Traceability

2 Applications

- Power-Supply Temperature Monitoring
- Computer Peripheral Thermal Protection
- Notebook Computers
- Cell Phones
- Battery Management
- Office Machines
- Thermostat Controls
- Environmental Monitoring and HVAC
- Electro Mechanical Device Temperature

3 Description

The TMP1075 is a lower power, higher accuracy replacement to the industry standard LM75 and TMP75 digital temperature sensors. Available in SOIC-8 and VSSOP-8 packages, the TMP1075 offers pin to pin and software compatibility to quickly upgrade any existing xx75 design. An additional new package with the TMP1075 is 2x2 mm DFN reducing the PCB footprint by 79% compared to an SOIC package.

The TMP1075 provides 30% improvement in accuracy over standard xx75 temperature sensors and offers an on-chip 12-bit analog-to-digital converter (ADC) providing a temperature resolution of 0.0625°C.

Compatible with two-wire SMBus and I²C interfaces, the TMP1075 supports up to 32 devices address and provides SMBus Reset and Alert function.

The TMP1075 devices are ideal for temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP1075 devices are specified for operation over a temperature range of −55°C to +125°C.

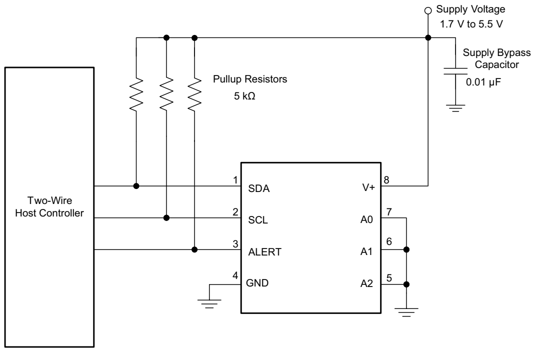
The TMP1075 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards.

Device Information(1)

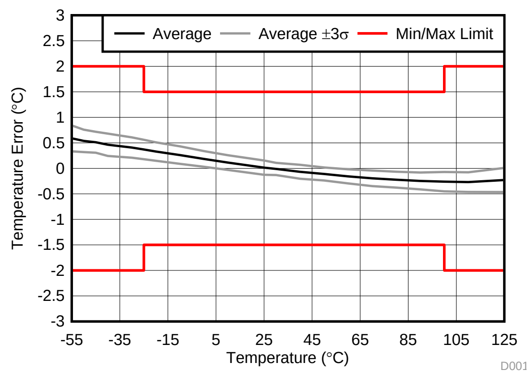
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP1075	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8) (preview)	4.90 mm × 3.91 mm
	DFN (8) (preview)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Temperature Accuracy



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4 Revision History

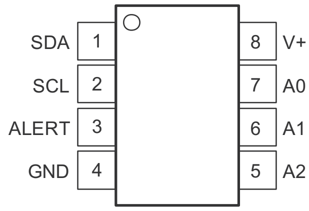
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2018) to Revision A **Page**

- Changed the TMP1075DGK orderable status from Advanced Information to Production Data ... 1
- Added SOIC and DFN packages ... 1
- Added the *Typical Characteristics* section ... 6
- Changed the *Functional Block Diagram* ... 9
- Changed *Digital Temperature Output* crossreference from: *Temperature Register (0x00)* to: *Temperature Data Format* . 10
- Changed the *Temperature Data Format* table ... 10
- Changed and renamed the *Address Pins and Slave Addresses for the TMP1075* table to *Address Pins State* ... 11
- Changed the *Two-Wire Timing Diagrams* section ... 13
- Added content to the *Device Functional Modes* section ... 15

5 Pin Configuration and Functions

DGK, D, and DSG Packages
8-Pin VSSOP, SOIC, and DFN
Top View



NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serial data. Open-drain output that requires a pullup resistor
2	SCL	I	Serial clock
3	ALERT	O	Overtemperature alert; Open-drain output that requires a pullup resistor
4	GND	—	Ground
5	A2	I	Address select A2: Connect to GND or V+
6	A1	I	Address select A1: Connect to GND, V+, SDA, or SCL
7	A0	I	Address select A0: Connect to GND, V+, SDA, or SCL
8	V+	I	Supply voltage, 1.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply, V+		6	V
Input voltage SCL, SDA, A1, A0	–0.3	6	V
Input voltage A2 pin	–0.3	(V+) + 0.3	V
Operating temperature	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.7		5.5	V
Operating free-air temperature, T_A	–55		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP1075 DGK (VSSOP) 8 PINS	TMP1075 D (SOIC) 8 PINS	TMP1075 DSG (DFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.5	130.4	87.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82	76.9	111.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	124.4	72.3	54	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.9	32	9.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	122.6	71.9	54.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	28.1	°C/W
M_T	Thermal mass	16.6	64.2	5.0	J/°C

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A = −55°C to +125°C and V+ = 1.7 V to 5.5 V (unless noted); typical specification are at T_A = 25°C and V+=3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–55		125	°C
	Accuracy (temperature error)	−25°C to +100°C		±0.5	±1.5	°C
		−55°C to +125°C		±1	±2	
	Accuracy (temperature error) vs supply	PSRR			±0.03	°C/V
	Resolution	1 LSB (12 bit)		0.0625		°C
	Repeatability[(1)]	25°C, V+= 3.3 V[(2)]		0.0625		°C
	Long-term drift[(3)]	300 hours at 150°C, 5.5V		0.0625		°C
DIGITAL INPUT/OUTPUT						
	Input capacitance			5		pF
V_{IH}	High-level input logic		0.8(V+)			V
V_{IL}	Low-level input logic				0.2(V+)	V
I_{IN}	Leakage input current		-0.25	0	0.25	µA
	Input voltage hysteresis	SCL and SDA pins		600		mV
V_{OL}	Low-level output logic	I_{OL} = -3 mA, SDA and ALERT pins	0	0.15	0.4	V
	ADC Conversion time	one-shot mode	4.5	5.5	7	ms
T_C	Conversion Time	CR1 = 0, CR0 = 0 (default)		27.5		ms
		CR1 = 0, CR0 = 1		55		
		CR1 = 1, CR0 = 0		110		
		CR1 = 1, CR0 = 1		220		
	Reset time	The time between reset till ADC conversion start		0.3		ms
	Conversion Rate Variation		-10	0	10	%
POWER SUPPLY						
	Operating voltage range		1.7	3.3	5.5	V
I_Q	Quiescent current (serial bus inactive)	CR1 = 0, CR0 = 0 (default)		10	20	µA
		CR1 = 0, CR0 = 1		5.5	9	µA
		CR1 = 1, CR0 = 0		4	6	
		CR1 = 1, CR0 = 1		2.7	4	
		During 5.5 ms active conversion		52	85	µA
I_{SD}	Shutdown current	Serial bus active, SCL frequency = 400 kHz, A0=A1=A2=GND		13		µA
		Serial bus inactive, A0=A1=A2=SCL=SDA=V+, 25°C		0.37	0.65	µA
		Serial bus inactive, A0=A1=A2=SCL=SDA=V+		0.37	3.5	µA
	Power supply thresholds	Supply rising, Power-on Reset		1.22		V
		Supply failing, Brown-out Detect		1.1		

(1) Repeatability is the ability to reproduce a reading when the measured temperature is applied consecutively, under the same conditions.
(2) One-shot mode setup, 1 sample per minute for 24 hours.
(3) Long-term drift is determined using accelerated operational life testing at a junction temperature of 150°C.

6.6 Timing Requirements

minimum and maximum specifications are over –55°C to 125°C and V+ = 1.7 V to 5.5 V (unless otherwise noted)(1)

		FAST MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time	600		160		ns
$t_{(SUSTO)}$	STOP condition setup time	600		160		ns
$t_{(HDDAT)}$	Data hold time(2)	0		0	130	ns
$t_{(SUDAT)}$	Data setup time	100		20		ns
$t_{(LOW)}$	SCL clock low period	1300		250		ns
$t_{(HIGH)}$	SCL clock high period	600		60		ns
$t_{(VDAT)}$	Data valid time (data response time)(3)		900		130	ns
t_{FDA}	Data fall time		300		100	ns
t_R	Clock rise time		300		40	ns
t_F	Clock fall time		300		40	ns
$t_{timeout}$	Timeout (SCL = SDA = GND)	20	30	20	30	ms
t_{RC}	Clock/ data rise time for SCL = 100 kHz		1000			ns

(1) The host and device have the same V+ value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.
(3) $t_{(VDAT)}$ = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse). = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{LPF}	Spike filter for I^3C compatibility	SCL= 12.5 MHz		50		ns

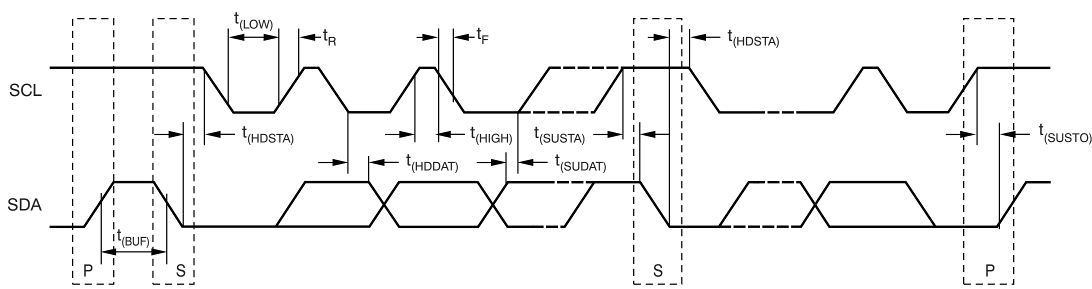


Figure 1. Two-Wire Timing Diagram

6.8 Typical Characteristics

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)

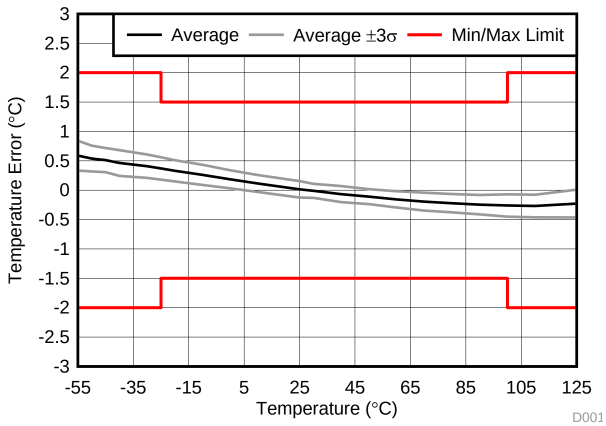


Figure 2. Temperature Error vs Temperature

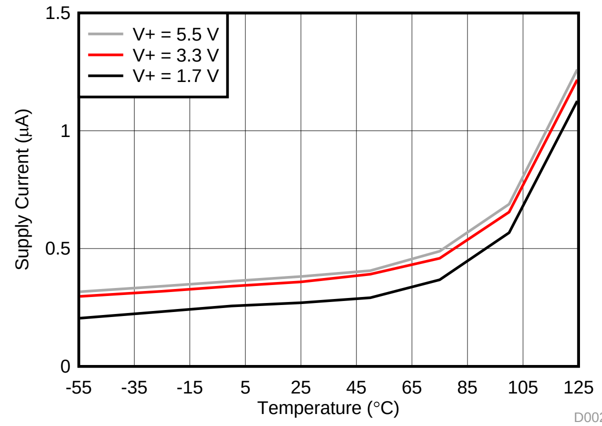


Figure 3. Shutdown Current vs Temperature

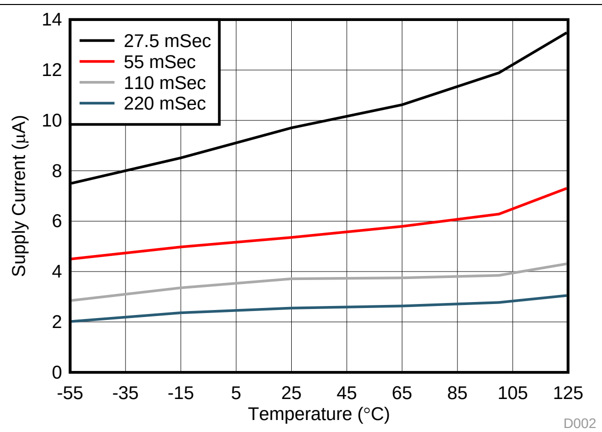


Figure 4. Average Current vs Conversion Rates and Temperature

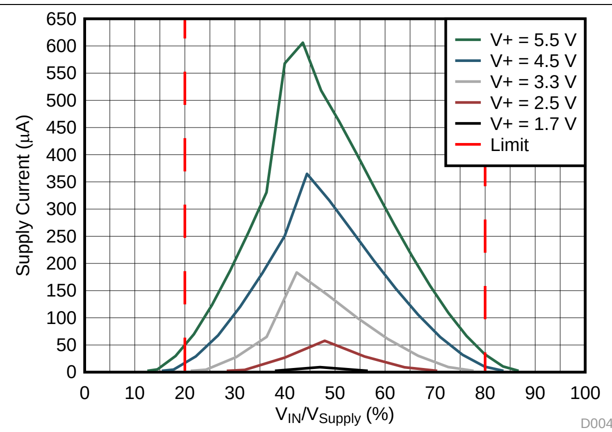


Figure 5. Supply Current vs Input Cell Voltage

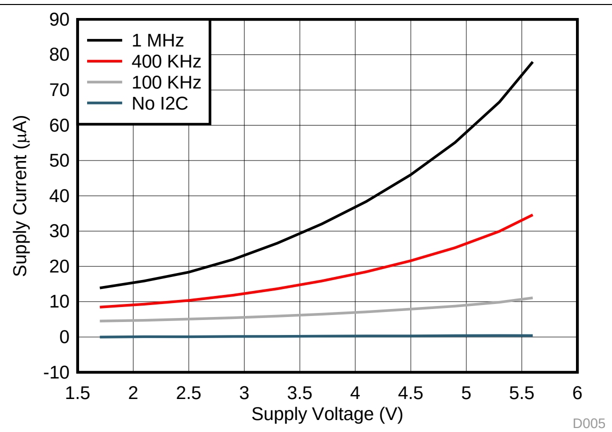


Figure 6. Supply Current vs I^2C Bus Clock and Supply Voltage in Shutdown Mode

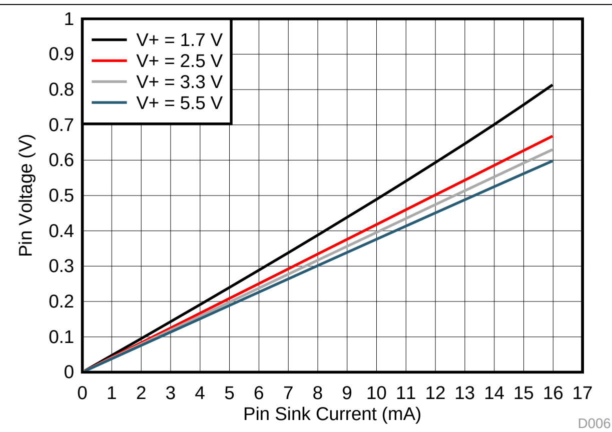


Figure 7. ALERT Pin Output Voltage vs Sink Current

Typical Characteristics (continued)

at T_A = 25°C and V+ = 3.3 V (unless otherwise noted)

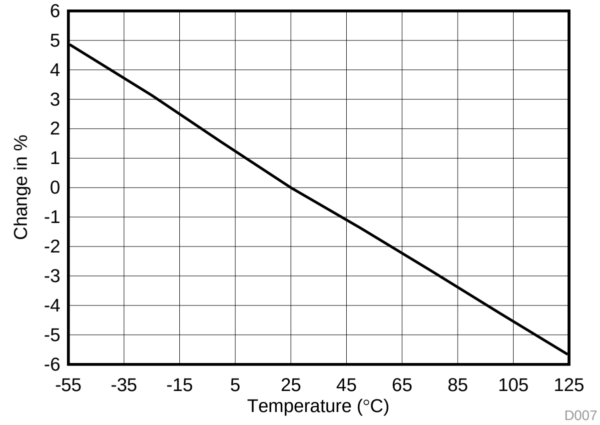


Figure 8. Sampling Period Change vs Temperature (1.7 V to 5.5 V)

7 Detailed Description

7.1 Overview

The TMP1075 device is a digital temperature sensor that is optimal for thermal management and thermal protection applications. The TMP1075 is a SMBus and is I^2C interface-compatible. It is also capable of coexisting in an I^3C bus when in Mixed Fast Mode. The device is specified over a temperature range of −55°C to +125°C. The *Functional Block Diagram* section shows an internal block diagram of TMP1075 device.

The temperature sensor thermal path runs through the package leads as well as the plastic package. The leads provide the primary thermal path due to the lower thermal resistance of the metal.

7.2 Functional Block Diagram

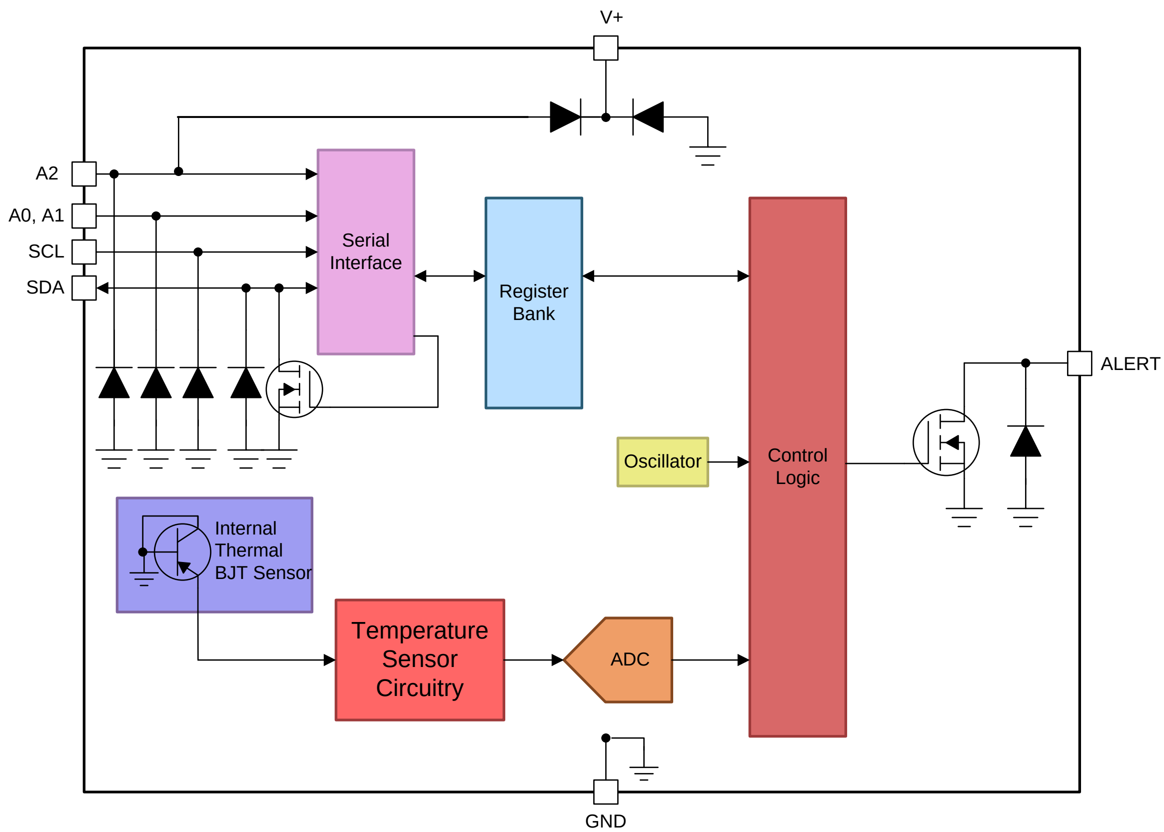


Figure 9. Functional Block Diagram

7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only Temperature register. Which is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data. However, only the first 12 MSBs are used to indicate temperature while the remaining 4 LSB are set to zero. Data format for the temperature is listed in Table 1. Negative numbers are represented in binary two's-complement format. After power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
127.9375	0111 1111 1111 0000	7FF0
100	0110 0100 0000 0000	6400
80	0101 0000 0000 0000	5000
75	0100 1011 0000 0000	4B00
50	0011 0010 0000 0000	3200
25	0001 1001 0000 0000	1900
0.25	0000 0000 0100 0000	0040
0.0625	0000 0000 0001 0000	0010
0	0000 0000 0000 0000	0000
–0.0625	1111 1111 1111 0000	FFF0
–0.25	1111 1111 1100 0000	FFC0
–25	1110 0111 0000 0000	E700
–50	1100 1110 0000 0000	CE00
–128	1000 000 0000 0000	8000

7.3.2 I²C and SMBus Serial Interface

The TMP1075 operates as a target device on the two-wire, SMBus and I²C interface-compatible bus. Connections to the bus are made through the open-drain I/O line SDA and SCL input pin. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP1075 supports the transmission protocol for fast mode up to 400 kHz and high-speed mode up to 2.56 MHz. All data bytes are transmitted MSB first.

7.3.2.1 Bus Overview

The device that initiates the data transfer is called a host, and the devices controlled by the host are the target. The bus must be controlled by a host device that generates the SCL that controls the bus access and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. This is indicated by the host pulling the data line SDA from a high to low logic level when SCL is high. All target devices on the bus shift in the device address byte on the rising edge of the clock with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the device being addressed responds to the host by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer, SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the host generates a STOP condition indicated by pulling SDA from low to high logic level when SCL is high.

7.3.2.2 Serial Bus Address

To communicate with the TMP1075, the host must first address devices through an address byte. The device address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP1075 features three address pins to allow up to 32 devices to be addressed on a single bus interface. Table 2 describes the pin logic levels used to connect up to 32 devices. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

Table 2. Address Pins State

A2	A1	A0	7-BIT ADDRESS	A2	A1	A0	7-BIT ADDRESS
0	0	SDA	1000000	0	SDA	SDA	1010000
0	0	SCL	1000001	0	SDA	SCL	1010001
0	1	SDA	1000010	0	SCL	SDA	1010010
0	1	SCL	1000011	0	SCL	SCL	1010011
1	0	SDA	1000100	1	SDA	SDA	1010100
1	0	SCL	1000101	1	SDA	SCL	1010101
1	1	SDA	1000110	1	SCL	SDA	1010110
1	1	SCL	1000111	1	SCL	SCL	1010111
0	0	0	1001000	0	SDA	0	1011000
0	0	1	1001001	0	SDA	1	1011001
0	1	0	1001010	0	SCL	0	1011010
0	1	1	1001011	0	SCL	1	1011011
1	0	0	1001100	1	SDA	0	1011100
1	0	1	1001101	1	SDA	1	1011101
1	1	0	1001110	1	SCL	0	1011110
1	1	1	1001111	1	SCL	1	1011111

7.3.2.3 Writing and Reading to the TMP1075

Accessing a particular register on the TMP1075 device is accomplished by writing the appropriate value to the Pointer register. After Reset, the register value is set to zero. The value for the Pointer register is the first byte transferred after the device address byte with the R/W bit low. Every write operation to the TMP1075 requires a value for the Pointer register (see Figure 10).

When reading from the TMP1075 device, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a device address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data are required. The host can then generate a START condition and send the device address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 11 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP1075 remembers the Pointer register value until the value is changed by the next write operation.

Register bytes are sent MSB first.

7.3.2.4 Operation Mode

The TMP1075 can operate as a receiver or transmitter. As a target device, the TMP1075 never drives the SCL line.

7.3.2.4.1 Receiver Mode

The first byte transmitted by the host is the device address with the R/$\overline{W}$ bit low. The TMP1075 then acknowledges reception of a valid address. The next byte transmitted by the host is the Pointer register. The TMP1075 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP1075 acknowledges reception of each data byte. The host can terminate data transfer by generating a START or STOP condition.

7.3.2.4.2 Transmitter Mode

The first byte is transmitted by the host and is the device address, with the R/$\overline{W}$ bit high. The target device acknowledges reception of a valid device address. The next byte is transmitted by the device and is the most significant byte of the register indicated by the Pointer register. The host acknowledges reception of the data byte. The next byte transmitted by the device is the least significant byte. The host acknowledges reception of the data byte. The host can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

7.3.2.5 SMBus Alert Function

The TMP1075 supports the SMBus Alert function. When the TMP1075 is operating in interrupt mode (TM = 1), the ALERT pin of the TMP1075 can be connected as an SMBus Alert signal. When a host senses that an alert condition is present on the ALERT line, the host sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP1075 is active, the devices acknowledge the SMBus Alert command and respond by returning the device address on the SDA line. The eighth bit (LSB) of the device address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the alert condition. This bit is equal to POL if the temperature is greater than or equal to T_{HIGH}. This bit is equal to $\overline{POL}$ if the temperature is less than T_{LOW}. See Figure 13 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the device address portion of the SMBus Alert command determines which device clears the alert status. If the TMP1075 wins the arbitration, the ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP1075 loses the arbitration, the ALERT pin remains active.

7.3.2.6 General Call- Reset Function

The TMP1075 responds to the two-wire general call address (0000 000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000 110, the TMP1075 resets the internal registers to the power-up reset values.

7.3.2.7 High-Speed Mode (HS)

For the two-wire bus to operate at frequencies above 400 kHz, the host device must issue an HS mode host code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1075 device does not acknowledge this byte, but it does switch the input filters on the SDA and SCL and the output filters on the SDA to operate in HS mode. After the HS mode host code is issued, the host transmits a two-wire device address to initiate a data transfer operation. The bus continues to operate in HS mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP1075 switches the input and output filters back to fast-mode operation.

7.3.2.8 Coexists in I^3C Mixed Fast Mode

A bus with both I^3C and I^2C interfaces is referred to as a mixed fast mode with clock speeds up to 12.5 MHz. In order for the TMP1075, which is an I^2C device, to coexist in the same bus, the device incorporated a spike suppression filter of 50 ns on the SDA and SCL pins to avoid any interference to the bus when communicating with I^3C devices.

7.3.2.9 Time-Out Function

The TMP1075 resets the serial interface if SDA is held low for 25 ms (typical) between a START and STOP condition. The TMP1075 releases the SDA bus is held low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained.

7.3.3 Timing Diagrams

The TMP1075 is two-wire SMBus and I^2C interface-compatible. Figure 10 to Figure 13 describe the various operations on the TMP1075. The following list provides bus definitions.

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the host device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a host receive, the termination of the data transfer can be signaled by the host generating a Not-Acknowledge on the last byte that is transmitted by the target device.

7.3.4 Two-Wire Timing Diagrams

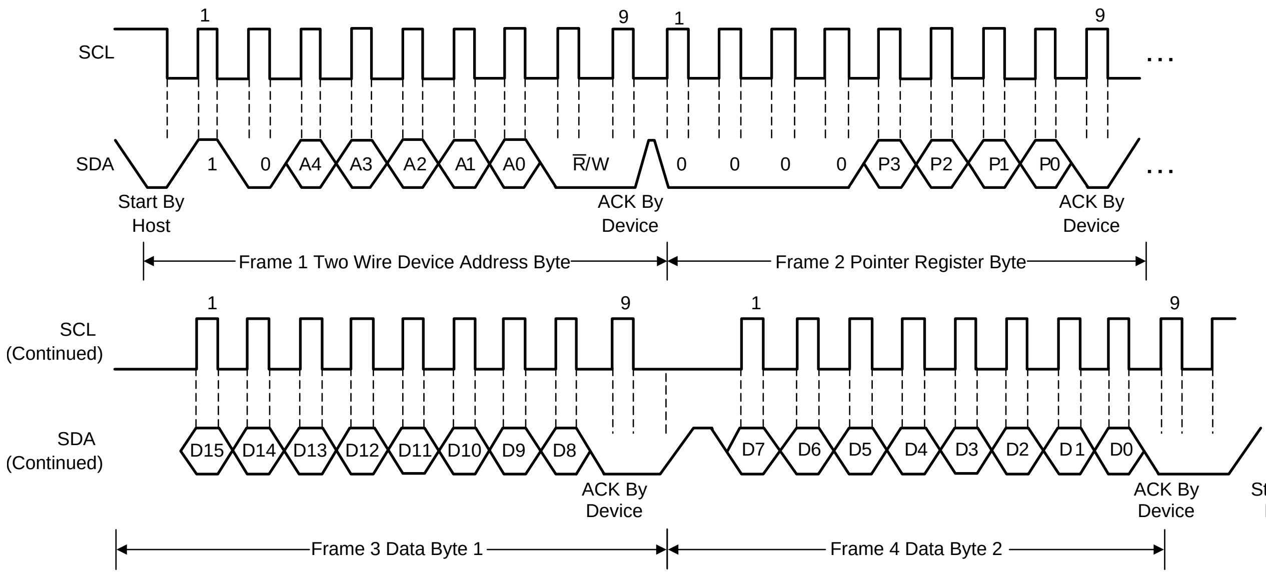


Figure 10. Two-Wire Timing Diagram for Write Word Format

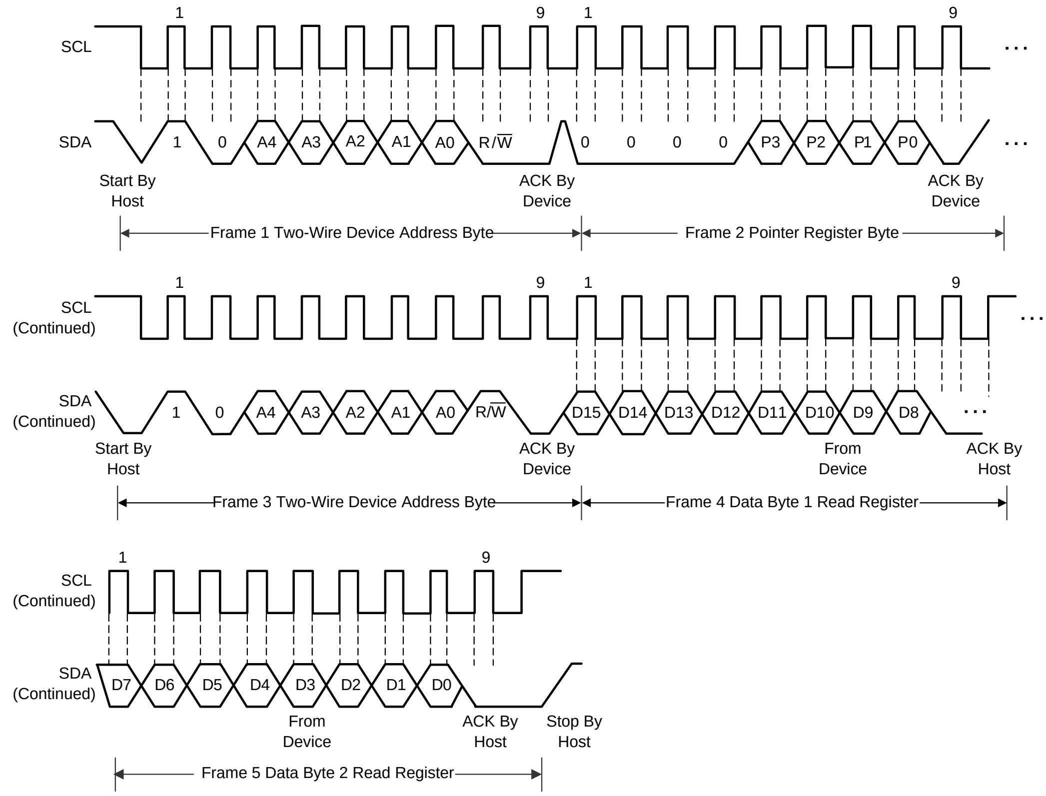


Figure 11. Two-Wire Timing Diagram for Read Word Format

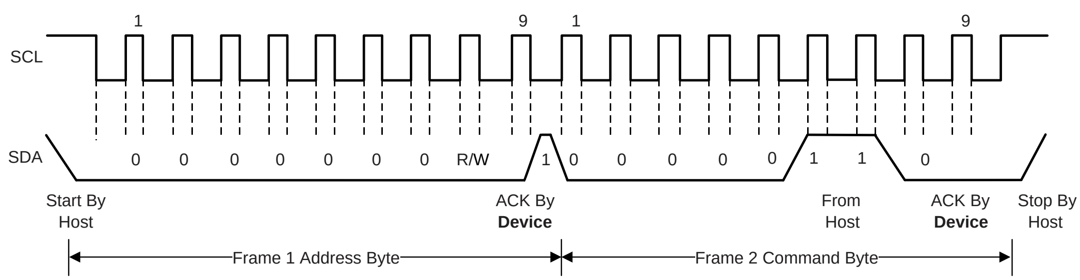


Figure 12. General-Call Reset Command Timing Diagram

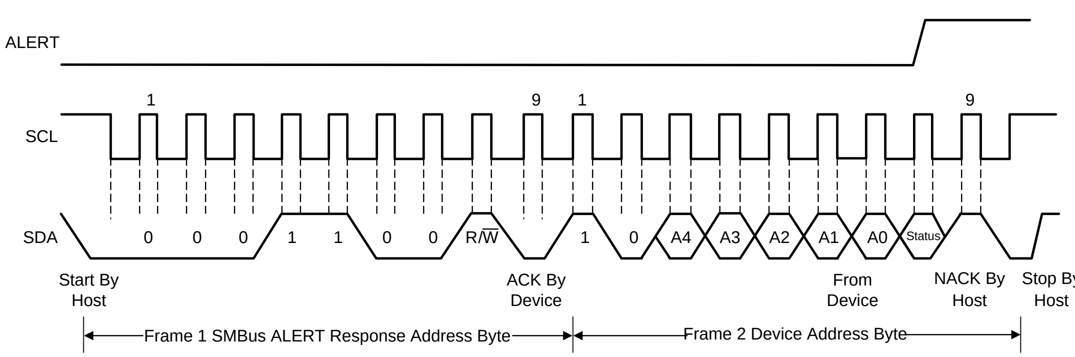


Figure 13. Timing Diagram for SMBus Alert

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

Shutdown mode (SD) of the TMP1075 device allows the user to conserve power by shutting down all device circuitry except the serial interface, which reduces current consumption to 0.37 µA (typical). SD is initiated when the SD bit in the configuration register is set to 1. When SD is equal to 0, the device stays in continuous conversion mode.

7.4.2 One-Shot Mode (OS)

The TMP1075 features a one-shot mode (OS) temperature measurement. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP1075 when continuous temperature monitoring is not required. When the configuration register is read, the OS bit always reads zero.

7.4.3 Continuous Conversion Mode (CC)

When the device is operating in continuous conversion mode (SD=0), every conversion cycle consists of an active conversion, followed by a standby as shown in Figure 14. The device consumes 52 µA (typical) during active conversion, while the low-power standby consumes 0.3 µA. Active conversion time is 5.5 ms before the part goes on standby. Table 8 shows the list of conversion cycle configured using [R1:R0] bits in the configuration register.

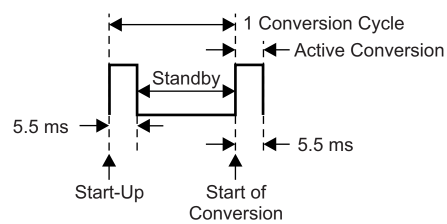


Figure 14. Conversion Rate Diagram

7.4.4 Thermostat Mode (TM)

The thermostat mode bit indicates whether ALERT pin operates in comparator mode (TM = 0) or interrupt mode (TM = 1). ALERT pin mode is controlled by TM (bit 9) of the configuration register. Any write to the TM bit changes the ALERT pin to a none active condition, clears the faults count, and clears the alert interrupt history. The ALERT pin can be disabled in both comparator and interrupt modes if both limit registers are set to the rail values T_{LOW} = –128°C and T_{HIGH} = +127.9375°C.

7.4.4.1 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of Fault Queue bits [F1:F0]. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

The difference between the two limits acts as a hysteresis on the comparator output, and a fault counter prevents false alerts as a result of system noise. The SMBus Alert response function is ignored in the comparator mode.

7.4.4.2 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the device starts to compare temperature readings with the High Limit register value. The ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of conversions as set by the Fault Queue bits [F1:F0]. The ALERT pin remains active until it is cleared by one of three events: a read of any register, a successful SMBus Alert response, or a shutdown command. After the ALERT pin is cleared, the device starts to compare temperature readings with the T_{LOW}. The ALERT pin

Device Functional Modes (continued)

becomes active again only when the temperature drops below T_{LOW} for a consecutive number of conversions as set by the Fault Queue bits. The ALERT pin remains active until cleared by any of the same three clearing events. After the ALERT pin is cleared by one of the events, the cycle repeats and the device resumes to compare the temperature to T_{HIGH}. The interrupt mode history is cleared by a change in the TM=0 bit, setting the device to SD mode, or resetting the device.

7.4.4.3 Polarity Mode (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is shown in Figure 15.

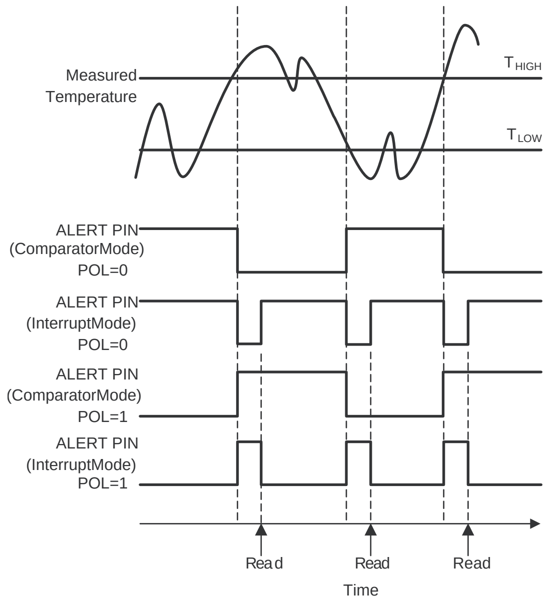


Figure 15. Output Transfer Function Diagrams

7.5 Programming

Table 3. Register Map

ADR (HEX)	POR (HEX)	TYPE	NAME	BIT FIELDS																DESCRIPTION
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	0000	RO	TEMP	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0	0	0	0	Temperature
01	00FF	RW	CFGR	OS	R1	R0	F1	F0	POL	TM	SD	1	1	1	1	1	1	1	1	Configuration
02	4B00	RW	L LIM	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	Low Limit
03	5000	RW	H LIM	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	0	0	0	0	High Limit
0F	7500	RO	DIE ID	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	Device ID

7.5.1 Pointer Register

Figure 16 shows the internal register structure of the TMP1075, and Table 3 lists the pointer addresses of the register map. Table 4 shows that the register map reset value of the pointer register is 00h.

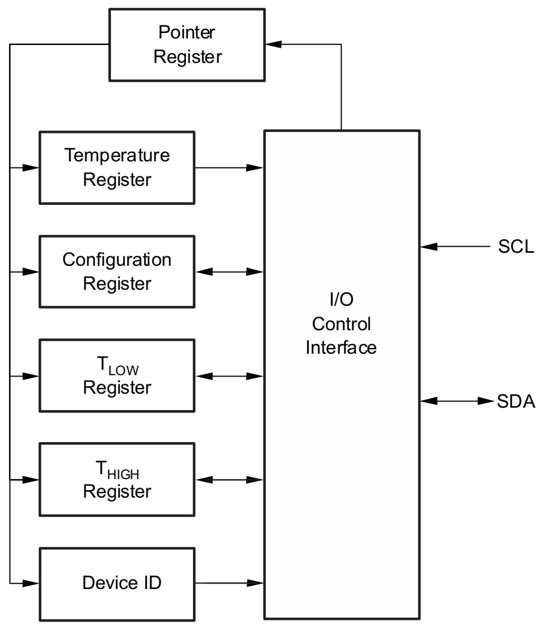


Figure 16. Internal Register Structure

7.5.1.1 Pointer Register Byte [reset = 00h]

Table 4. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	Register Bits			

7.5.2 Temperature Register

The Temperature register of the TMP1075 is a 12-bit, read-only register that stores the result of the most recent conversion (see Table 5). The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Following power-up or reset, the Temperature register value is 0°C until the first conversion is complete.

Table 5. Temperature Register (0x00) [default reset = 0000h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0	0	0	0

7.5.3 Configuration Register

The Configuration register is an 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP1075 is shown in Table 6 followed by a breakdown of the register bits. The power-up or reset value of the Configuration register are all bits equal to 00FFh.

Table 6. Configuration Register (0x01) [default reset = 00FFh]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OS	R1	R0	F1	F0	POL	TM	SD	1	1	1	1	1	1	1	1

7.5.3.1 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements to trigger the alert function. Table 7 defines the number of measured faults that can be programmed to trigger an alert condition in the device.

Table 7. Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

7.5.3.2 Conversion Rate (R1, R0)

When the device is in continuos conversion mode (SD=0), the result is updated based on the conversion rate setting shown in Table 8 (for description refer to section Continuous Conversion Mode (CC)).

Table 8. Conversion Rate

R1	R0	Conversion Rate (Typical)
0	0	27.5 ms
0	1	55 ms
1	0	110 ms
1	1	220 ms

7.5.4 High and Low Limit Registers

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature register.

Table 9. T_{LOW} Register (0x02) [default reset = 4B00h = 75°C]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0

Table 10. T_{HIGH} Register (0x03) [default reset = 5000h = 80°C]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	0	0	0	0

7.5.5 Die ID Register (0x0F)

The MSB byte of the die ID register reads the static value 0x75 hex to indicate the device name for TMP1075 as shown in Table 11.

Table 11. Die ID Register (0x0F) [default reset = 7500h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP1075 can measure the PCB temperature of the location where the user mounts the device. The TMP1075 features two-wire SMBus and I^2C interface compatibility, with the TMP1075 allowing up to 32 devices on one bus. The TMP1075 requires a pullup resistor on the SDA pin, and if needed, on the SCL and ALERT pins. A 0.01-µF bypass capacitor is also required as shown in Figure 17.

8.2 Typical Application

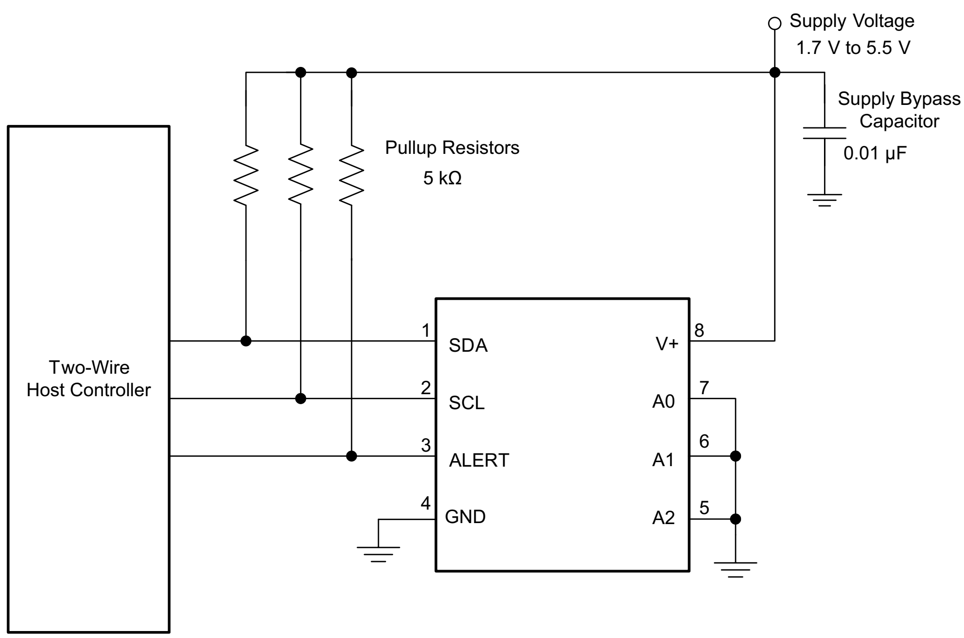


Figure 17. Typical Connections

8.2.1 Design Requirements

The recommended value for the pullup resistor is 5 kΩ. In some applications, the pullup resistor can be lower or higher than 5 kΩ, but the maximum current through the pullup current is recommended to not exceed 3 mA on the SCL and SDA pins. The SCL, SDA, A0, A1, and ALERT lines can be pulled up to a supply that is higher than V+. The A2 pin can only be connected to GND or V+. When the ALERT pin is not used, it can either be connected GND or left floating.

8.2.2 Detailed Design Procedure

Place the TMP1075 device in close proximity to the heat source that must be monitored with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

Typical Application (continued)

8.2.3 Application Curve

For application curves, see Table 12:

Table 12. Table of Graphs

FIGURE	TITLE
Figure 8	Sampling Period Change vs Temperature (1.7V to 5.5V)

9 Power Supply Recommendations

The TMP1075 operates with a power supply in the range of 1.7 V to 5.5 V. A power-supply bypass capacitor is required for precision and stability. Place this power-supply bypass capacitor as close to the supply and ground pins of the device as possible. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies can require a bigger bypass capacitor to reject power-supply noise.

To minimize device self-heating and improve temperature precision, it is recommended to:

- Use the minimum supply voltage rail available
- Avoid communication over I^2C bus during ADC conversion
- Use one-shot mode to minimize power consumption
- Set I^2C signal levels V_{IL} close to ground and V_{IH} above 90% of V+
- Maintain the I2C bus signals positive edge less than 1 µs by using a pull-up resistor < 10 kΩ
- Connect the address pins A_0 and A_1 to either ground or V+

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close to the supply and ground pins as possible. The recommended value of this bypass capacitor is 0.01 μF. Pullup the open-drain output pins SDA and ALERT through 5 kΩ pullup resistors. The SCL requires a pullup resistor only if the microprocessor output is open drain.

10.2 Layout Example

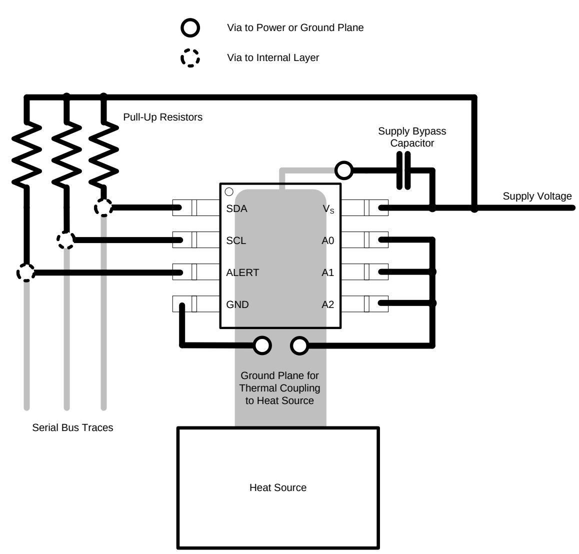


Figure 18. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP1075DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	1075	Samples
TMP1075DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	1075	Samples
TMP1075DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	1075	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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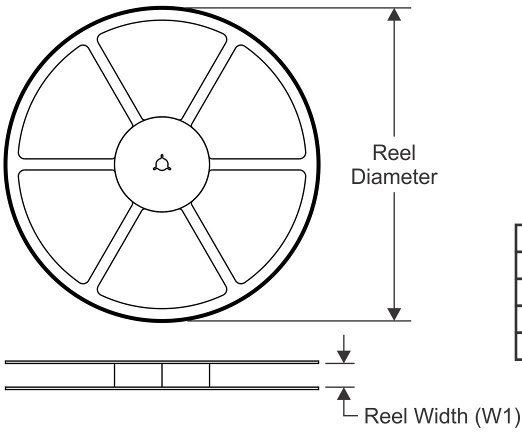
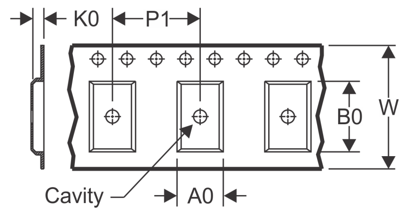
TAPE AND REEL INFORMATION

REEL DIMENSIONS

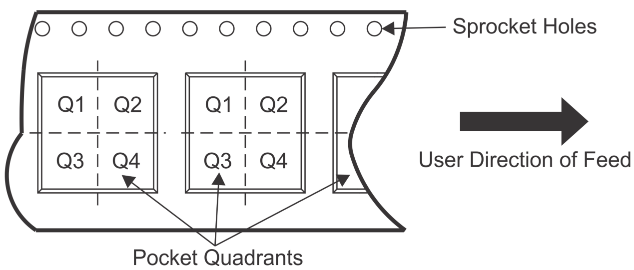


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

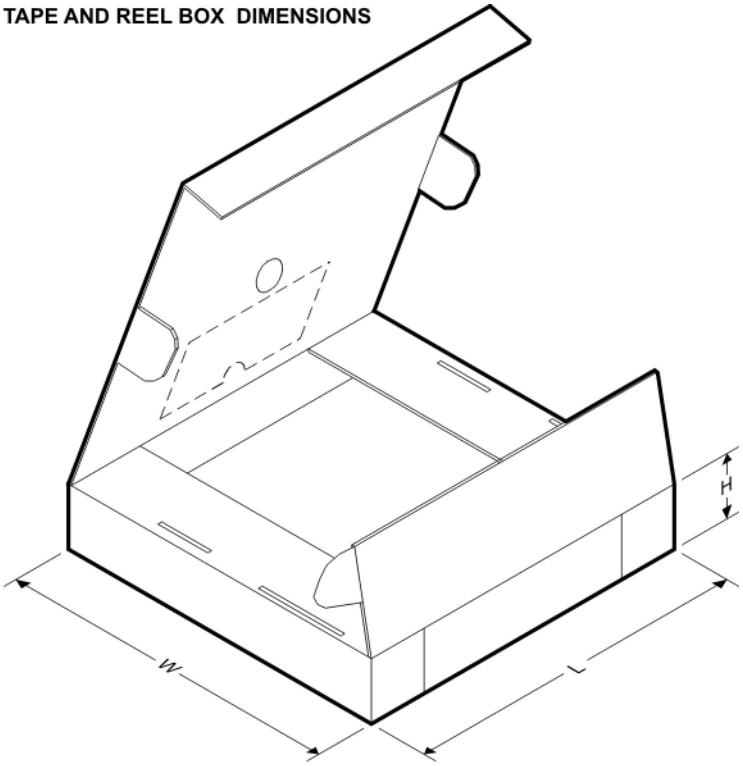
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP1075DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP1075DGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP1075DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

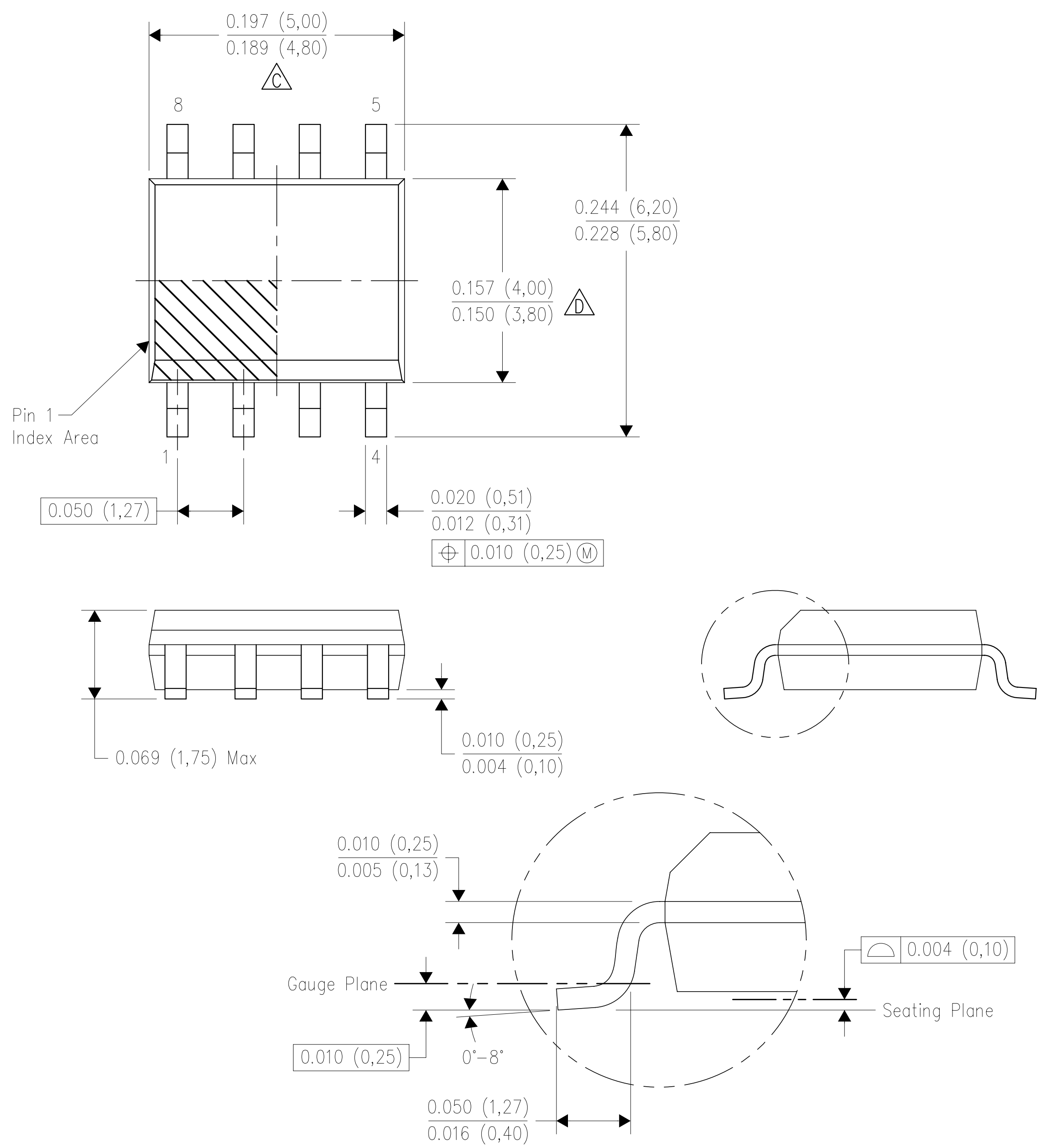
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP1075DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP1075DGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP1075DR	SOIC	D	8	2500	367.0	367.0	35.0

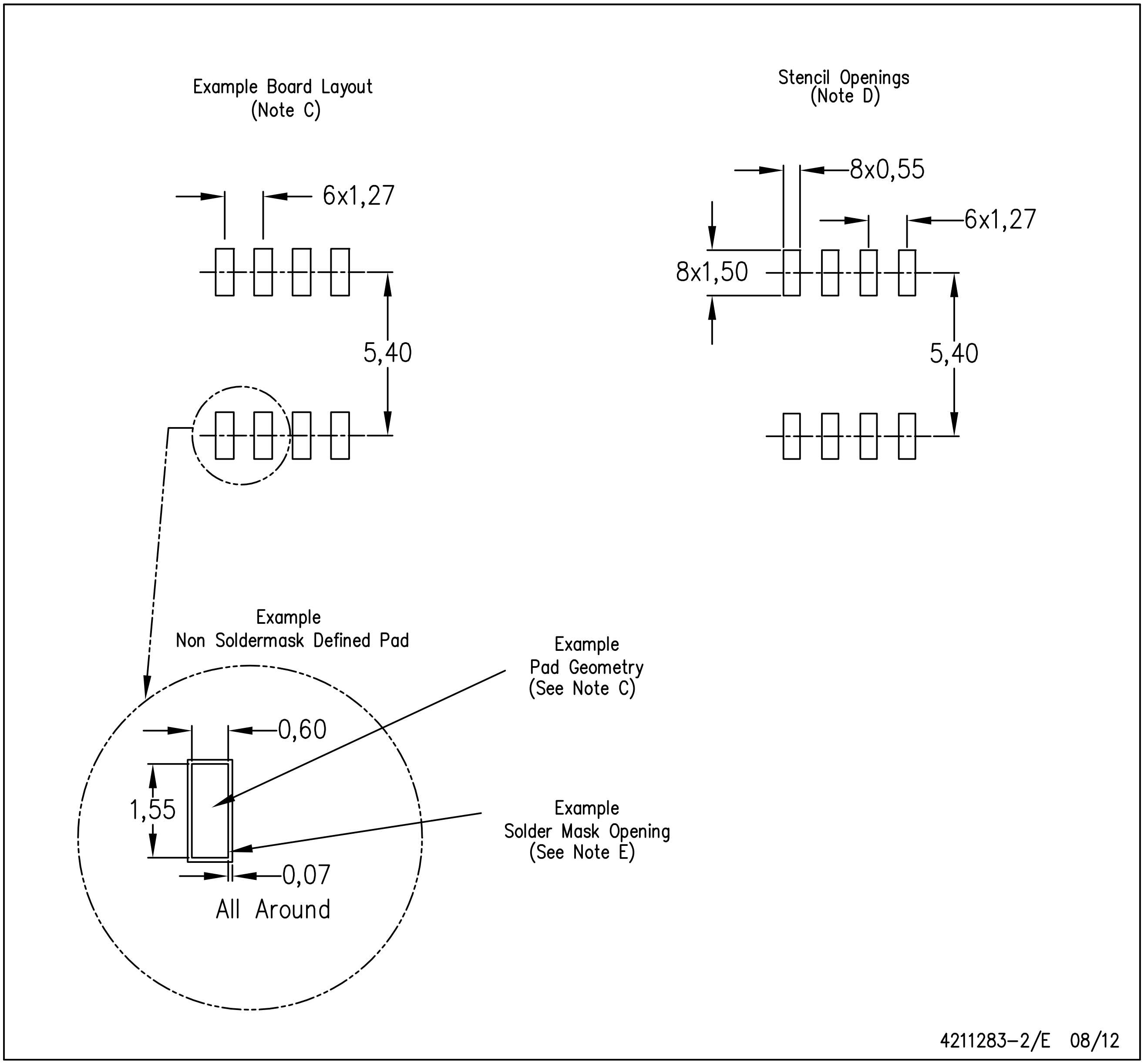
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

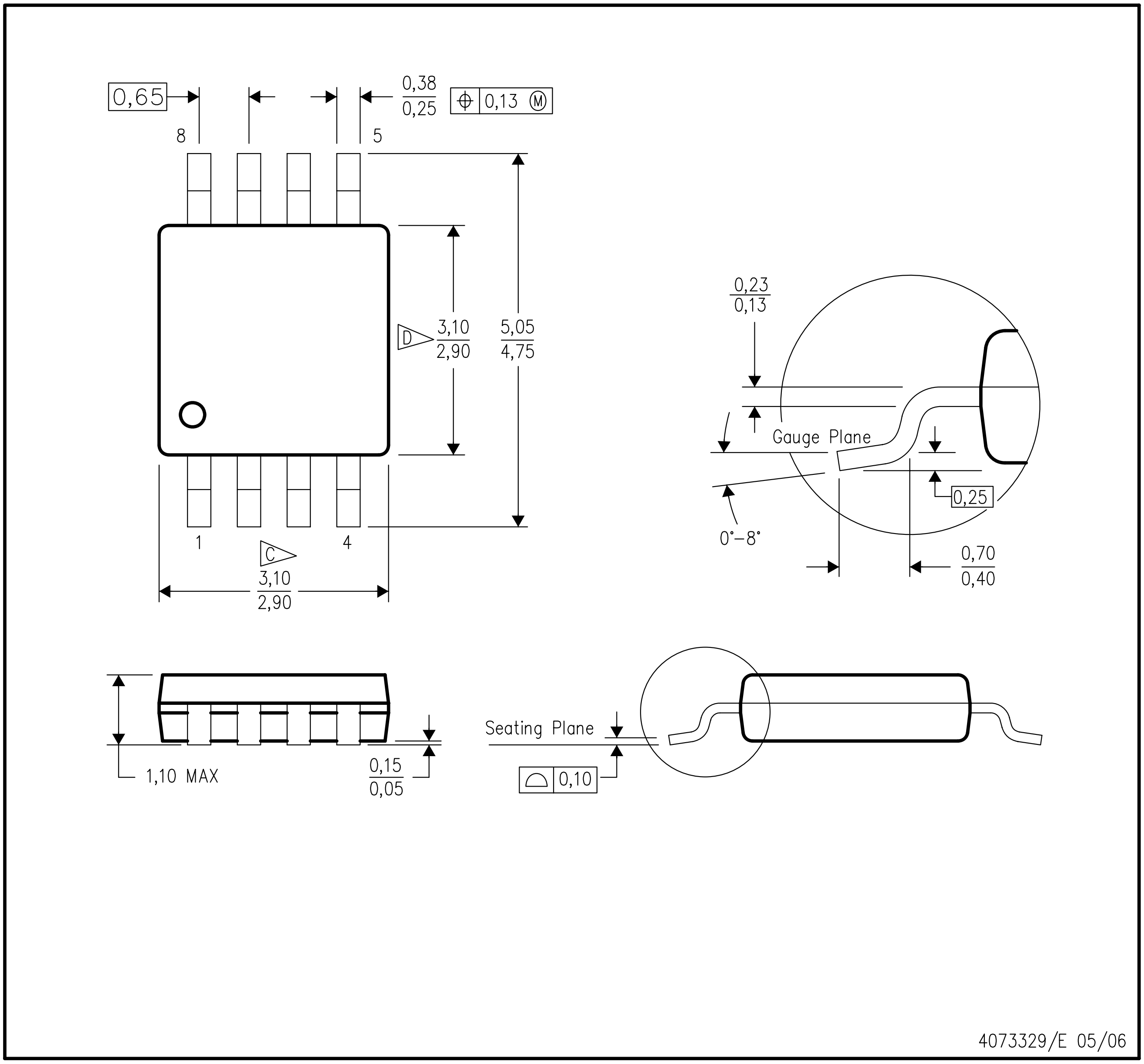
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



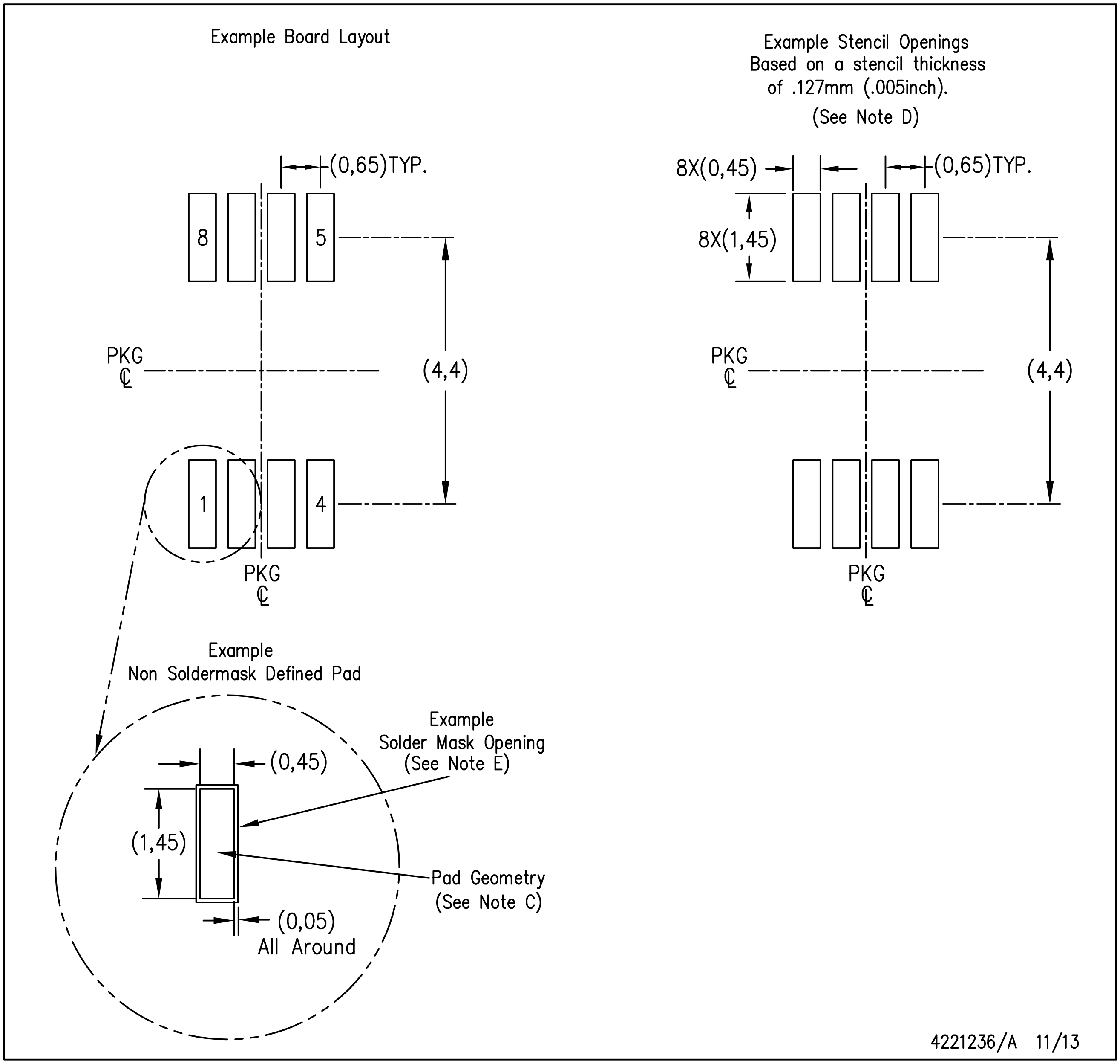
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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