AM26C32 Quadruple Differential Line Receiver

1 Features

- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11
- Low Power, I_{CC} = 10 mA Typical
- ±7-V Common-Mode Range With ±200-mV Sensitivity
- Input Hysteresis: 60 mV Typical
- t_{pd} = 17 ns Typical
- Operates From a Single 5-V Supply
- 3-State Outputs
- Input Fail-Safe Circuitry
- Improved Replacements for AM26LS32 Device
- Available in Q-Temp Automotive

2 Applications

- High-Reliability Automotive Applications
- Factory Automation
- ATM and Cash Counters
- Smart Grid
- AC and Servo Motor Drives

3 Description

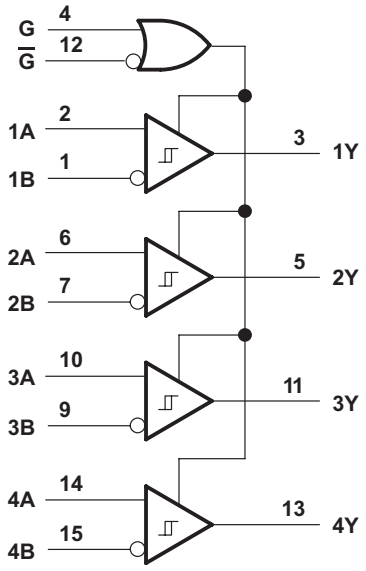
The AM26C32 device is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high. The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining AC and DC performance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AM26C32N	PDIP (16)	19.30 mm × 6.35 mm
AM26C32NS	SO (16)	10.20 mm × 5.30 mm
AM26C32D	SOIC (16)	9.90 mm × 3.90 mm
AM26C32PW	TSSOP (16)	5.00 mm × 4.40 mm
AM26C32J	CDIP (16)	21.34 mm × 6.92 mm
AM26C32W	CFP (16)	10.16 mm × 6.73 mm
AM26C32FK	LCCC (20)	8.90 mm × 8.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision J (February 2014) to Revision K **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

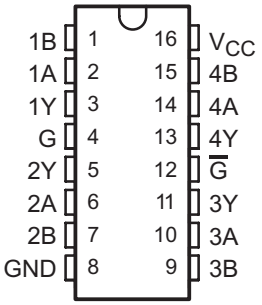
Changes from Revision I (September 2004) to Revision J **Page**

- Updated document to new TI data sheet format - no specification changes ... 1
- Deleted *Ordering Information* table. ... 1
- Updated *Features* ... 1
- Added ESD Warning ... 3

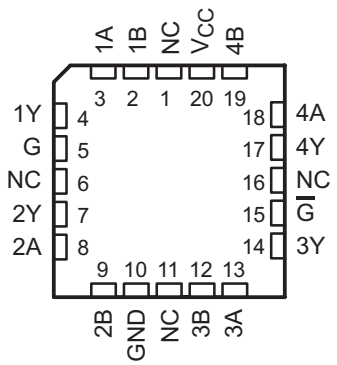
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5 Pin Configuration and Functions

D, N, NS, PW, J or W Package
16-Pin SOIC, PDIP, SO, TSSOP, CDIP, or CFP
Top View



FK Package
20-Pin LCCC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	LCCC	SOIC, PDIP, SO, TSSOP, CFP, or CDIP		
1A	3	2	I	RS422/RS485 differential input (noninverting)
1B	2	1	I	RS422/RS485 differential input (inverting)
1Y	4	3	O	Logic level output
2A	8	6	I	RS422/RS485 differential input (noninverting)
2B	9	7	I	RS422/RS485 differential input (inverting)
2Y	7	5	O	Logic level output
3A	13	10	I	RS422/RS485 differential input (noninverting)
3B	12	9	I	RS422/RS485 differential input (inverting)
3Y	14	11	O	Logic level output
4A	18	14	I	RS422/RS485 differential input (noninverting)
4B	19	15	I	RS422/RS485 differential input (inverting)
4Y	17	13	O	Logic level output
G	5	4	I	Active-high select
$\overline{G}$	15	12	I	Active-low select
GND	10	8	—	Ground
NC(1)	1	—	—	Do not connect
	6			
	11			
	16			
V_{CC}	20	16	—	Power Supply

(1) NC – no internal connection.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (2)			7	V
V_I	Input voltage	A or B inputs	–11	14	V
		G or $\overline{G}$ inputs	–0.5	V_{CC} + 0.5	
V_{ID}	Differential input voltage		–14	14	V
V_O	Output voltage		–0.5	V_{CC} + 0.5	V
I_O	Output current			±25	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V_{cc}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IC}	Common-mode input voltage		-7		+7	V
I_{OH}	High-level output current				–6	mA
I_{OL}	Low-level output current				6	mA
T_A	Operating free-air temperature	AM26C32C	0		70	°C
		AM26C32I	–40		85	
		AM26C32Q	–40		125	
		AM26C32M	–55		125	

6.4 Thermal Information

THERMAL METRIC (1)		AM26C32				UNIT
		D (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	$V_O = V_{OH(min)}$, I_{OH} = –440 µA	V_{IC} = –7 V to 7 V			0.2	V
			V_{IC} = 0 V to 5.5 V			0.1	
V_{IT-}	Differential input low-threshold voltage	V_O = 0.45 V, I_{OL} = 8 mA	V_{IC} = –7 V to 7 V	–0.2(2)			V
			V_{IC} = 0 V to 5.5 V	–0.1(2)			
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)				60		mV
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V, I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –6 mA		3.8			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 6 mA			0.2	0.3	V
I_{OZ}	OFF-state (high-impedance state) output current	$V_O = V_{CC}$ or GND			±0.5	±5	µA
I_I	Line input current	V_I = 10 V, Other input at 0 V				1.5	µA
		V_I = –10 V, Other input at 0 V				–2.5	µA
I_{IH}	High-level enable current	V_I = 2.7 V				20	µA
I_{IL}	Low-level enable current	V_I = 0.4 V				–100	µA
r_i	Input resistance	One input to ground		12	17		kΩ
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V			10	15	mA

(1) All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

6.6 Switching Characteristics

over operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AM26C32C AM26C32I			AM26C32Q AM26C32M			UNIT
			MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 2	9	17	27	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	9	17	27	ns
t_{TLH}	Output transition time, low- to high-level output	See Figure 2		4	9		4	10	ns
t_{THL}	Output transition time, high- to low-level output			4	9		4	9	ns
t_{PZH}	Output enable time to high-level	See Figure 3		13	22		13	22	ns
t_{PZL}	Output enable time to low-level			13	22		13	22	ns
t_{PHZ}	Output disable time from high-level	See Figure 3		13	22		13	26	ns
t_{PLZ}	Output disable time from low-level			13	22		13	25	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

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6.7 Typical Characteristics

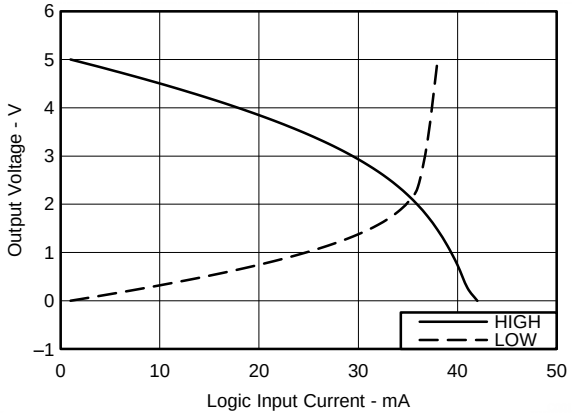
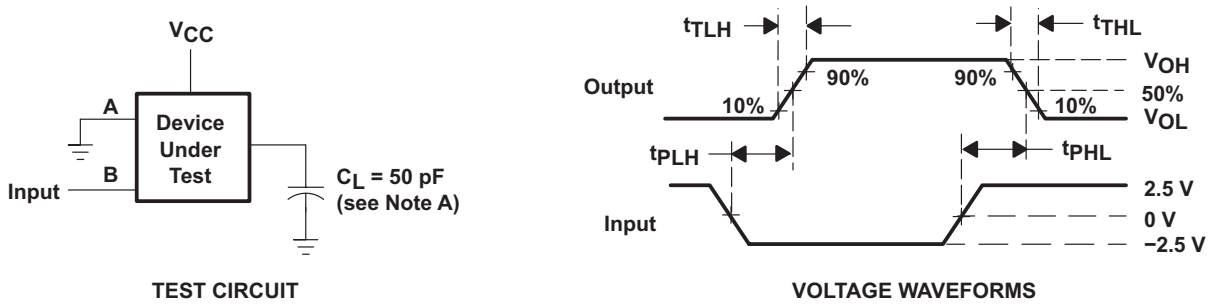


Figure 1. Output Voltage vs Input Current

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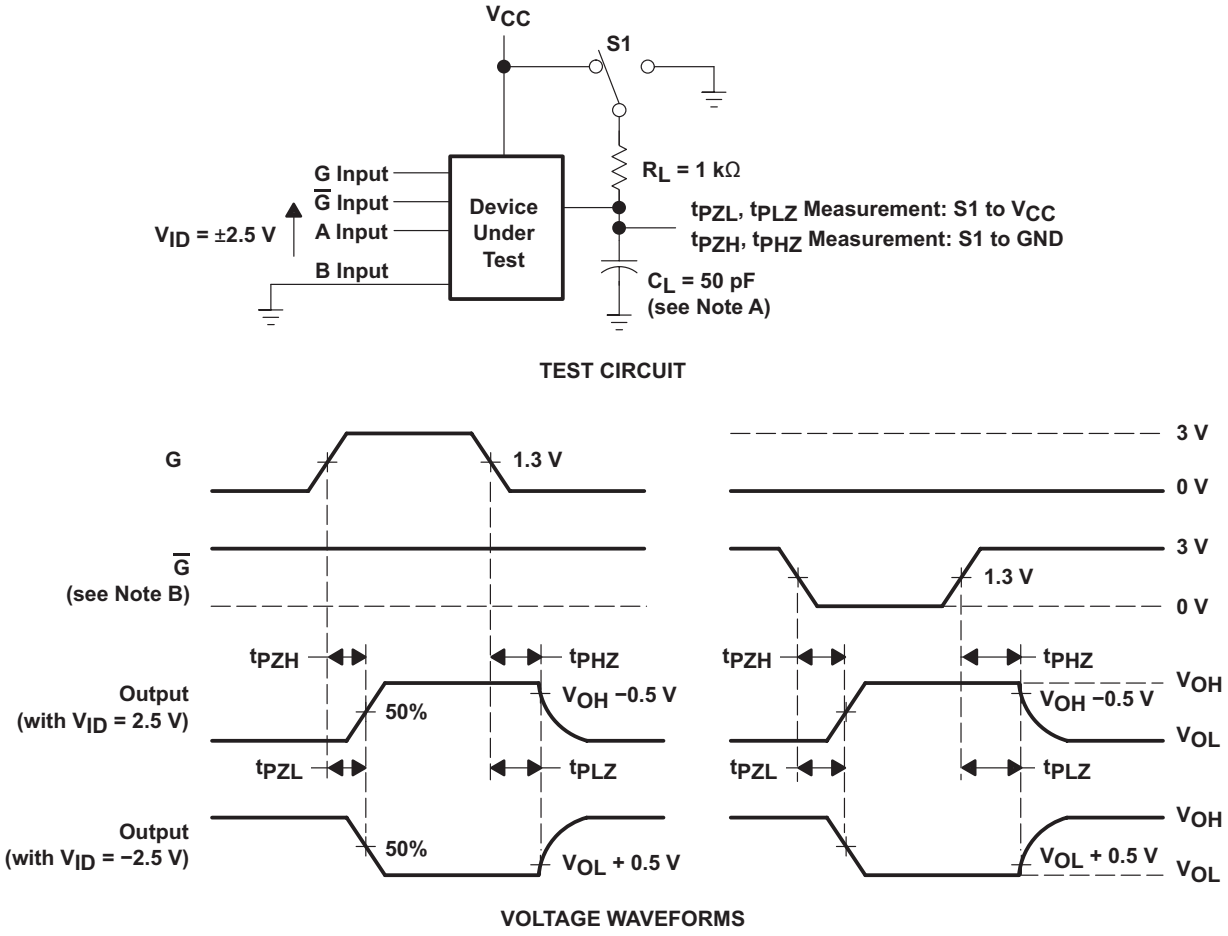
7 Parameter Measurement Information



TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

Figure 2. Switching Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r = t_f$ = 6 ns.

Figure 3. Enable/Disable Time Test Circuit and Output Voltage Waveforms

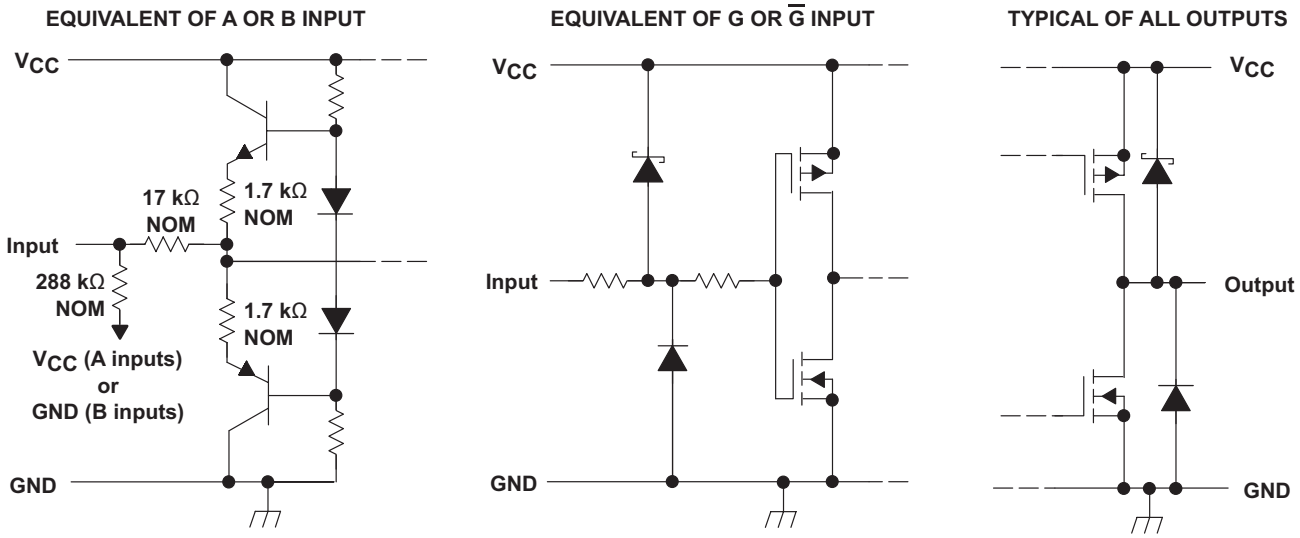
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8 Detailed Description

8.1 Overview

The AM26C32 is a quadruple differential line receiver that meets the necessary requirements for NSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11. This device allows a low power or low voltage MCU to interface with heavy machinery, subsystems and other devices through long wires of up to 1000m, giving any design a reliable and easy to use connection. As any RS422 interface, the AM26C32 works in a differential voltage range, which enables very good signal integrity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ±7-V Common-Mode Range With ±200-mV Sensitivity

For a common-mode voltage varying from -7V to 7V, the input voltage is acceptable in low ranges greater than 200 mV as a standard.

8.3.2 Input Fail-Safe Circuitry

RS-485 specifies that the receiver output state should be logic high for differential input voltages of $V_{AB} \geq +200$ mV and logic low for $V_{AB} \leq -200$ mV. For input voltages in between these limits, a receiver's output state is not defined and can randomly assume high or low. Removing the uncertainty of random output states, modern transceiver designs include internal biasing circuits that put the receiver output into a defined state (typically high) in the absence of a valid input signal.

A loss of input signal can be caused by an pen circuit caused by a wire break or the unintentional disconnection of a transceiver from the bus. The AM26C32 has an internal circuit that ensures functionality during an idle bus.

8.3.3 Active-High and Active-Low

The device can be configure using the G and $\overline{G}$ logic inputs to select receiver output. The high voltage or logic 1 on the G pin, allows the device to operate on an active-high and having a low voltage or logic 0 on the $\overline{G}$ enables active low operation. These are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.3.4 Operates from a Single 5-V Supply

Both the logic and receivers operate from a single 5-V rail, making designs much more simple. The line drivers and receivers can operate off the same rail as the host controller or a similar low voltage supply, thus simplifying power structure.

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8.4 Device Functional Modes

8.4.1 Enable and Disable

The receivers implemented in these RS422 devices can be configured using the G and $\overline{G}$ pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

Table 1. Function Table (Each Receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
A/B	G	$\overline{G}$	Y
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of RS-422 (and, indirectly, RS-485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26C31C and AM26C32C, respectively, were tested at room temperature with a 5-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable; the second plot shows input waveforms to the receiver at the far end of the cable.

9.2 Typical Application

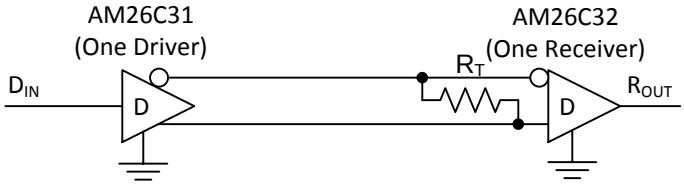


Figure 4. Differential Terminated Configuration

9.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, Zo , of the cable and can vary from about 80 Ω to 120 Ω.

9.2.2 Detailed Design Procedure

Figure 4 shows a configuration with no termination. Although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the RS-422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

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Typical Application (continued)

9.2.3 Application Curve

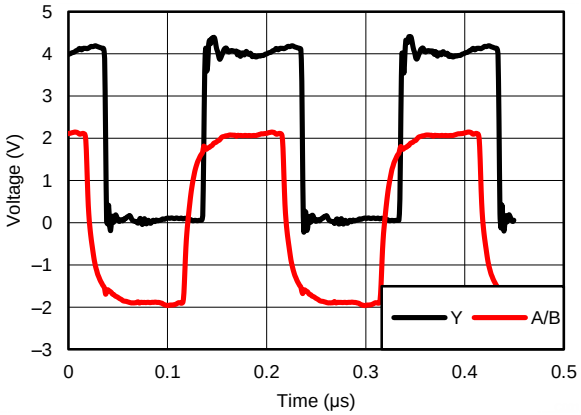


Figure 5. Differential 120-Ω Terminated Output Waveforms (Cat 5E Cable)

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10 Power Supply Recommendations

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

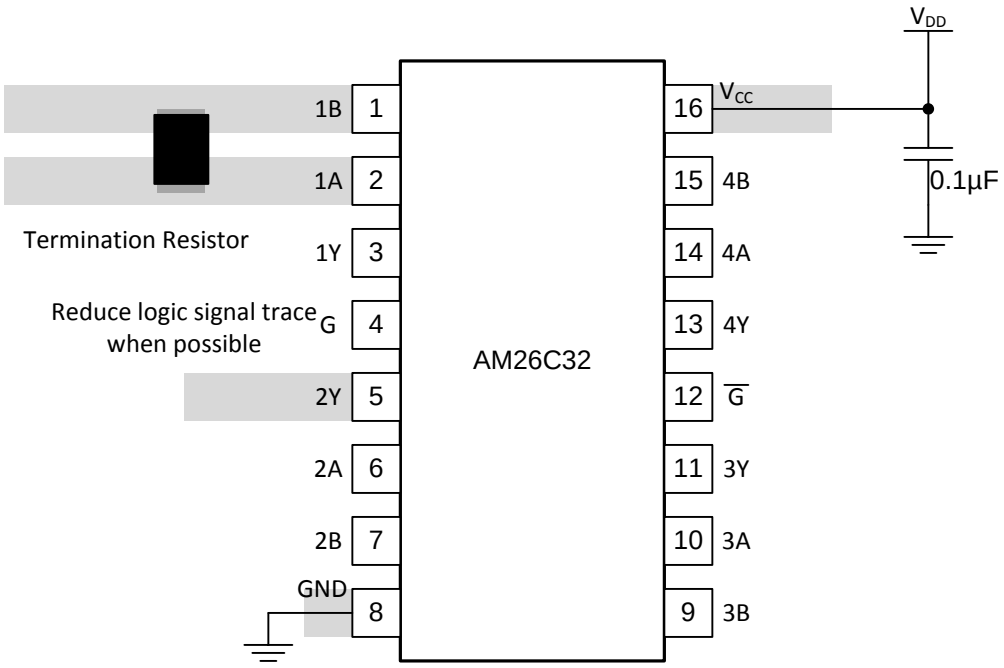


Figure 6. Trace Layout on PCB and Recommendations

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12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9164001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB	Samples
5962-9164001QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QEA AM26C32MJB	Samples
5962-9164001QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QFA AM26C32MWB	Samples
AM26C32CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		26C32	Samples
AM26C32CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AM26C32C	Samples
AM26C32CN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	AM26C32CN	Samples
AM26C32CNE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	AM26C32CN	Samples
AM26C32CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	Samples
AM26C32CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	26C32	Samples
AM26C32ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C32IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C32I	Samples
AM26C32IN	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	AM26C32IN	Samples
AM26C32INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C32I	Samples
AM26C32MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9164001Q2A AM26C32 MFKB	Samples
AM26C32MJB	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QEA AM26C32MJB	Samples
AM26C32MWB	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9164001QFA AM26C32MWB	Samples
AM26C32QD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C32Q	Samples
AM26C32QDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	26C32Q	Samples
AM26C32QDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C32Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26C32, AM26C32M :

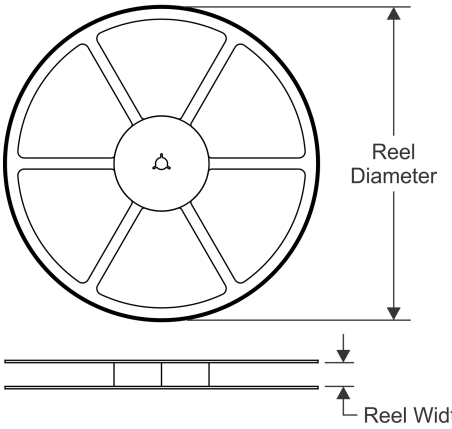
- Catalog: AM26C32
- Enhanced Product: AM26C32-EP, AM26C32-EP
- Military: AM26C32M

NOTE: Qualified Version Definitions:

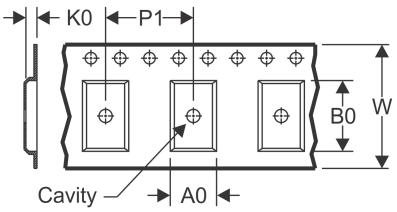
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

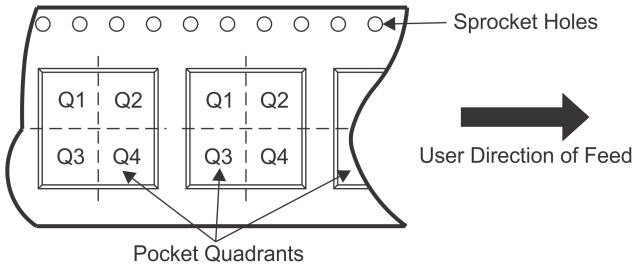


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

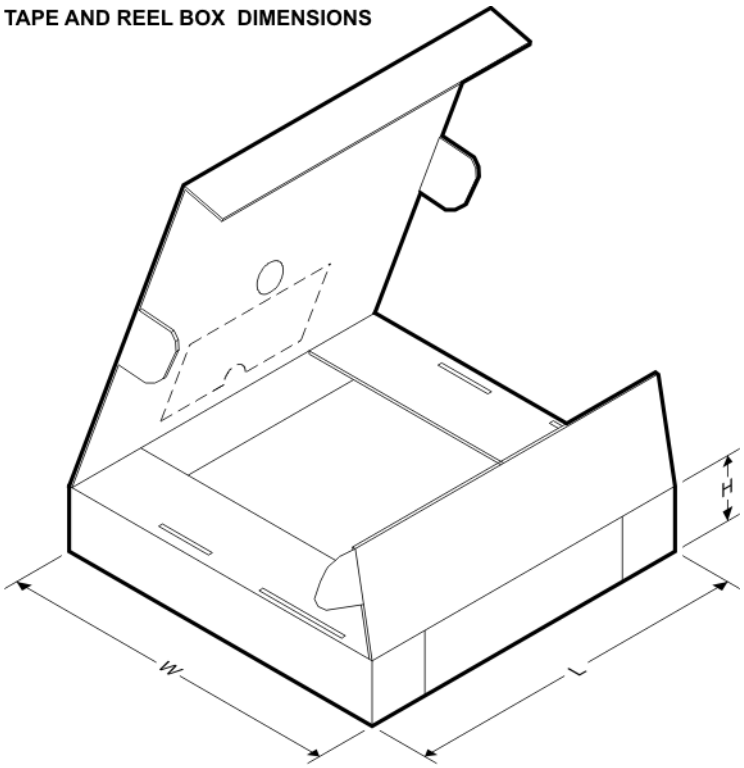
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C32CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
AM26C32CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C32IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26C32QDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

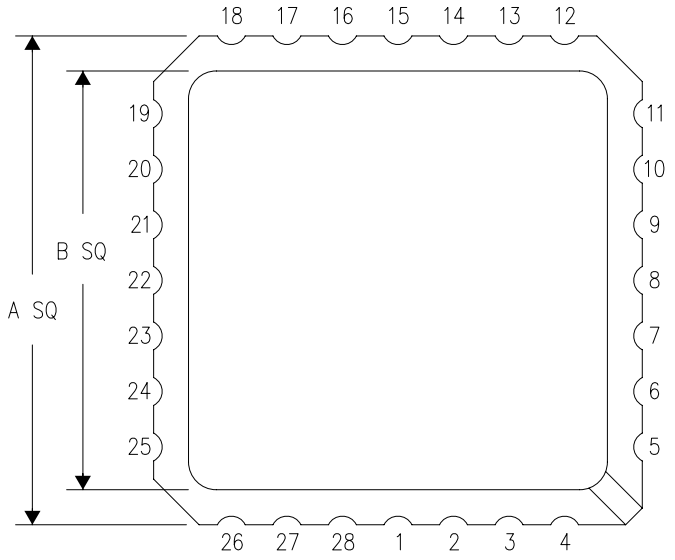


*All dimensions are nominal

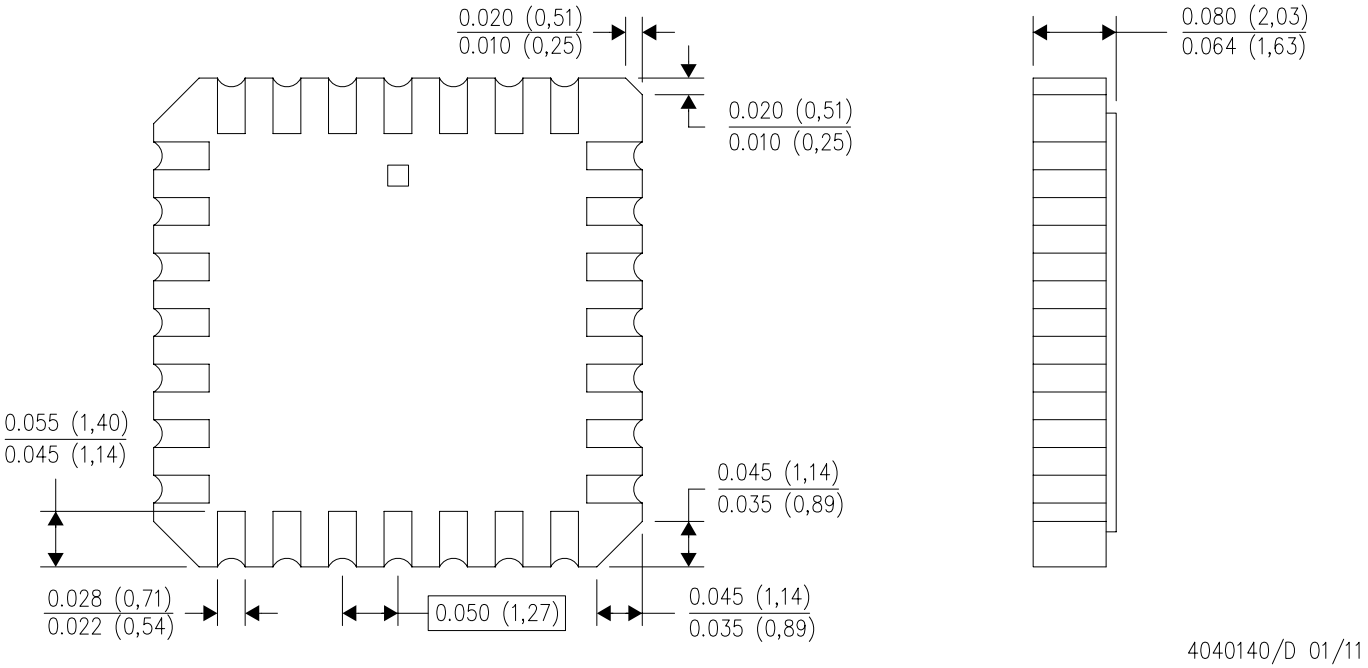
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C32CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
AM26C32CDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26C32IDR	SOIC	D	16	2500	333.2	345.9	28.6
AM26C32IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26C32QDR	SOIC	D	16	2500	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



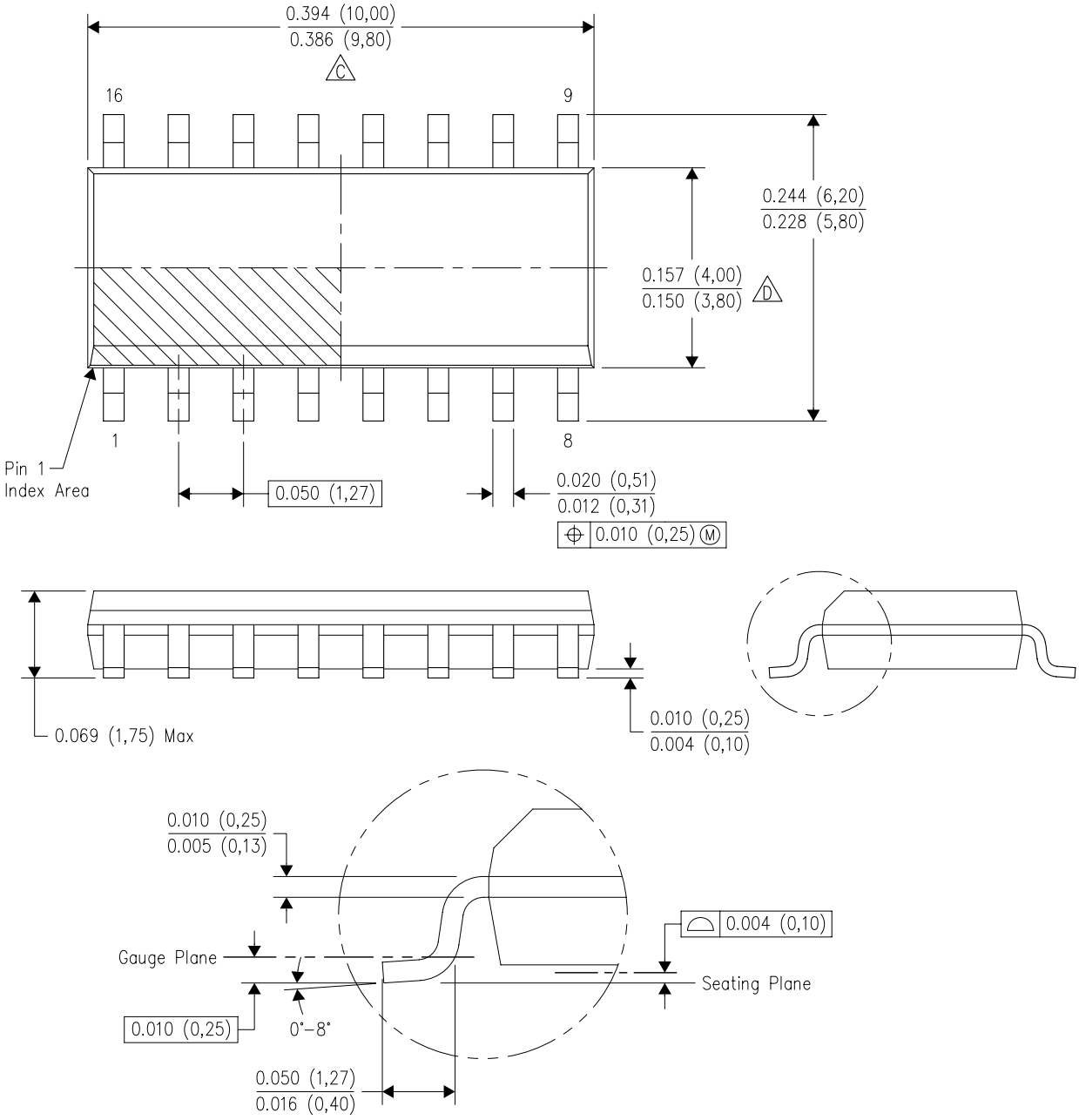
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

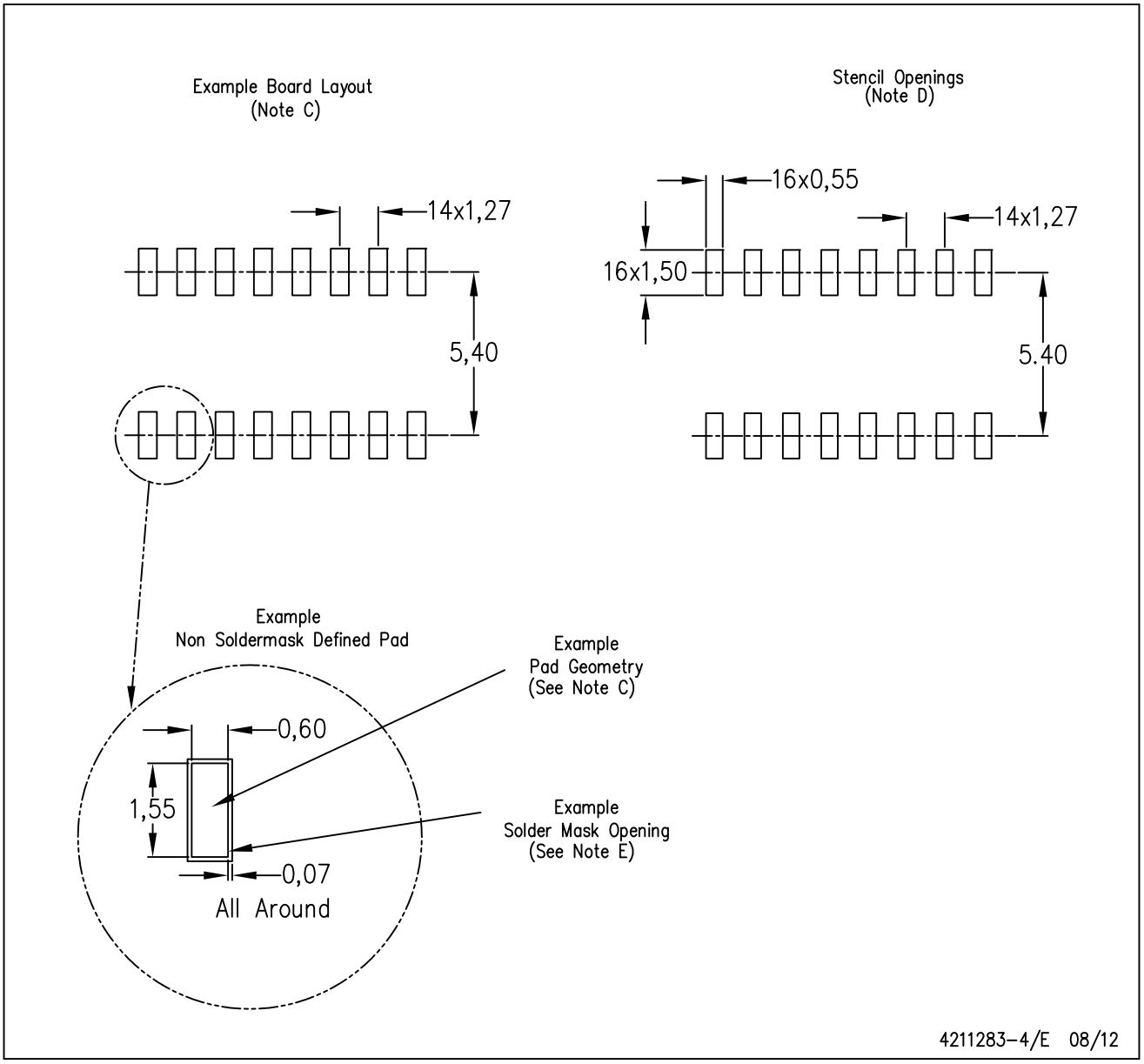
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



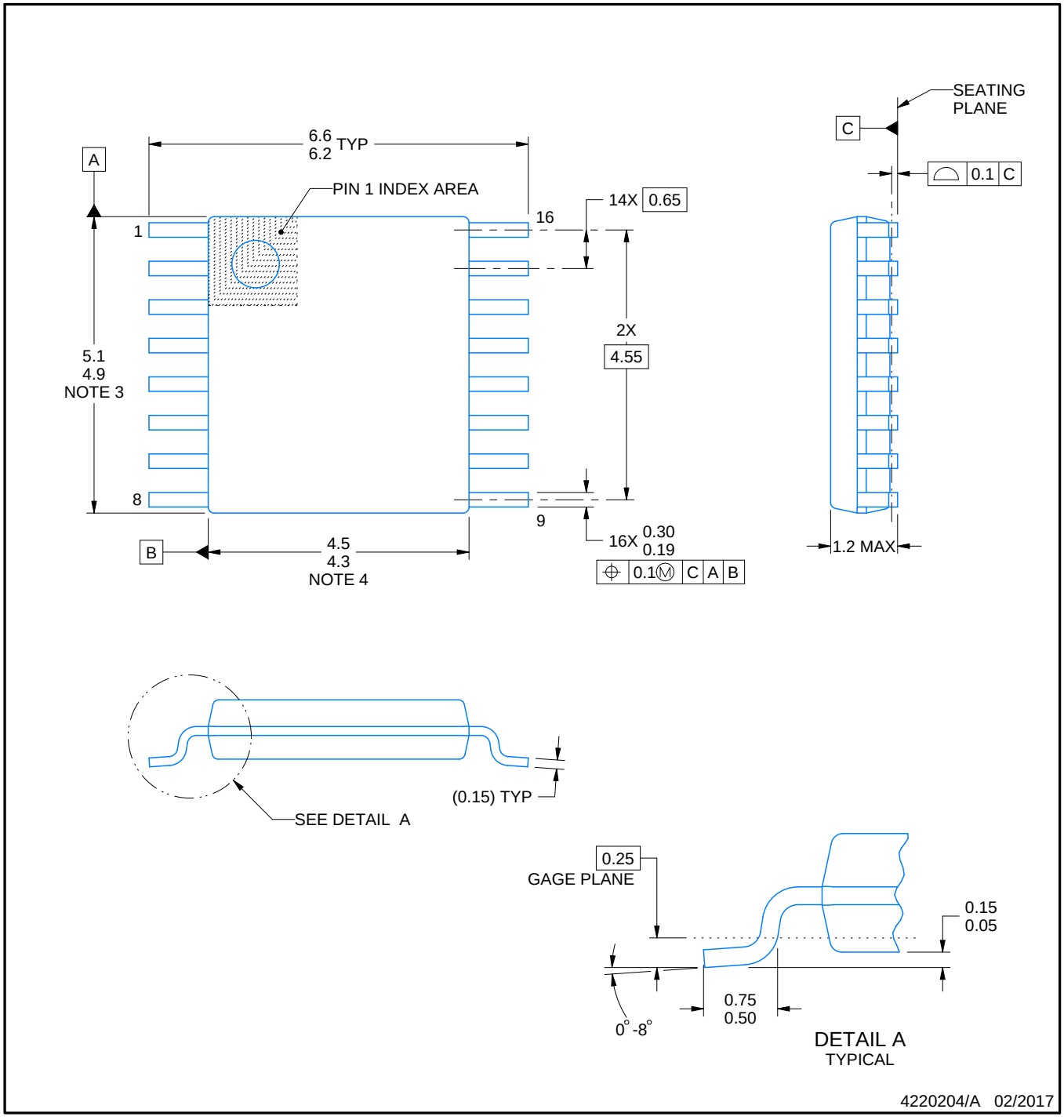
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

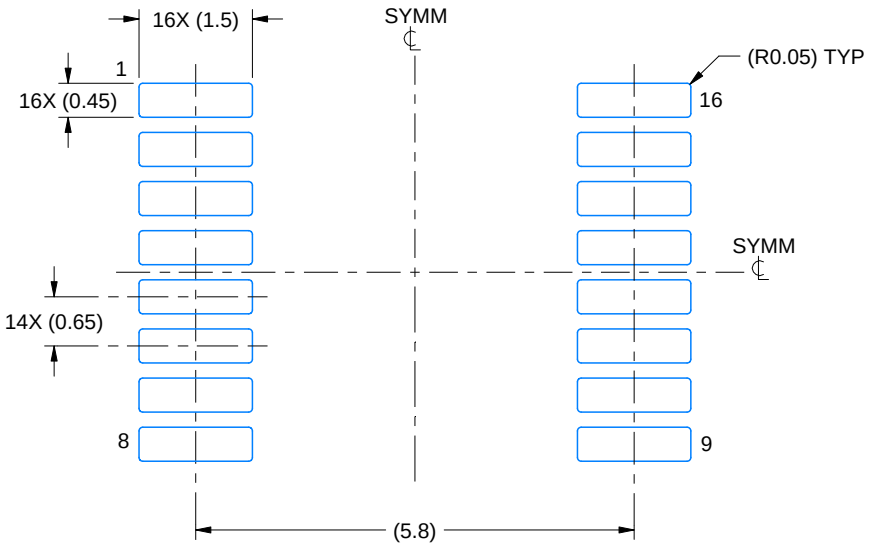
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

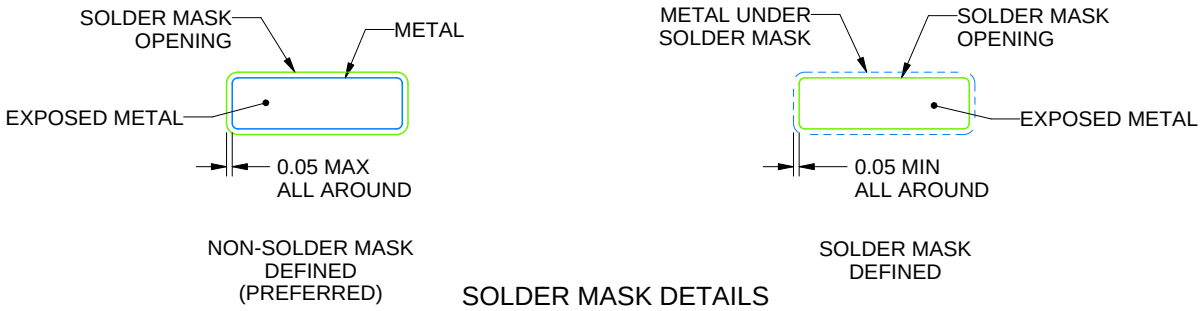


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

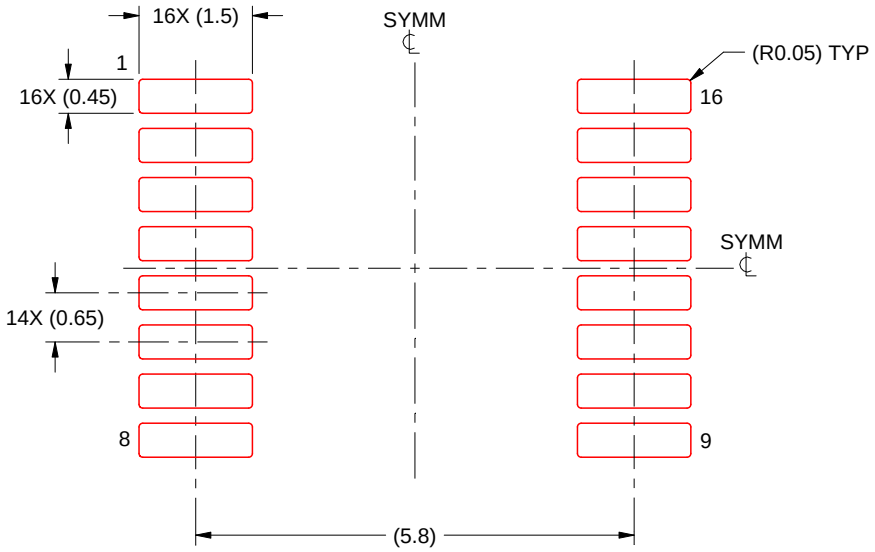


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

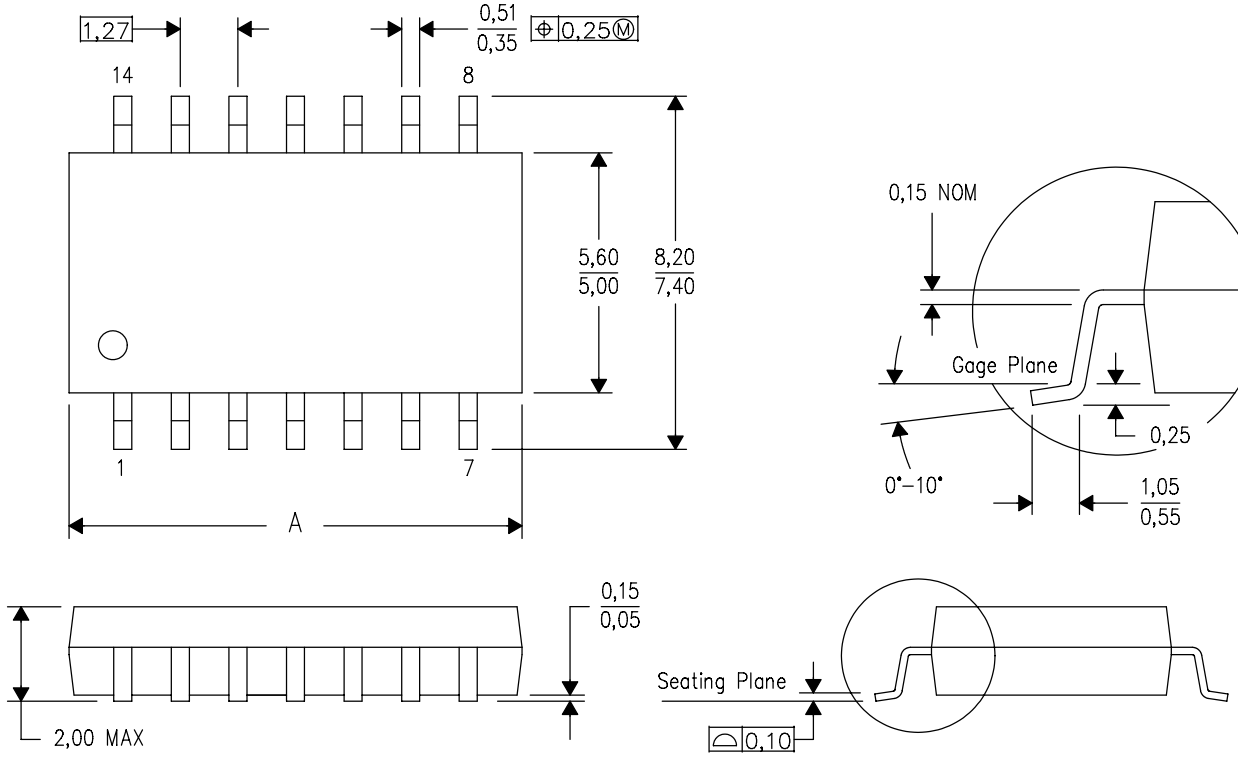
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

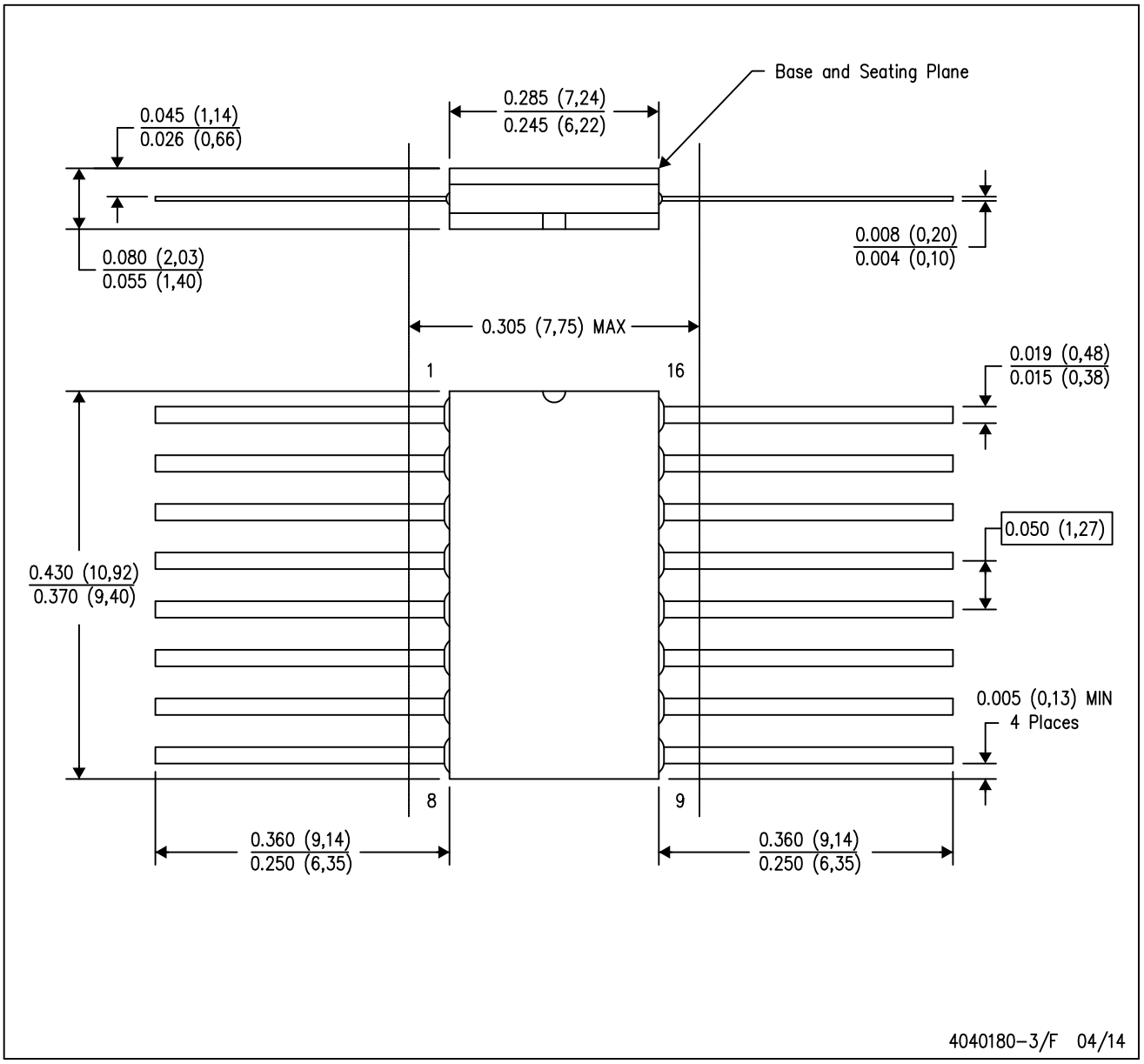


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK

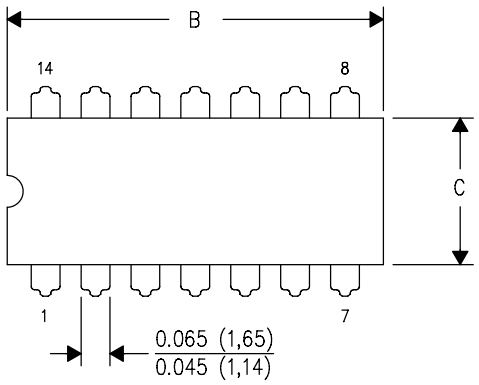


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

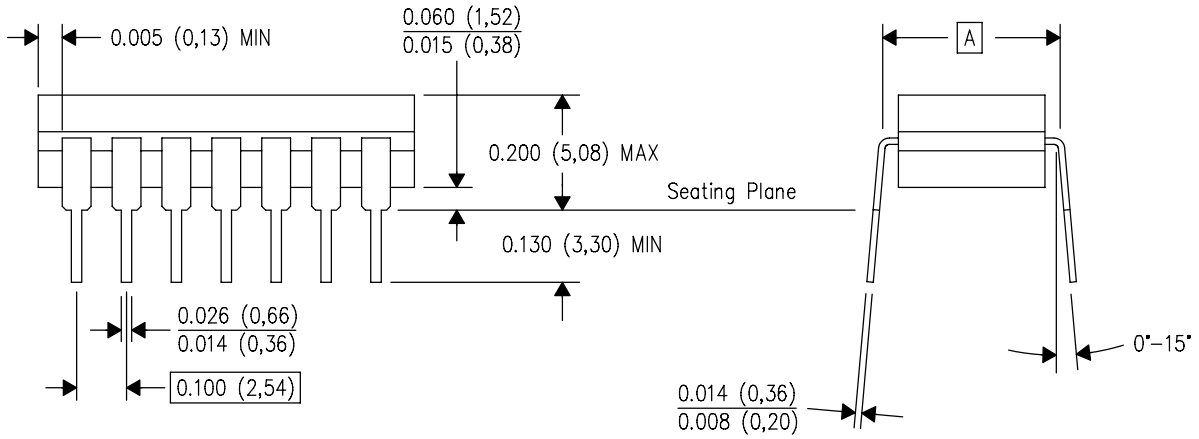
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



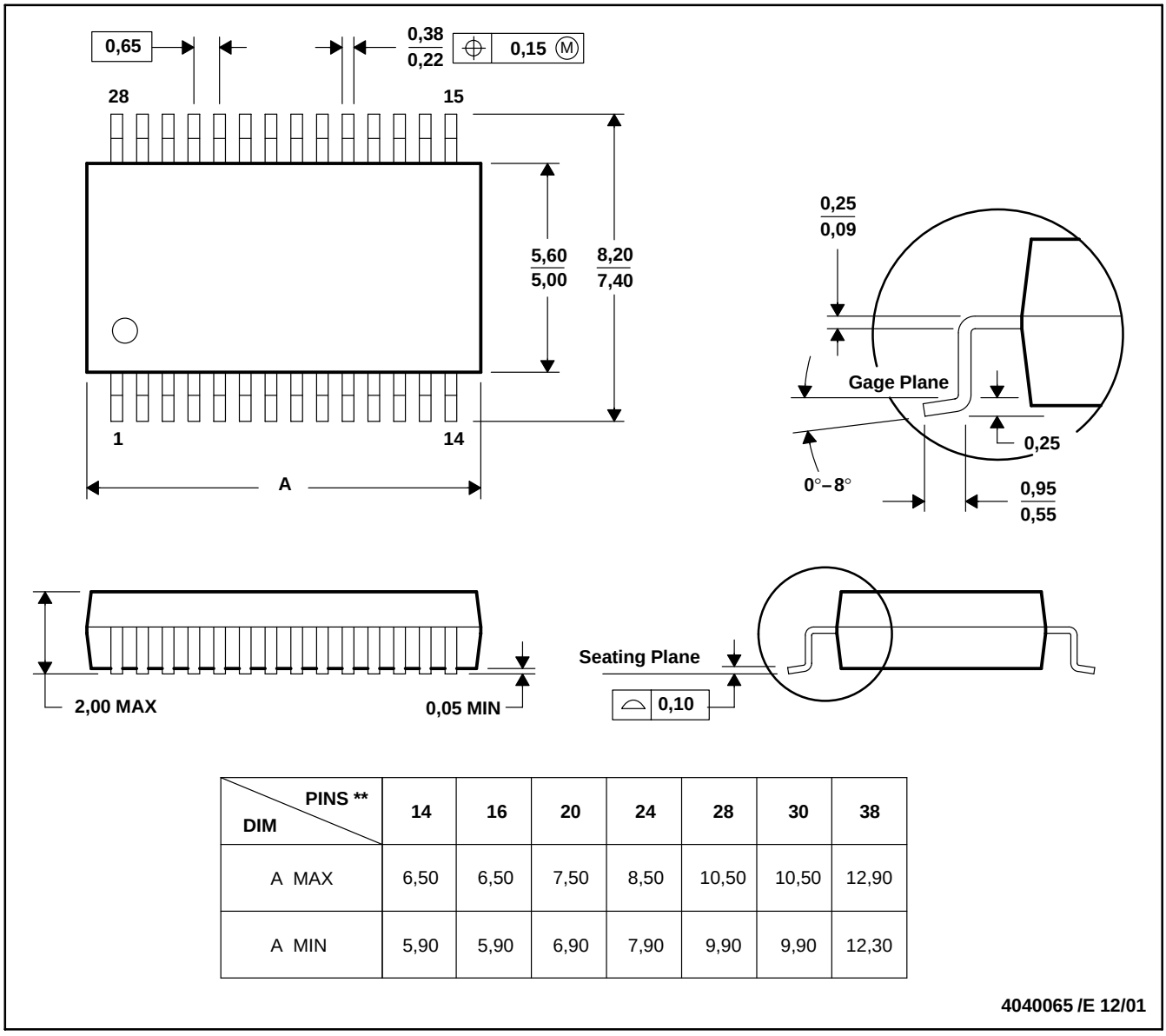
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

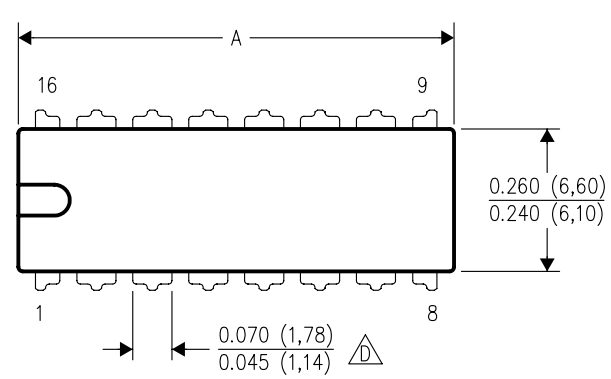
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

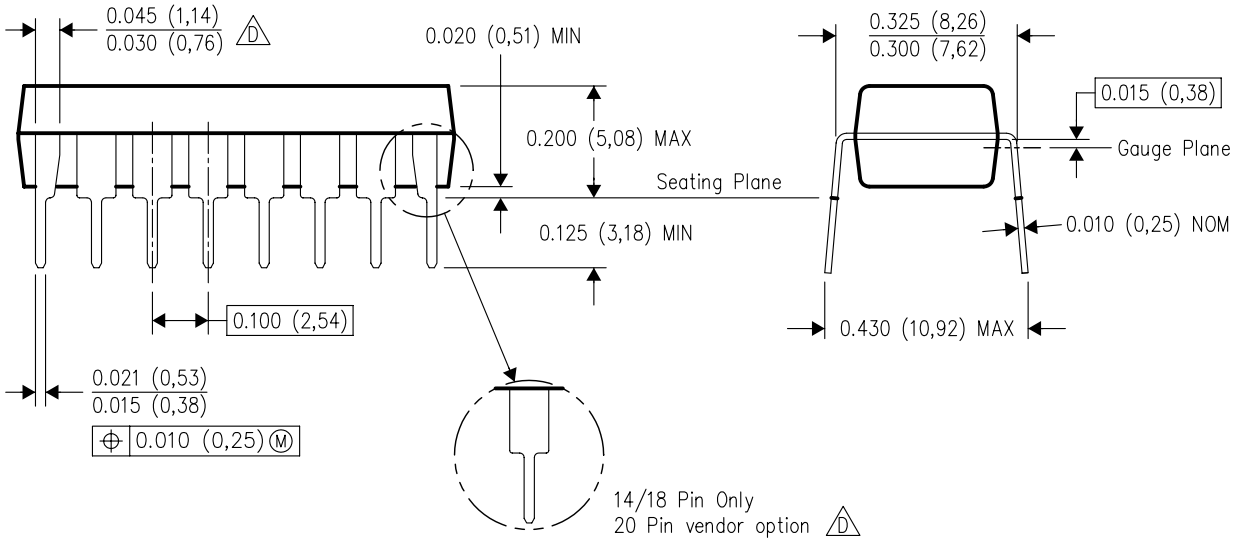
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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