National Semiconductor

December 2004

# LM2648
# Two-Phase, Synchronous Step-Down 3-Channel Switching Regulator Controller

## General Description

The LM2648 consists of two current mode and two voltage mode synchronous buck regulator controllers providing 3 outputs at a switching frequency of 300kHz.

Each pair of switching regulator controllers operate 180˚ out of phase. This feature reduces the input ripple RMS current, thereby significantly reducing the required input capacitance. The two current mode regulator outputs operate as a dual-phase, single output regulator for high current applications.

Current-mode feedback control on Channel 3 assures superior line and load regulation and wide loop bandwidth assures excellent response to fast load transients. Channels 1 and 2 employ voltage-mode feedback control.

The LM2648 features analog soft-start circuitry that is independent of the output load and output capacitance. This makes the soft-start behavior more predictable than traditional soft-start circuits. Sequential startup is built in and requires a single capacitor to set the timing.

The LM2648 has over-voltage protection and under-voltage protection for all outputs. Two additional comparator inputs (analog and logic level) are provided to shut down the IC for any user defined protection. The FAULT_DELAY pin allows delayed shut off time for the IC during an under-voltage or PROT-IN2 fault. The LM2648 also features an adjustable UVLO feature.

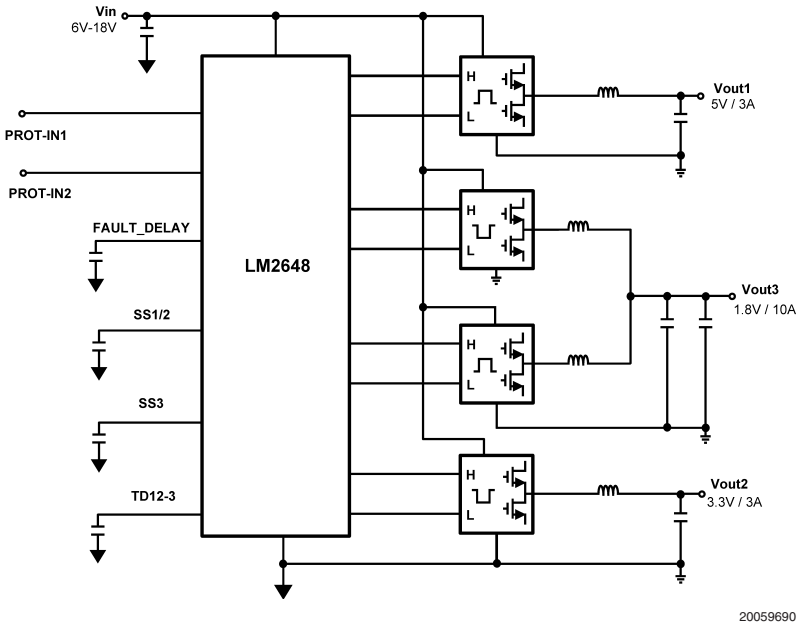
## Features

- Four synchronous buck regulators
- Channel 3: Two-phase, current mode controller
- 4.5V to 18V input range
- Built in sequential startup
- Channels 1 and 2: Independent, 180˚ out of phase voltage mode controllers
- Single soft start for channels 1 and 2
- Adjustable cycle-by-cycle current limit for each channel
- Adjustable reference current
- Adjustable input under-voltage lockout
- Output over-voltage latch protection
- Output under-voltage protection with delay
- Two comparator inputs for user defined protection - one with delay
- Thermal shutdown
- Self-discharge of output capacitors when the regulator is off
- TSSOP package

## Applications

- Embedded Computer Systems
- Interactive Games
- Set-top Boxes/Home Gateways

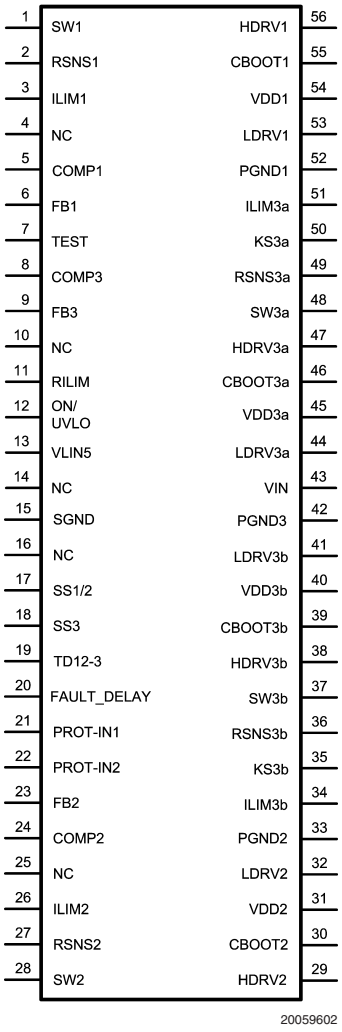
## Block Diagram




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## Connection Diagram

**TOP VIEW**




20059602

**56-Lead TSSOP (MTD)**
**Order Number LM2648MTD**
**See NS Package Number MTD56**

## Pin Descriptions

**SW1 (Pin 1):** Switch-node connection for Channel 1, which is connected to the source of the top MOSFET of Channel 1. It serves as the negative supply rail for the top-side gate drive, HDRV1.

**RSNS1 (Pin 2):** The negative (-) Kelvin sense for the internal current limit comparator of Channel 1. Connect this pin to the low side of the current sense resistor that is placed between VIN and the drain of the top MOSFET. Always use a separate trace to connect this pin.

**ILIM1 (Pin 3):** Current limit threshold setting for Channel 1. It sinks a variable current adjusted by RILIM (Pin11), which is converted to a voltage through a resistor connected from this pin to the top of the current sense resistor. The voltage across the resistor is compared with the voltage across the external current sense resistor to determine if an overcurrent condition has occurred on Channel 1.

**NC (Pin 4):** All NC pins should be connected to SGND.

**COMP1 (Pin 5):** Compensation pin for Channel 1. This is the output of the internal error amplifier. The compensation network should be connected between this pin and the feedback pin, FB1 (PIN 6).

**FB1 (Pin 6):** Feedback input for channel 1. Connect to Vout through a voltage divider to set the channel 1 output voltage.

**TEST (Pin 7):** Connect to SGND.

**COMP3 (Pin 8):** Compensation pin for Channel 3. This is the output of the internal transconductance amplifier. The compensation network should be connected between this pin and SGND.

**FB3 (Pin 9):** Feedback input for channel 3. Connect to Vout through a voltage divider to set the Channel 3 output voltage.

**NC (Pin 10):** All NC pins should be connected to SGND.

**RILIM (Pin 11):** Connect a resistor from this pin to SGND to set the internal ILIM reference current.

**ON/UVLO (Pin 12):** This is a dual function pin providing thresholds for user adjustable UVLO and device shutdown.

## Pin Descriptions (Continued)

Thresholds are 1.2V and 1.9V typical for shutdown and UVLO respectively. Connect to Vin through a voltage divider to set the external UVLO threshold.

**VLIN5 (Pin 13):** The output of the internal 5V LDO regulator derived from VIN. It supplies the internal bias for the chip and supplies the bootstrap circuitry for gate drive. Bypass this pin to signal ground with a minimum of 4.7uF capacitor. VLIN5 should not be used as an external voltage supply.

**NC (Pin 14):** All NC pins should be connected to SGND.

**SGND (Pin 15):** The ground connection for the signal-level circuitry. It should be connected to the ground rail of the system.

**NC (Pin 16):** All NC pins should be connected to SGND.

**SS1/2 (Pin 17):** This pin is the soft start control for channels 1 and 2. Connect a capacitor from this pin to SGND to control the ramp rate of the output voltage during startup.

**SS3 (Pin 18):** The soft start pin for channel 3. See Pin 17 (SS1/2).

**TD12-3 (Pin 19):** Sequential start timing pin. A capacitor from this pin to ground sets the delay time between channel 1 and 2 and channel 3 entering softstart.

**FAULT_DELAY (Pin 20):** A capacitor from this pin to ground sets the delay time for UVP and PROT-IN2 latch off. The capacitor is charged from a 5uA current source. When the FAULT_DELAY capacitor charges to 2V (typical), the system immediately latches off. Connecting this pin to ground will disable the UVP and PROT-IN2 functions.

**PROT_IN1 (Pin 21):** A comparator input that latches off all channels simultaneously when the applied voltage is above 1.239V (typical) voltage level.

**PROT_IN2 (Pin 22):** A TTL/CMOS compatible input that activates FAULT_DELAY when the applied voltage is above a 1.45V typical threshold.

**FB2 (Pin 23):** Feedback input for channel 2. Connect to Vout through a voltage divider to set the Channel 2 output voltage.

**COMP2 (Pin 24):** Compensation pin for Channel 2. This is the output of the internal error amplifier. The compensation network should be connected between this pin and the feedback pin FB2 (Pin 23).

**NC (Pin 25):** All NC pins should be connected to SGND.

**ILIM2 (Pin 26):** Current limit threshold setting for Channel 2. See ILIM1 (Pin 3).

**RSNS2 (Pin 27):** The negative (-) Kelvin sense for the internal current limit comparator of Channel 2. See RSNS1 (Pin 2).

**SW2 (Pin 28):** Switch-node connection for Channel 2. See SW1 (Pin1).

**HDRV2 (Pin 29):** Top-side gate-drive output for Channel 2. HDRV is a floating drive output that rides on the corresponding SW node voltage.

**CBOOT2 (Pin 30):** Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 2 top-side gate drive. Connect this pin to VDD2 (Pin 31) through a diode, and connect the low side of the bootstrap capacitor to SW2 (Pin28).

**VDD2 (Pin 31):** The supply rail for the Channel 2 low-side gate drive. Connected to VLIN5 (Pin 13) through a 4.7ohm resistor and bypassed to PGND with a ceramic capacitor of at least 1uF. Tie all VDDx pins together.

**LDRV2 (Pin 32):** Low-side gate-drive output for Channel 2.

**PGND2 (Pin 33):** The power ground connection for channel 2. Connect to the ground rail of the system.

**ILIM3b (Pin 34):** Current limit threshold setting for Channel 3b. See ILIM1 (Pin 3).

**KS3b (Pin 35):** The positive (+) Kelvin sense for the internal current sense amplifier of Channel 3b. Use a separate trace to connect this pin to the current sense point. It should be connected to VIN as close as possible to the node of the current sense resistor.

**RSNS3b (Pin 36):** The negative (-) Kelvin sense for the internal current sense amplifier of Channel 3b. See RSNS1 (Pin 2).

**SW3b (Pin 37):** Switch-node connection for Channel 3b. See SW1 (Pin1).

**HDRV3b (Pin 38):** Top-side gate-drive output for Channel 3b. See HDRV2 (Pin 29).

**CBOOT3b (Pin 39):** Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 3b top-side gate drive. See CBOOT2 (Pin 30).

**VDD3b (Pin 40):** The supply rail for the Channel 3b low-side gate drive. Tie all VDDx pins together.

**LDRV3b (Pin 41):** Low-side gate-drive output for Channel 3b.

**PGND3 (Pin 42):** The power ground connection for channel 3. Connect to the ground rail of the system.

**VIN (Pin 43):** The power input pin for the chip. Connect to the positive (+) input rail of the system. Bypass to PGND with a 1uF capacitor.

**LDRV3a (Pin 44):** Low-side gate-drive output for Channel 3a.

**VDD3a (Pin 45):** The supply rail for the Channel 3a low-side gate drive. Tie all VDDx pins together.

**CBOOT3a (Pin 46):** Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 3a top-side gate drive. See CBOOT2 (Pin 30).

**HDRV3a (Pin 47):** Top-side gate-drive output for Channel 3a. See HDRV2 (Pin 29).

**SW3a (Pin 48):** Switch-node connection for Channel 3a. See SW1 (Pin1).

**RSNS3a (Pin 49):** The negative (-) Kelvin sense for the internal current sense amplifier of Channel 3a. See RSNS1 (Pin 2).

**KS3a (Pin 50):** The positive (+) Kelvin sense for the internal current sense amplifier of Channel 3a. See KS3b (Pin 35).

**ILIM3a (Pin 51):** Current limit threshold setting for Channel 3a. See ILIM1 (Pin 3).

**PGND1 (Pin 52):** The power ground connection for channel 1. Connect to the ground rail of the system.

**LDRV1 (Pin 53):** Low-side gate-drive output for Channel 1.

**VDD1 (Pin 54):** The supply rail for the Channel 1 low-side gate drive. Tie all VDDx pins together.

**CBOOT1 (Pin 55):** Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 1 top-side gate drive. See CBOOT2 (Pin 30).

**HDRV1 (Pin 56):** Top-side gate-drive output for Channel 1. See HDRV2 (Pin 29).

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

Voltages from the indicated pins to SGND/PGND:

| | |
|---|---|
| VIN, ILIMx, KS3a, KS3b | −0.3V to 20V |
| SWx, RSNSx | −0.3V to (VIN + 0.3)V |
| FB1, FB2, FB3x, VDDx,ON/UVLO | −0.3V to 7V |
| COMPx, FAULT_DELAY, SSx | −0.3V to (VLIN5 + 0.3)V |
| CBOOT1 to SW1, CBOOT2 to SW2, CBOOT3x to SW3x | −0.3V to 7V |
| LDRV1, LDRV2, LDRV3x | −0.3V to (VDD+0.3)V |
| HDRV1 to SW1, HDRV2 to SW2, HDRV3x to SW3x | −0.3V |
| HDRV1 to CBOOT1, HDRV2 to CBOOT2, HDRV3x to CBOOT3x | 0.3V |
| Power Dissipation ($T_A$ = 25˚C), (Note 2) | 1.3W |
| Ambient Storage Temperature Range | −65˚C to +150˚C |
| Soldering Dwell Time, Temperature (Note 3) | |
| Infrared | 10-20sec, 240˚C |
| Vapor Phase | 75sec, 219˚C |
| ESD Rating (Note 4) | 2kV |

## Operating Ratings (Note 1)

| | |
|---|---|
| VIN (VIN and VLIN5 separate) | 5.5V to 18V |
| VIN (VIN tied to VLIN5) | 4.5V to 5.5V |
| Junction Temperature | 0˚C to +125˚C |

## Electrical Characteristics

Unless otherwise specified, $V_{IN}$ = 12V, SGND = PGND = 0V, VLIN5 = VDD1 = VDD2 = VDD3x. Limits appearing in **boldface** type apply over the full operating junction temperature range. Specifications appearing in plain type are measured using low duty cycle pulse testing with $T_A$ = 25˚C (Note 5), (Note 6). Min/Max limits are guaranteed by design, test, or statistical analysis.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **System** | | | | | | |
| $\Delta V_{OUT}/V_{OUT}$ | Load Regulation | VIN = 12V, $V_{comp1,\ 2}$ = 1V to 3V, $V_{comp3}$ = 0.5V to 1.5V | | .04 | | % |
| $\Delta V_{OUT}/V_{OUT}$ | Line Regulation | 5.5V ≤ VIN ≤ 18V, $V_{compx}$ =1.25V | | .04 | | % |
| $V_{FB1}$, $V_{FB2}$ | Feedback Voltage | 5.5V ≤ VIN ≤ 18V | **1.218** | 1.239 | **1.260** | V |
| $V_{FB3}$ | Feedback Voltage | 5.5V ≤ VIN ≤ 18V | **1.220** | 1.241 | **1.262** | V |
| $I_{VIN}$ | Input Supply Current | $V_{ON/UVLO}$ > 2.25V (not switching) 5.5V ≤ VIN ≤ 18V | | 1.66 | **2.2** | mA |
| | | Standby 1.5V < $V_{ON/UVLO}$ < 1.7V | | | | |
| | | Shutdown (Note 7) $V_{ON/UVLO}$ = 0V | | 45 | **120** | µA |
| VLIN5 | VLIN5 Output Voltage | IVLIN5 = 0 to 50mA, 7V ≤ VIN ≤ 18V | **4.65** | 5.0 | **5.35** | V |
| **Current Limit** | | | | | | |
| $V_{Clos1,\ 2,\ 3}$ | Current Limit Comparator Offset ($V_{ILIMX}$-$V_{RSNSX}$) | | | 0 | ±7.0 | mV |
| $V_{CLx1,\ 2,\ 3}$ | Current Limit Sink Current | $R_{ILIM}$ = 1.238/20µA | **18.2** | 20 | **21.8** | µA |
| $V_{RILIM}$ | ILIM Reference Voltage | | | 1.238 | | V |
| **Soft Start** | | | | | | |
| $I_{ss1/2_SC}$ | Soft-Start Source Current | $V_{ss}$ = 1V | **0.5** | 2.05 | **3.8** | µA |
| $I_{ss3_SC}$ | Soft-Start Source Current | $V_{ss}$ = 1V | **0.5** | 2.05 | **3.8** | µA |
| $I_{ss1/2_SK}$ | Soft-Start Sink Current | $V_{ss1/2,\ 3}$ = 1V, ON/UVLO = 1.6V | **2** | 4.9 | **9** | µA |
| $I_{ss3_SK}$ | Soft-Start Sink Current | $V_{ss1/2,\ 3}$ = 1V, ON/UVLO = 1.6V | **2** | 5.0 | **9** | µA |
| $I_{SC_TD12-3}$ | Delay Timer Source Current | $V_{TD}$ = 1.5V | **6.2** | 9.8 | **13.2** | µA |

## Electrical Characteristics (Continued)

Unless otherwise specified, $V_{IN}$ = 12V, SGND = PGND = 0V, VLIN5 = VDD1 = VDD2 = VDD3x. Limits appearing in **boldface** type apply over the full operating junction temperature range. Specifications appearing in plain type are measured using low duty cycle pulse testing with $T_A$ = 25˚C (Note 5), (Note 6). Min/Max limits are guaranteed by design, test, or statistical analysis.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{SK_TD12-3}$ | Delay Timer Sink Current | $V_{TD}$ = 0.4V | **192** | 274 | **356** | µA |
| $V_{TD12-3}$ | Delay Timer Threshold Voltage | Rising | **1.70** | 1.94 | **2.20** | V |
| $I_{ss1/2_sc}$/ $I_{ss3_sc}$ | Soft-Start Source Current Ratio | | **-13%** | 1.0 | **+13%** | A/A |
| $I_{ss1/2_sc}$/ $I_{sc_TD12-3}$ | Soft-Start to Delay Timer Source Current Ratio | | **-32%** | 0.209 | **+32%** | A/A |
| **Shutdown** | | | | | | |
| $V_{Standby}$ | Standby Threshold (ON/UVLO pin) | Rising Shutdown to Standby | **0.95** | 1.2 | **1.44** | V |
| | Hysteresis | | | 149 | | mV |
| $V_{ON}$ | ON Threshold (ON/UVLO pin) | Rising Standby to On | **1.75** | 1.98 | **2.20** | V |
| | Hysteresis | | | 205 | | mV |
| $S_{W_R1, 2}$ | SW1, 2 ON Resistance | $V_{SW1}$ = $V_{SW2}$ = 0.4V | 440 | 570 | 700 | Ω |
| $S_{W_R3a, 3b}$ | SW3a, 3b ON Resistance | $V_{SW3a}$ = $V_{SW3b}$ = 0.4V | 200 | 249 | 310 | Ω |
| $V_{SW_dis}$ | SW3a Quick Discharge Threshold at FB3 (falling edge) | LDRV3a = High | | .81 | | V |
| **Protection** | | | | | | |
| $I_{SC_FAULTDELAY}$ | FAULT_DELAY source current | FAULT_DELAY = 2.0V | **3.54** | 4.7 | **5.9** | µA |
| $I_{SK_FAULTDELAY}$ | FAULT_DELAY sink current | FAULT_DELAY = 0.4V | | 0.27 | | mA |
| $V_{FAULT_DELAY}$ | FAULT_DELAY threshold Voltage | Rising | **1.75** | 1.96 | **2.20** | V |
| $V_{UVP}$ | FB1, 2, 3 Under Voltage Protection Latch Threshold | As a percentage of nominal output voltage (falling edge) | **75** | 80.6 | **86** | % |
| | Hysteresis | | | 4 | | % |
| $V_{OVP}$ | FB1, 2, 3 Over-voltage Shutdown Latch Threshold | As a percentage of nominal output voltage (rising edge) | **106** | 112 | **119** | % |
| $V_{UVLO_INT}$ | VLIN5 Under Voltage Lockout Threshold | Rising | | 4.2 | | V |
| | Hysteresis | | | 8 | | % |
| $V_{PROT-IN1}$ | Analog protection threshold | | **1.19** | 1.239 | **1.4** | V |
| $V_{PROT-IN2}$ | Logic protection threshold | | **0.8** | 1.48 | **2** | V |
| $I_{sk_prot-in2}$ | PROT-IN2 sink current | | | 2 | | µA |
| **Gate Drive** | | | | | | |
| $I_{CBOOT}$ | CBOOTx Leakage Current | $V_{CBOOTX}$ = 7V | | 10 | | nA |
| $I_{SC_DRV}$ | HDRVx and LDRVx Source Current | HDRV = LDRV = 2.5V | | 0.5 | | A |
| $I_{sk_HDRV}$ | HDRVx Sink Current | HDRVX = 2.5V | | 0.8 | | A |

## Electrical Characteristics (Continued)

Unless otherwise specified, $V_{IN}$ = 12V, SGND = PGND = 0V, VLIN5 = VDD1 = VDD2 = VDD3x. Limits appearing in **boldface** type apply over the full operating junction temperature range. Specifications appearing in plain type are measured using low duty cycle pulse testing with $T_A$ = 25˚C (Note 5), (Note 6). Min/Max limits are guaranteed by design, test, or statistical analysis.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{sk_LDRV}$ | LDRVx Sink Current | LDRVX = 2.5V | | 1.1 | | A |
| $R_{HDRV}$ | HDRVx Source On-Resistance | $V_{CBOOTx}$ = 5V, $V_{SWx}$ = 0V | | 3.1 | | Ω |
| | HDRVx Sink On-Resistance | | | 1.5 | | Ω |
| $R_{LDRV}$ | LDRVx Source On-Resistance | $V_{VDDx}$ = 5V | | 3.1 | | Ω |
| | LDRVx Sink On-Resistance | | | 1.1 | | Ω |
| **Oscillator** | | | | | | |
| $F_{osc}$ | Oscillator Frequency | | **260** | 300 | **340** | kHz |
| Don_max1, 2 | Ch. 1, 2 Maximum On-Duty Cycle | $V_{FB1}$ = $V_{FB2}$ = 1V, Measured at pins HDRV1 and HDRV2 | **91** | 93 | | % |
| Don_max3 | Ch. 3a, 3b Maximum On-Duty Cycle | | **91** | 94 | | % |
| $T_{on_min}$ | Ch.3 Minimum On-Time | | | 166 | | ns |
| $SS_{OT_delta}$ | HDRVx Delta On Time | HDRV1 and 2 ; HDRV3a and b | | | 150 | ns |
| **Error Amplifier** | | | | | | |
| $I_{FB1, 2}$ | Ch. 1, 2 Feedback Input Bias Current | $V_{FB1, 2_}$ = 1V | | 43 | **150** | nA |
| $I_{comp1, 2_SC}$ | COMP Output Source Current | $V_{COMP1, 2}$ = 2.6V | **0.5** | 1.1 | | mA |
| $I_{comp1, 2_SK}$ | COMP Output Sink Current | $V_{COMP1, 2}$ = 1.2V | **.21** | 0.4 | | mA |
| GBW1, 2 | Unity Gain Bandwidth | | | 8.5 | | MHz |
| G1, G2 | Error amplifier DC Gain | | | 80 | | dB |
| SR1, 2 | Slew Rate | | | 4.5 | | V/µs |
| $V_{CLAMPH1, 2}$ | Error Amp High Clamp | | | 3.1 | | V |
| $V_{CLAMPL1, 2}$ | Error Amp Low Clamp | | | 1 | | V |
| $I_{FB3}$ | Ch 3 Feedback Input Bias Current | $V_{FB3}$ = 1.5V | | 74 | **±200** | nA |
| $I_{COMP3_SC}$ | COMP Output Source Current | $V_{comp3}$ = 1.5V | **27** | 115 | | µA |
| $I_{COMP3_SK}$ | COMP Output Sink Current | $V_{comp3}$ = 0.5V | **27** | 111 | | µA |
| gm3 | Transconductance | | | 650 | | µmho |
| $GI_{SNS3}$ | Ch.3 Current Sense Amplifier Gain | $V_{comp3}$ = 1.25V | 4.2 | 5.4 | 6.8 | |

## Electrical Characteristics (Continued)

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Range indicates conditions for which the device is intended to be functional, but does not guarantee specfic performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** The maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where $T_{JMAX}$ is the maximum junction temperature, $T_A$ is the ambient temperature and $\theta_{JA}$ is the junction-to-ambient thermal resistance of the specified package. The 1.3W rating results from using 125˚C, 25˚C, and 75˚C/W for $T_{JMAX}$, $T_A$, and $\theta_{JA}$ respectively. A $\theta_{JA}$ of 75˚C/W represents the worst-case condition of no heat sinking of the 56-pin TSSOP. A thermal shutdown will occur if the temperature exceeds the maximum junction temperature of the device. $\theta_{JC}$ = 26˚C/W.

**Note 3:** For detailed information on soldering plastic small-outline packages, refer to the *Packaging Databook* available from National Semiconductor Corporation.

**Note 4:** For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

**Note 5:** A typical is the center of characterization data measured with low duty cycle pulse tsting at $T_A$ = 25˚C. Typicals are not guaranteed.

**Note 6:** All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_A = T_J$ = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

**Note 7:** All switching controllers are off. The linear regulator VLIN5 remains on.

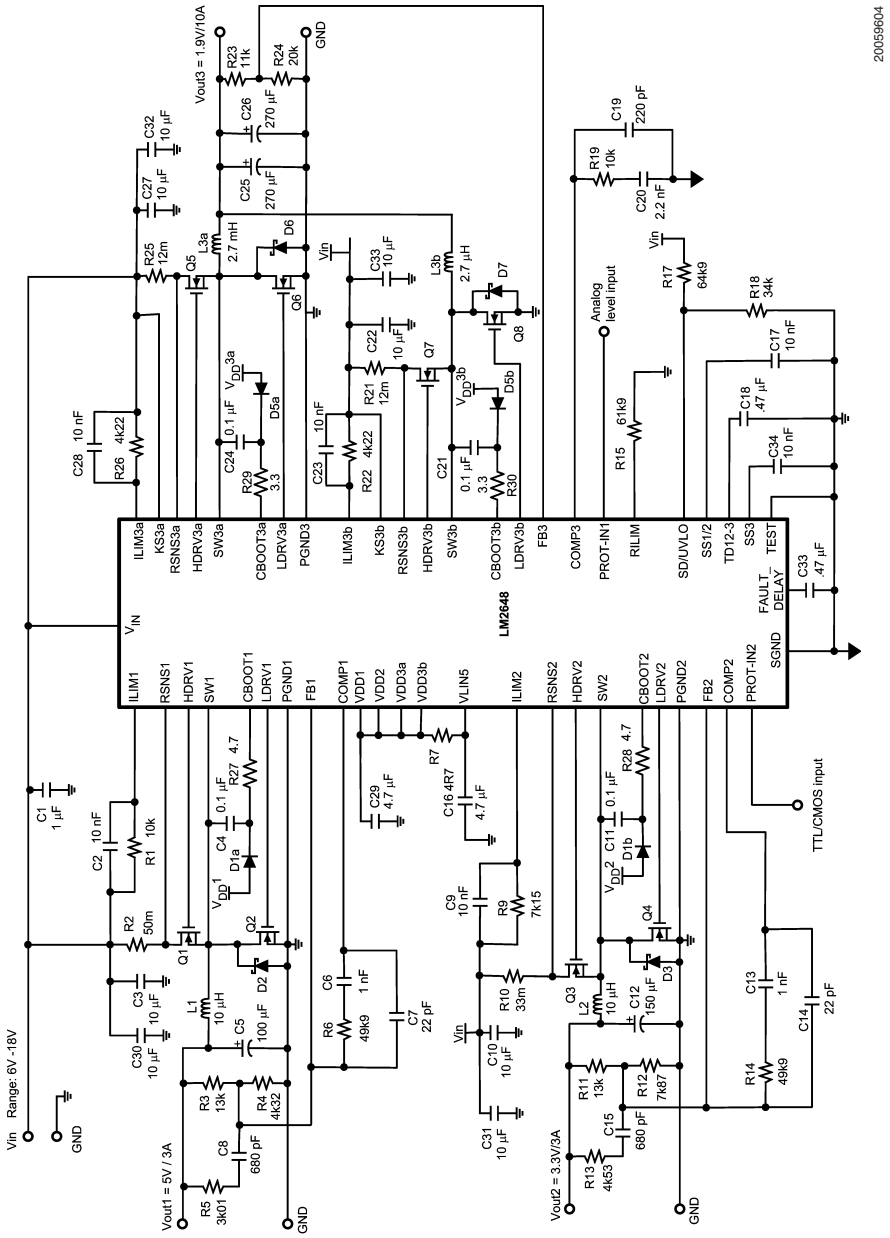
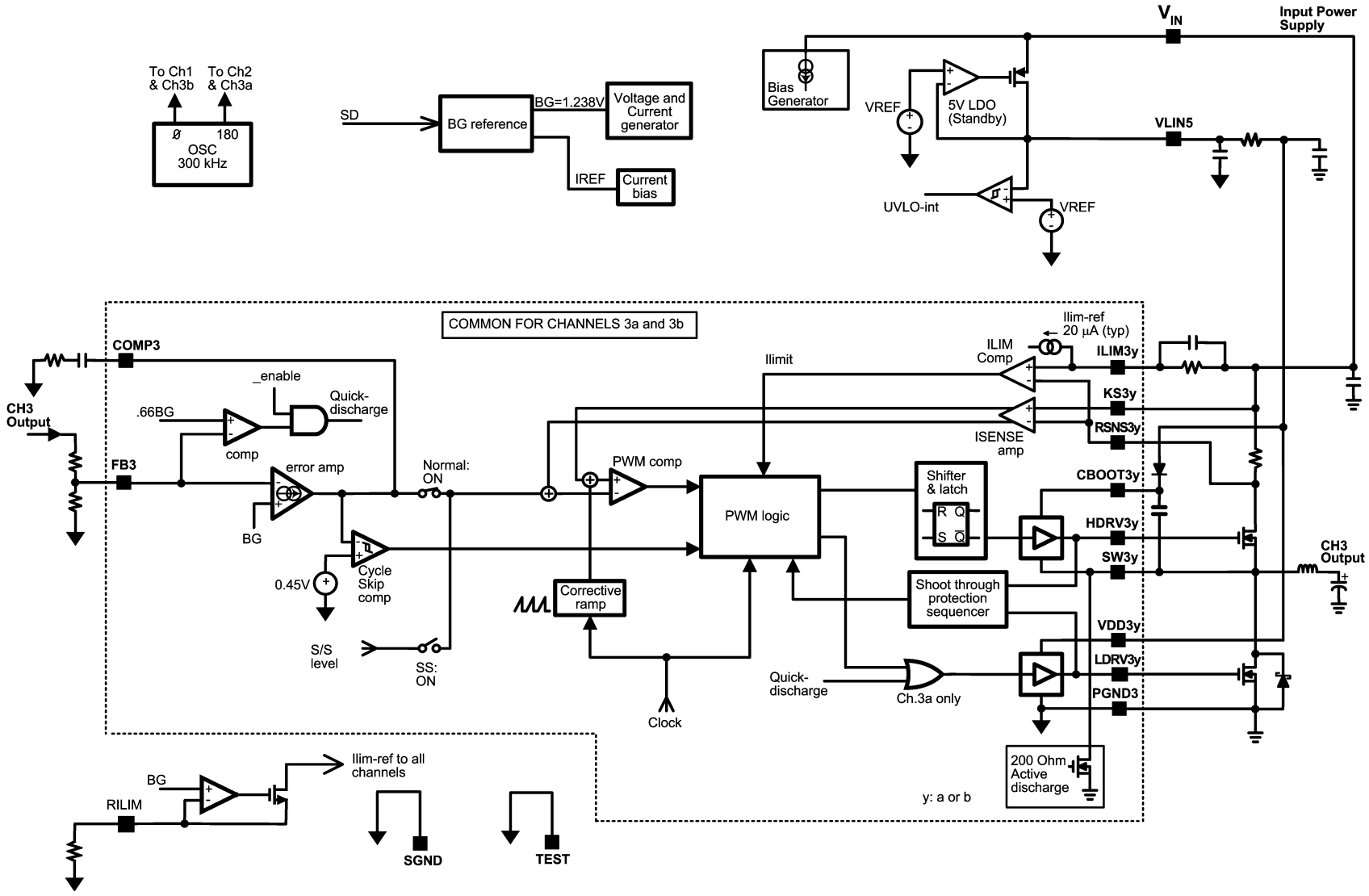
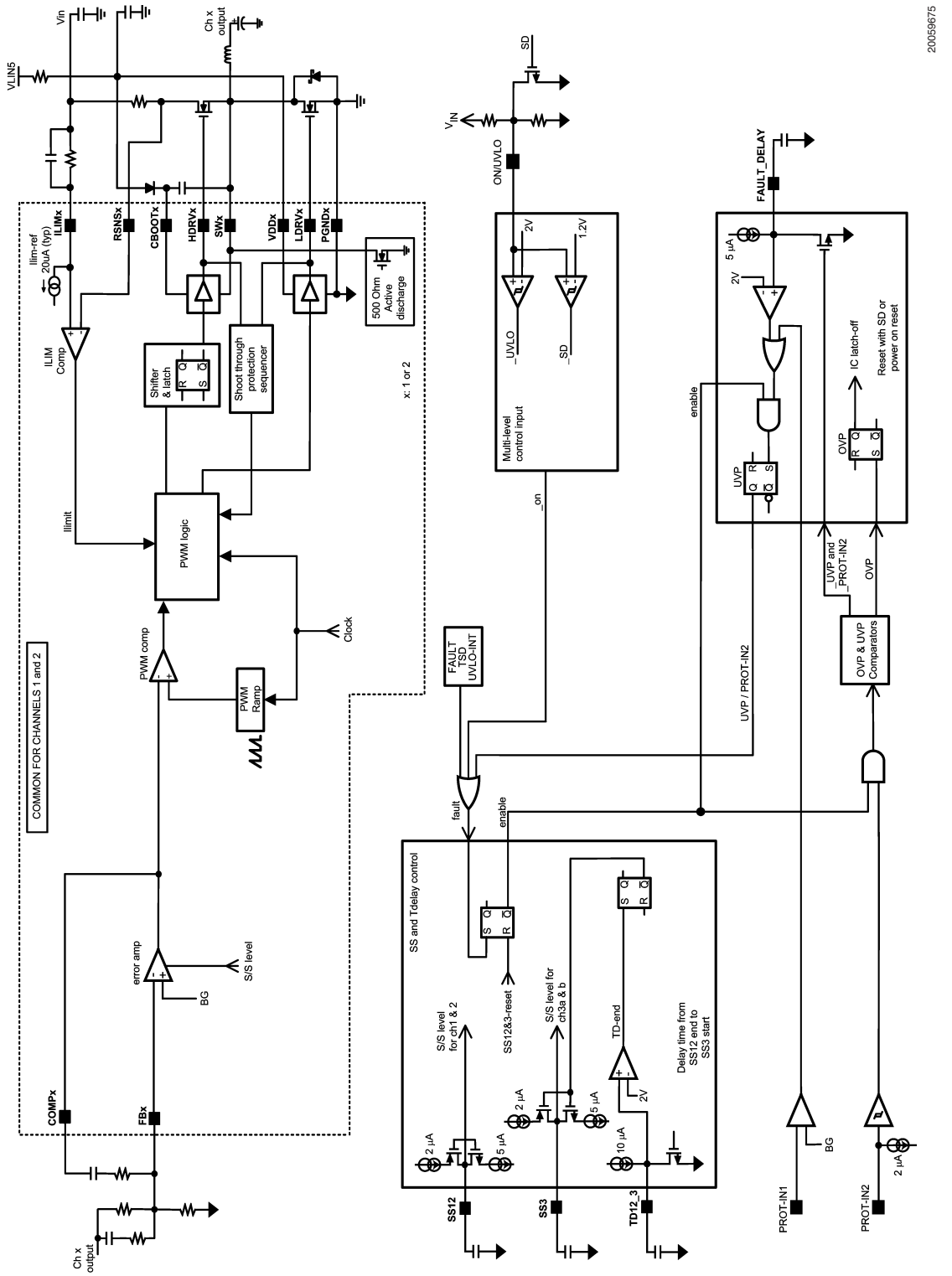



**FIGURE 1. Typical Application Circuit**

# Block Diagrams

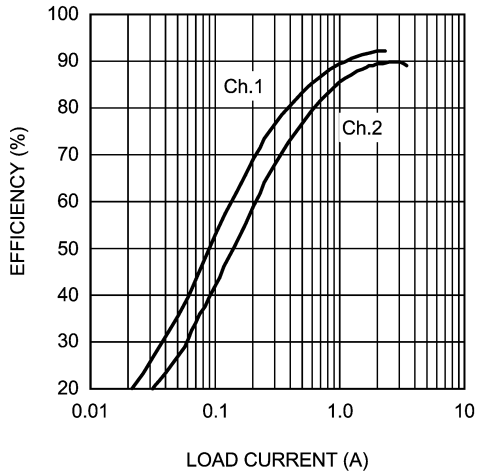


## Block Diagrams (Continued)



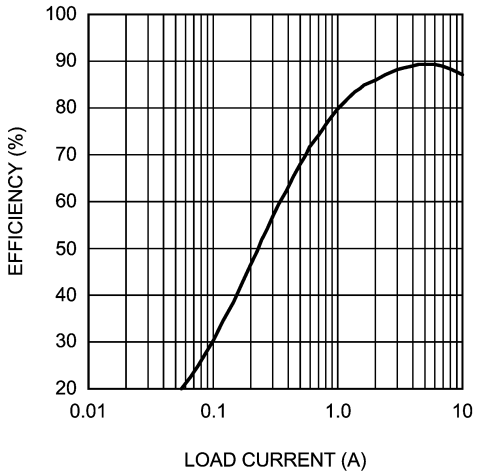
# Typical Performance Characteristics

**Efficiency vs Load Current**
**Ch.1 = 5V, Ch.2 = 3.3V, $V_{IN}$ = 12V, Ch.1/2/3: ON**



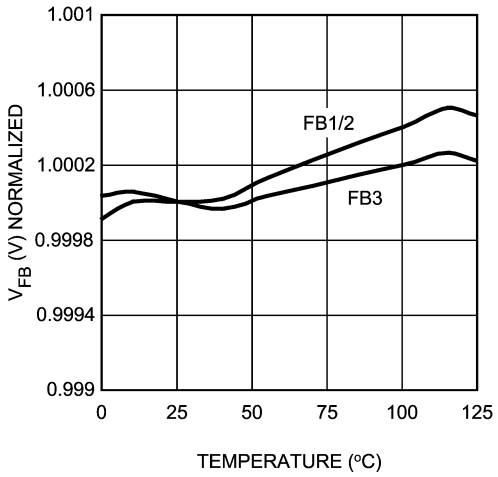

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**Efficiency vs Load Current**
**Ch.3 = 1.9V, $V_{IN}$ = 12V, Ch.1/2/3: ON**



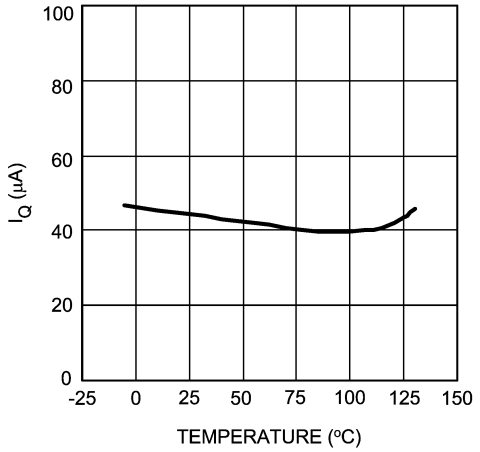

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**FB Voltage vs Temperature**



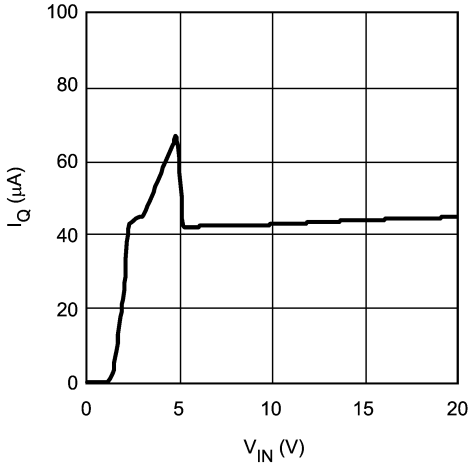

20059666

**Input Supply Current vs Temp. Shutdown Mode**



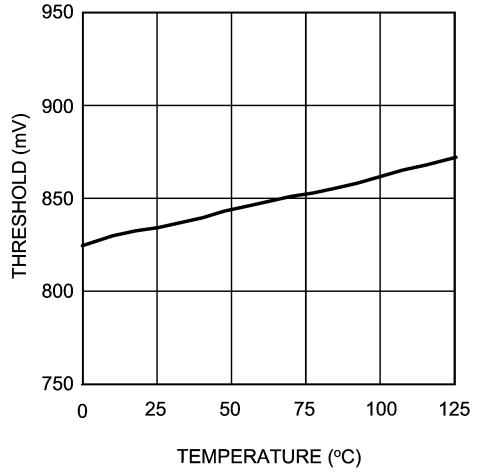

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**Input Supply Current vs $V_{IN}$ Shutdown Mode**




20059668

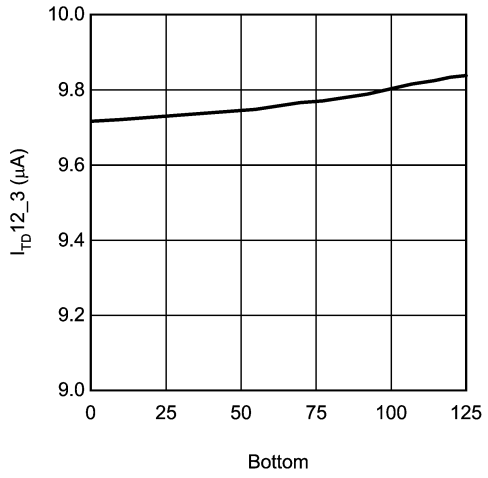
**FB3 Quick Discharge Threshold Voltage vs Temperature**




20059669

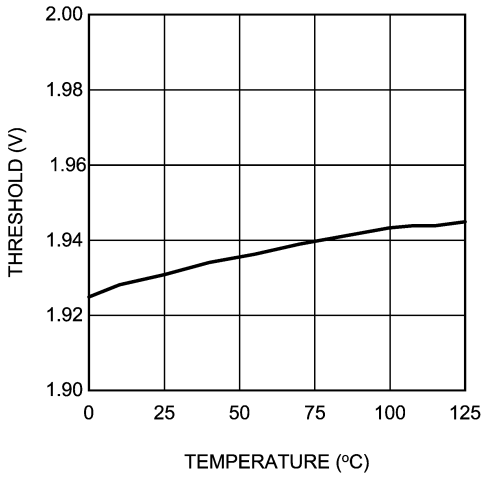
## Typical Performance Characteristics (Continued)

**TD1 2-3 Source Current vs Temperature**



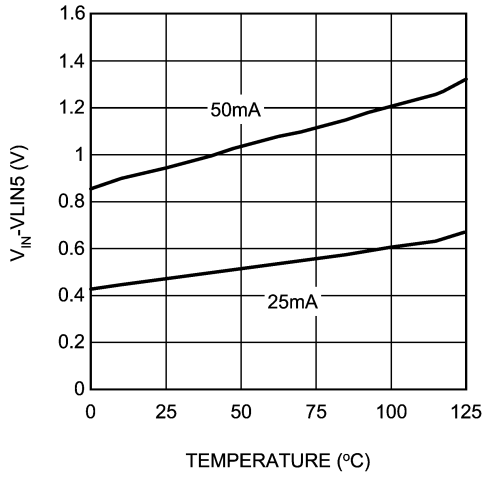

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**TD1 2-3 Threshold Voltage vs Temperature**



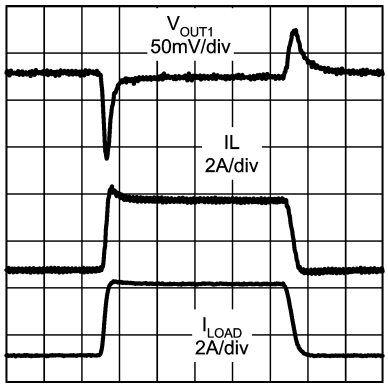

20059671

**VIN - VLIN5 Saturation Voltage vs Temperature**



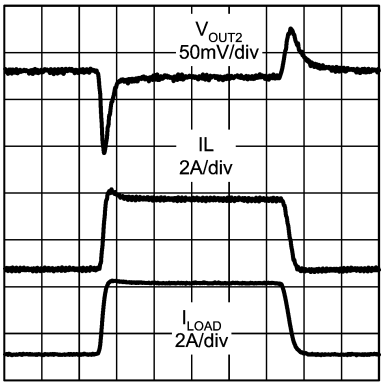

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**Ch.1 Load Transient Response**
**$5V_{OUT}$, $12V_{IN}$ (20µsec/div)**



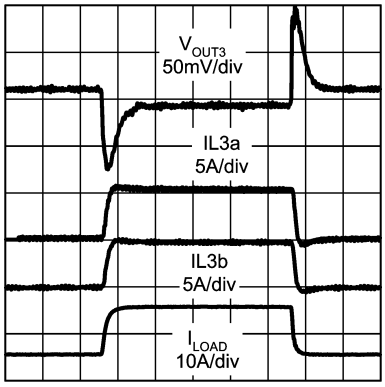

20059680

**Ch.2 Load Transient Response**
**$3.3V_{OUT}$, $12V_{IN}$ (20µsec/div)**




20059681

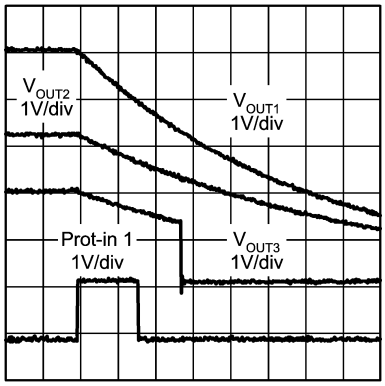
**Ch.3 Load Transient Response**
**$1.9V_{OUT}$, $12V_{IN}$ (20µsec/div)**




20059682

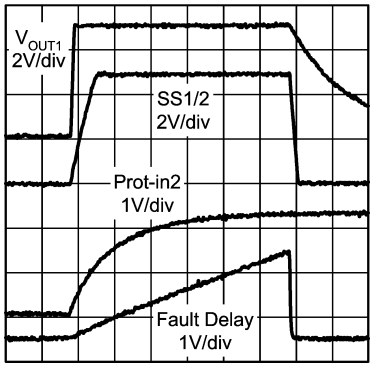
## Typical Performance Characteristics (Continued)

**Prot-in1 Shutdown (10ms/div)**



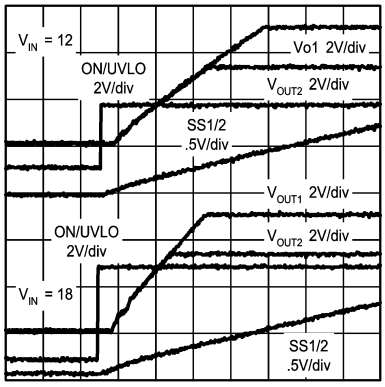

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**Prot-in2 Startup (40ms/div)**



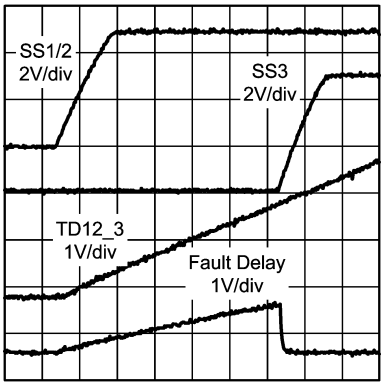

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**Softstart 1 and 2 (1ms/div)**



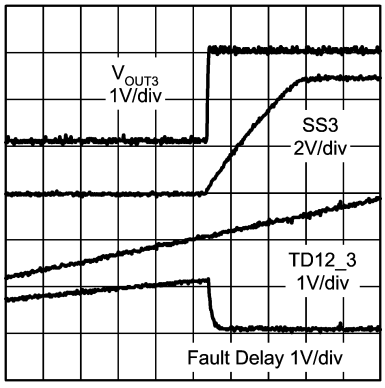

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**Ch.3 Sequential Startup (20ms/div)**



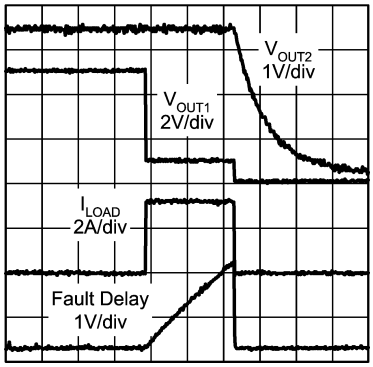

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**Ch.3 Softstart (10ms/div)**




20059687

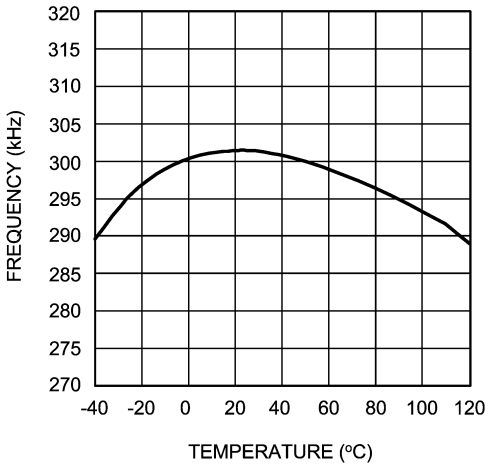
**Overcurrent UVP Shutdown (100ms/div)**




20059688

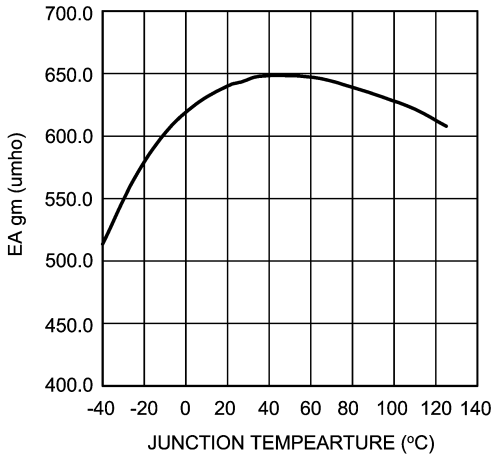
## Typical Performance Characteristics (Continued)

**Operating Frequency vs Temperature**




20059678

**Ch.3 Error Amplifier Gain vs Temperature**




20059679

# Operation Descriptions

### ON and UVLO

The ON/UVLO pin provides a dual threshold shutdown and under voltage lock out function. When this pin is pulled above 1.2V, the internal bias circuitry starts up and the device enters standby mode. The ON/UVLO pin has 149mV (typical) of hysteresis. This pin also provides a user programmable UVLO function. The lock out threshold at this pin is 1.98V with 200mV hysteresis (typical). Above this threshold, SS1/2 begins to source current. Connecting this pin through a voltage divider to $V_{IN}$ allows the user to set a secondary UVLO threshold above the internal UVLO level.

The internal UVLO threshold, which is sensed via the VLIN5 internal LDO, is 4.2V (typical). Below either UVLO threshold, both HDRVx and LDRVx will be turned off and the internal MOSFETs will be turned on to discharge the output capacitors through the SWx pins. As the input voltage increases again above 4.2V, UVLO will be de-activated, and the device will restart again from the soft start phase. If the voltage at VLIN5 remains below 4.5V, but above the 4.2V UVLO threshold, the device cannot be guaranteed to operate within specification.

If the input voltage is between 4.2V and 5.2V, the VLIN5 pin will not regulate, but will follow approximately 200mV below the input voltage. VLIN5 can be directly connected to the ON/UVLO pin to disable the external UVLO function. This is especially useful if the input voltage range will cause ON/UVLO to exceed its absolute maximum voltage rating (7V typ.).

### SOFT START

The soft start pins, SS1/2 and SS3, must each be connected to SGND through a capacitor. If the SS capacitor is too small, the duty cycle may increase too rapidly, causing the device to latch off due to output voltage overshoot above the OVP threshold. This becomes more likely in applications requiring low output voltage, high input voltage and light load. A typical value of approximately 10nF is recommended.

The size of the soft start capacitors controls the ramp up rate of the output voltages. As the input voltage rises or the ON/UVLO pin rises above 1.9V, an internal 2µA current charges the soft start capacitor. During soft start, the error amplifier output voltage is clamped and the duty cycle is controlled only by the soft start voltage. As the SSx pin voltage ramps up, the duty cycle increases proportional to the soft start ramp, causing the output voltage to ramp up. The rate at which the duty cycle increases depends on the capacitance of the soft start capacitor. The higher the capacitance, the slower the output voltage ramps up. When the corresponding output voltage exceeds 98% (typical) of the target voltage, the regulator switches from soft start to normal operating mode. At this time, the error amplifier clamp releases and feedback control takes over. The soft start capacitor value can be calculated with the following equation:

$$C_{ss} = \frac{I_{ss} \times V_{in} \times t}{V_{peak} \times V_{nom}}$$

Where t is the desired ramp-up time for the output voltage and Vnom is the target output voltage. Vpeak equals 2V for channels 1 and 2 and 1V for channel 3. When a fault occurs, the SSx pins are pulled low by a 5µA current sink. The device will not restart until the fault is reset and both SSx pins are below 80mV (typical). During soft start, over-voltage protection, prot-in1, prot-in2, under-voltage protection and current limit remain in effect.

### SEQUENTIAL STARTUP

Channel 3 is designed to start only after the delay pin (TD12-3) has reached its threshold. When channels 1 and 2 begin softstart, TD12-3 begins sourcing current (10µA typical). A capacitor from TD12-3 to SGND is used to set the delay time for channel 3 turn-on. Once TD12-3 has reached its threshold, SS3 begins sourcing current and the channel 3 output begins ramping up.

### OVER VOLTAGE PROTECTION (OVP)

If the output voltage on any channel rises above 110% (typical) of nominal, over voltage protection activates and all channels will latch off. There is a 10 µs delay between an over voltage event on channel 1 or 2 and latch off. When the OVP latch is set, the high side FET drivers, HDRVx, are immediately turned off and the low side FET drivers, LDRVx, are turned on to discharge the output capacitors through the inductors. To reset the OVP latch, either the input voltage must be cycled, or the device must be shut down at the ON/UVLO pin.

### UNDER VOLTAGE PROTECTION (UVP)

If the output voltage on any channel falls below 80% (typical) of nominal, under voltage protection activates. An under-voltage event will shut off the FAULT_DELAY MOSFET, which will allow the FAULT_DELAY capacitor to charge at 5µA (typical). When the capacitor charges to the FAULT_DELAY threshold (2V typical) all channels will latch off. FAULT_DELAY will then be disabled and discharged to 0V. When the UVP latch is set, both the high side and low side FET drivers will be turned off, and the output capacitors will be discharged through the internal MOSFET. If the fault condition is removed before the FAULT_DELAY threshold is reached, the pin will be discharged. To reset the UVP latch, either the input voltage must be cycled, or the device must be shut down. The UVP feature can be disabled by grounding the FAULT_DELAY pin.

**NOTE:** The FAULT_DELAY time must be greater than Tss1/2+Tss3+TD12-3. If it is not, the device will latch off due to an under voltage condition during startup. The FAULT_DELAY function becomes immediately active above the UVLO threshold, and is therefore active during soft start.

### COMPARATOR INPUT PROTECTION

The LM2648 features two PROT-IN pins, which can be used for any user defined protection scheme. When PROT-IN1 rises above 1.239V (typical), this sets the PROT-IN1 latch and shuts down the device. PROT-IN2 has a TTL/CMOS compatible input threshold with hysteresis. This pin also sinks a constant 2 µA (typical) current. A PROT-IN2 fault will activate FAULT_DELAY (see Under Voltage Protection) and can thus be deactivated by connecting FAULT_DELAY to SGND.

The protection latches will turn off both the high and low side FET drivers and will turn on the internal MOSFETs to discharge the output capacitors through the switch nodes. Like the UVP and OVP latches, both PROT-IN latches can only be reset by shutting down the device, or by cycling the input voltage.

## Operation Descriptions (Continued)

### ACTIVE OUTPUT DISCHARGE

Each channel has an embedded MOSFET with the drain connected to the SWx pin to provide a smooth controlled shutdown ramp. Each MOSFET will discharge the output capacitor of its channel if the device enters a fault state caused by one of the following conditions:

1. UVP or Prot-in2
2. UVLO (Internal or External)
3. Thermal shut-down (TSD)
4. Prot-in1

The MOSFETS provide 500Ω of discharge resistivity for channels 1 and 2 and 200Ω for channel 3.

Channel 3 has a secondary quick discharge feature. When the channel 3 output voltage falls below 65% of nominal, LDRV3a is turned on (LDRV3b remains off). This provides a faster discharge for the second half of the channel 3 shutdown process.

### CURRENT SENSING

As shown in *Figure 2*, the KSx and RSNSx pins are the inputs of the current sense amplifier for channel 3. Current sensing is accomplished by sensing the voltage across a current sense resistor connected from $V_{IN}$ to the drain of the top FET. Keeping the differential current-sense voltage below 200mV ensures linear operation of the current sense amplifier. Therefore, the current sense resistor must be small enough so that the current sense voltage does not exceed 200mV when the top FET is on. There is a leading edge blanking circuit that forces the top FET on for at least 166ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. Additionally, a minimum voltage of at least 50mV across the sense resistor is recommended to ensure a high SNR at the current sense amplifier.

Assuming a maximum sense voltage of 200mV, the current sense resistor can be calculated as follows:

$$R_{sns\ max} = \frac{200\,mV}{I_{max} + \frac{1}{2} I_{rip}}$$

where Imax is the maximum expected load current, including overload multiplier (ie:120%), and Irip is the inductor ripple current (*See Inductor Selection below*). The above equation gives the maximum recommended value for the sense resistor, Rsns. Conduction losses will increase with Rsns, thus lowering efficiency.

To ensure accurate current sensing, special attention in board layout is required. The KSx and RSNSx pins require separate traces to form a Kelvin connection to the corresponding current sense nodes.

Current sensing on channels 1 and 2 is used only to monitor the current limit. Current is sensed identical to channel 3, except that it does not require a KS pin and there is no blanking time. As with channel 3, RSNSx is connected to the bottom side of the current sense resistor. The top side of the current sense resistor connects to both VIN and the current limit resistor. Both KSx and RSNSx must be connected with separate traces to ensure accurate current limiting.

### CURRENT LIMITING

The peak current limit is set with an external resistor connected between the ILIMx pin and the top of the current sense resistor. An adjustable internal current sink on the ILIMx pin produces a voltage across the ILIM resistor to set the current limit threshold. This voltage is compared with the current sense voltage. A 10nF capacitor across the resistor is required to filter unwanted noise that could improperly trip the current limit comparator.

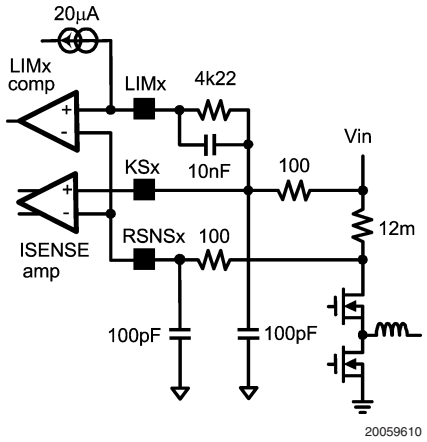



**FIGURE 2. Ch.3 Current Sense and Current Limit**

Current limit is activated when the inductor current is high enough to cause the voltage across the current sense resistor to exceed the voltage across the current limit resistor. This will toggle the comparator, which turns off the top FET immediately. The current limit comparator is disabled when the top FET is turned off and during the leading edge blanking time. The equation for current limit resistor, Rlim, is as follows:

$$R_{lim} = \frac{(I_{max} + \frac{1}{2} I_{rip}) R_{sns}}{I_{REF}}$$

Where $I_{max}$ is the load current at which the current limit comparator will be tripped, and $I_{REF}$ is the reference sink current (20µA typical). This calculated Rlim value guarantees that the minimum current limit will not be less than $I_{max}$. It is recommended that a 1% tolerance resistor be used.

### REFERENCE CURRENT SETTING

The ILIMx current sink value can be adjusted using the RILIM pin. The RILIM pin is connected through a resistor to SGND to set the reference current at the current limit pins (ILIMx). The resistor value can be determined using the following equation:

$$R_{IREF} = \frac{1.238}{I_{REF}}$$

Where $I_{REF}$ is the desired reference current. Generally, a default value of 61.9kΩ is used, which provides the recommended reference current of 20µA. Once an initial value is selected, $R_{IREF}$ can be adjusted to precisely trim the current limit setting on all three channels.

## Operation Descriptions (Continued)

### Channel 3 Dual Phase Operation

Channel 3 consists of two 180˚ out of phase converters operating in parallel to provide a single output voltage. In high current demand applications, current sharing between the two switching channels greatly reduces the stress and heat on the output stage components while lowering input ripple current. The sum of inductor ripple currents is also reduced which results in lowered output ripple voltage. When designing channel 3, simply design each switcher (3a and 3b) to supply half of the load current. Accurate current sensing is critical to ensure equal current sharing.

Since each switcher has separate current sense and limit pins, channel 3 can also be operated in single phase mode. This requires that either channel 3a or 3b remains unused. To operate channel 3 as a single phase controller, make the following pin connections to the unused channel. Connect ILIM3x and KS3x to VIN, RSNS3x and SW3x to GND, leave HDRV3x and LDRV3x open, and connect CBOOT3X to VDD3X.

### SWITCHING NOISE REDUCTION

Power MOSFETs are very fast switching devices. In synchronous rectifier converters, the rapid increase of drain current in the top FET coupled with parasitic inductance will generate unwanted Ldi/dt noise spikes at the source node of the FET (SWx node) and also at the VIN node. The magnitude of this noise will increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, it must be suppressed using one of the following methods.

It is strongly recommended to add R-C filters to the current sense amplifier inputs of channel 3 as shown in *Figure 2*. This will reduce the susceptibility to switching noise, especially during heavy load transients and short on-time conditions. The filter components should be connected as close as possible to the IC.

As shown in *Figure 3*, adding a resistor in series with the SWx pin will slow down the gate drive (HDRVx), thus slowing the rise and fall time of the top FET, yielding a longer drain current transition time.

Usually a 3.3Ω to 4.7Ω resistor is sufficient to suppress the noise. Top FET switching losses will increase with higher resistance values.

Small resistors (1-5 ohms) can also be placed in series with the HDRVx pin or the CBOOTx pin to effectively reduce switch node ringing. A CBOOT resistor will slow the rise time of the FET, whereas a resistor at HDRV will reduce both rise and fall times.

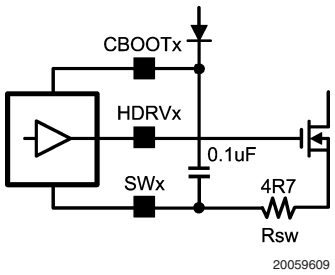



**FIGURE 3. SW Series Resistor**

### OUTPUT VOLTAGE SETTING

The output voltage for each channel is set by the ratio of a voltage divider as shown in *Figure 4*. The resistor values can be determined by the following equation:

$$R_1 = \frac{R_2}{\left(\frac{V_{nom}}{V_{fb}} - 1\right)}$$

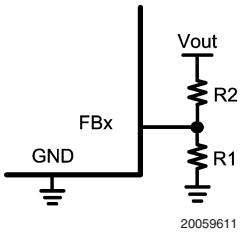



**FIGURE 4. Output Voltage Setting**

Although increasing the value of R1 and R2 will increase efficiency, this will also decrease accuracy. In the case of channels 1 and 2, increasing R2 will decrease loop gain, resulting in degraded transient response. The output voltage is limited by both maximum duty cycle and minimum on time. It is recommended that the nominal output voltage does not exceed 1V less than the minimum input voltage. In general, the minimum possible output voltage is approximately 1.3V. However, at maximum input voltage the minimum output will be determined by the minimum on time (166ns typ.) and may be as high as 1.35V for an input voltage of 18V.

For input voltages below 5.5V, VLIN5 should be connected to VIN through a small resistor (approximately 4.7Ω). This will ensure that VLIN5 does not fall below the UVLO threshold.

### LAYOUT RECOMMENDATIONS

To ensure proper operation, a few key layout guidelines should be followed.

The PGND and SGND pins and nodes should be connected to isolated ground planes which connect at a single point. This will help to keep the signal ground and thus the COMP and FB pins isolated from switching noise.

All current sensing and limiting pins should be Kelvin connected directly to the current sense points. This will help ensure accurate current sensing and limiting.

All FB voltage dividers should be placed close to the device, and the FB traces should be kept away from sources of noise.

Input capacitors should be connected as close as possible to the top of the current sense resistors.

## Component Selection

### INPUT CAPACITOR SELECTION

The fact that the switching channels of the LM2648 are 180˚ out of phase will reduce the RMS value of the ripple current seen by the input capacitors. This will help extend input capacitor life span and result in a more efficient system. Input capacitors must be selected that can handle both the maximum ripple RMS current at highest ambient tempera-

## Component Selection (Continued)

ture as well as the maximum input voltage. Input RMS ripple current can be approximately calculated with the equation below:

$$I_{irrm} = \sqrt{I_1^2 D_1 (1 - D_1) + I_2^2 D_2 (1 - D_2) - 2 I_1 I_2 D_1 D_2}$$

Where D1 is the duty cycle of channel 1 or 3a, whichever is larger, and D2 is the duty cycle of channel 2 or 3b, whichever is larger. I1 and I2 are the sum of the load currents of channels 1 nd 3a and of channels 2 and 3b respectively.

Additionally, the input capacitor should always be placed as close as possible to the current sense resistor.

When using ceramic input capacitors, care must be taken to limit transient voltage spikes during turn on. These spikes can be greater than twice the nominal input voltage and can easily exceed the maximum rating of the device.

Using an additional tantalum or other high ESR capacitor at the input is usually effective in dampening input spikes and protecting the device during turn on.

### OUTPUT CAPACITOR SELECTION

In applications that exhibit large and fast load current swings, the slew rate of such a load current transient may be beyond the response speed of the regulator. Therefore, to meet voltage transient requirements during worst-case load transients, special consideration should be given to output capacitor selection. The total combined ESR of the output capacitors must be lower than a certain value, while the total capacitance must be greater than a certain value. Also, in applications where the specification of output voltage regulation is tight and ripple voltage must be low, starting from the required output voltage ripple will often result in fewer design iterations.

### ALLOWED TRANSIENT VOLTAGE EXCURSION

The allowed output voltage excursion during a load transient ($\Delta$Vc_s) is:

$$\Delta V_{c_s} = (\delta\% - \varepsilon\%) \times V_{nom} - \frac{1}{2} V_{rip} .$$

Where $\pm\delta$% is the output voltage regulation window and $\pm\epsilon$% is the output voltage initial accuracy.

Example: Vnom = 5V, $\delta$% = 7%, $\epsilon$% = 3.4%, Vrip = 40mV peak to peak.

$$\Delta V_{c_s} = (7\% - 3.4\%) \times 5V - \frac{40\ mV}{2}$$
$$= 160\ mV.$$

Since the ripple voltage is included in the calculation of $\Delta$Vc_s, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply maximum load current change specification, $\Delta$Ic_s.

### MAXIMUM ESR CALCULATION

Unless the rise and fall times of a load transient are slower than the response speed of the control loop, if the total combined ESR (Re) is too high, the load transient requirement will not be met, no matter how large the capacitance.

The maximum allowed total combined ESR is:

$$R_{e_max} = \frac{\Delta V_{c_s}}{\Delta I_{c_s}}$$

Example: $\Delta$Vc_s = 160mV, $\Delta$Ic_s = 3A. Then Re_max = 53.3m$\Omega$.

Maximum ESR criterion can be used when the associated capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used in parallel.

### MINIMUM CAPACITANCE CALCULATION

In a switch mode power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the present switching cycle has just finished. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \times \left[\Delta V_{c_s} - \sqrt{(\Delta V_{c_s})^2 - (\Delta I_{c_s} \times R_e)^2}\right]}{V_{nom} \times R_e^2}$$

Notice it is already assumed the total ESR, Re, is no greater than Re_max, otherwise the term under the square root will be a negative value. Also, it is assumed that L has already been selected, therefore the minimum L value should be calculated before Cmin and after Re (see Inductor Selection below). Example: Re = 20m$\Omega$, Vnom = 5V, $\Delta$Vc_s = 160mV, $\Delta$Ic_s = 3A, L = 8$\mu$H

$$C_{min} = \frac{8\ \mu H \times \left[160\ mV - \sqrt{(160\ mV)^2 - (3A \times 20\ m\Omega)^2}\right]}{5 \times (20\ m\Omega)^2}$$
$$= 47\ \mu F.$$

Generally speaking, Cmin decreases with decreasing Re, $\Delta$Ic_s, and L, but with increasing Vnom and $\Delta$Vc_s.

### Inductor Selection

The size of the output inductor can be determined from the desired output ripple voltage, Vrip, and the impedance of the output capacitors at the switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in} - V_{nom}}{f \times V_{in}} \times \frac{V_{nom} \times R_e}{V_{rip}}$$

In the above equation, Re is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to Re. In the case of ceramic capacitors, replace Re with the true impedance.

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest input and output voltages and load

## Component Selection (Continued)

transient requirements should be considered. If an inductance value larger than Lmin is selected, make sure that the Cmin requirement is not violated.

Since inductor ripple current is often the criterion for selecting an output inductor, it is a good idea to double-check this value. The equation is:

$$I_{rip} = \frac{(V_{in} - V_{nom})}{f \times L} \times D$$

Where D is the duty cycle, defined by $V_{nom}/V_{in}$.

Also important is the ripple content, which is defined by Irip /Inom. Generally speaking, a ripple content of less than 50% is ok. Larger ripple content will cause too much loss in the inductor.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current and the RMS current rating should be higher than the maximum load current.

### MOSFET Selection

### BOTTOM FET SELECTION

During normal operation, the bottom FET is switching on and off at almost zero voltage. Therefore, only conduction losses are present in the bottom FET. The most important parameter when selecting the bottom FET is the on resistance (Rdson). The lower the on resistance, the lower the power loss. The bottom FET power loss peaks at maximum input voltage and load current. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$R_{dson_max} = \frac{1}{I_{max}^2 \times \left(1 - \frac{V_{nom}}{V_{in_max}}\right)} \times \frac{T_{j_max} - T_{a_max}}{[\,1 + TC \times (T_{j_max} - 25^oC)\,] \times R_{\theta ja}}$$

where Tj_max is the maximum allowed junction temperature in the FET, Ta_max is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on resistance which is typically in the range of 10,000ppm/˚C.

If the calculated Rdson_max is smaller than the lowest value available, multiple FETs can be used in parallel. This effectively reduces the Imax term in the above equation, thus reducing Rdson. When using two FETs in parallel, multiply the calculated Rdson_max by 4 to obtain the Rdson_max for each FET. In the case of three FETs, multiply by 9.

### TOP FET SELECTION

The top FET has two types of losses: switching loss and conduction loss. The switching losses mainly consist of crossover loss and bottom diode reverse recovery loss. Since it is rather difficult to estimate the switching loss, a general starting point is to allot 60% of the top FET thermal capacity to switching losses. The best way to precisely determine switching losses is through bench testing. The equation for calculating the on resistance of the top FET is thus:

$$R_{ds_max} = \frac{V_{in_min} \times .4}{I_{max}^2 \times V_{nom}} \times \frac{T_{j_max} - T_{a_max}}{[\,1 + TC \times (T_{j_max} - 25^oC)\,] \times R_{\theta ja}}$$

When using FETs in parallel, the same guidelines apply to the top FET as apply to the bottom FET.

### Loop Compensation

The general purpose of loop compensation is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked to determine small-signal performance. Loop gain is equal to the product of control-output transfer function and the output-control transfer function (the compensation network transfer function). Generally speaking it is a good idea to have a loop gain slope that is -20dB /decade from a very low frequency to well beyond the crossover frequency. The crossover frequency should not exceed one-fifth of the switching frequency, i.e. 60kHz in the case of LM2648. The higher the bandwidth is, the faster the load transient response speed will potentially be. However, if the duty cycle saturates during a load transient, further increasing the small signal bandwidth will not help. Since the control-output transfer function usually has very limited low frequency gain, it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain will be relatively large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the shape of the control-output plot.

**Channel 3**

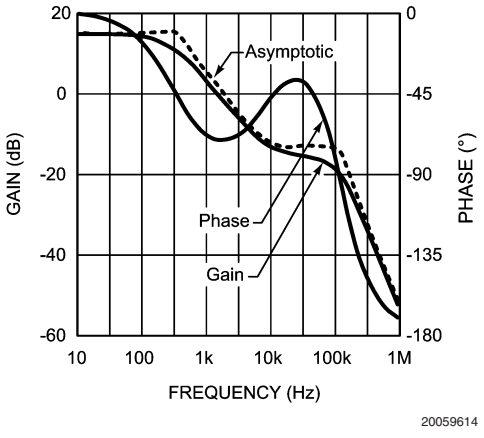



**FIGURE 5. Control-Output Transfer Function**

As shown in *Figure 5*, the control-output transfer function consists of one pole (fp), one zero (fz), and a double pole at fn (half the switching frequency). The following can be done to create a -20dB /decade roll-off of the loop gain: Place the first pole at 0Hz, the first zero at fp, the second pole at fz, and the second zero at fn. The resulting output-control transfer function is shown in *Figure 6*.

## Component Selection (Continued)

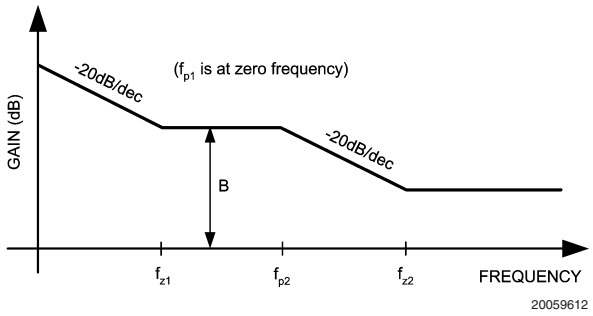



**FIGURE 6. Output-Control Transfer Function**

The control-output corner frequencies, and thus the desired compensation corner frequencies, can be determined approximately by the following equations:

$$f_z = \frac{1}{2\pi R_e C_o}$$

$$f_p = \frac{1}{2\pi R_o C_o} + \frac{.5}{2\pi L f C_o}$$

Since fp is determined by the output network, it will shift with loading (Ro) and duty cycle. First determine the range of frequencies (fpmin/max) of the pole across the expected load range, then place the first compensation zero within that range.

Example: $R_e$ = 20mΩ, $C_o$ = 100µF, L = 8 µH, $R_{omax}$ = 5V/100mA = 50Ω, $R_{omin}$ = 5V/3A = 1.7Ω:

$$f_z = \frac{1}{2\pi \times 20\ m\Omega \times 100\ \mu F} = 80\ kHz$$

$$f_p\ min = \frac{1}{2\pi \times 50\Omega \times 100\mu F} + \frac{.5}{2\pi \times 300k \times 8\mu \times 100\mu F} = 363Hz$$

$$f_p\ max = \frac{1}{2\pi \times 1.7\Omega \times 100\ \mu F} + \frac{.5}{2\pi \times 300k \times 8\mu \times 100\ \mu F} = 1.27\ kHz$$

Once the fp range is determined, $R_{c1}$ should be calculated using:

$$R_{c1} = \frac{B}{gm}\left(\frac{R_1 + R_2}{R_1}\right)$$

Where B is the desired gain in V/V at fp, gm is the transconductance of the error amplifier, and R1 and R2 are the feedback resistors. A gain value around 10dB (3.3V/V) is generally a good starting point.

Example: B = 3.3V/V, gm = 650 µmho, R1 = 20kΩ, R2 = 60.4kΩ:

$$R_{c1} = \frac{3.3}{650\mu}\left(\frac{20k + 60.4k}{20k}\right) = 20.4\ k\Omega \cong 20\ k\Omega$$

Bandwidth will vary proportional to the value of $R_{c1}$. Next, $C_{c1}$ can be determined with the following equation:

$$C_{c1} = \frac{1}{2\pi \times f_p \times R_{c1}}$$

Example: $f_p$min = 363 Hz, $R_{c1}$ = 20kΩ:

$$C_{c1} = \frac{1}{2\pi \times 363\ Hz \times 20\ k\Omega} \cong 22\ nF$$

The value of $C_{c1}$ should be within the range determined by $f_p$min/max. A higher value will generally provide a more stable loop, but too high a value will slow the transient response time.

The compensation network (*Figure 7*) will also introduce a low frequency pole which will be close to 0Hz.

A second pole should also be placed at fz. This pole can be created with a single capacitor $C_{c2}$ and a shorted $R_{c2}$ (see *Figure 7*). The minimum value for this capacitor can be calculated by:

$$C_{c2\ min} = \frac{1}{2\pi \times f_z \times R_{c1}}$$

$C_{c2}$ may not be necessary, however it does create a more stable control loop. Under high load current conditions, $C_{c2}$ can also help reduce noise in the control loop. For this purpose a typical value of approximately 220pF is recommended, regardless of the calculated value below.

Example: fz = 80 kHz, $R_{c1}$ = 20kΩ:

$$C_{c2\ min} = \frac{1}{2\pi \times 80\ kHz \times 20\ k\Omega} \cong 100\ pF$$

A second zero can also be added with a resistor in series with $C_{c2}$. If used, this zero should be placed at fn, where the control to output gain rolls off at -40dB/dec. Generally, fn will be well below the 0dB level and thus will have little effect on stability. $R_{c2}$ can be calculated with the following equation:

$$R_{c2} = \frac{1}{2\pi \times f_n \times C_{c2}}$$

## Component Selection (Continued)

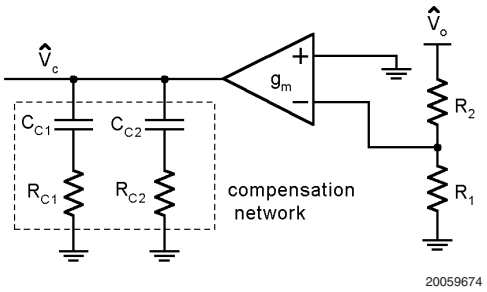



**FIGURE 7. Ch.3 Compensation Network**

### Channel 1 and 2

Because the loop characteristics for channels 1 and 2 do not change with loading, the compensation network is somewhat more straightforward than for channel 3. As shown in *Figure 8*, the control-output transfer function consists of one double pole and one zero.

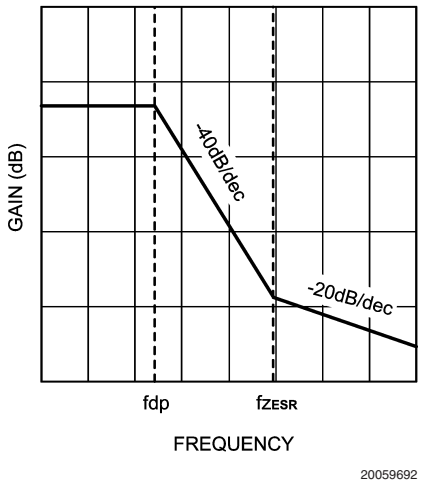



**FIGURE 8. Control-Output Transfer Function**

Therefore, three poles and two zeros are required from the compensation network. The resulting output-control transfer function is shown in *Figure 9*

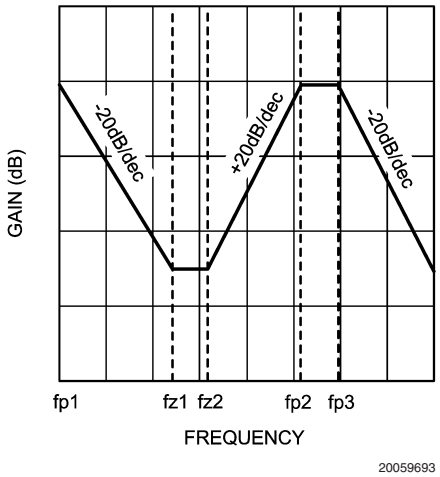



**FIGURE 9. Output-Control Transfer Function**

The power stage double pole and zero frequencies are given by the following equations:

Double Pole:

$$fdp = \frac{1}{2 \times \pi \times \sqrt{L \times C_o}}$$

Zero:

$$fz_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_o}$$

The voltage mode compensation network is shown below.

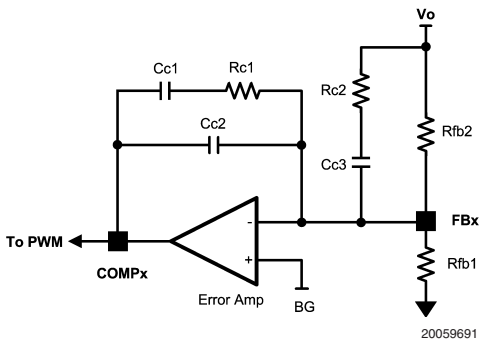



**FIGURE 10. Ch. 1 and 2 Compensation Network**

The compensation network creates the first pole at 0Hz. The other poles and zeros can be calculated by the following equations:

Pole2:

$$f_{p2} = \frac{1}{2 \times \pi \times R_{c2} \times C_{c3}}$$

Pole3: (if $C_{c1} >> C_{c2}$)

## Component Selection (Continued)

$$f_{p3} = \frac{1}{2 \times \pi \times R_{c1} \times C_{c2}}$$

Zero1:

$$f_{z1} = \frac{1}{2 \times \pi \times R_{c1} \times C_{c1}}$$

Zero2: (if $R_{fb2} >> R_{c2}$)

$$f_{z2} = \frac{1}{2 \times \pi \times R_{fb2} \times C_{c3}}$$

**PROCEDURE**

The following procedure will create a 20dB/decade loop gain roll-off. First set fz2 approximately one half decade above fdp. Since this zero is set using one of the feedback resistors, the output voltage may have to be re-adjusted using Rfb1 after the compensation has been set. Also, the DC loop gain will increase as Rfb2 decreases.

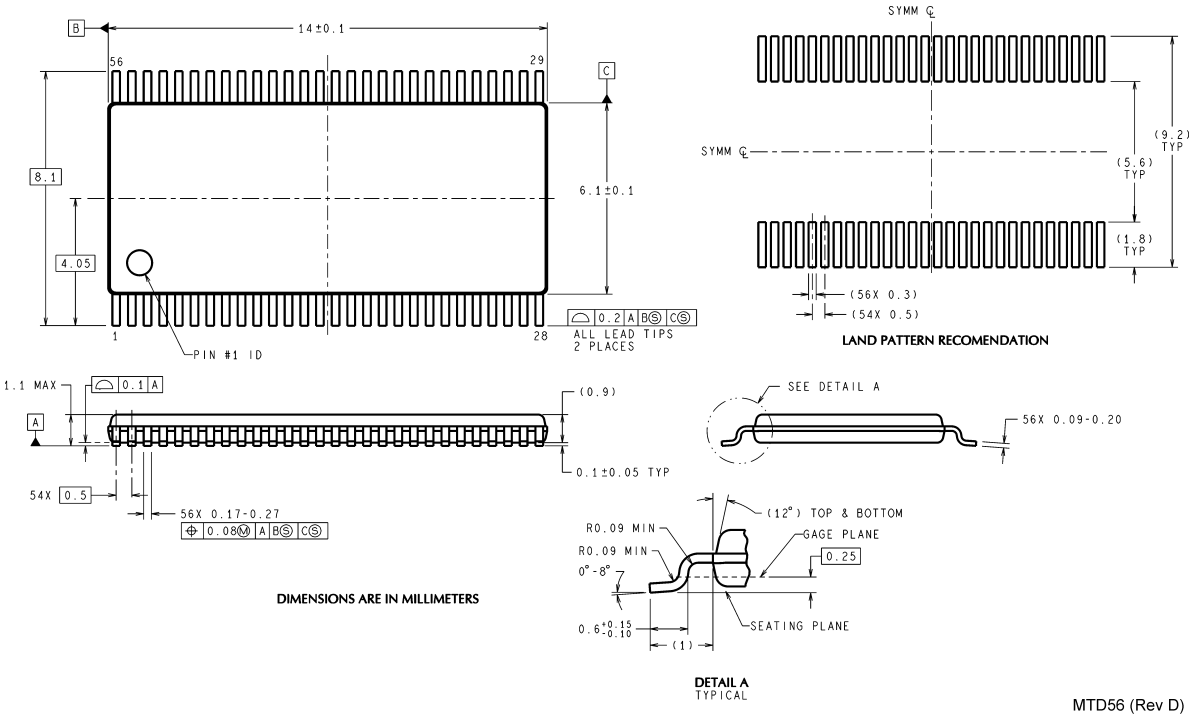
Next, set fz1 approximately one half decade below fdp.

Set fp2 to be equal to fzESR.

Finally, set fp3 to 150kHz (half the switching frequency).

Once the compensation has been set, the bandwidth can be most easily varied by using Rc2 to shift fp2, or by using Cc2 to shift fp3.

## Physical Dimensions inches (millimeters)
unless otherwise noted




MTD56 (Rev D)

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**Order Number LM2648MTD**
**NS Package Number MTD56**

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