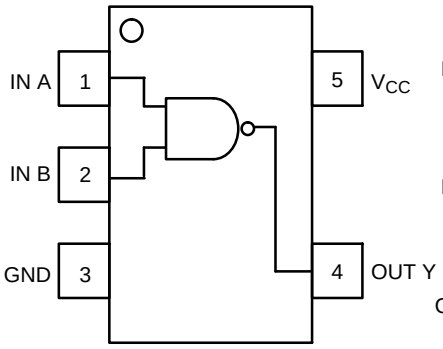
NL17SZ00

Single 2-Input NAND Gate

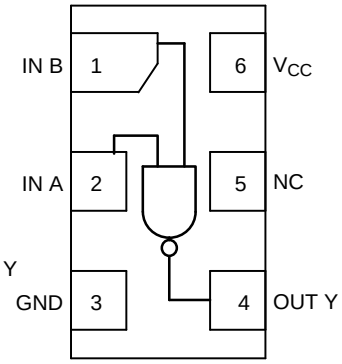
The NL17SZ00 is a single 2−input NAND Gate in three tiny footprint packages. The device performs much as LCX multi−gate products in speed and drive.

Features

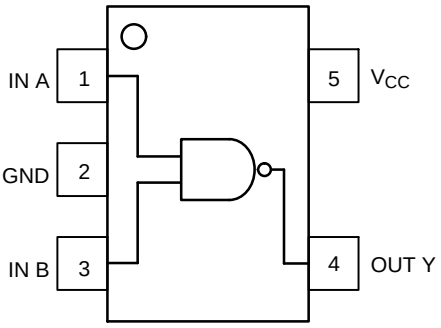
- Tiny SOT−353, SOT−553 and SOT−953 Packages
- 2.7 ns T_{PD} at 5 V (typ)
- Source/Sink 24 mA at 3.0 V
- Over−Voltage Tolerant Inputs
- Pin For Pin with NC7SZ00P5X, TC7SZ00FU and TC7SZ00AFE
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant



SOT−353/SC70−5/ SC−88A/SOT−553



UDFN



SOT−953

Figure 1. Pinouts (Top View)

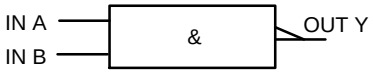
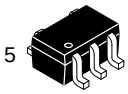


Figure 2. Logic Symbol

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

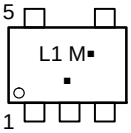
ON Semiconductor®

www.onsemi.com

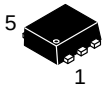


SOT−353/SC70−5/SC−88A
DF SUFFIX
CASE 419A

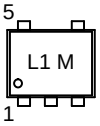
MARKING DIAGRAMS



L1 = Specific Device Marking
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.



SOT−553
XV5 SUFFIX
CASE 463B



L1 = Specific Device Marking
M = Date Code



UDFN6
1.45 x 1.0
CASE 517AQ





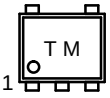
UDFN6
1.0 x 1.0
CASE 517BX



X = Specific Device Marking
M = Date Code



SOT−953
CASE 527AE



T = Specific Device Code
M = Month Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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PIN ASSIGNMENT (SOT−353/ SC70−5/SC−88A/SOT−553/ UDFN)

Pin	Function
1	IN A
2	IN B
3	GND
4	OUT Y
5	V_{CC}

PIN ASSIGNMENT (SOT−953)

Pin	Function
1	IN A
2	GND
3	IN B
4	OUT Y
5	V_{CC}

FUNCTION TABLE

Input		Output Y = AB
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to + 7.0	V
V_{IN}	DC Input Voltage		−0.5 to + 7.0	V
V_{OUT}	DC Output Voltage (SOT−353/SC70−5/SC−88A/SOT−553/UDFN Packages)	Power−Down Mode	−0.5 to + 7.0	V
V_{OUT}	DC Output Voltage (SOT−953 Package)		−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current		−50	mA
I_{OK}	DC Output Diode Current (SOT−953 Package)	V_{OUT} < GND, V_{OUT} > V_{CC}	±50	mA
I_{OK}	DC Output Diode Current (SOT−353/SC70−5/SC−88A/SOT−553 Packages)	V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOT−353 (Note 1) SOT−553	350 496	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOT−353 SOT−553	186 135	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
ESD	ESD Classification	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	2000 200 N/A	
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A, rated to EIA/JESD22−A114−B.
3. Tested to EIA/JESD22−A115−A, rated to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.65	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage (SOT−353/SC70−5/SC−88A/SOT−553/UDFN Packages)		0	5.5	V
V_{OUT}	DC Output Voltage (SOT−953 Package)		0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.0 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V
V_{IL}	Low−Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC}	V
V_{OH}	High−Level Output Voltage V_{IN} = V_{IL} or V_{IH}	I_{OH} = −100 μA I_{OH} = −3 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V_{CC} 1.4 2.1 2.4 2.7 2.5 4.0		V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH} or V_{OH}	I_{OL} = 100 μA I_{OL} = 3 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		 0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0			1		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 5.5 V or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t_R = t_F = 3.0 ns

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	1.65	2.0	5.4	11.4	2.0	12	ns
		R_L = 1 MΩ, C_L = 15 pF	1.8	2.0	4.5	9.5	2.0	10.0	
		R_L = 1 MΩ, C_L = 15 pF	2.5 to 0.2	0.8	3.0	6.5	0.8	7.0	
		R_L = 1 MΩ, C_L = 15 pF	3.3 ± 0.3	0.5	2.4	4.5	0.5	4.7	
		R_L = 500 Ω, C_L = 50 pF		1.5	2.4	5.0	1.5	5.2	
		R_L = 1 MΩ, C_L = 15 pF	5.0 ± 0.5	0.5	2.0	3.9	0.5	4.1	
		R_L = 500 Ω, C_L = 50 pF		0.8	2.4	4.3	0.8	4.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	>4	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF
		10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	30	

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

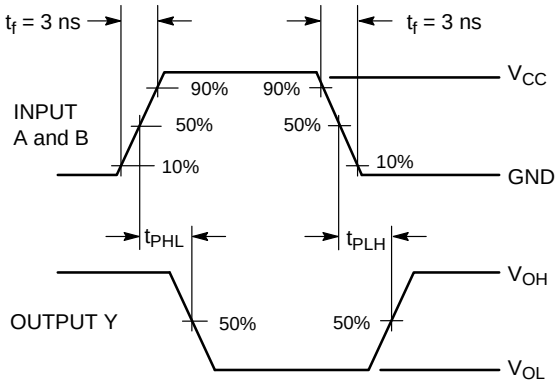
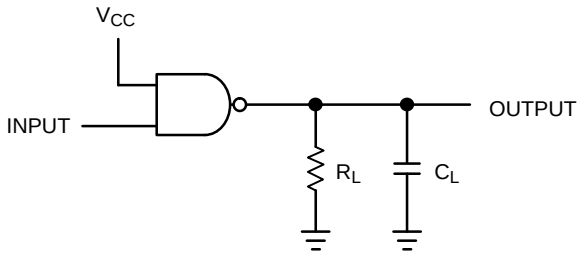


Figure 3. Switching Waveform



A 1−MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

DEVICE ORDERING INFORMATION

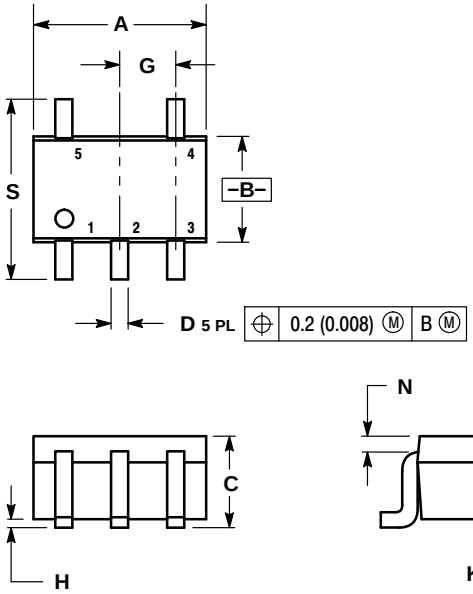
Device Order Number	Package Type	SHipping†
NL17SZ00DFT2G	SOT−353 (Pb−Free)	3000 / Tape & Reel
NLV17SZ00DFT2G*	SOT−353 (Pb−Free)	3000 / Tape & Reel
NL17SZ00XV5T2G	SOT−553 (Pb−Free)	4000 / Tape & Reel
NL17SZ00AMUTCG (In Development)	UDFN6, 1.45 x 1.0 (Pb−Free)	3000 / Tape & Reel
NL17SZ00CMUTCG (In Development)	UDFN6, 1.0 x 1.0 (Pb−Free)	3000 / Tape & Reel
NL17SZ00P5T5G	SOT−953 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

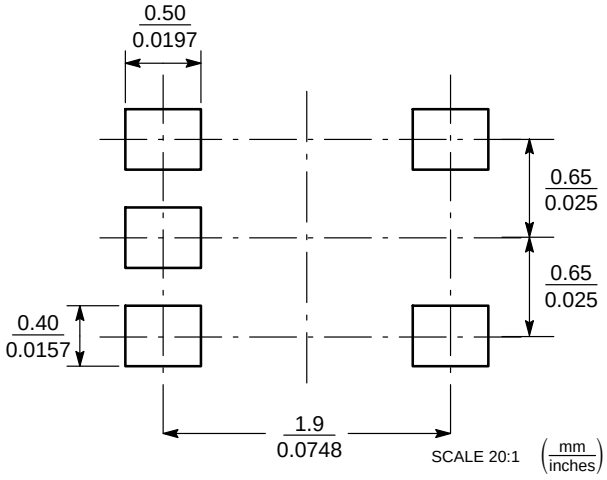
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

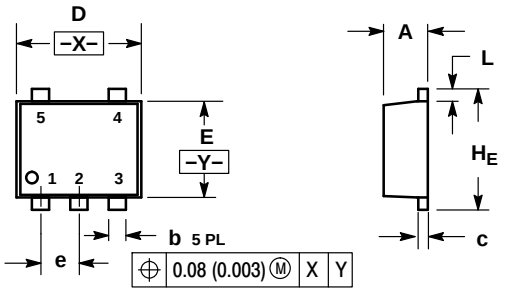
SOLDER FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

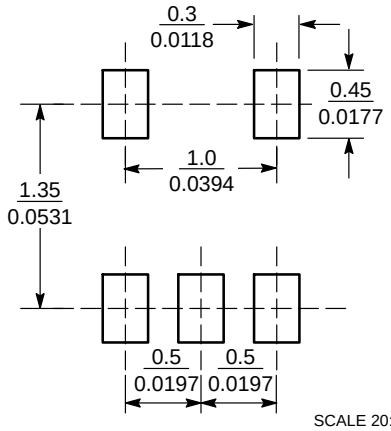
SOT−553
XV5 SUFFIX
CASE 463B
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.063	0.067

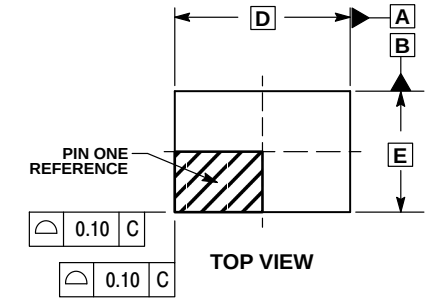
SOLDERING FOOTPRINT*

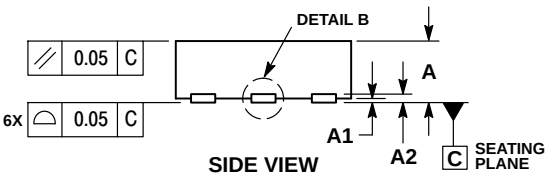


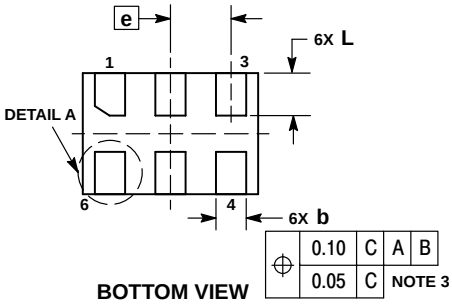
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

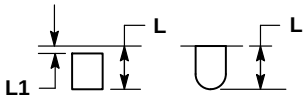
PACKAGE DIMENSIONS

UDFN6, 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

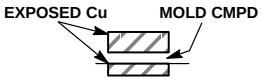








DETAIL A
OPTIONAL CONSTRUCTIONS

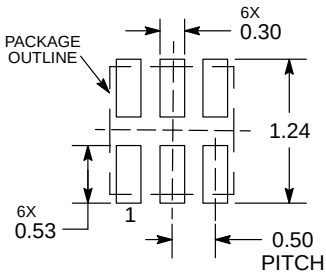


DETAIL B
OPTIONAL CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	−−−	0.15

MOUNTING FOOTPRINT

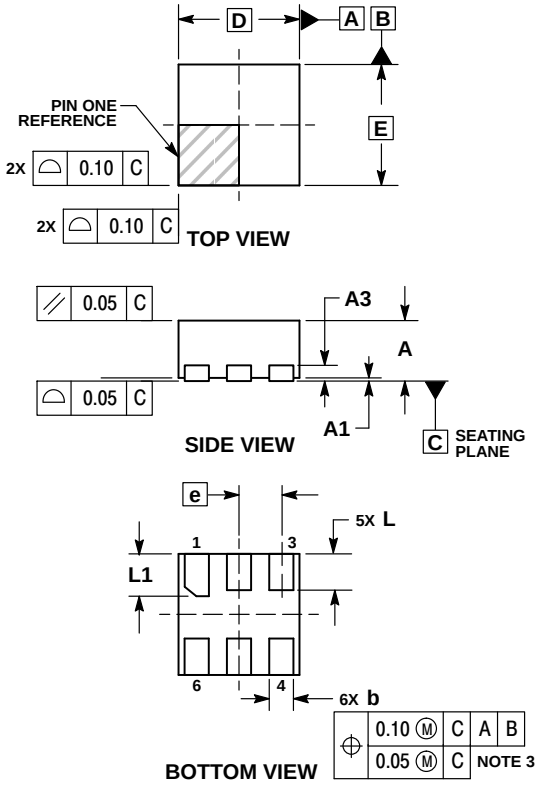


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

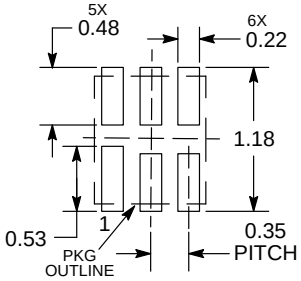
UDFN6, 1x1, 0.35P
CASE 517BX
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

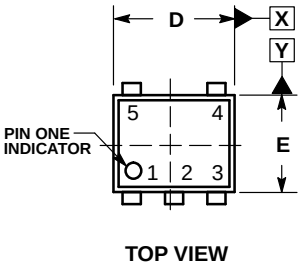


DIMENSIONS: MILLIMETERS

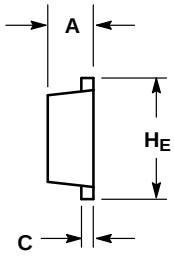
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

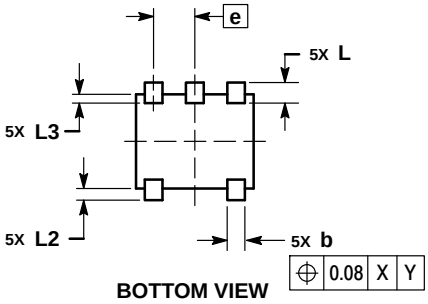
SOT−953
CASE 527AE
ISSUE E



TOP VIEW



SIDE VIEW

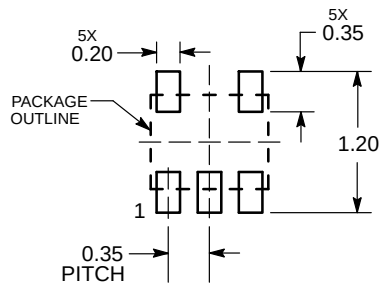


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.175 REF		
L2	0.05	0.10	0.15
L3	−−−	−−−	0.15

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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