FRE9160D, FRE9160R, FRE9160H

30A, -100V, 0.095 Ohm, Rad Hard, P-Channel Power MOSFETs

June 1998

Features

- 30A, -100V, RDS(on) = 0.095Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
  - Meets Pre-Rad Specifications to 100KRAD(Si)
  - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
  - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
  - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
  - Survives 2E12 Typically If Current Limited to IDM
- Photo Current - 10.0nA Per-RAD(Si)/sec Typically
- Neutron
  - Pre-RAD Specifications for 3E13 Neutrons/cm^2
  - Usable to 3E14 Neutrons/cm^2

Description

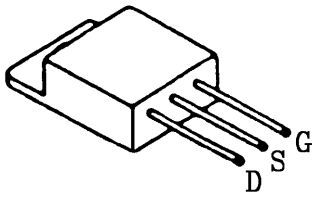
The Intersil Corporation Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13 for 500V product to 1E14 for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n^0) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

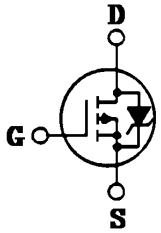
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Intersil Corporation High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-258AA



Symbol



Absolute Maximum Ratings (TC = +25^{o}C) Unless Otherwise Specified

		FRE9160D, R, H	UNITS
Drain-Source Voltage	VDS	-100	V
Drain-Gate Voltage (RGS = 20kΩ)	VDGR	-100	V
Continuous Drain Current			
TC = +25^{o}C	ID	30	A
TC = +100^{o}C	ID	19	A
Pulsed Drain Current	IDM	90	A
Gate-Source Voltage	VGS	±20	V
Maximum Power Dissipation			
TC = +25^{o}C	PT	150	W
TC = +100^{o}C	PT	60	W
Derated Above +25^{o}C		1.20	W/^{o}C
Inductive Current, Clamped, L = 100μH, (See Test Figure)	ILM	90	A
Continuous Source Current (Body Diode)	IS	30	A
Pulsed Source Current (Body Diode)	ISM	90	A
Operating And Storage Temperature	TJC, TSTG	-55 to +150	^{o}C
Lead Temperature (During Soldering)			
Distance > 0.063 in. (1.6mm) From Case, 10s Max	TL	300	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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File Number **3268.2**

Pre-Radiation Electrical Specifications TC = +25^{O}C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	-100	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	-2.0	-4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = -20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = +20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = -100V, VGS = 0 VDS = -80V, VGS = 0 VDS = -80V, VGS = 0, TC = +125^{O}C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20µs	-	90	A
Drain-Source On-State Volts	VDS(on)	VGS = -10V, ID = 30A	-	-2.99	V
Drain-Source On Resistance	RDS(on)	VGS = -10V, ID = 19A	-	0.095	Ω
Turn-On Delay Time	td(on)	VDD = -50V, ID = 30A	-	90	ns
Rise Time	tr	Pulse Width = 3µs	-	440	
Turn-Off Delay Time	td(off)	Period = 300µs, Rg = 10Ω	-	250	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	170	
Gate-Charge Threshold	QG(th)	VDD = -50V, ID = 30A IGS1 = IGS2 0 ≤ VGS ≤ 20	4	18	nc
Gate-Charge On State	QG(on)		85	350	
Gate-Charge Total	QGM		180	750	
Plateau Voltage	VGP		-3	-14	V
Gate-Charge Source	QGS		21	85	nc
Gate-Charge Drain	QGD		35	140	
Diode Forward Voltage	VSD	ID = 30A, VGD = 0	-0.6	-1.8	V
Reverse Recovery Time	TT	I = 30A; di/dt = 100A/µs	-	400	ns
Junction-To-Case	Rθjc		-	0.83	^{O}C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	48	

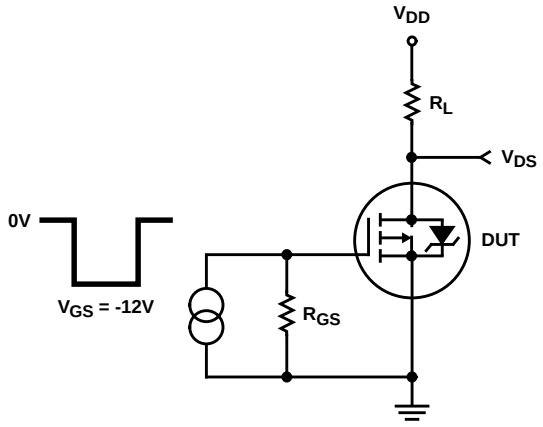


FIGURE 1. RESISTIVE SWITCHING TEST CIRCUIT

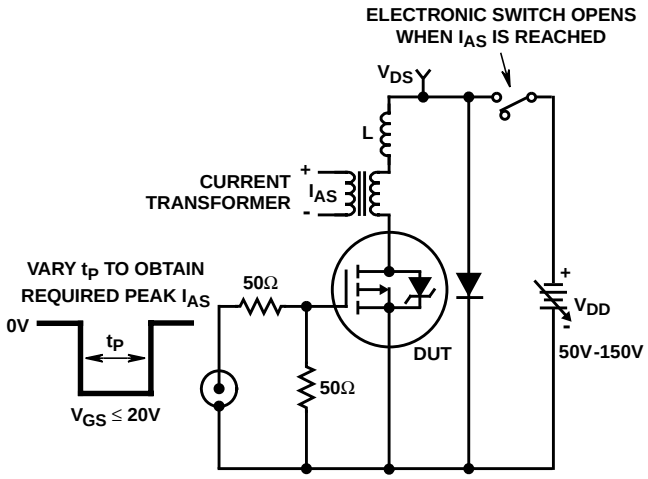


FIGURE 2. UNCLAMPED ENERGY TEST CIRCUIT

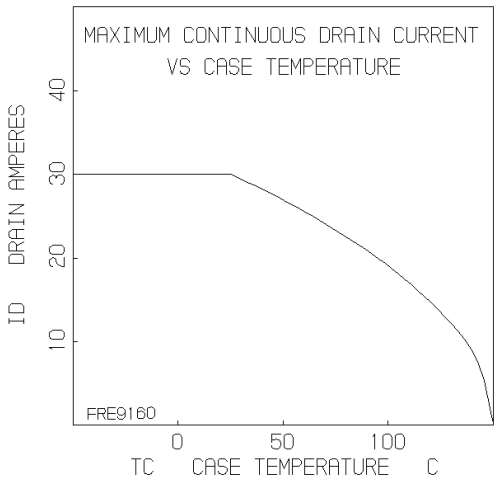
Post-Radiation Electrical Specifications TC = +25^{o}C, Unless Otherwise Specified

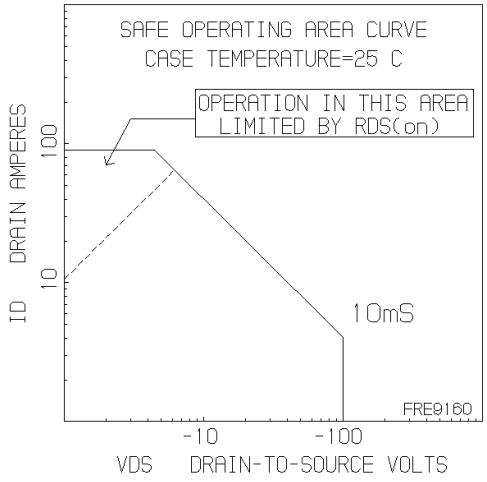
PARAMETER		SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS
					MIN	MAX	
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	FRE9160D, R	VGS = 0, ID = 1mA	-100	-	V
	(Note 5, 6)	BVDSS	FRE9160H	VGS = 0, ID = 1mA	-95	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	FRE9160D, R	VGS = VDS, ID = 1mA	-2.0	-4.0	V
	(Note 3, 5, 6)	VGS(th)	FRE9160H	VGS = VDS, ID = 1mA	-2.0	-6.0	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	FRE9160D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	FRE9160H	VGS = -20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	FRE9160D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	FRE9160H	VGS = 20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	FRE9160D, R	VGS = 0, VDS = -80V	-	25	µA
	(Note 5, 6)	IDSS	FRE9160H	VGS = 0, VDS = -80V	-	100	µA
Drain-Source On-State Volts	(Note 1, 4, 6)	VDS(on)	FRE9160D, R	VGS = -10V, ID = 30A	-	-2.99	V
	(Note 1, 5, 6)	VDS(on)	FRE9160H	VGS = -16V, ID = 30A	-	-4.49	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	FRE9160D, R	VGS = -10V, ID = 19A	-	0.095	Ω
	(Note 1, 5, 6)	RDS(on)	FRE9160H	VGS = -14V, ID = 19A	-	0.143	Ω

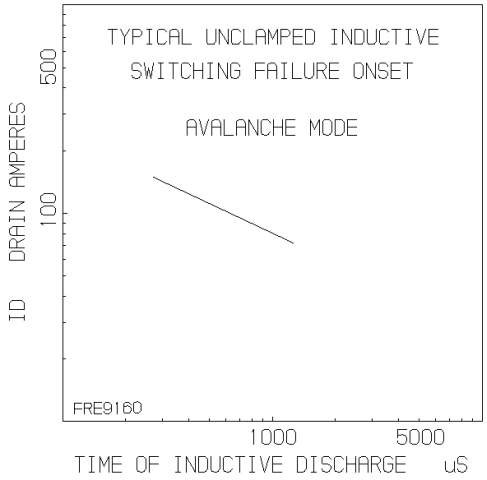
NOTES:

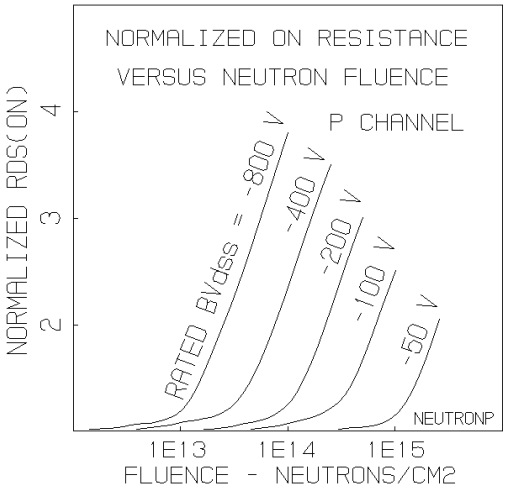
1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for “D”, 100KRAD(Si) for “R”. Neutron = 3E13
5. Gamma = 1000KRAD(Si). Neutron = 3E13
6. Insitu Gamma bias must be sampled for both VGS = -10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 6/8/90 on TA17761 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, Intersil Application Note AN8831, Oct. 1988

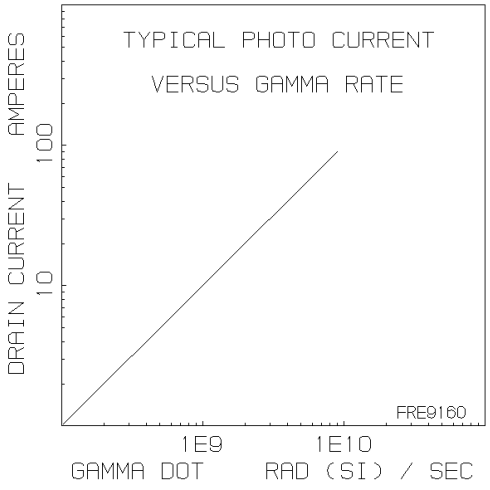
Typical Performance Characteristics

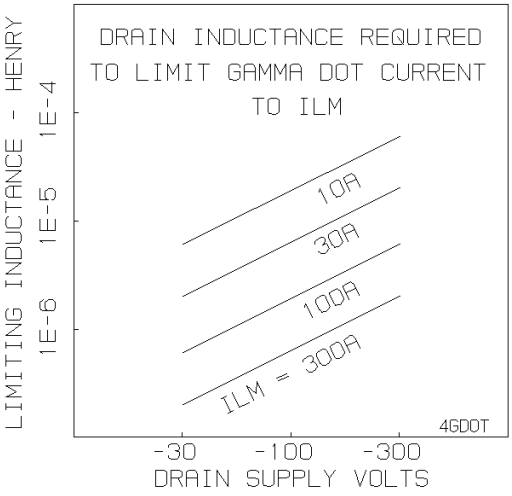












Rad Hard Data Packages - Intersil Power Transistors

TXV Equivalent

1. Rad Hard TXV Equivalent - Standard Data Package

A. Certificate of Compliance

B. Assembly Flow Chart

C. Preconditioning - Attributes Data Sheet

D. Group A - Attributes Data Sheet

E. Group B - Attributes Data Sheet

F. Group C - Attributes Data Sheet

G. Group D - Attributes Data Sheet

2. Rad Hard TXV Equivalent - Optional Data Package

A. Certificate of Compliance

B. Assembly Flow Chart

C. Preconditioning
- Attributes Data Sheet
- Precondition Lot Traveler
- Pre and Post Burn-In Read and Record Data

D. Group A
- Attributes Data Sheet
- Group A Lot Traveler

E. Group B
- Attributes Data Sheet
- Group B Lot Traveler
- Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
- Bond Strength Data (Subgroup B3)
- Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)

F. Group C
- Attributes Data Sheet
- Group C Lot Traveler
- Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
- Bond Strength Data (Subgroup C6)

G. Group D
- Attributes Data Sheet
- Group D Lot Traveler
- Pre and Post RAD Read and Record Data

Class S - Equivalents

1. Rad Hard "S" Equivalent - Standard Data Package

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
Attributes Data Sheet
Hi-Rel Lot Traveler
HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data

F. Group A - Attributes Data Sheet

G. Group B - Attributes Data Sheet

H. Group C - Attributes Data Sheet

I. Group D - Attributes Data Sheet

2. Rad Hard Max. "S" Equivalent - Optional Data Package

A. Certificate of Compliance

B. Serialization Records

C. Assembly Flow Chart

D. SEM Photos and Report

E. Preconditioning
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
- HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- X-Ray and X-Ray Report

F. Group A
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups A2, A3, A4, A5 and A7 Data

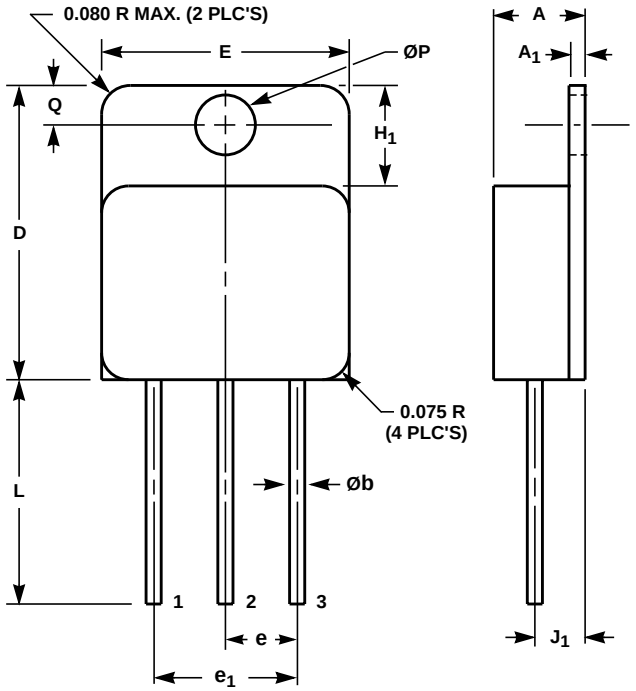
G. Group B
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups B1, B3, B4, B5 and B6 Data

H. Group C
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Subgroups C1, C2, C3 and C6 Data

I. Group D
- Attributes Data Sheet
- Hi-Rel Lot Traveler
- Pre and Post Radiation Data

TO-258AA

3 LEAD JEDEC STYLE TO-258AA HERMETIC METAL PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.250	0.270	6.35	6.85	-
A_1	0.035	0.045	0.89	1.14	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.815	0.830	20.71	21.08	-
E	0.685	0.695	17.40	17.65	-
e	0.200 TYP		5.08 TYP		4
e_1	0.400 BSC		10.16 BSC		4
H_1	0.270	0.290	6.86	7.36	-
J_1	0.130	0.150	3.31	3.81	4
L	0.600	0.650	15.24	16.51	-
ØP	0.155	0.165	3.94	4.19	-
Q	0.115	0.125	2.93	3.17	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-258AA outline dated 2-88. Except Øb.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 2 dated 5-98.

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Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029