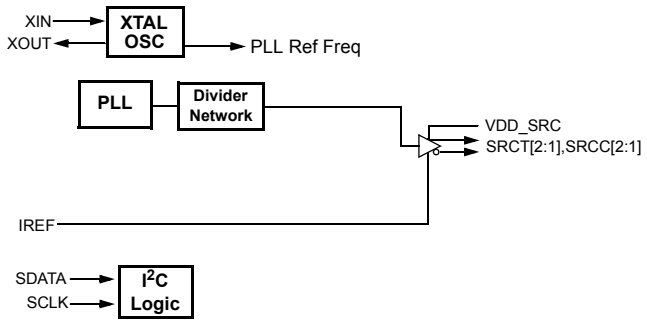
PCI-Express Clock Generator

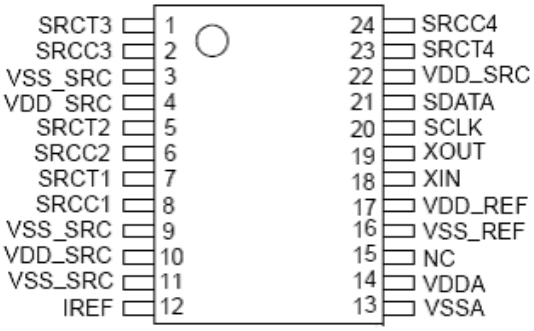
Features

- Four 100-MHz differential SRC clocks
- Low-voltage frequency select input
- I^2C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 24-pin TSSOP package

Block Diagram



Pin Configuration



24 TSSOP

Pin Description

Pin No.	Name	Type	Description
12	IREF	I	A precision resistor attached to this pin is connected to the internal current reference.
20	SCLK	I, PU	SMBus compatible SCLOCK. This pin has an internal pull-up.
21	SDATA	I/O, PU	SMBus compatible SDATA. This pin has an internal pull-up.
1, 2, 5, 6, 7, 8, 23, 24	SRCT/C[4:1]	O, DIF	100-MHz Differential Serial reference clock.
18	XIN	I	14.318-MHz Crystal Input
19	XOUT	O	14.318-MHz Crystal Output
4, 10, 22	VDD_SRC	PWR	3.3V power supply for SRC outputs
3, 9, 11	VSS_SRC	GND	Ground for SRC outputs
14	VDDA	PWR	3.3V Analog Power for PLLs
13	VSSA	GND	Analog Ground
17	VDD_REF	PWR	3.3V power supply for Xtal
16	VSS_REF	GND	Ground for Xtal
15	NC	NC	No Connect

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:5)	Chip select address, set to ‘00’ to access device
(4:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '00000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1

Table 2. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	SRC[T/C]4	SRC[T/C]4 Output Enable- only for CY28SRC04 0 = Disable (Hi-Z), **1 = Enable**
5	1	SRC[T/C]3	SRC[T/C]3 Output Enable- only for CY28SRC04 0 = Disable (Hi-Z), **1 = Enable**
4	1	SRC[T/C]2	SRC[T/C]2 Output Enable- only for CY28SRC02 and CY28SRC04 0 = Disable (Hi-Z) **1 = Enable**
3	1	SRC[T/C]1	SRC[T/C]1 Output Enable- only for CY28SRC02 and CY28SRC04 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC [T/C]0	SRC[T/C]0 Output Enable- only for CY28SRC01 0 = Disable (Hi-Z), 1 = Enable
1	0	Reserved	Reserved

Byte 0: Control Register 0 (continued)

Bit	@Pup	Name	Description
0	0	Reserved	Reserved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	SRCT/C	Spread Spectrum Selection '0' = –0.35% '1' = –0.50%
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	SRC	SRC Spread Spectrum Enable 0 = Spread off, 1 = Spread on
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved

Byte 4: Control Register 4 (continued)

Bit	@Pup	Name	Description
0	1	Reserved	Reserved

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 1 = REF/N Clock, 0 = Tri-state
6	0	TEST_MODE	Test Clock Mode Entry Control 1 = REF/N or Tri-state mode, 0 = Normal operation
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Byte 7: Control Register 7

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	1		Revision Code Bit 1
4	1		Revision Code Bit 0
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	12 pF–16 pF	1 mW	7 pF	±50 ppm	±50 ppm	5 ppm

Crystal Recommendations

The CY28SRC04 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28SRC04 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

The following diagram shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

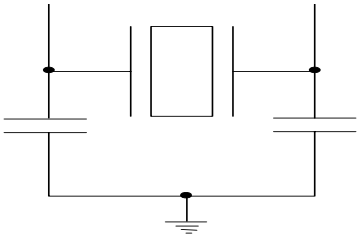


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

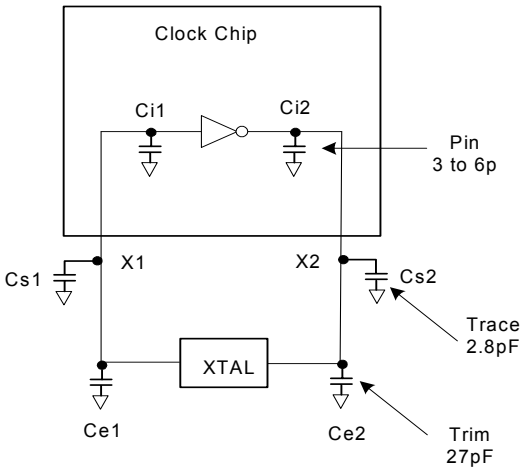


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitance loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL .....Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs .....Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DDA}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to VSS	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		
Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.					

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD_SRC, VDDA	3.3V Operating Voltage	3.3V ± 5%	3.135	3.465	V
$V_{ILSMBUS}$	Input Low Voltage	SDATA, SCLK	–	1.0	V
$V_{IHSMBUS}$	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL}	Input Low Voltage	V_{DD}	V_{SS} – 0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Leakage Current	Except Pull-ups or Pull downs 0<VIN<VDD	–5	5	mA
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA	2.4	-	V
I_{OZ}	High-Impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	5	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		0.7*V_{DD}	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	0.3*V_{DD}	V
I_{DD}	Dynamic Supply Current	At max load and frequency	–	400	mA
IPD_D	Power Down Supply Current	PD asserted, Outputs driven	–	70	mA
IPD_T	Power Down Supply Current	PD asserted, Outputs Hi-Z	-	2	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between 0.3V_{DD} and 0.7V_{DD}	–	10.0	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	10.12800	9.872001	ns
$T_{PERIODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
TSKEW	Any SRCS clock to Any SRCS clock Skew	Measured at crossing point V_{OX}	-	250	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 3*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 3*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 3.* Measure SE	–	0.2	V
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
TLTJ	Long Term Jitter	Measurement at 1.5V@1us	-	TBD	ps

Test and Measurement Set-up

For Differential SRC Output Signals

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

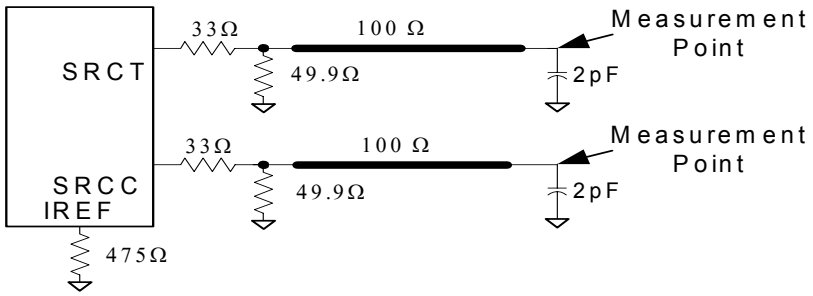


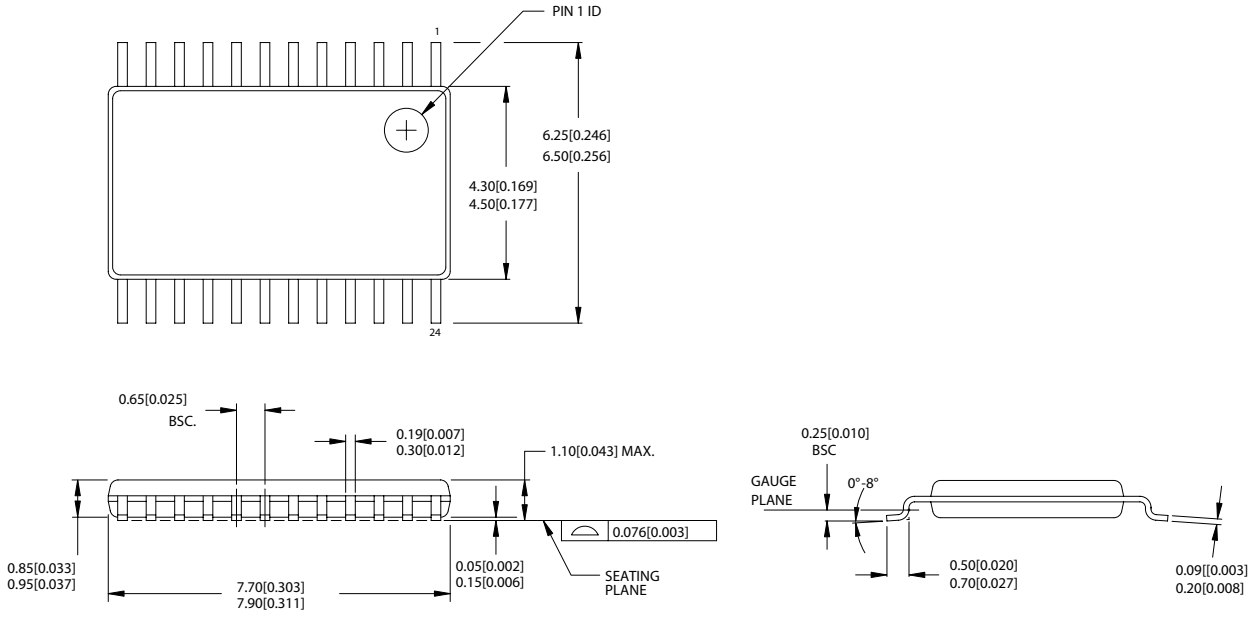
Figure 3. 0.7V Load Configuration

Ordering Information

Part Number	Package Type	Product Flow
Standard		
CY28SRCZC-04	24-pin TSSOP	Commercial, 0° to 70°C
CY28SRCZC-04T	24-pin TSSOP—Tape and Reel	Commercial, 0° to 70°C

Package Diagrams

24-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z24



51-85119-*A

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Document History Page

Document Title: CY28SRC04 PCI-Express Clock Generator Document Number: 001-00043				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	371761	See ECN	RGL	New Data Sheet
*A	384078	See ECN	RGL	1) Swap Pin 1 and 2 in Pin Configuration 2) Swap Pin 5 and 6 in Pin Configuration