

DATA SHEET



TEA6840H

New In Car Entertainment (NICE)
car radio

Preliminary specification
File under Integrated Circuits, IC01

1999 Jul 12

New In Car Entertainment (NICE) car radio

TEA6840H

FEATURES

- FM mixer for conversion of FM RF from 65 to 108 MHz to IF of 10.7 MHz; the mixer provides inherent image rejection
- FM RF mixer can be set to receive weather band radio up to 162.55 MHz; weather band radio flag output
- AM mixer 1 for conversion of AM RF to AM IF1 10.7 MHz
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- AM mixer 2 for conversion of AM IF1 to AM IF2 450 kHz
- Crystal oscillator providing mixer frequencies for AM mixer 2 and reference for synthesizer PLL, IF count, timing for Radio Data System (RDS) update and reference frequency for car audio signal processor IC
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for car audio signal processor ICs (TEA688x, SAA77xx)
- Digital alignment circuit for conversion of LC oscillator tuning voltage to controlled alignment voltage of FM antenna tank circuit
- AGC pin diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC pin diode drive can be activated by the I²C-bus as a local/distance function; AGC threshold is a programmable and keyed function switchable via the I²C-bus
- FM IF linear amplifiers with high dynamic input range
- FM quadrature demodulator with automatic centre frequency adjustment and Total Harmonic Distortion (THD) compensation
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I²C-bus
- AM RF pin diode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold is programmable via the I²C-bus; AM IF2 AGC and demodulator
- AM AF output switchable to provide AM IF2 for AM stereo decoder
- AM noise blanker with blanking at AM IF2
- Several test modes available for fast IC and system tests.



GENERAL DESCRIPTION

The TEA6840H is a single chip car radio tuner for AM and FM intended for microcontroller tuning with the I²C-bus providing the following functions:

- AM double conversion receiver for LW/MW/SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM single conversion receiver with integrated image rejection for IF = 10.7 MHz capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6840H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

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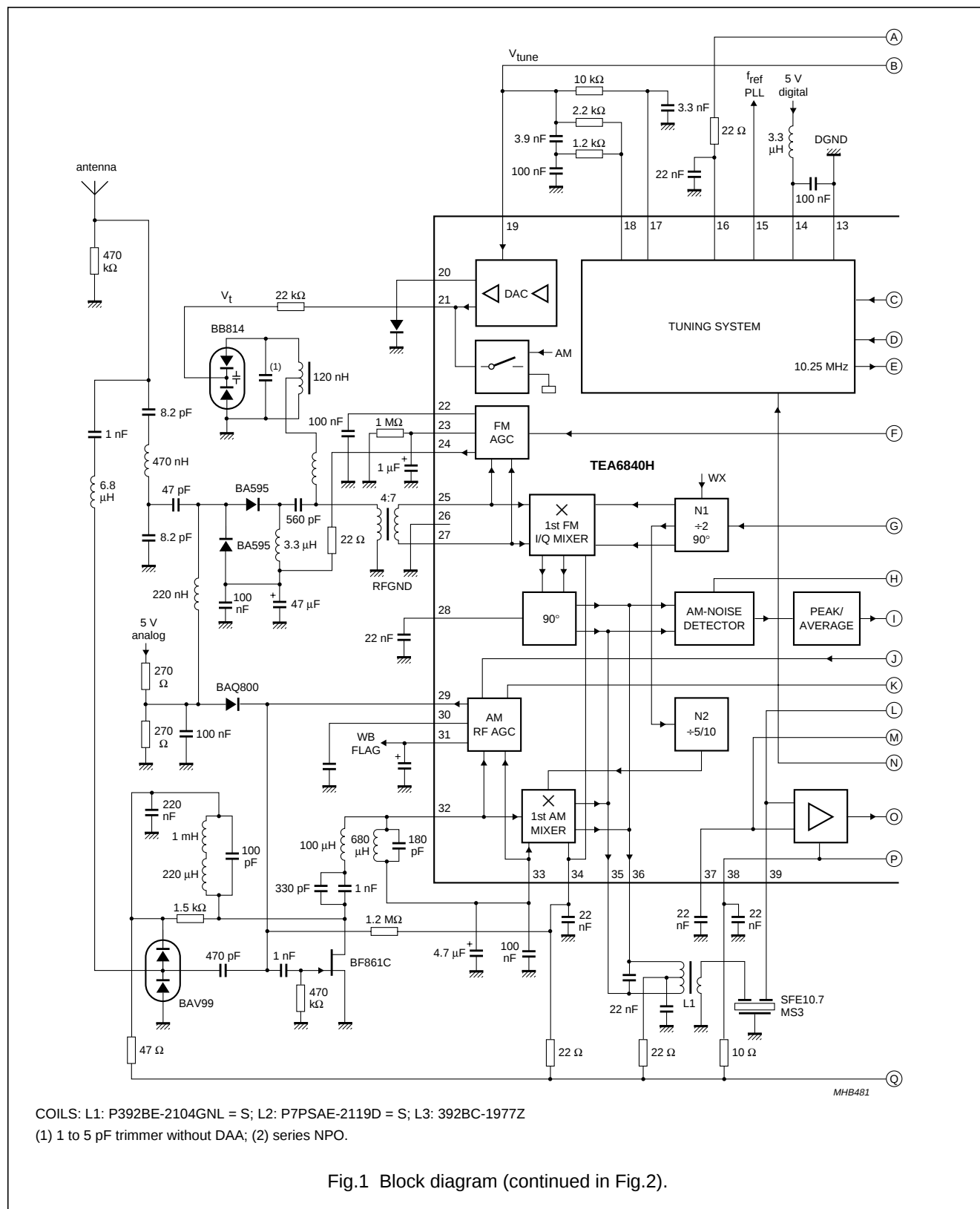
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DDA1}	analog supply voltage 1		8	8.5	9	V
I _{DDA1}	analog supply current 1	FM mode	45	56	67	mA
		AM mode	39	49	59	mA
V _{DDA2}	analog supply voltage 2		4.75	5	5.25	V
I _{DDA2}	analog supply current 2	FM mode	6.5	8.1	9.8	mA
		AM mode	4.7	5.9	7.1	mA
V _{DDD}	digital supply voltage		4.75	5	5.25	V
I _{DDD}	digital supply current	FM mode	18	23	28	mA
		AM mode	18	23	28	mA
f _{AM(ant)}	AM input frequency	LW	0.144	–	0.288	MHz
		MW	0.522	–	1.710	MHz
		SW	5.85	–	9.99	MHz
f _{FM(ant)}	FM input frequency		65	–	108	MHz
f _{FM(WB)(ant)}	FM weather band input frequency		162.4	–	162.55	MHz
T _{amb}	operating ambient temperature		–40	–	+85	°C
AM overall system parameters (1 × SFE10.7; 1 × SFR450H)						
S+N/N	signal plus noise-to-noise ratio	m = 0.3	–	58	–	dB
THD	total harmonic distortion	m = 0.8	–	0.3	–	%
		m = 0.9	–	0.5	–	%
FM overall system parameters (3 × SFE10.7MS3)						
S+N/N	signal plus noise-to-noise ratio	Δf = 22.5 kHz; de-emphasis = 50 μs	–	65	–	dB
THD	total harmonic distortion	Δf = 75 kHz	–	0.6	1	%

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BLOCK DIAGRAM



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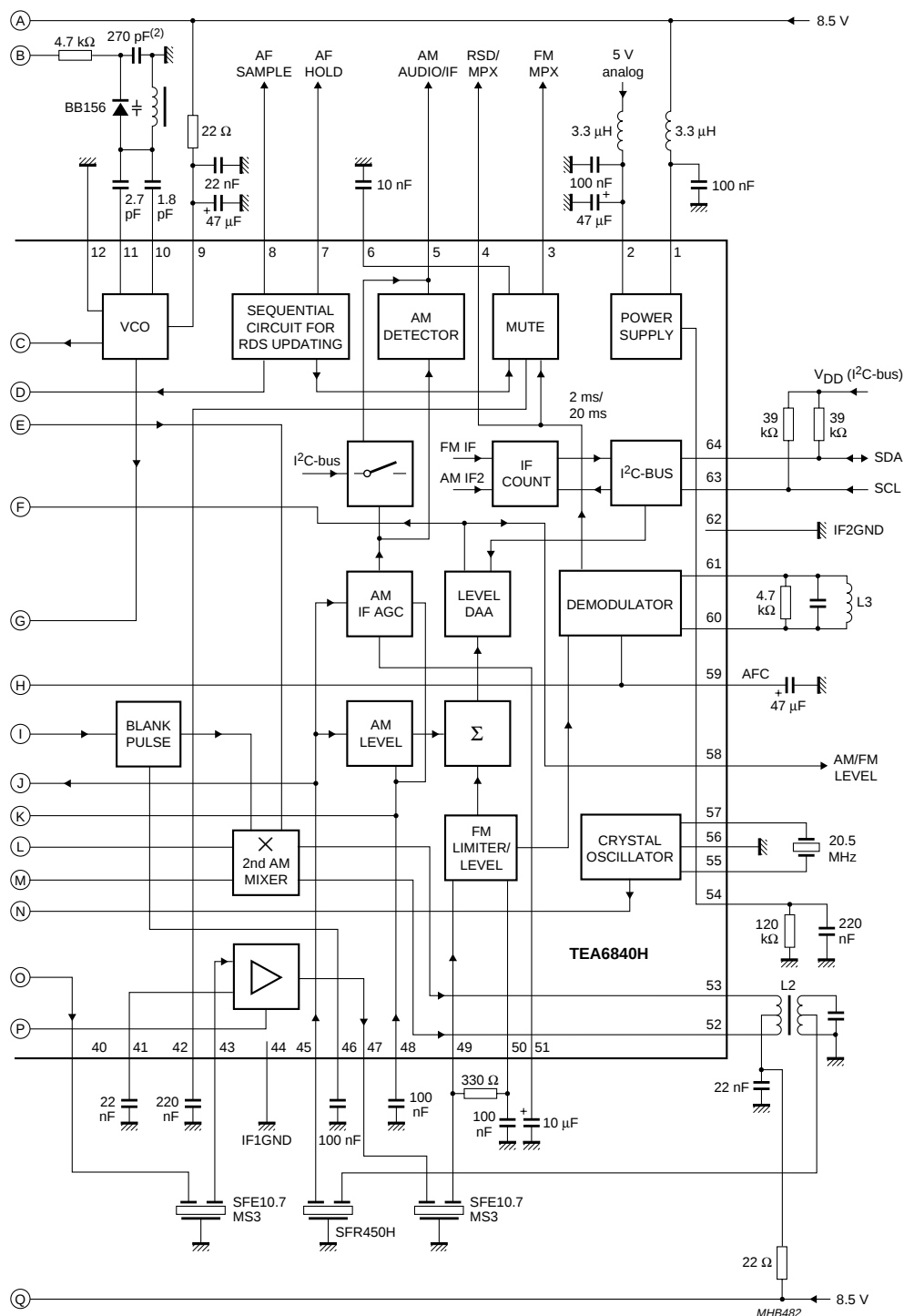


Fig.2 Block diagram (continued from Fig.1).

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PINNING

SYMBOL	PIN	DESCRIPTION
V _{DDA1}	1	analog supply voltage 1 (8.5 V) for on-chip power supply
V _{DDA2}	2	analog supply voltage 2 (5 V) for on-chip power supply
FMMPX	3	FM demodulator MPX output
RDSMPX	4	MPX for RDS decoder and signal processor (not muted)
AMAFIF2	5	AM demodulator AF output or IF2 for AM stereo (multiplexed by I ² C-bus)
TRDSMUTE	6	time constant for RDS update mute
AFHOLD	7	AF hold flag output for car audio signal processor IC
AFSAMPLE	8	AF sample flag output for car audio signal processor IC
V _{DDA3}	9	analog supply voltage 3 (8.5 V) for VCO
OSCTNK	10	VCO tank circuit
OSCFDB	11	VCO feedback
VCOGND	12	VCO ground
DGND	13	digital ground
V _{DDD}	14	digital supply voltage (5 V)
f _{ref}	15	reference frequency output for signal processor IC
V _{DDA4}	16	analog supply voltage 4 (8.5 V) for tuning PLL
CPOUT	17	charge pump output
V _{tune}	18	tuning voltage
DAAIN	19	input of digital alignment circuit for antenna tank circuit
DAATD	20	temperature compensation diode for digital alignment circuit of antenna tank circuit
DAAOUT	21	output of digital alignment circuit for antenna tank circuit
T1FMAGC	22	1st time constant of FM front-end AGC
T2FMAGC	23	2nd time constant of FM front-end AGC
IFMAGC	24	pin diode drive current output of FM front-end AGC
FMMIXIN1	25	input 1 of FM RF mixer
RFGND	26	RF ground
FMMIXIN2	27	input 2 of FM RF mixer
V _{ref(FMMIX1)}	28	reference voltage for FM mixer
IAMAGC	29	pin diode drive current output of AM front-end AGC
T2AMAGC	30	2nd time constant of AM front-end AGC
T1AMAGC	31	1st time constant output of AM front-end AGC
AMMIX1IN1	32	1st AM mixer input 1
AMMIX1IN2	33	1st AM mixer input 2
V _{DDA5}	34	analog supply voltage 5 (8.5 V) for FM and AM RF
MIX1OUT1	35	1st AM/FM mixer IF (10.7 MHz) output (HIGH)
MIX1OUT2	36	1st AM/FM mixer IF (10.7 MHz) output (LOW)
IFAMP1DEC	37	2nd AM mixer and 1st FM IF amplifier decoupling
V _{DDA6}	38	analog supply voltage 6 (8.5 V) for 1st and 2nd IF amplifier
IFAMP1IN	39	1st IF amplifier/2nd AM mixer (10.7 MHz) input
IFAMP1OUT	40	1st IF amplifier (10.7 MHz) output

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SYMBOL	PIN	DESCRIPTION
IFAMP2DEC	41	2nd IF amplifier decoupling and AGC capacitor for AM noise blanker
C _{offset}	42	DC feedback for offset compensation RDS mute
IFAMP2IN	43	2nd IF amplifier (10.7 MHz) input
IF1GND	44	AM IF1 ground
AMIF2IN	45	AM IF2 (450 kHz) input for demodulator AGC and AM level detector
AMNBHOLD	46	AM noise blanker hold output
IFAMP2OUT	47	2nd IF amplifier (10.7 MHz) output
AMIF2DEC	48	decoupling for AM IF2 input
FMLIMIN	49	FM limiter (10.7 MHz) input
FMLIMDEC	50	FM limiter decoupling
C _{AGC}	51	AMIFAGC capacitor
AMMIX2OUT1	52	2nd AM mixer (450 kHz) output 1
AMMIX2OUT2	53	2nd AM mixer (450 kHz) output 2
I _{ref}	54	reference current for power supply
XTAL1	55	crystal oscillator 1
XTALGND	56	crystal oscillator ground
XTAL2	57	crystal oscillator 2
V _{level}	58	level voltage output for AM and FM
C _{AFC}	59	FM demodulator AFC capacitor
QDET1	60	quadrature demodulator tank 1
QDET2	61	quadrature demodulator tank 2
IF2GND	62	AM IF2 ground
SCL	63	I ² C-bus clock line input
SDA	64	I ² C-bus data line input/output

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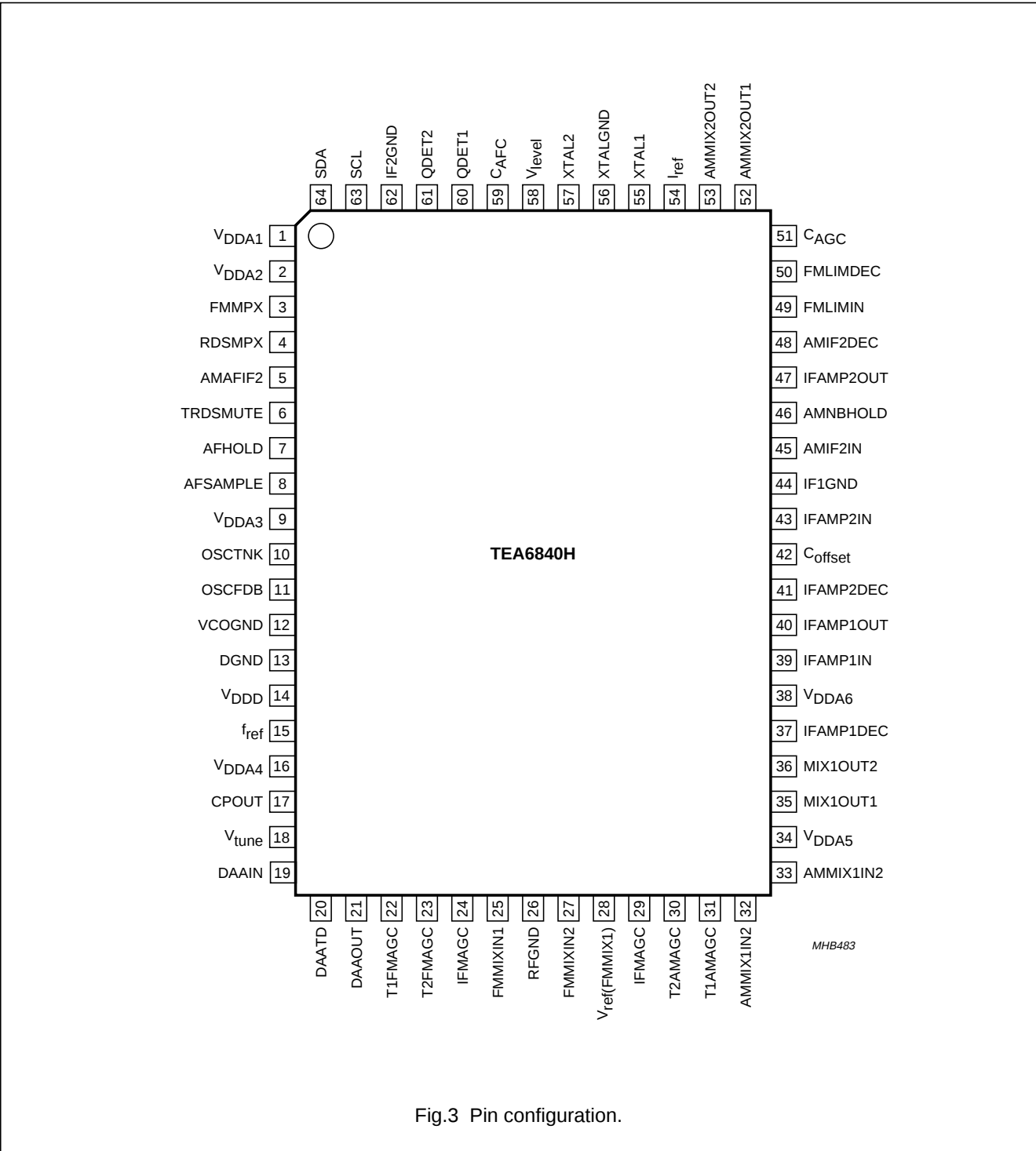


Fig.3 Pin configuration.

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FUNCTIONAL DESCRIPTION

FM mixer 1

FM quadrature mixer converts FM RF (65 to 162.55 MHz) to an IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity.

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands.

- US FM = 87.9 to 107.9 MHz
- US weather = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76.0 to 91 MHz
- East Europe FM = 65.8 to 74 MHz.

VCO

The L and C tuned VCO provides the Local Oscillator (LO) signal for both FM and AM mixer 1. It has a frequency range of 151.2 to 248.2 MHz.

Crystal oscillator

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- LO for 2nd AM mixer
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm
- Reference frequency (75.4 kHz) for the TEA6880H.

PLL

Fast synthesizer PLL tuning system with local control for inaudible RDS updating.

DAA

Digital Auto Alignment circuitry (FM RF DAA) for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit.

FM keyed AGC

FM contains keyed wide-band RF AGC. AGC detection occurs at the FM mixer. The wide-band RF signal switches a narrow band signal (IF) from the FM IF level detector circuitry that controls the FM RF AGC block.

It includes an AGC pin diode drive circuit for the FM RF AGC. The pin diode drive can be activated via the I²C-bus as a local/distance function.

The AGC threshold is programmable and the keyed AGC function is switchable via the I²C-bus.

FM IF amplifiers

The two FM IF amplifiers provide 10 dB and 4 dB amplification with high linearity and dynamic range.

FM demodulator

The FM quadrature demodulator includes automatic centre frequency adjustment and THD compensation.

AM tuner

The AM tuner is realized in a double conversion technique and is capable of selecting LW/MW and SW bands.

AM mixer 1 converts AM RF to an IF1 of 10.7 MHz, while AM mixer 2 converts 10.7 MHz IF1 to 450 kHz IF2.

- LW = 144 to 288 kHz
- MW = 530 to 1710 kHz (US AM band)
- SW = 5.85 to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

AM RF and IF2 AGC

The AM RF includes a pin diode drive circuit. The threshold detection points for AM AGC are performed at AM mixer 1 and AM IF2. AGC thresholds are programmable via the I²C-bus.

AM detector

The AM detector provides AM level information and AM AF or AM IF2.

AM AF/IF2 SWITCH

The AM output provides either a detected AM Audio Frequency (AF) or the corresponding AM IF2 signal. The IF2 signal can be used for AM stereo decoder processing.

AM noise blanker

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of the 2nd mixer.

Trigger sensitivity can be modified by changing the resistor value at pin 46.

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FM/AM level detector

FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I²C-bus.

Test mode

The test mode of the IC is activated by:

- Sending the test byte (byte 5) to the IC
- Connecting pin 15 through a 100 k Ω resistor to V_{DDA1}
- Applying 50 μ A to pin 15.

If the test mode is enabled by pin 15:

- The settling time of the AM IF2 AGC is reduced to less than 100 ms in the nominal application

- The digital-to-analog converters for the antenna Data Access Arrangement (DAA) and the level DAA can be clocked directly by the SCL line of the I²C-bus
- The output at pin 15 can be selected by the I²C-bus: TEA6880H reference frequency, PLL reference frequency or PLL programmable divider output frequency
- The RDS update control circuit can be clocked directly via pin 20
- Pin 31 can be used to enable the load PLL circuit of the RDS update control circuit
- Charge pumps can be set into 3-state mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DDA1}	analog supply voltage 1 for on-chip power supply		−0.3	+10	V
V _{DDA2}	analog supply voltage 2 for on-chip power supply		−0.3	+6.5	V
V _{DDA4}	analog supply voltage 4 for tuning PLL		−0.3	+10	V
V _{DDA5}	analog supply voltage 5 for FM and AM RF		−0.3	+10	V
V _{DDA6}	analog supply voltage 6 for 1st IF amplifier		−0.3	+10	V
V _{DDA7}	analog supply voltage 7 for 2nd IF amplifier		−0.3	+10	V
V _{DDD}	digital supply voltage		−0.3	+6.5	V
T _{stg}	storage temperature		−55	+150	°C
T _{amb}	operating ambient temperature		−40	+85	°C
V _{es}	electrostatic handling	note 1	−200	+200	V
		note 2	−2000	+2000	V

Notes

1. Charge device model (R = 0 Ω , C = 200 pF).
2. Human body model (R = 1.5 k Ω , C = 100 pF).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	48	K/W

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DC CHARACTERISTICS

$V_{DDA1} = 8.5\text{ V}$; $V_{DDA2} = 5\text{ V}$; $V_{DDD} = 5\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V _{DDA1}	analog supply voltage at pins 1, 9, 16, 34, 35, 36, 38, 42, 52 and 53		8	8.5	9	V
V _{DDA2}	analog supply voltage at pin 2		4.75	5	5.25	V
V _{DDD}	digital supply voltage at pin 14		4.75	5	5.25	V
I _{DDA}	analog supply current internal power supply	FM mode	6.5	8.1	9.8	mA
		AM mode	4.7	5.9	7.1	mA
I _{DDD}	digital supply current	FM mode	18	23	28	mA
		AM mode	18	23	28	mA
FM mode						
I ₃₅	bias current FM mixer output 1		4.8	6	7.2	mA
I ₃₆	bias current FM mixer output 2		4.8	6	7.2	mA
I ₃₈	supply current FM IF amplifier 1 and 2		12	14	16	mA
I _{DDA1}	analog supply current internal power supply		–	15	–	mA
I _{DDA4}	analog supply current tuning PLL	test mode; data byte 5 bit 3 = 1	–	2.9	–	mA
I _{DDA3}	analog supply current VCO		–	6.5	–	mA
I _{DDA5}	analog supply current RF		–	5	–	mA
AM mode						
I ₃₅	bias current AM mixer 1 output 1		4.8	6	7.2	mA
I ₃₆	bias current AM mixer 1 output 2		4.8	6	7.2	mA
I ₅₂	bias current AM mixer 2 output 1		3.6	4.5	5.4	mA
I ₅₃	bias current AM mixer 2 output 2		3.6	4.5	5.4	mA
I _{DDA1}	analog supply current internal power supply		–	17.5	–	mA
I _{DDA4}	analog supply current tuning PLL	test mode; data byte 5 bit 3 = 1	–	1.6	–	mA
I _{DDA3}	analog supply current VCO		–	6.5	–	mA
I _{DDA5}	analog supply current RF		–	1.8	–	mA
Power supply						
REFERENCE CURRENT GENERATOR; PIN 54						
V _{O(ref)}	output reference voltage		4	4.25	4.5	V
R _O	output resistance		8	11	13	kΩ
I _{O(source)(max)}	maximum output source current		–100	–	+100	nA

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AC CHARACTERISTICS

$V_{DDA1} = 8.5\text{ V}$; $V_{DDA2} = 5\text{ V}$; $V_{DDD} = 5\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; see Figs 8 and 9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
f _{osc}	oscillator frequency		151.2	–	248.2	MHz
V ₁₁	input bias voltage		2.2	2.8	3.4	V
V ₁₀	DC output voltage		5	6.1	7.2	V
V _{10(rms)}	AC output voltage (RMS value)	f _{osc} = 200 MHz	–	1.5	–	V
C/N	carrier-to-noise ratio	f _{osc} = 200 MHz; Δf = 10 kHz	–	101	–	$\frac{\text{dBc}}{\sqrt{\text{Hz}}}$
RR	ripple rejection	f _{ripple} = 100 Hz; V _{DDA3(ripple)} = 100 mV (RMS); f _{osc} = 250 MHz	–	97	–	dB
		f _{ripple} = 100 Hz; V _{DDA3(ripple)} = 100 mV (RMS); f _{osc} = 200 MHz	–	99	–	dB
Crystal oscillator; pins 55, 56 and 57						
f _{osc}	standard frequency		20.4996	20.5	20.5004	MHz
V _{bias(XTAL)}	DC bias voltage (pins 55 and 57)		1.7	2.1	2.5	V
R ₅₅₋₅₇	real part of input impedance (pins 55 to 57)	V ₅₅₋₅₇ = 1 mV	–500	–	–	Ω
C ₅₅₋₅₇	input capacitance (pins 55 to 57)		8	10	12	pF
R _{XTAL}	crystal motional resistance	start of operation	–	–	500	Ω
C _{XTAL}	crystal shunt capacitance		–	–	18	pF
V _{XTAL(rms)}	crystal voltage (pins 55 to 57) (RMS value)		–	350	–	mV
C/N	carrier-to-noise ratio	f _{osc} = 20.5 MHz (10.25 MHz); Δf = 10 kHz	–	112	–	$\frac{\text{dBc}}{\sqrt{\text{Hz}}}$
I ₅₆	start-up current	V ₅₅ = V ₅₇ = 2.1 V	–	9	–	mA
	operating current	V ₅₅ – V ₅₇ = ±400 mV	–	1.5	–	mA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator divider N1						
D/D _{N1}	oscillator divider ratio N1	data byte 4 bit 0 = 0, bit 1 = 0 and bit 2 = 0 for FM standard; bit 1 = 0, bit 2 = 1 for FM EE; bit 1 = 1, bit 2 = 0 for FM local	–	2	–	
		data byte 4 bit 0 = 0, bit 1 = 1 and bit 2 = 1 for FM WX	–	1	–	
Oscillator divider N2						
D/D _{N2}	oscillator divider ratio N2	data byte 4 bit 0 = 1, bit 2 = 1; AM mode	–	10	–	
		data byte 4 bit 0 = 1, bit 2 = 0; AM mode	–	5	–	
Synthesizer						
PROGRAMMABLE DIVIDER						
D/D _{prog}	programmable divider ratio		512	–	32767	
D/D _{step}	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
D/D _{Nref}	crystal oscillator divider ratio N _{ref}	f _{osc} = 20.5 MHz; data byte 4 bit 4 = 0, bit 5 = 0 and bit 6 = 0; f _{ref} = 100 kHz	–	205	–	
		f _{osc} = 20.5 MHz; data byte 4 bit 4 = 0, bit 5 = 0 and bit 6 = 1; f _{ref} = 50 kHz	–	410	–	
		f _{osc} = 20.5 MHz; data byte 4 bit 4 = 0, bit 5 = 1 and bit 6 = 0; f _{ref} = 25 kHz	–	820	–	
		f _{osc} = 20.5 MHz; data byte 4 bit 4 = 0, bit 5 = 1 and bit 6 = 1; f _{ref} = 20 kHz	–	1025	–	
		f _{osc} = 20.5 MHz; data byte 4 bit 4 = 1, bit 5 = 0 and bit 6 = 0; f _{ref} = 10 kHz	–	2050	–	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP: PINS 17 AND 18						
$I_{\text{sink(lcp1)}}$	low charge pump 1 peak sink current (pin 17)	$V_{17} = 0.4$ to 7.6 V; data byte 4 bit 0 = 0, bit 1 = 1 and bit 2 = 1 for FM WX	200	300	400	μA
$I_{\text{source(lcp1)}}$	low charge pump 1 peak source current (pin 17)	$V_{17} = 0.4$ to 7.6 V; data byte 4 bit 0 = 0, bit 1 = 1 and bit 2 = 1 for FM WX	−200	−300	−400	μA
$I_{\text{sink(hcp1)}}$	high charge pump 1 peak sink current (pin 17)	$V_{17} = 0.4$ to 7.6 V; data byte 4 bit 0 = 1, bit 1 = 1 and bit 2 = 1; AM stereo; N2 divider set to 10 (LW, MW)	0.7	1	1.3	mA
$I_{\text{source(hcp1)}}$	high charge pump 1 peak source current (pin 17)	$V_{17} = 0.4$ to 7.6 V; data byte 4 bit 0 = 1, bit 1 = 1 and bit 2 = 1; AM stereo; N2 divider set to 10 (LW, MW)	−0.7	−1	−1.3	mA
$I_{\text{sink(cp2)}}$	charge pump 2 peak sink current (pin 17)	$V_{17} = 0.3$ to 7.1 V; data byte 4 bit 0 = 0, bit 1 = 0 and bit 2 = 0; FM standard	100	130	160	μA
$I_{\text{source(cp2)}}$	charge pump 2 peak source current (pin 17)	$V_{17} = 0.3$ to 7.6 V; data byte 4 bit 0 = 0, bit 1 = 0 and bit 2 = 0; FM standard	−100	−130	−160	μA
$I_{\text{sink(cp3)}}$	charge pump 3 peak sink current (pin 18)	$V_{18} = 0.4$ to 7.6 V; data byte 4 bit 0 = 0, bit 1 = 0 and bit 2 = 0; FM standard	2.1	3	3.9	mA
$I_{\text{source(cp3)}}$	charge pump 3 peak source current (pin 17)	$V_{18} = 0.4$ to 7.6 V; data byte 4 bit 0 = 0, bit 1 = 0 and bit 2 = 0; FM standard	−2.1	−3	−3.9	mA
$I_{\text{Z(cp)}}$	charge pumps 3-state currents (pins 17 and 18)	data byte 5 bit 3 = 1; $V_{17,18} = 0$ to 8.5 V	−5	−	+5	nA
ANTENNA DAA: PINS 19, 20 AND 21						
$I_{\text{bias(cp)}}$	charge pump buffer input bias current (pin 19)	$V_{\text{DAAIN}} = 0.4$ to 8.0 V; FM mode	−10	−	+10	nA
		$V_{\text{DAAIN}} = 0$ to 8.5 V; AM mode	−10	−	+10	nA
$V_{\text{i(cp)}}$	charge pump buffer input voltage (pin 19)		0	−	8.5	V
$V_{\text{o(DAA)(min)}}$	minimum DAA output voltage (pin 21)	$V_{\text{DAAIN}} = 4.0$ V; $V_{\text{DAATD}} = 0.7$ V; FM mode	−	−	0.5	V
$V_{\text{o(DAA)(max)}}$	maximum DAA output voltage (pin 21)	data byte 3 bits 0 to 6 set to logic 1; $V_{\text{DAAIN}} = 4.0$ V; $V_{\text{DAATD}} = 0.7$ V; FM mode	8	−	8.5	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{O(DAA)}$	DAA output voltage (pin 21)	AM mode	—	—	0.3	V
		data byte 3 bits 0 to 6 set to logic 0; $V_{DAAIN} = 4.0$ V; $V_{DAATD} = 0.7$ V; note 1	1.5	1.65	1.8	V
		$V_{DAAIN} = 4$ V; data byte 3 = 10101011; FM mode	3.8	4	4.2	V
$V_{O(n)(DAA)}$	DAA output noise voltage (pin 21)	$V_{DAAIN} = 4$ V; data byte 3 bit 6 = 1 and bits 5 to 0 = 0; B = 300 Hz to 15 kHz; FM mode	—	30	100	μ V
$G_{CONV(DAA)}$	DAA conversion gain (pin 21)	$V_{DAAOUT} = 0.2$ to 8.25 V; data byte 3 bits 0 to 6 set to logic 1; $V_{DAAIN} = 3.0$ V; $V_{DAATD} = 0.7$ V; note 1	6.2	6.5	6.8	V
		$V_{DAAIN} = 2$ V; data byte 3 = 11010101; FM mode	3	3.3	3.6	V
		$V_{DAAIN} = 2$ V; data byte 3 = 10101010; FM mode	1.8	2	2.2	V
ΔT	temperature drift (pin 21)	$T_{amb} = -40$ to $+85$ °C; data byte 3 = 10101011; $V_{DAATD} = 0.7$ V	−8	—	+8	mV
$V_{21n} - V_{21(n+1)}$	DAA step accuracy (pin 21)	$n = 0$ to 127 ; $V_{DAAOUT} < 8.0$ V; FM mode	$0.5V_{LSB}$	V_{LSB}	$1.5V_{LSB}$	mV
$I_{sink(DAA)}$	DAA output sink current (pin 21)	$V_{DAAOUT} = 0.2$ to 8.25 V	50	—	—	μ A
$I_{source(DAA)}$	DAA output source current (pin 21)	$V_{DAAOUT} = 0.2$ to 8.25 V	−50	—	—	μ A
$I_{source(cd)}$	compensation diode source current (pin 20)	$V_{DAATD} = 0.2$ to 1.5 V	−50	−40	−30	μ A
$TC_{cd(source)}$	temperature coefficient compensation diode source current (pin 20)	$V_{DAATD} = 0.2$ to 1.5 V; $T_{amb} = -40$ to $+85$ °C	−300	—	+300	$\frac{10^{-12}}{K}$
t_{st}	DAA output settling time	$V_{DAAOUT} = 0.2$ to 8.25 V; $C_L = 270$ pF	—	—	30	μ s
RR	ripple rejection	$f_{ripple} = 100$ Hz; $V_{DDA4} = 1$ mV	—	50	—	dB
$C_{L(DAA)}$	DAA output load capacitance (pin 21)	$V_{DDAOUT} < 8.0$ V; FM mode	—	—	270	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF counter (FM IF1/AM IF2 counter)						
N _{IF}	IF counter length for AM and FM		–	8	–	bit
T _{count(IF)}	IF counter period	data byte 4 bit 7 = 1	–	2	–	ms
		data byte 4 bit 7 = 0	–	20	–	ms
R _{precount}	FM IF counter prescaler ratio	data byte 4 bit 3 = 1	–	10	–	
		data byte 4 bit 3 = 0	–	100	–	
Reference frequency for car sound processor IC; note 2						
REFERENCE FREQUENCY DIVIDER						
R _{ref}	crystal oscillator divider ratio		–	272	–	
f _{ref}	reference frequency	f _{xtal} = 20.5 MHz	–	75.368	–	kHz
VOLTAGE GENERATOR; PIN 15						
V _{o(p-p)}	AC output voltage (peak-to-peak value)		60	100	170	mV
V _O	DC output voltage		3.2	3.4	3.9	V
R _O	output resistance		–	–	50	kΩ
R _{L(min)}	minimum load resistance		1	–	–	MΩ
AM signal channel						
RF AGC STAGE						
V _{i(RF)}	RF input voltage for AGC start level (pin 32)	data byte 5 bit 5 = 0, bit 6 = 0	–	375	–	mV
		data byte 5 bit 5 = 1, bit 6 = 0	–	500	–	mV
		data byte 5 bit 5 = 0, bit 6 = 1	–	625	–	mV
		data byte 5 bit 5 = 1, bit 6 = 1	–	750	–	mV
V _{i(IF2)}	IF2 input voltage (pin 45)	AGC start level	0.5	0.85	1	V
I _{sink(AGC)(max)}	maximum AGC sink current (pin 29)	V ₃₂ > 500 mV (peak)	–	15	–	mA
R _O	output resistance (pin 29)	I ₂₉ = 1 μA	1	–	–	MΩ
C _O	AM AGC current generator output capacitance (pin 29)		–	5	7	pF
I _{att}	attack current AGC peak detector (pin 30)	data byte 5 bit 5 = 1, bit 6 = 1; V ₃₂₋₃₃ = 1 V; V ₃₀ = 3 V; V ₄₅₋₄₈ = 0 V	–	3.15	–	mA
I _{dec}	decay current AGC peak detector (pin 30)	data byte 5 bit 5 = 1, bit 6 = 1; V ₃₂₋₃₃ = 0 V; V ₃₀₋₃₂ = 250 mV; V ₃₀ = 3 V; V ₄₅₋₄₈ = 0 V	–	2.6	–	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM MIXER 1 (IF1 = 10.7 MHz)						
R_i	input resistance (pin 32 to 33)		50	70	100	k Ω
C_i	input capacitance (pin 32 to 33)		–	5	7	pF
V_i	DC input voltage (pins 32 and 33)		2.3	2.7	3.1	V
R_o	output resistance (pin 35 to 36)		100	–	–	k Ω
C_o	output capacitance (pin 35 to 36)		–	5	7	pF
$V_{i(max)}$	maximum input voltage (pin 32)	1 dB compression point of $V_{35-36(p-p)}$	500	–	–	mV
$V_{o(max)(p-p)}$	maximum output voltage (pin 35 to 36) (peak-to-peak value)		12	15	–	V
$g_{m(CONV)}$	conversion transconductance		2.0	2.55	3.2	mA/V
$\Delta g_{m(CONV)}(T)$	conversion transconductance temperature dependency		–	–0.09	–	%/K
IP3	3rd-order intermodulation	$R_{35-36(ACL)} = 2.8 \text{ k}\Omega$	135	138	–	dB μ V
IP2	2nd-order intermodulation	$R_{35-36(ACL)} = 2.8 \text{ k}\Omega$	–	170	–	dB μ V
$V_{i(n)(eq)}$	equivalent input noise voltage (pin 32 to 33)	band limited noise; $R_{gen} = 750 \Omega$; $R_{35-36(ACL)} = 2.8 \text{ k}\Omega$	–	5.8	–	$\frac{nV}{\sqrt{Hz}}$
F_{AMMIX1}	noise figure of AM mixer 1		–	4.5	7.1	dB
I_{bias}	mixer bias current (pins 35 and 36)	AM position	4.8	6	7.2	mA
WEATHER BAND FLAG						
$I_{L(max)}$	maximum load current (pin 31)		–5	–	+5	μ A
$V_{o(max)}$	maximum output voltage for FM mode (pin 31 to 26)		0	–	0.5	V
$V_{o(min)}$	minimum output voltage for WX mode (pin 31 to 26)		5.1	6	6.9	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM MIXER 2 (IF2 = 450 kHz)						
R_i	input resistance (pin 39 to 37)		270	330	390	Ω
C_i	input capacitance (pin 39 to 37)		–	5	7	pF
V_i	DC input voltage (pins 39 and 37)		2.4	2.7	3	V
R_o	output resistance (pin 52 to 53)		100	–	–	k Ω
C_o	output capacitance (pin 52 to 53)		–	5	7	pF
$V_{i(max)(peak)}$	maximum input voltage (pin 39 to 37) (peak value)	1 dB compression point of $V_{52-53(p-p)}$	1.1	–	–	V
$V_{o(max)(p-p)}$	maximum output voltage (pin 52 to 53) (peak-to-peak value)	$V_{DDA1} = 8.5\text{ V}$	12	15	–	V
$g_{m(CONV)}$	conversion transconductance		1.3	1.6	1.9	mA/V
$\frac{\Delta g_{m(CONV)}}{g_{m(CONV)} \times \Delta T}$	conversion transconductance temperature dependency		–	-9×10^{-4}	–	1/K
IP3	3rd-order intermodulation	$R_{52-53(ACL)} = 4\text{ k}\Omega$	134	137	–	dB μ V
IP2	2nd-order intermodulation	$R_{52-53(ACL)} = 4\text{ k}\Omega$	–	170	–	dB μ V
$V_{i(n)(eq)}$	equivalent input noise voltage (pin 39 to 37)	$R_{gen} = 330\text{ }\Omega$; $R_{52-53(ACL)} = 4\text{ k}\Omega$	–	15	22	$\frac{nV}{\sqrt{Hz}}$
F_{AMMIX2}	noise figure of AM mixer 2		–	16	19.5	dB
I_{bias}	mixer bias current (pins 52 and 53)	AM position	3.6	4.5	5.4	mA
IF2 AGC STAGE AND AM DETECTOR						
$V_{AGC(start)}$	AGC start voltage (pin 45 to 48)	input carrier voltage	–	14	30	μ V
$V_{AGC(stop)}$	AGC stop voltage (pin 45 to 48)	maximum input peak voltage	1	–	–	V
ΔAGC	AGC range	between start and stop of AGC; $m = 0.8$	–	89	–	dB
R_i	input resistance (pin 45 to 48)		1.8	2	2.2	k Ω
C_i	input capacitance (pin 45 to 48)		–	–	5	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_i	input voltage for $\alpha = -10$ dB audio attenuation (pin 45 to 48)	data byte 5 bit 4 = 1; mute on	–	75	120	μV
		data byte 5 bit 4 = 0; mute off	–	6	10	μV
$V_{\text{AGC(ctl)}}$	AGC control voltage	$V_{45-48} = 1$ mV	4.1	4.3	4.7	V
$V_{5(\text{min})(\text{rms})}$	minimum AM IF2 output level (pin 5) (RMS value)	data byte 4 bit 0 = 1, bit 1 = 1; $m = 0$; $V_{45-48} = 14$ μV	1.5	3	4.5	mV
$V_{5(\text{max})(\text{rms})}$	maximum AM IF2 output level (pin 5) (RMS value)	data byte 4 bit 0 = 1, bit 1 = 1; $m = 0$; $V_{45-48} = 5.0$ mV	130	180	230	mV
R_o	output resistance (pin 5)	data byte 4 bit 0 = 1, bit 1 = 1	–	–	500	Ω
		data byte 4 bit 0 = 1, bit 1 = 0	–	–	500	Ω
$V_{o(\text{rms})}$	AM AF output voltage level (pin 5) (RMS value)	data byte 4 bit 0 = 1, bit 1 = 0; $m = 0.3$; $f_{\text{mod}} = 400$ Hz; $V_{45-48} = 100$ μV to 500 mV (RMS)	240	290	340	mV
C_o	output capacitance (pin 5)	data byte 4 bit 0 = 1, bit 1 = 0	–	5	7	pF
$V_{\text{SEN}(\text{rms})}$	sensitivity voltage (pin 45 to 48) (RMS value)	$m = 0.3$; $f_{\text{mod}} = 400$ Hz; $B_{\text{AF}} = 2.5$ kHz; $R_{\text{source}} = 2$ k Ω $S + N/N = 26$ dB	–	45	65	μV
		$S + N/N = 46$ dB	–	600	900	μV
$S+N/N$	maximum signal plus noise-to-noise ratio	$m = 0.3$; $f_{\text{mod}} = 400$ Hz; $B_{\text{AF}} = 2.5$ kHz; $R_{\text{source}} = 2$ k Ω	54	60	–	dB
THD	total harmonic distortion	$B_{\text{AF}} = 2.5$ kHz; $C_{\text{AGC}} = 22$ μF ; $V_{45-48} = 100$ μV to 500 mV (RMS)				
		$m = 0.8$; $f_{\text{mod}} = 400$ Hz	–	0.5	1	%
		$m = 0.9$; $f_{\text{mod}} = 400$ Hz	–	1	2	%
		$m = 0.8$; $f_{\text{mod}} = 100$ Hz	–	1.25	2.5	%
		$m = 0.9$; $f_{\text{mod}} = 100$ Hz	–	1.75	3.5	%
RR	ripple rejection (pin 5)	$f_{\text{ripple}} = 100$ Hz; $V_{\text{DDA2(ripple)}} = 100$ mV (RMS)	30	40	–	dB
t_{sw}	FM to AM switching time	$C_{\text{AGC}} = 22$ μF	–	1000	1500	ms
t_{settle}	AM AGC settling time	$C_{\text{AGC}} = 22$ μF normal operation	–	–	1800	ms
		test mode	–	–	180	ms

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM IF2 LEVEL DETECTOR; see Fig.4						
V_{level}	level output DC voltage (pin 58)	$V_{45-48} = 10 \mu\text{V}$ to 1 V	0	–	7	V
		$V_{45-48} < 1 \mu\text{V}$; default setting of level DAA and level slope	0.1	0.5	0.9	V
		$V_{45-48} = 1.4 \text{ mV}$; default setting of level DAA	1.6	2.2	2.8	V
ΔV_{level}	level starting point for adjustment of step size	default setting of level slope	30	40	50	mV
$V_{\text{level(slope)}}$	slope of level voltage	default setting of level slope	650	800	950	$\frac{\text{mV}}{20 \text{ dB}}$
ΔV_{step}	level slope adjustment of step size	$V_{45-48} = 1.4 \text{ mV}$	45	60	75	$\frac{\text{mV}}{20 \text{ dB}}$
$V_{\text{O(B)}}$	bandwidth level output voltage (pin 58)		200	300	–	mV
R_{O}	output resistance at level voltage pin (pin 58)		–	–	500	Ω
RR	ripple rejection (pin 58)	$f_{\text{ripple}} = 100 \text{ Hz}$; $V_{\text{DDA1(ripple)}} = 100 \text{ mV (RMS)}$	–	40	–	dB
AM NOISE BLANKER; TEST SIGNAL AND TEST CIRCUIT; see Fig.5						
V_{O}	DC output voltage (pin 46)		4.3	4.6	5.1	V
t_{sup}	suppression time		6	7.5	10	μs
f_{trigger}	trigger sensitivity	$V_{35} = 200 \text{ mV (peak)}$; $V_{58} < 1.8 \text{ V}$	–	1000	–	Hz
		$V_{35} = 200 \text{ mV (peak)}$; $V_{58} > 2.2 \text{ V}$	–	–	100	Hz
		$V_{35} = 20 \text{ mV (peak)}$	–	–	100	Hz
$I_{\text{sink(AGC)}}$	AM noise blanker AGC sink current (pin 6)	$V_6 = 3 \text{ V}$	35	50	65	μA
V_{AGC}	AM noise blanker AGC voltage (pin 6)	$V_{32-33} = 0 \text{ V}$	1.9	2.2	2.5	V
FM signal channel						
RF AGC						
$V_{\text{i(RF)(rms)}}$	RF input voltage for start of wide-band AGC (pin 25 to 27) (RMS value)	data byte 5 bit 5 = 0, bit 6 = 0	–	4	–	mV
		data byte 5 bit 5 = 1, bit 6 = 0	–	8	–	mV
		data byte 5 bit 5 = 0, bit 6 = 1	–	12	–	mV
		data byte 5 bit 5 = 1, bit 6 = 1	–	16	–	mV
$I_{\text{drive(pd)}}$	pin diode drive current (pin 24)	$V_{24} = 0.5$ to 4.0 V	8	11.5	15	mA
I_{ch}	charge current AGC peak detector (pin 22)		–350	–600	–850	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{dis}	discharge current AGC peak detector (pin 22)		15	25	35	μA
V_{th}	threshold voltage for narrow-band AGC (pin 58)	data byte 5 bit 7 = 1; standard setting of level DAA	500	950	1400	mV
RF MIXER						
R_i	input resistance (pin 25 to 27)		–	1.4	–	$k\Omega$
C_i	input capacitance (pin 25 to 27)		–	5	7	pF
R_o	output resistance (pin 35 to 36)		100	–	–	$k\Omega$
C_o	output capacitance (pin 35 to 36)		–	5	7	pF
$V_{i(RF)(max)}$	maximum RF input voltage (pin 25 to 27)	1 dB compression point of $V_{35-36(p-p)}$	70	100	–	mV
V_{ref}	reference voltage (pin 28)	FM mode	6.5	7.1	7.9	V
		AM mode	2.7	3.1	3.4	V
$V_{o(max)(p-p)}$	maximum output voltage (pin 35 to 36) (peak-to-peak value)		3	–	–	V
$g_{m(CONV)}$	conversion transconductance		8.5	12.5	18	mA/V
$g_{m(CONV)}(T)$	conversion transconductance temperature dependency		–	–0.1	–	%/K
$V_{i(n)(eq)}$	equivalent input noise voltage (pin 25 to 27)	$R_{gen} = 600 \Omega$; $R_L = 2.8 k\Omega$; noise of R_{gen} not included	–	2.6	3.1	$\frac{nV}{\sqrt{Hz}}$
F_{FMixer}	noise figure of FM mixer		–	3	4.6	dB
I_{bias}	mixer bias current (pins 35 and 36)	FM position	4.8	6	7.2	mA
IP3	3rd-order intermodulation		116	119	–	dB μV
IRR	image rejection ratio		25	30	–	dB
IF AMPLIFIER 1						
G_{AMP1}	amplifier gain	$R_L = 330 \Omega$; $V_{39-37} = 1 mV$	8.5	10.5	12.5	dB
$V_{i(max)(M)}$	maximum input peak voltage (pin 39 to 37)	1 dB compression point of $V_{40(peak)}$	300	–	–	mV
$V_{o(max)(M)}$	maximum output peak voltage (pin 40)		1.2	1.5	–	V
R_i	input resistance (pin 39 to 37)		270	330	390	Ω

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_i	input capacitance (pin 39 to 37)		–	5	7	pF
R_o	output resistance (pin 40)		270	330	390	Ω
C_o	output capacitance (pin 40)		–	5	7	pF
$V_{i(n)(eq)}$	equivalent input noise voltage (pin 39 to 37)	$R_{gen} = 330 \Omega$; $R_L = 330 \Omega$; noise of R_{gen} not included	–	7	10	$\frac{nV}{\sqrt{Hz}}$
F_{IFAMP1}	noise figure of IF amplifier 1		–	9.5	13	dB
IP3	3rd-order intermodulation		120	123	–	dB μ V
IF AMPLIFIER 2						
G_{AMP2}	amplifier gain	$R_L = 330 \Omega$; $V_{43-41} = 1 \text{ mV}$	3	4.5	6	dB
$V_{i(max)(M)}$	maximum input peak voltage (pin 43 to 41)	1 dB compression point of $V_{47(peak)}$	600	–	–	mV
$V_{o(max)(M)}$	maximum output peak voltage (pin 47)		1.2	1.5	–	V
R_i	input resistance (pin 43 to 41)		270	330	390	Ω
C_i	input capacitance (pin 43 to 41)		–	5	7	pF
R_o	output resistance (pin 47)		270	330	390	Ω
C_o	output capacitance (pin 47)		–	5	7	pF
$V_{i(n)(eq)}$	equivalent input noise voltage (pin 43 to 41)	$R_{gen} = 330 \Omega$; $R_L = 330 \Omega$; noise of R_{gen} not included	–	9	12	$\frac{nV}{\sqrt{Hz}}$
F_{IFAMP2}	noise figure of IF amplifier 2		–	12	15	dB
IP3	3rd-order intermodulation		129	132	–	dB μ V
FM demodulator and level detector see Figs 6 and 7						
FM LIMITER						
G_{lim}	limiter gain	$R_{gen} = 50 \Omega$	74	80	–	dB
R_i	input resistance (pin 49 to 50)		270	330	390	k Ω
C_i	input capacitance (pin 49 to 50)		–	5	7	pF
$V_{o(lim)(p-p)}$	limiter output voltage (pin 60 to 61) (peak-to-peak value)		500	700	–	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM DEMODULATOR						
$V_{o(rms)}$	RDS MPX output voltage (pin 4) (RMS value)	$\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 57 \text{ kHz}$; $V_{49-50} = 20 \text{ } \mu\text{V}$ to 1 V	180	230	280	mV
$V_{start(lim)(rms)}$	start of limiting of RDS MPX output voltage (pin 49 to 50) (RMS value)	$\alpha_{AF} = -3 \text{ dB}$	—	10	15	μV
	start of limiting of MPX output voltage (RMS value)	$\alpha_{AF} = -3 \text{ dB}$	—	10	15	μV
$I_{o(max)}$	maximum RDS MPX output current (pin 4)		—	—	100	μA
R_o	output resistance (pin 4)		—	—	500	Ω
R_L	load resistance (pin 50)		20	—	—	k Ω
C_L	load capacitance (pin 50)		—	—	50	pF
B	bandwidth RDS MPX output (pin 4)	$C_L = 0$; $R_L > 20 \text{ k}\Omega$	200	300	—	kHz
PSRR	power supply ripple rejection (pin 4)	$f_{ripple} = 100 \text{ Hz}$ to 20 kHz	—	40	—	dB
$V_{o(rms)}$	MPX output voltage (pin 3) (RMS value)	$\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; $V_{49-50} = 20 \text{ } \mu\text{V}$ to 1 V ; de-emphasis = $75 \text{ } \mu\text{s}$	180	230	280	mV
$V_{o(SEN)(rms)}$	sensitivity for MPX output voltage (pin 49 to 50) (RMS value)	$\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$ $S+N/N = 26 \text{ dB}$	—	10	15	μV
		$S+N/N = 46 \text{ dB}$	—	50	75	μV
S+N/N	maximum signal plus noise-to-noise ratio of MPX output voltage	$\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; $V_{49-50} = 10 \text{ mV}$; de-emphasis = $75 \text{ } \mu\text{s}$	67	70	—	dB
THD	total harmonic distortion of MPX output voltage	$\Delta f = 75 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; de-emphasis = $75 \text{ } \mu\text{s}$; $200 \text{ } \mu\text{V} < V_{49-50} < 800 \text{ mV}$	—	0.35	0.7	%
$V_{o(sup)(MPX)}$	AM suppression of MPX output voltage	$\Delta f = 22.5 \text{ kHz}$; $f_{mod} = 1 \text{ kHz}$; $m = 0.3$; de-emphasis = $75 \text{ } \mu\text{s}$ $V_{49-50} = 500 \text{ } \mu\text{V}$ to 300 mV	50	60	—	dB
		$V_{49-50} = 20$ to $500 \text{ } \mu\text{V}$	—	40	—	dB
		$V_{49-50} = 300 \text{ mV}$ to 1 V	—	40	—	dB
$I_{o(max)}$	maximum MPX output current (pin 3)		—	—	100	μA
$R_{L(max)}$	minimum load resistance (pin 3)		20	—	—	k Ω
$R_{o(max)}$	maximum output resistance (pin 3)		—	—	500	Ω

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C _{L(max)}	maximum load capacitance (pin 3)		–	–	50	pF
B _{MPX}	bandwidth MPX output	C _L = 0; R _L > 20 kΩ	200	–	–	kHz
PSRR	power supply ripple rejection	f _{ripple} = 100 Hz to 20 kHz	–	40	–	dB
MPX MUTE						
α _{mute}	muting depth	during RDS update	60	80	–	dB
t _{att}	attack time MPX mute	C ₆ = 10 nF	0.75	1	1.25	ms
t _{decay}	decay time MPX mute	C ₆ = 10 nF	0.75	1	1.25	ms
I _{dis}	discharge current (pin 6)	V ₆ = 3 V; data byte 3 bit 7 = 1	24	32	38	μA
I _{ch}	charge current (pin 6)	V ₆ = 3 V; data byte 3 bit 7 = 0	–24	–32	–38	μA
DEMODULATOR AFC						
G _{AFC}	AFC gain	detuning Δf = 100 kHz	28	32	–	dB
V _{offsetDC}	residual DC offset (pin 4)	L _{demod} = typical value V ₄₉₋₅₀ = 10 to 80 μV V ₄₉₋₅₀ = 80 μV to 800 mV	– –	0.1 10	1 30	V mV
		L _{demod} = ±6% V ₄₉₋₅₀ = 10 to 80 μV V ₄₉₋₅₀ = 80 μV to 800 mV	– –	0.240 25	1 500	V mV
FM IF LEVEL DETECTOR						
V _{LEVEL}	level output DC voltage (pin 58)	V ₄₉₋₅₀ = 10 μV to 1 V V ₄₉₋₅₀ < 1 μV; default setting of level DAA V ₄₉₋₅₀ = 1 mV; default setting of level DAA	0 0.1 1	– 0.35 1.5	7 0.9 2.1	V V V
ΔV _{level}	level starting point for adjustment of step size	default setting of level slope	30	40	50	mV
V _{level(slope)}	slope of level voltage	default setting of level slope	650	800	950	$\frac{\text{mV}}{20 \text{ dB}}$
ΔV _{step}	level slope adjust step size	V ₄₉₋₅₀ = 1 mV	45	50	75	$\frac{\text{mV}}{20 \text{ dB}}$
V _{O(B)}	bandwidth level output voltage (pin 58)	V ₄₉₋₅₀ = 10 mV; f _{mod} = 22.5 kHz; default setting of DAA	200	300	–	mV
I _{source}	output source current (pin 58)		–	–	–300	μA
I _{sink}	output sink current (pin 58)		50	–	–	μA
R _O	output resistance at level voltage (pin 58)		–	–	500	Ω
RR	ripple rejection (pin 58)	f _{ripple} = 100 Hz; V _{DDA1(ripple)} = 100 mV (RMS)	–	40	–	dB

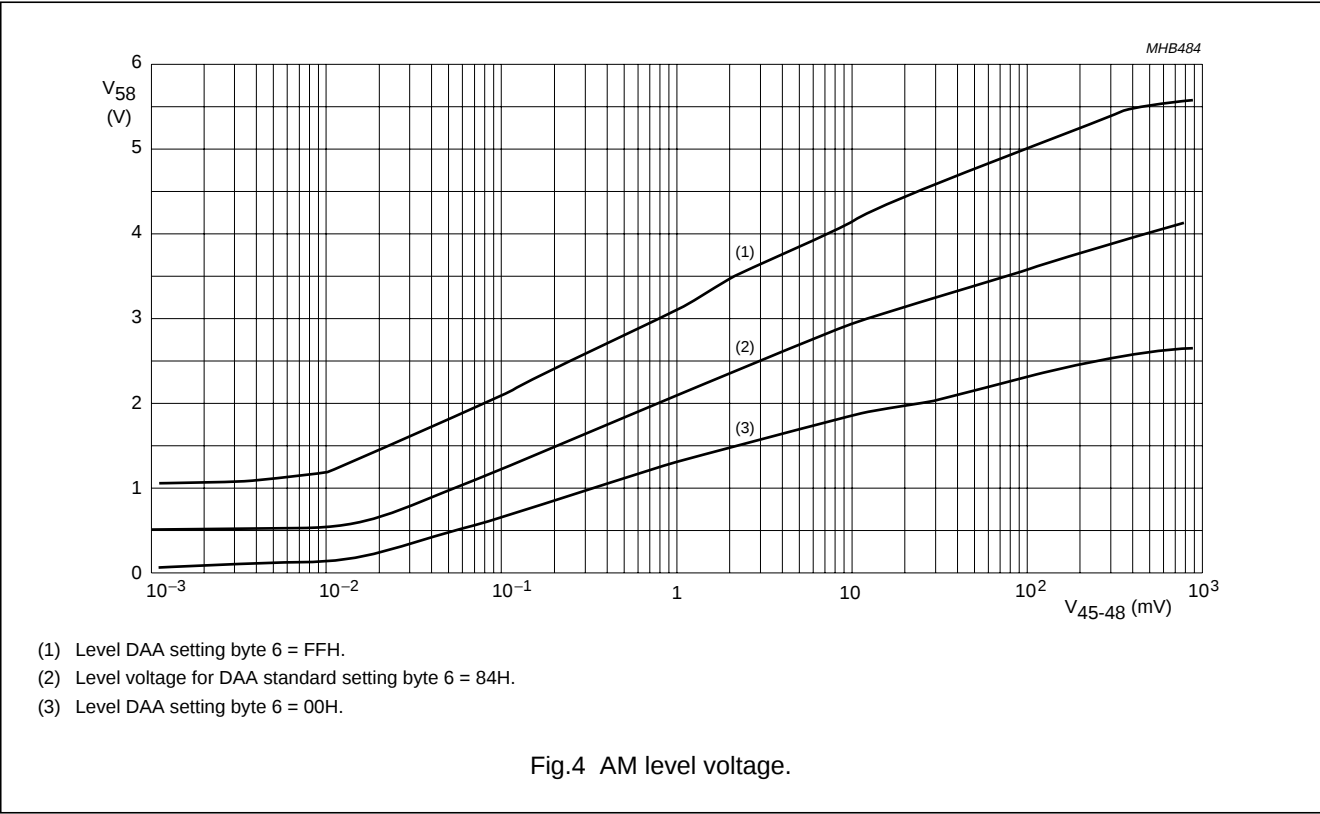
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RDS update						
I _{sink(max)}	AFHOLD maximum sink current (pin 7)	after first bus transmission with AF = 1 (start of RDS update); V _{AFHOLD} = 0.5 V	1.0	1.2	1.4	mA
	AFSAMPLE maximum sink current (pin 8)	no RDS update in progress; V _{AFSAMPLE} = 0.5 V	1.0	1.2	1.4	mA
Test mode (pins 15, 20, 31 and 63); note 2						
V _{i(ext)}	external input voltage to clock state-machine (pin 20)	V _{DAATD(L)} = 2.5 V; V _{DAATD(H)} = 3.5 V	2.5	–	3.5	V
	external input voltage to clock DAA (pin 63)	V _{SCL(L)} = 0 V; V _{SCL(H)} = 5 V	0	–	5	V
V _{pulse}	enabling of load PLL signal (pin 31)	pin 15 in test mode	5.1	6	6.9	V

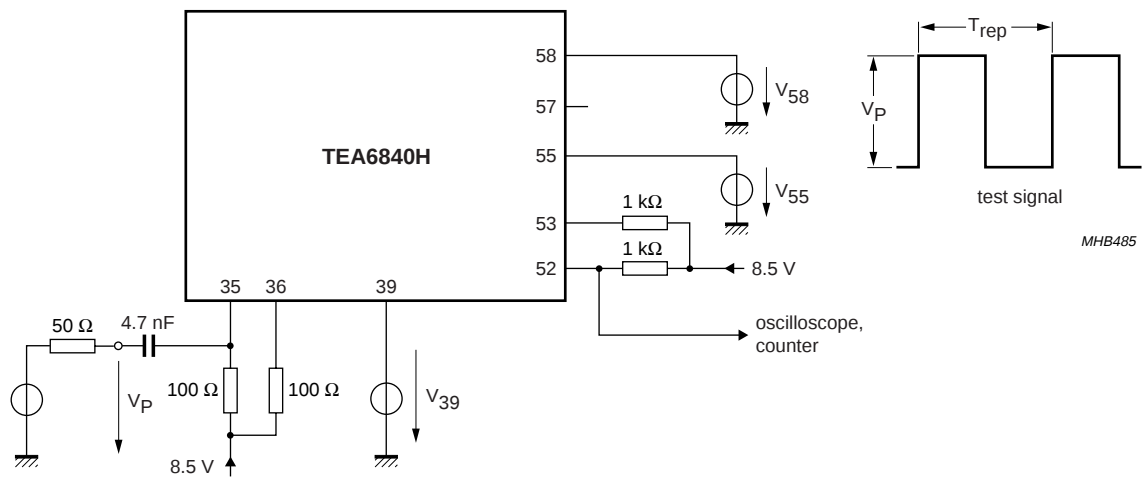
Notes

1. DAA conversion gain formula: $V_{21} = \left[2 \times \left(0.75 \times \frac{n}{128} + 0.25 \right) \times (V_{19} + V_{20}) \right] - V_{20}$; where n = 0 to 127.
2. Pin 15: R_{ext} = 68 kΩ connected to ground activates the 2nd I²C-bus address and R_{ext} = 100 kΩ connected to V_{DDA1} sets the IC into test mode.



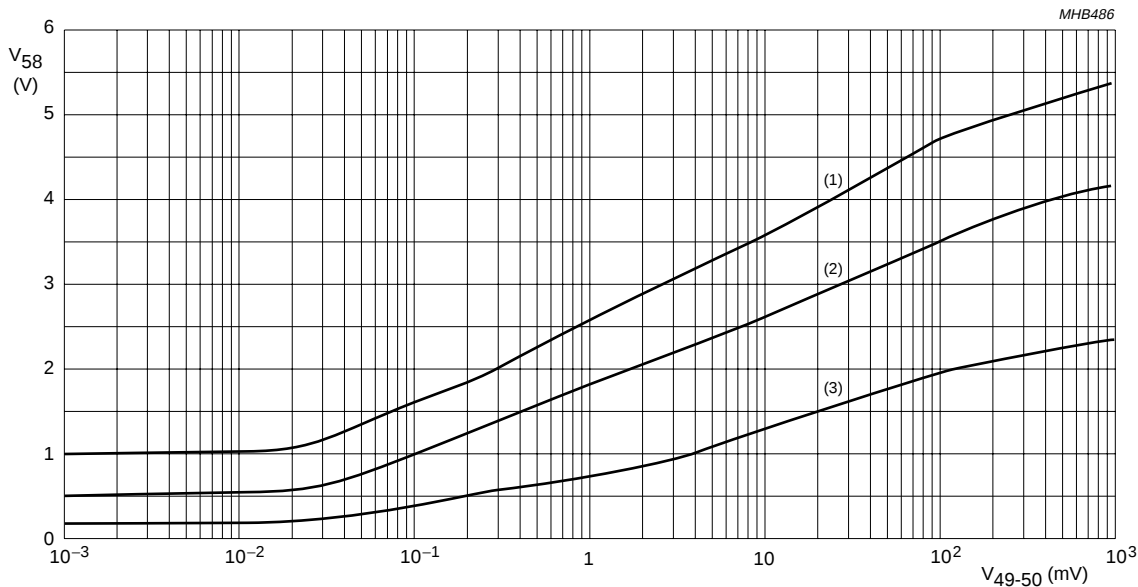
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$T_{rep} = 500 \text{ Hz}$; $t_r < 50 \text{ ns}$; $t_f < 50 \text{ ns}$; duty factor 50%; $V_{55} = 3 \text{ V}$; $V_{39} = 4 \text{ V}$.

Fig.5 Test circuit for AM noise blanker.

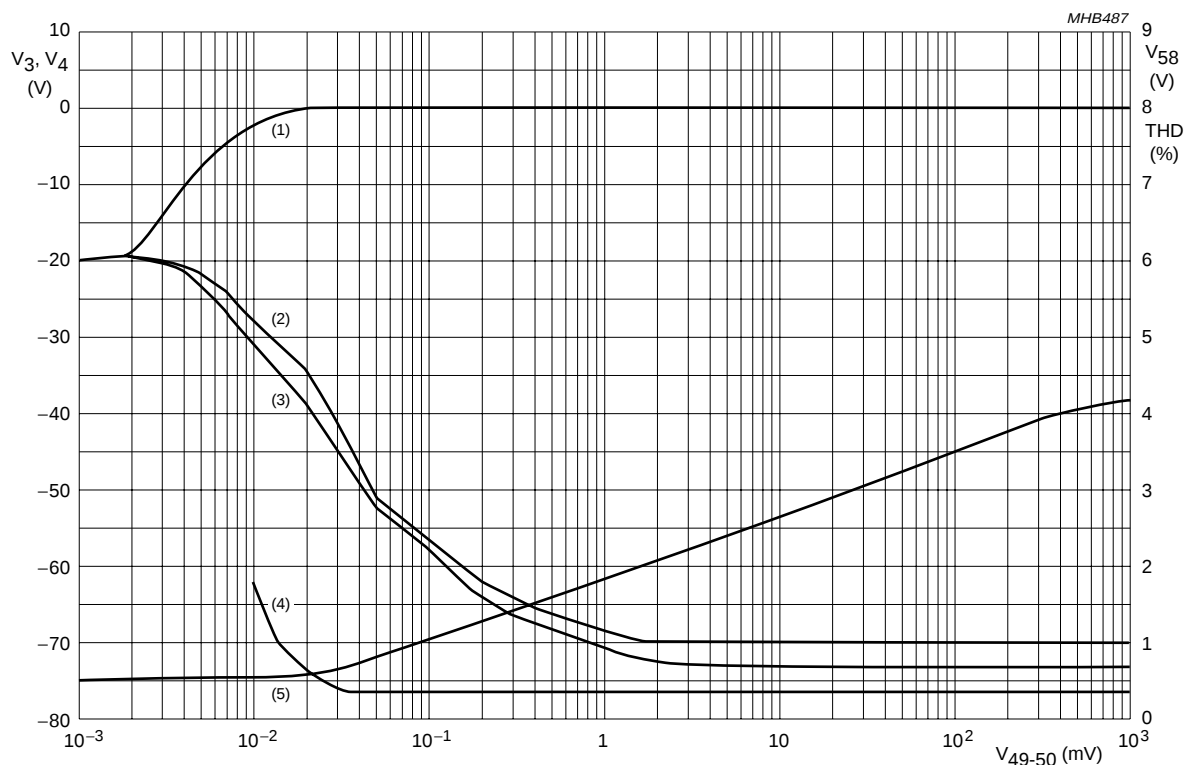


- (1) Level DAA setting byte 6 = FFH.
- (2) Level voltage for DAA standard setting byte 6 = 84H.
- (3) Level DAA setting byte 6 = 00H.

Fig.6 FM level voltage.

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- (1) Output voltage for FMMPX and RDSMPX: $f_{IF} = 10.7$ MHz; $\Delta f = 22.5$ kHz; $f_{mod} = 1$ kHz.
- (2) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 μ s for FMMPX.
- (3) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 μ s for RDSMPX.
- (4) THD for FMMPX and RDSMPX.
- (5) Level for standard setting of level DAA, byte 6 = 84H.

Fig.7 (S + N)/N, THD and level voltage for FM mode as a function of FM demodulator input voltage.

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I²C-BUS AND I²C-BUS CONTROLLED FUNCTIONS**I²C-bus specification**

The standard I²C-bus specification is expanded by the following definitions.

- 1st chip address C2: 1100001 $\overline{R/W}$
- 2nd chip address C0: 1100000 $\overline{R/W}$.

Structure of the I²C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

A second I²C-bus address can be selected by connecting pin 15 via a 68 k Ω resistor to GND.

Connecting pin 15 to V_{DDA1} via a 100 k Ω resistor or feeding 50 μ A into that pin switches the IC into the test mode.

TEST MODE

During test mode the digital-to-analog converters of the level and antenna DAA functions can be sequenced by the I²C-bus SCL line.

During test mode either the TEA6880H reference frequency, the PLL reference frequency divider or the programmable divider output can be switched to pin 15.

DATA TRANSFER FOR THE TEA6840H

Data sequence:

- Address
- Byte 1
- Byte 2
- Byte 3
- Byte 4
- Byte 5
- Byte 6.

The data transfer has to be in this order. The LSB = 0 indicates a WRITE operation to the TEA6840H. Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

In byte 5, 4 bits are reserved for test mode purposes. Those can only be used when the test mode is activated by the select pin 15.

Hints: When the IC is used together with the Car Analog Sound Processor IC (TEA6880H) and when the SCL and SDA lines are connected via Car Analog Sound Processor IC's I²C-bus buffer interface, the pull-up resistors of the tuner IC should be connected to the digital supply voltage of the TEA6880H. Otherwise a bus pull-down can occur switching off the tuner IC supply when the I²C-bus buffer interface of the TEA6880H is enabled for data transfer to the tuner IC.

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting the mute bit (data byte 3 bit 7) to logic 1.

To select an FM frequency, two I²C-bus transmissions are necessary. First data byte 3 bit 7 = 1 and second data byte 3 bit 7 = 0.

Default settings by power-on reset: To be defined.

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Table 1 Data to be received by the IC

DATA BYTE	BIT	DESCRIPTION	RESULT
1	0 to 6	define the setting of the programmable counter of the synthesizer PLL	
	7	start RDS update	bit 7 = 1
		no RDS update started	bit 7 = 0
2	0 to 7	define the setting of the programmable counter of the synthesizer PLL	
3	0 to 6	define the setting of the antenna DAA circuit	
	7	FM audio output muted; writing to programmable divider enabled for AM and FM	bit 7 = 1
		FM audio output not muted	bit 7 = 0
4	0	AM mode	bit 0 = 1
		FM mode	bit 0 = 0
	1 and 2	for FM mode: FM band and local/distance select for AM mode: division ratio N2 divider (AM band select) and switching for AM stereo	
	3	IF counter prescaler ratio = 10	bit 3 = 1
		IF counter prescaler ratio = 100	bit 3 = 0
	4	LSB for reference frequency for synthesizer	
	5	reference frequency for synthesizer	
	6	MSB for reference frequency for synthesizer	
	7	IF counter period = 2 ms	bit 7 = 1
		IF counter period = 20 ms	bit 7 = 0
5	0 and 1	bits only valid in test mode; setting define output at pin 15	
	2	external clock for level and antenna DAA enabled (only valid in test mode)	bit 2 = 1
		external clock for level and antenna DAA disabled (only valid in test mode)	bit 2 = 0
	3	3-state active (only valid in test mode)	bit 3 = 1
		3-state off (only valid in test mode; charge pumps operational)	bit 3 = 0
	4	AM soft mute on	bit 4 = 1
		AM soft mute off	bit 4 = 0
	5	LSB for wide band AGC setting for AM and FM	
	6	MSB for wide band AGC setting for AM and FM	
	7	keyed function on	bit 7 = 1
		keyed function off	bit 7 = 0
6	0	LSB for the definition of the level slope setting of the level DAA	
	1	definition of the level slope setting of the level DAA	
	2	MSB for the definition of the level slope setting of the level DAA	
	3	LSB for the definition of the starting point setting of the level DAA	
	4 to 6	definition of the starting point setting of the level DAA	
	7	MSB for the definition of the starting point setting of the level DAA	

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Table 2 Reference frequency setting in byte 4

BIT 4	BIT 5	BIT 6	FREQUENCY SETTING (kHz)
0	0	0	100
0	0	1	50
0	1	0	25
0	1	1	20
1	0	0	10
1	0	1	10
1	1	0	10
1	1	1	10

Table 3 AM/FM setting in byte 4

BIT 0	BIT 1	BIT 2	DESCRIPTION
0	0	0	FM standard: dead zone high current charge pump active, FM AGC defined by RF level and threshold level setting by I ² C-bus
0	1	0	FM local: dead zone high current charge pump active, FM AGC source current set to maximum
0	0	1	FM East Europe: dead zone high current charge pump switched off, current of low current charge pump set to 1 mA
0	1	1	FM weather band: division ratio N1 set to 1 and I and Q phase shift network switched on, WX flag signal activated
1	0	0	AM mono, N2 divider set to 5 (SW)
1	1	0	AM stereo, N2 divider set to 5 (SW)
1	0	1	AM mono, N2 divider set to 10 (LW, MW)
1	1	1	AM stereo, N2 divider set to 10 (LW, MW)

In AM mode dead zone high current charge pump switched off, current of low current charge pump set to 1 mA.

Table 4 Test bits setting in byte 5

BIT 0	BIT 1	OUTPUT AT PIN 15
0	0	75.368 kHz TEA6880H reference frequency
0	1	PLL synthesizer reference frequency
1	0	tuner oscillator frequency divided by division ratio of programmable divider
1	1	not used (no output)

Standard setting of the level DAA in byte 6

Definition of the starting point of the level voltage: bit 7 = 1, bits 3 to 6 set to logic 0.

Definition of the slope of the level voltage: bit 2 = 1, bit 0 and bit 1 set to logic 0.

Data to be transmitted by the IC

Data byte 1 bits 0 to 7: output of the IF counter result.

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I²C-BUS PROTOCOL**Table 5** Write mode

S ⁽¹⁾	CHIP ADDRESS (write)	A ⁽²⁾	DATA BYTE(S)	A ⁽²⁾	P ⁽³⁾
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Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 6 Read mode

S ⁽¹⁾	CHIP ADDRESS (read)	A ⁽²⁾	DATA BYTE 1
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Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 7 Chip address byte

CHIP ADDRESS							READ/WRITE
1	1	0	0	0	0	0/1 ⁽¹⁾	R/W ⁽²⁾

Notes

1. Defined by address pin 15. Logic 1 = 1st chip address; logic 0 = 2nd chip address.
2. Logic 0 = write operation to TEA6840H; logic 1 = read operation from TEA6840H.

Table 8 Read mode: 1st data byte

IF COUNTER RESULT							
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0

Table 9 Write mode: data byte 1

FUNCTION	SETTING OF PROGRAMMABLE COUNTER OF SYNTHESIZER PLL						
Logic 1 = start of RDS update	PCA6	PCA5	PCA4	PCA3	PCA2	PCA1	PCA0

Table 10 Write mode: data byte 2

SETTING OF PROGRAMMABLE COUNTER OF SYNTHESIZER PLL							
PCB7	PCB6	PCB5	PCB4	PCB3	PCB2	PCB1	PCB0

Table 11 Write mode: data byte 3

FUNCTION	SETTING OF ANTENNA DIGITAL AUTO ALIGNMENT						
Logic 1 = FM audio muted; writing to programmable divider enabled; logic 0 = FM audio not muted	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

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Table 12 Write mode: data byte 4

IF-COUNTER PERIOD	REFERENCE FREQUENCY FOR SYNTHESIZER			IF-COUNTER PRESCALE	FM MODE: BAND AND LOCAL/DISTANT SELECT; AM MODE: BAND AND AM STEREO SELECT		AM/FM SWITCH
Logic 1 = 2 ms	RFS2	RFS1	RFS0	logic 1: ratio = 10	logic 1: N2 = 10	logic 1 = AM stereo	logic 1 = AM mode
Logic 0 = 20 ms	RFS2	RFS1	RFS0	logic 0: ratio = 100	logic 0: N2 = 5	logic 0 = AM mono	logic 0 = FM mode

Table 13 Data byte 4; reference frequency setting; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	f _{ref} (kHz)
X	0	0	0	X	X	X	X	100
X	1	0	0	X	X	X	X	50
X	0	1	0	X	X	X	X	25
X	1	1	0	X	X	X	X	20
X	0	0	1	X	X	X	X	10
X	1	0	1	X	X	X	X	10
X	0	1	1	X	X	X	X	10
X	1	1	1	X	X	X	X	10

Note

1. X = see Table 1.

Table 14 Data byte 4 (FM mode); note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FM
X	X	X	X	X	0	0	0	standard
X	X	X	X	X	0	1	0	local
X	X	X	X	X	1	0	0	east europe
X	X	X	X	X	1	1	0	weather band

Note

1. X = see Table 1.

Table 15 Data byte 4 (AM mode); note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	AM
X	X	X	X	X	0	0	1	AM mono; N2 = 5 (SW)
X	X	X	X	X	0	1	1	AM stereo; N2 = 5 (SW)
X	X	X	X	X	1	0	1	AM mono; N2 = 10 (LW and MW)
X	X	X	X	X	1	1	1	AM stereo; N2 = 10 (LW and MW)

Note

1. X = see Table 1.

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Table 16 Write mode: data byte 5

KEYED FM AGC	SETTING OF WIDE-BAND AGC FOR AM/FM		AM SOFT MUTE	IN TEST MODE CHARGE PUMP 3-STATE	IN TEST MODE EXTERNAL CLOCK FOR LEVEL AND ANTENNA DAA	IN TEST MODE SETTING OF PIN 15	
Logic 1 = on	WBA1	WBA0	logic 1 = on (default)	logic 1 = 3-state on	logic 1 = external clock enabled	TMS1	TMS0
Logic 0 = off	WBA1	WBA0	logic 0 = off	logic 0 = 3-state off	logic 0 = external clock disabled	TMS1	TMS0

Table 17 Data byte 5: setting of wide band AGC for AM; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	V ₃₂₋₃₃ (mV) (peak)
X	0	0	X	X	X	X	X	375
X	0	1	X	X	X	X	X	500
X	1	0	X	X	X	X	X	625
X	1	1	X	X	X	X	X	750

Note

1. X = see Table 1.

Table 18 Data byte 5: setting of wide band AGC for FM; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	V ₂₅₋₂₇ (mV) (RMS)
X	1	1	X	X	X	X	X	4
X	1	0	X	X	X	X	X	8
X	0	1	X	X	X	X	X	12
X	0	0	X	X	X	X	X	16

Note

1. X = see Table 1.

Table 19 Data byte 5: setting function of pin 15 in test mode; note 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	OUTPUT AT PIN 15
X	X	X	X	X	X	0	0	TEA6880H reference frequency
X	X	X	X	X	X	0	1	tuner oscillator frequency divided by division ratio of programmable divider
X	X	X	X	X	X	1	0	PLL synthesizer reference frequency
X	X	X	X	X	X	1	1	not used

Note

1. X = see Table 1.

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Table 20 Write mode: data byte 6

SETTING OF LEVEL DAA STARTING POINT					SETTING OF LEVEL DAA SLOPE		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0

Table 21 Data byte 6: standard setting

SETTING OF LEVEL DAA STARTING POINT					SETTING OF LEVEL DAA SLOPE		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

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TEST CIRCUIT

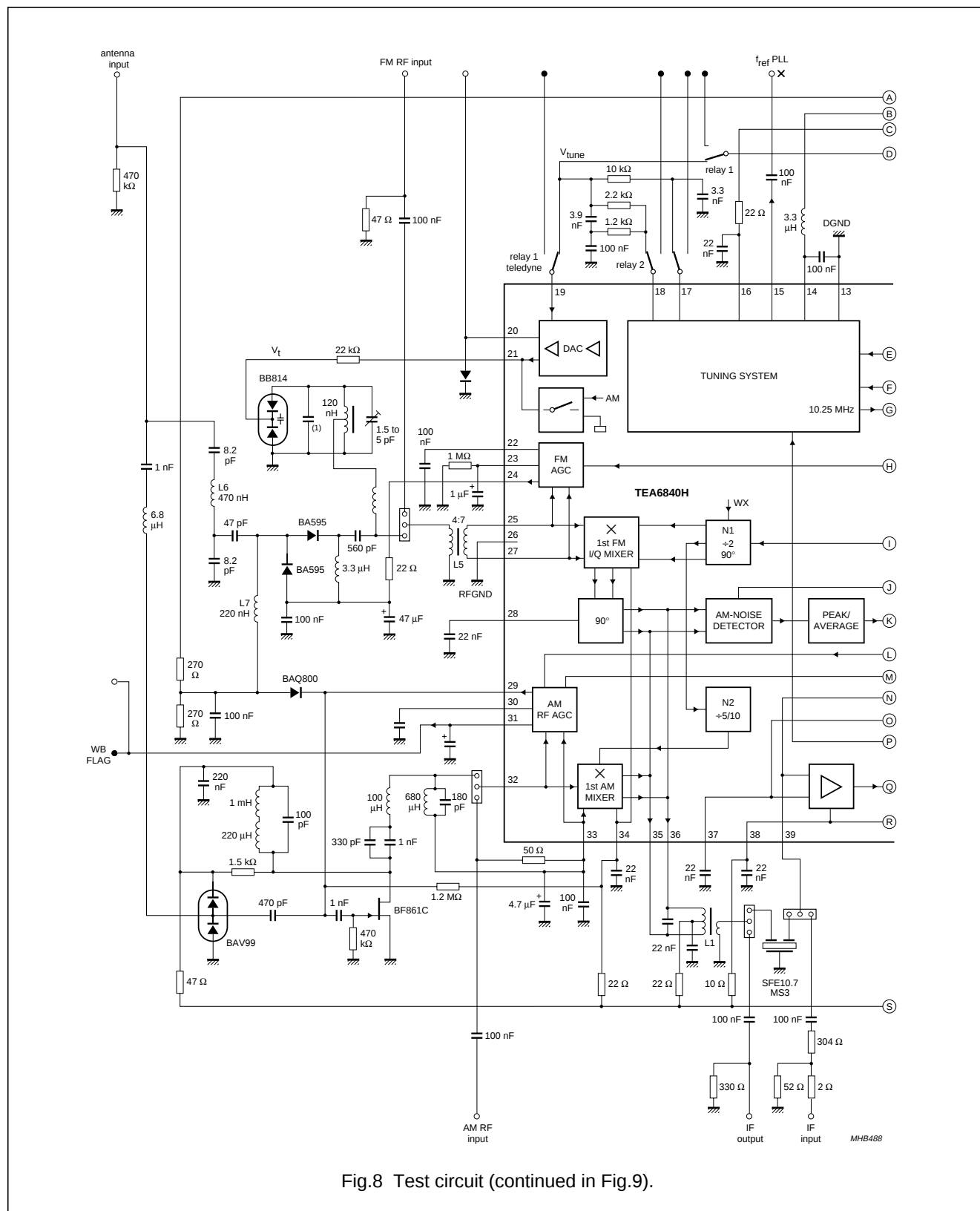


Fig.8 Test circuit (continued in Fig.9).

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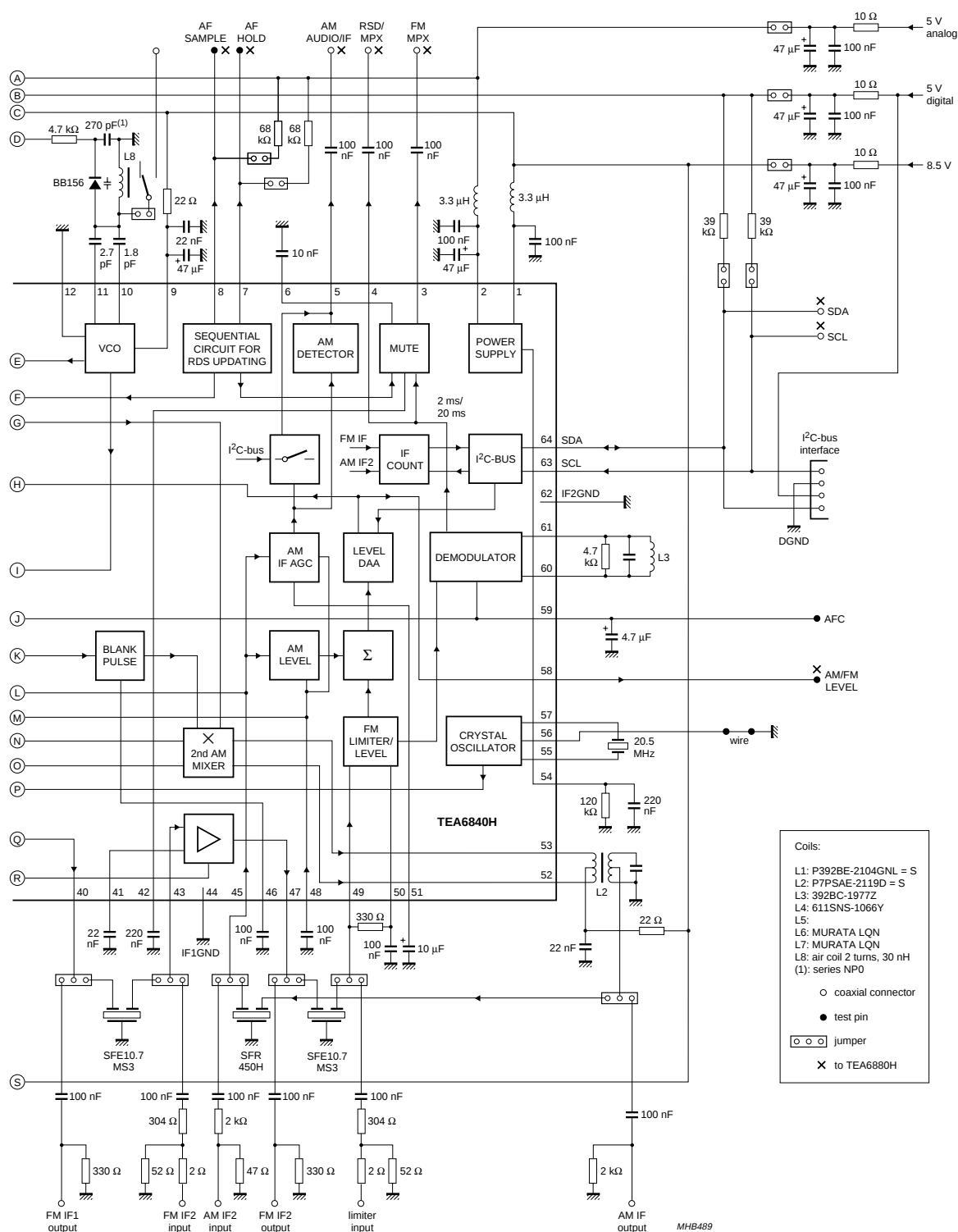


Fig.9 Test circuit (continued from Fig.8).

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Table 22 DC operating points

SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM			FM		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
V _{DDA1}	1	external 8.5			external 8.5		
V _{DDA2}	2	external 5			external 5		
FMMPX	3	floating			3	3.5	4
RDSMPX	4	floating			2.6	3.1	3.3
AMAFIF2	5	4	4.3	4.6	floating		
TRDSMUTE	6	1.9	2.2	2.5	0.7 (muted)	1.2 (muted)	1.7 (muted)
					5.2 (not muted)	5.7 (not muted)	6.2 (not muted)
AFHOLD	7	open-collector			open-collector		
AFSAMPLE	8	0	0.2	0.5	0	0.2	0.5
V _{DDA3}	9	external 8.5			external 8.5		
OSCTNK	10	5	6.1	7.2	5	6.1	7.2
OSCFDB	11	2.2	2.8	3.4	2.2	2.8	3.4
VCOGND	12	external 0			external 0		
DGND	13	external 0			external 0		
V _{DDD}	14	external 5			external 5		
f _{ref}	15	3.2	3.4	3.7	3.2	3.4	3.7
V _{DDA4}	16	external 8.5			external 8.5		
CPOUT	17	0	–	8.5	0	–	8.5
V _{tune}	18	0	–	8.5	0	–	8.5
DAAIN	19	0	–	8.5	0	–	8.5
DAATD	20	floating			0.2	–	1.5
DAAOUT	21	–	0.2	0.3	0.2	–	8.25
T1FMAGC	22	floating			1	–	7
T2FMAGC	23	7.5	8	8.3	3.9	4.6	5.3
IFMAGC	24	floating			1.5 (external biasing)	–	4 (external biasing)
FMMIXIN1	25	1	1.3	1.6	2.3	2.8	3.3
RFGND	26	external 0			external 0		
FMMIXIN2	27	1	1.3	1.6	2.3	2.8	3.3
V _{ref} (FMMIX1)	28	2.7	3.1	3.4	6.5	7.1	7.9
IAMAGC	29	open-collector			open-collector		
T2AMAGC	30	2.5	2.8	3.1	floating		
T1AMAGC	31	0	2.8	4.6	0 (no WX)	0.3 (no WX)	0.5 (no WX)
AMMIX1IN1	32	2.3	2.75	3.1	floating		
AMMIX1IN2	33	2.3	2.75	3.1	floating		
V _{DDA5}	34	external 8.5			external 8.5		
MIX1OUT1	35	external 8.5			external 8.5		

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SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM			FM		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
MIX1OUT2	36	external 8.5			external 8.5		
IFAMP1DEC	37	2.4	2.7	3	2.3	2.7	3.1
V _{DDA6}	38	external 8.5			external 8.5		
IFAMP1IN	39	2.4	2.7	3	2.3	2.7	3.1
IFAMP1OUT	40	7.2	7.9	–	3.6	4	4.4
IFAMP2DEC	41	3	4	5	2.7	3.1	3.5
C _{offset}	42	floating			3	3.5	4
IFAMP2IN	43	3	4	5	2.7	3.1	3.5
IF1GND	44	external 0			external 0		
AMIF2IN	45	2.4	2.7	3.2	floating		
AMNBHOLD	46	4.3	4.6	5.1	8	8.4	–
IFAMP2OUT	47	7.2	7.9	–	3.4	3.9	4.4
AMIF2DEC	48	2.4	2.7	3.2	floating		
FMLIMIN	49	2.5	3	3.5	2.5	2.8	3.1
FMLIMDEC	50	2.5	3	3.5	2.5	2.8	3.1
C _{AGC}	51	3.6	4.3	4.8	4.1	4.6	5.1
AMMIX2OUT1	52	external 8.5			external 8.5		
AMMIX2OUT2	53	external 8.5			external 8.5		
I _{ref}	54	4	4.25	4.5	4	4.25	4.5
XTAL1	55	1.7	2.1	2.5	1.7	2.1	2.5
XTALGND	56	external 0			external 0		
XTAL2	57	1.7	2.1	2.5	1.7	2.1	2.5
V _{level}	58	0.05	–	7	0	–	7
C _{AFC}	59	floating			1.2	3.4	4.1
QDET1	60	floating			3.6	4.1	4.6
QDET2	61	floating			3.6	4.1	4.6
IF2GND	62	external 0			external 0		
SCL	63	4.8	5	5.2	4.8	5	5.2
SDA	64	4.8	5	5.2	4.8	5	5.2

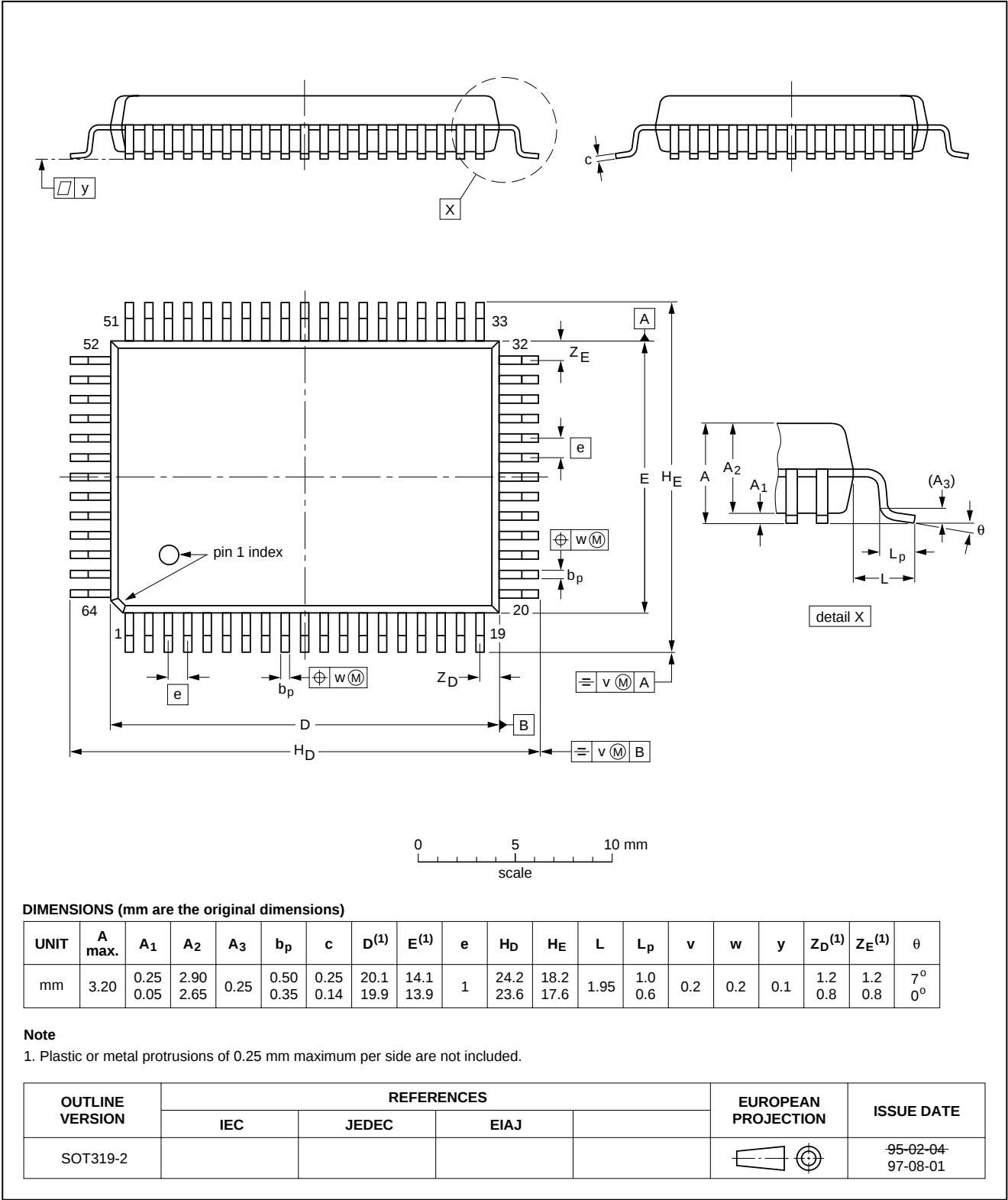
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TEA6840H

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT319-2



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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

New In Car Entertainment (NICE) car radio

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

New In Car Entertainment (NICE) car radio

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