LINEAR SYSTEMS

LS842
MONOLITHIC DUAL
N-CHANNEL JFET

micross

Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS842 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS842 features a 25-mV offset and 40-µV/°C drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS842 Applications:

- Wideband Differential Amps
- High-Speed,Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES	
LOW DRIFT	$\lvert V_{GS1-2} / T \rvert \le 40\mu V/°C$
LOW LEAKAGE	I_G = 10pA TYP.
LOW NOISE	e_n = 8nV/√Hz TYP.
LOW OFFSET VOLTAGE	$\lvert V_{GS1-2} \rvert \le 25mV$

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-65°C to +150°C
Operating Junction Temperature		+150°C
Maximum Voltage and Current for Each Transistor – Note 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	60V
$-V_{DSO}$	Drain to Source Voltage	60V
$-I_{G(f)}$	Gate Forward Current	50mA
Maximum Power Dissipation		
Device Dissipation @ Free Air – Total		400mW @ +125°C

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED				
SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$\lvert V_{GS1-2} / T \rvert$ max.	DRIFT VS. TEMPERATURE	40	µV/°C	V_{DG}=20V, I_D=200µA T_A=-55°C to +125°C
$\lvert V_{GS1-2} \rvert$ max.	OFFSET VOLTAGE	25	mV	V_{DG}=20V, I_D=200µA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

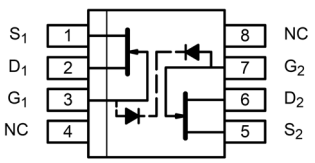
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	60	60	--	V	V_{DS} = 0 I_D=1nA
BV_{GGO}	Gate-To-Gate Breakdown	60	--	--	V	I_G= 1nA I_D= 0 I_S= 0
	TRANSCONDUCTANCE					
Y_{fss}	Full Conduction	1000	--	4000	µmho	V_{DG}= 20V V_{GS}= 0V f = 1kHz
Y_{fs}	Typical Operation	500	--	1000	µmho	V_{DG}= 20V I_D= 200µA
$\lvert Y_{FS1-2} / Y_{FS} \rvert$	Mismatch	--	0.6	3	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	0.5	2	5	mA	V_{DG}= 20V V_{GS}= 0V
$\lvert I_{DSS1-2} / I_{DSS} \rvert$	Mismatch at Full Conduction	--	1	5	%	
	GATE VOLTAGE					
V_{GS}(off) or V_p	Pinchoff voltage	1	2	4.5	V	V_{DS}= 20V I_D= 1nA
V_{GS}(on)	Operating Range	0.5	--	4	V	V_{DS}=20V I_D=200µA
	GATE CURRENT					
$-I_G$max.	Operating	--	10	50	pA	V_{DG}= 20V I_D= 200µA
$-I_G$max.	High Temperature	--	--	50	nA	T_A= +125°C
$-I_G$max.	Reduced V_{DG}	--	5	--	pA	V_{DG} = 10V I_D= 200µA
$-I_{GSS}$max.	At Full Conduction	--	--	100	pA	V_{DG}= 20V , V_{DS} =0
	OUTPUT CONDUCTANCE					
Y_{OSS}	Full Conduction	--	--	10	µmho	V_{DG}= 20V V_{GS}= 0V
Y_{OS}	Operating	--	0.1	1	µmho	V_{DG}= 20V I_D= 200µA
$\lvert Y_{OS1-2} \rvert$	Differential	--	0.01	0.1	µmho	
	COMMON MODE REJECTION					
CMR	-20 log $\lvert V_{GS1-2} / V_{DS} \rvert$	--	100	--	dB	ΔV_{DS} = 10 to 20V I_D=200µA
	-20 log $\lvert V_{GS1-2} / V_{DS} \rvert$	--	75	--		ΔV_{DS} = 5 to 10V I_D=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 20V V_{GS}= 0V R_G= 10MΩ f= 100Hz NBW= 6Hz
e_n	Voltage	--	--	10	nV/√Hz	V_{DS}=20V I_D=200µA f=1KHz NBW=1Hz
		--	--	15		V_{DS}=20V I_D=200µA f=10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	4	10	pF	V_{DS}= 20V, I_D=200µA
C_{RSS}	Reverse Transfer	--	1.2	5		
C_{DD}	Drain-to-Drain	--	0.1	--		

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS842 / LS842 in PDIP & SOIC
LS842 / LS842 available as bare die
Please contact Micross for full package and die dimensions

PDIP & SOIC (Top View)



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