TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

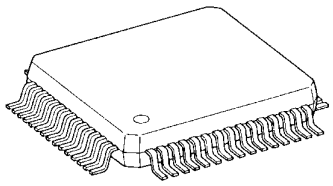
TC94A04AFG,TC94A04AFDG

1 chip Audio Digital Processor

TC94A04AFG/AFDG is a single-chip audio Digital Signal Processor, incorporating 4 way stereo analog switch, 2 ch AD converter, 4 ch DA converter, and electronic volume for trimming.

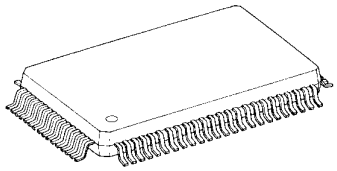
It is possible to realize many applications, such as sound field control -hall simulation, for example-, digital filter for equalizers, surround, base boost and something.

TC94A04AFG



P-QFP60-1414-0.80N

TC94A04AFDG



P-QFP80-1420-0.80M

Weight
P-QFP60-1414-0.80N: 1.08 g (typ.)
P-QFP80-1420-0.80M: 1.57 g (typ.)

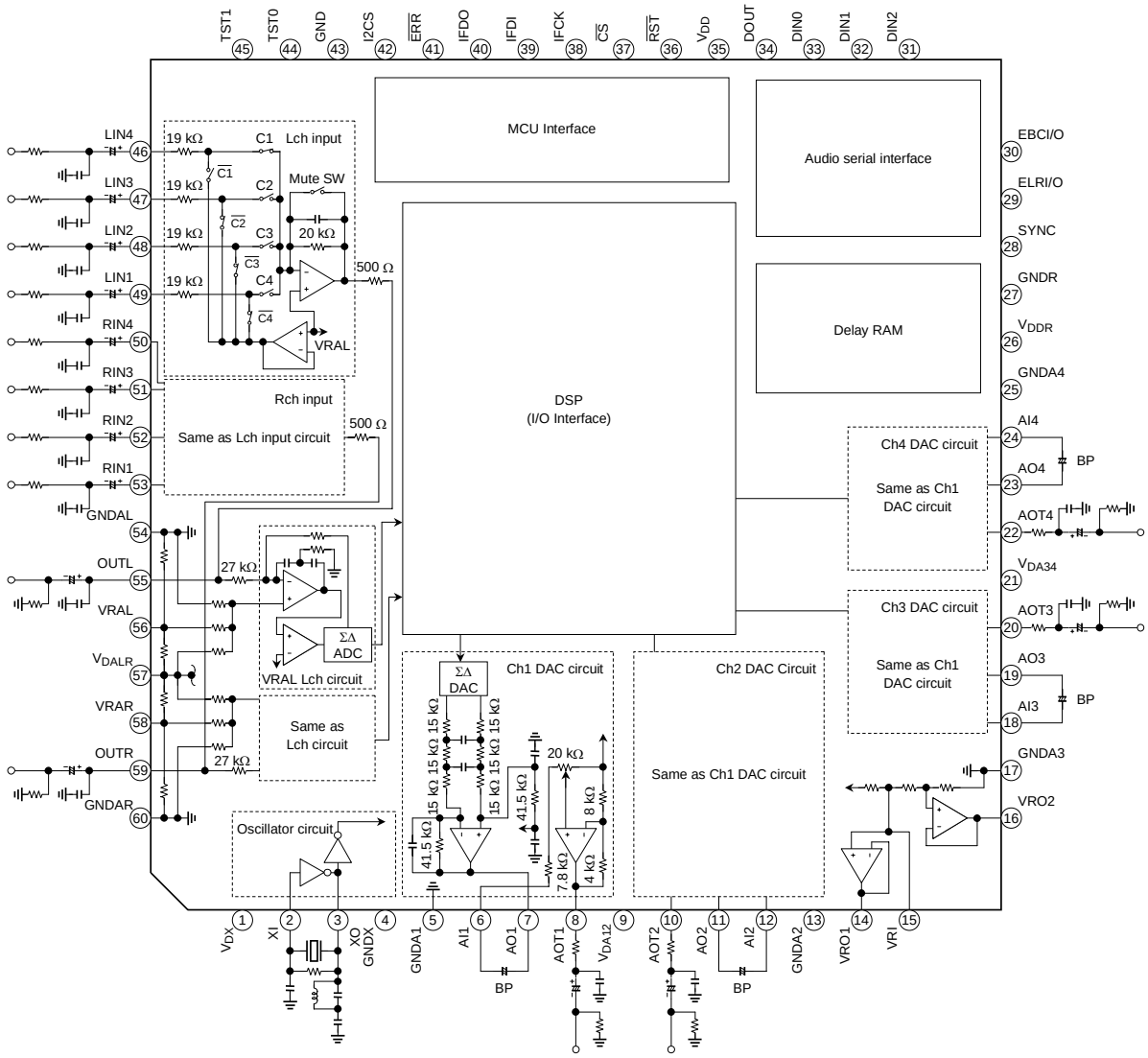
Features

- Incorporates a 4 ch-stereo analog switch for AD converter input.
- Incorporates a 1 ch stereo line-out.
- Incorporates a 1 bit Σ Δ-type AD converter (two channels).
  THD: −82dB (typ.) S/N: 95dB (typ.)
- Incorporates a 1 bit Σ Δ-type DA converter (four channels).
  THD: −86dB (typ.) S/N: 98dB (typ.)
- Incorporates a trimming analog volume for each output of DA converter. 0dB to −24dB (1dB step)
- As digital input/output port, this has 3 input port (6 ch) and 1 output port (2 ch), enabling input/output of sampling of 96 kHz/24 bit.
- Incorporates a built-in digital de-emphasis filter.
- Incorporates a digital attenuator.
- Incorporates a boot ROM to set a coefficient automatically, which enables to transfer an initial data from built-in ROM/RAM to registers at the time of resetting
  Boot ROM: 512 words
- The DSP block specifications are as follows:
  Data bus: 24 bits
  Multiplier/adder: 24 bits × 16 bits + 43 bits → 43 bits
  Accumulator: 43 bits (sign extension: 4 bits)
  Program ROM: 1024 words × 32 bits
  Coefficient RAM: 384 words × 16 bits
  Coefficient ROM: 256 words × 16 bits
  Offset RAM: 16 words × 11 bits
  Data RAM: 256 words × 24 bits
  Interface buffer RAM: 32 words × 16 bits
  Operation speed: 22.5 MIPS (510 step/fs: master clock = 768 fs, fs = 44.1 kHz)

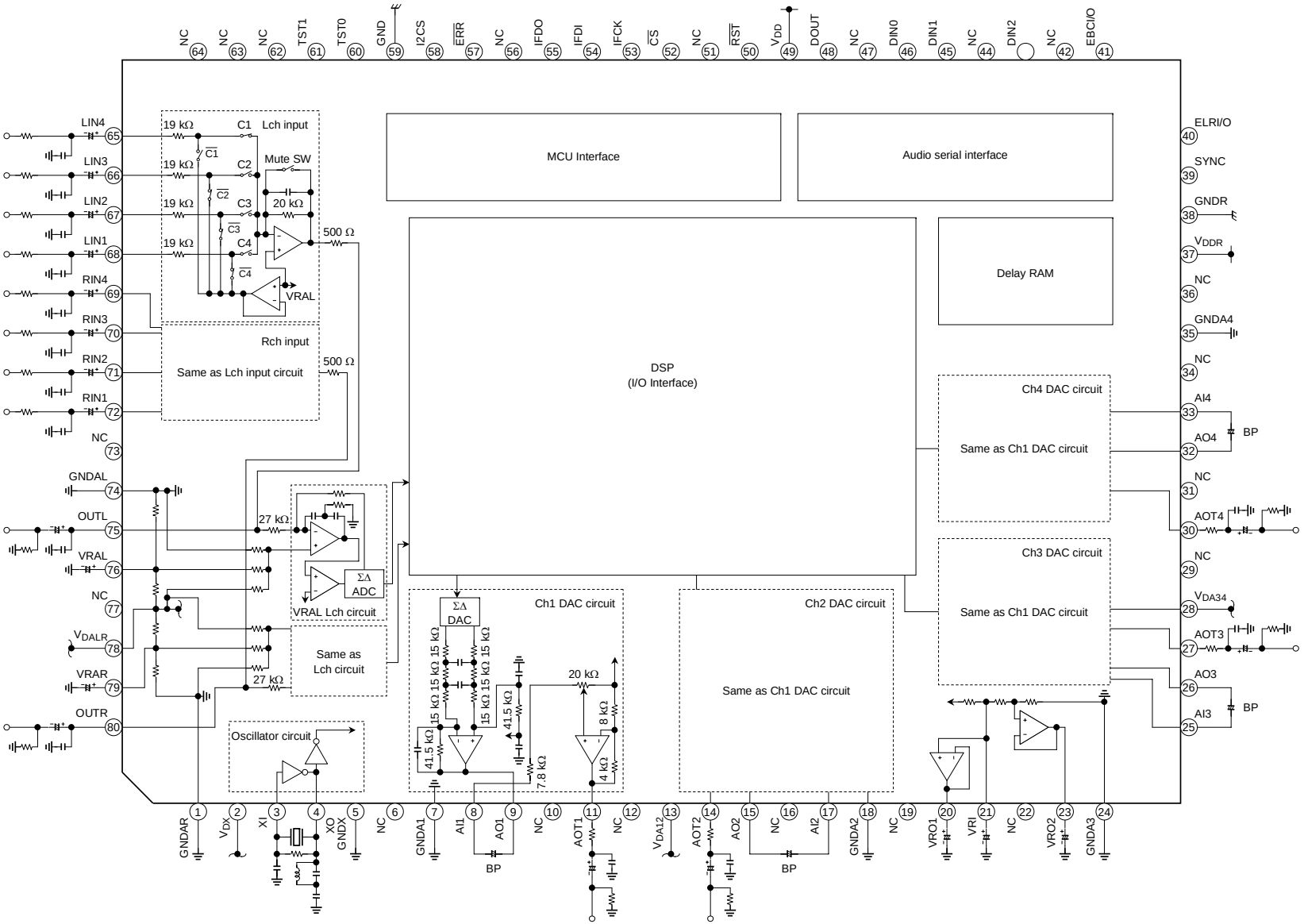
  Note 1: At the time of an analog input, approximately 170 steps (85 step/ch) in 510 step are used for the operation of the decimation filter for AD converters.
- Incorporates data delay RAM (32 kbits).
  Delay RAM: 2048 words × 16 bits (32 kbits)
- The microcontroller interface can be selected between Toshiba original 3 line mode and I^2C mode.
- CMOS silicon structure supports high speed.
- Power supply is a single 5 V.
- The package are 60-pin and 80 pin flat package.

Block Diagram/Pin Connection

TC94A04AFG



TC94A04AFDG



Pin Functions

Pin No.		Symbol	I/O	Function	Remarks
TC94A 04AFG	TC94A 04AFDG (Note 3)				
1	2	V_{DX}	—	Power pin for oscillator circuit	
2	3	XI	I	Crystal oscillator connecting or clock input pin	
3	4	XO	O	Crystal oscillator connecting pin	
4	5	GNDX	—	Ground pin for crystal oscillator circuit.	
5	7	GNDA1	—	Analog ground pin for DAC-Lch	
6	8	AI1	I	DAC-Lch attenuator input pin	
7	9	AO1	O	DAC-Lch signal output terminal	
8	11	AOT1	O	DAC-Lch attenuator output pin	
9	13	V_{DA12}	—	Analog power pin for DAC-L/Rch	
10	14	AOT2	O	DAC-Rch attenuator output pin	
11	15	AO2	O	DAC-Rch signal output pin	
12	17	AI2	I	DAC-Rch attenuator input pin	
13	18	GNDA2	—	Analog ground terminal for DAC-Rch	
14	20	VRO1	O	Reference voltage output pin-1 for DAC	
15	21	VRI	I	Reference voltage pin for DAC	
16	23	VRO2	O	Reference voltage output pin-2 for DAC	
17	24	GNDA3	—	Analog ground pin for DAC-Cch	
18	25	AI3	I	DAC-Cch attenuator input pin	
19	26	AO3	O	DAC-Cch signal input pin	
20	27	AOT3	O	DAC-Cch attenuator output pin	
21	28	V_{DA34}	—	Analog power pin for DAC-C/Sch	
22	30	AOT4	O	DAC-Sch signal output pin	
23	32	AO4	O	DAC-Sch signal output pin	
24	33	AI4	I	DAC-Sch attenuator input pin	
25	35	GNDA4	—	Analog ground pin for DAC-Sch	
26	37	V_{DDR}	—	Power pin for delay RAM	
27	38	GNDR	—	Ground pin for delay RAM	
28	39	SYNC	I	Program SYNC signal input pin	Schmitt input, TTL/CMOS (Note 2)
29	40	ELRI/O	I/O	LR clock input/output pin for serial data (DIN/DOUT)	Schmitt input, TTL/CMOS (Note 2)
30	41	EBCI/O	I/O	Bit clock input/output pin for serial data (DIN/DOUT)	Schmitt input, TTL/CMOS (Note 2)
31	43	DIN2	I	Serial data input pin 2	Schmitt input, TTL/CMOS (Note 2)

Note 2: 28 to 33 pin (TC94A04AFG): Input level changes TTL/CMOS level by the command (42h: VS). Output is fixed to CMOS level.
In case of TC94A04AFDG, pin number are 39 to 41 pins and 43 to 46 pins.

Note 3: In case of TC94A04AFDG, these are NC pins as below. Normally open, otherwise it connects to V_{DD} or GND. 6, 10, 12, 16, 19, 22, 29, 31, 34, 36, 42, 44, 47, 51, 56, 62 to 64, 73, 77 pins.

Pin No.		Symbol	I/O	Function	Remarks
TC94A 04AF	TC94A 04AFD (Note 3)				
32	45	DIN1	I	Serial data input pin 1	Schmitt input, TTL/CMOS (Note 2)
33	46	DIN0	I	Serial data input pin 0	Schmitt input, TTL/CMOS (Note 2)
34	48	DOUT	O	Serial data output pin	
35	49	V_{DD}	—	Power pin	
36	50	$\overline{RST}$	I	Reset pin	Schmidt input
37	52	$\overline{CS}$	I	Microcontroller interface chip select signal input pin	Schmidt input
38	53	IFCK	I	Microcontroller interface data shift clock input pin	Schmidt input
39	54	IFDI	I/O	Microcontroller interface data input/output pin (I^2C bus)	Schmidt input
40	55	IFDO	O	Microcontroller interface data output pin	
41	57	$\overline{ERR}$	O	Error flag output pin	Open drain output
42	58	I2CS	I	Microcontroller interface switching pin (I^2C bus/Toshiba bus)	Schmitt input
43	59	GND	—	GND pin	
44	60	TST0	I	Test pin 0	
45	61	TST1	I	Test pin 1	
46	65	LIN4	I	ADC-Lch signal input pin 4	
47	66	LIN3	I	ADC-Lch signal input pin 3	
48	67	LIN2	I	ADC-Lch signal input pin 2	
49	68	LIN1	I	ADC-Lch signal input pin 1	
50	69	RIN4	I	ADC-Rch signal input pin 4	
51	70	RIN3	I	ADC-Rch signal input pin 3	
52	71	RIN2	I	ADC-Rch signal input pin 2	
53	72	RIN1	I	ADC-Rch signal input pin 1	
54	74	GNDAL	—	Analog ground pin for ADC-Lch	
55	75	OUTL	O	Lch analog line-out pin	
56	76	VRAL	I	Reference voltage pin for ADC-Lch	
57	78	V_{DALR}	—	Analog power pin for ADC-L/Rch	
58	79	VRAR	I	Reference voltage pin for ADC-Rch	
59	80	OUTR	O	Rch analgo lline-out pin	
60	1	GNDAR	—	Analog ground pin for ADC-Rch	

Note 2: 28 to 33 pin (TC94A04AFG): Input level changes TTL/CMOS level by the command (42h: VS). Output is fixed to CMOS level.
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Explanation of Block Operations

1. Explanation Pin Operations

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Symbol</th><th rowspan="2">Function</th></tr>
<tr><th>TC94A 04AFG</th><th>TC94A 04AFDG (Note 3)</th></tr>
<tr><td>2
3</td><td>3
4</td><td>XI
XO</td><td>Master mode: Connect the crystal oscillator
Slave mode: Supplies an external master clock to XI.
Master clock is 768 fs. Each master-clock frequency to fs is as follows.
<table>
<tr><th>fs</th><th>768 fs</th></tr>
<tr><td>32 kHz</td><td>24.576 MHz</td></tr>
<tr><td>44.1 kHz</td><td>33.868 MHz</td></tr>
<tr><td>48 kHz</td><td>36.864 MHz</td></tr>
<tr><td>96 kHz</td><td>36.864 MHz</td></tr>
</table></td></tr>
<tr><td>1, 4 to 25</td><td>2, 5 to 35</td><td>Omitted</td><td>—</td></tr>
<tr><td>26</td><td>37</td><td>V_{DDR}</td><td>Power pin for delay RAM</td></tr>
<tr><td>27</td><td>38</td><td>GNDR</td><td>Ground pin for delay RAM</td></tr>
<tr><td>28</td><td>39</td><td>SYNC</td><td>Program SYNC signal input pin</td></tr>
<tr><td>29</td><td>40</td><td>ELRI/O</td><td>LR clock pin for serial data input (DIN)/serial data output (DOUT).
When you carry out a slave operation to a serial input/output data, please set it as an input. And when you carry out a master operation, please set it as an output (command 43h: SIOS).
Output frequency can perform selection of 1 fs/2 fs by ELRQS (command: 40h).</td></tr>
<tr><td>30</td><td>41</td><td>EBCI/O</td><td>Bit clock pin for serial data input (DIN)/serial data output (DOUT).
When you carry out a slave operation to a serial input/output data, please set it as an input. And when you carry out a master operation, please set it as an output (command 43h: SIOS). Output frequency can be select as follows by EBCQS (command: 40h).
<table>
<tr><th>EBCQS [1:0]</th><th>Output Frequency</th></tr>
<tr><td>0</td><td>32 fs</td></tr>
<tr><td>1</td><td>64 fs</td></tr>
<tr><td>2</td><td>128 fs</td></tr>
<tr><td>3</td><td>for test</td></tr>
</table></td></tr>
<tr><td>31
32
33</td><td>43
45
46</td><td>DIN2
DIN1
DIN0</td><td>Serial data input pin. The serial data of a total of 6-channels can be inputted. Switching of the number of channel is set by CHSI (command: 42h). Moreover, switching of master/slave function is set by SIS (command: 42h)</td></tr>
<tr><td>34</td><td>48</td><td>DOUT</td><td>Serial data output pin. Connected to internal register for output in DSP block.
The internal register connected is set up by CHSO (command: 43h).</td></tr>
<tr><td>35</td><td>49</td><td>V_{DD}</td><td>Power pin</td></tr>
<tr><td>36</td><td>50</td><td>$\overline{RST}$</td><td>Reset pin. “L” at initialization.</td></tr>
</table>

Note 3: In case of TC94A04AFDG, these are NC pins as below. Normally open, otherwise it connects to V_{DD} or GND. 6, 10, 12, 16, 19, 22, 29, 31, 34, 36, 42, 44, 47, 51, 56, 62 to 64, 73, 77 pins.

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Symbol</th><th rowspan="2">Function</th></tr>
<tr><th>TC94A 04AFG</th><th>TC94A 04AFDG (Note 3)</th></tr>
<tr><td>37
38
39
40
41
42</td><td>52
53
54
55
57
58</td><td>$\overline{CS}$
IFCK
IFDI
IFDO
$\overline{ERR}$
I2CS</td><td>Microcontroller interface pin
<table><tr><th>I2CS</th><th>Transmission Mode</th></tr><tr><td>0</td><td>Toshiba original bus mode</td></tr><tr><td>1</td><td>I^2C bus mode</td></tr></table><table><tr><th></th><th>Toshiba Original Bus Mode</th><th>I^2C Bus Mode</th></tr><tr><td>$\overline{CS}$</td><td>Chip select</td><td>Chip select (can be fixed to “L”)</td></tr><tr><td>IFCK</td><td>Transmit/receive clock</td><td>Transmit/receive clock</td></tr><tr><td>IFDI</td><td>Data/command input</td><td>Data input/output</td></tr><tr><td>IFDO</td><td>Data output (monitor data)</td><td>Fixed to “L” level output</td></tr><tr><td>$\overline{ERR}$</td><td>Error flag signal output (for runaway detector)</td><td>Error flag signal output (for runaway detector)</td></tr></table></td></tr>
<tr><td>43</td><td>59</td><td>GND</td><td>Ground pin</td></tr>
<tr><td>44
45</td><td>60
61</td><td>TST0
TST1</td><td>Test pin. Fixed to “L”</td></tr>
<tr><td>46
47
48
49</td><td>65
66
67
68</td><td>LIN4
LIN3
LIN2
LIN1</td><td>Four channel analog L-ch input pin. Incorporates an analog selector. And an input switching is selected by Command AIS (command: 42h) (MIX is also possible). The selected signal is outputted from OUTL (55 pin).</td></tr>
<tr><td>50
51
52
53</td><td>69
70
71
72</td><td>RIN4
RIN3
RIN2
RIN1</td><td>Four channel analog R-ch input pin. Incorporates an analog selector. And an input switching is selected by Command AIS (command: 42h) (MIX is also possible). The selected signal is outputted from OUTR (59 pin).</td></tr>
<tr><td>54 to 60</td><td>74 to 80, 1</td><td>Omitted</td><td>—</td></tr>
</table>

Note 3: In case of TC94A04AFDG, these are NC pins as below. Normally open, otherwise it connects to V_{DD} or GND. 6, 10, 12, 16, 19, 22, 29, 31, 34, 36, 42, 44, 47, 51, 56, 62 to 64, 73, 77 pins.

2. Microcontroller Interface

2.1 Standard Transmission Mode

When I2CS = "L", data can be transmitted or received in Standard Transmission mode.

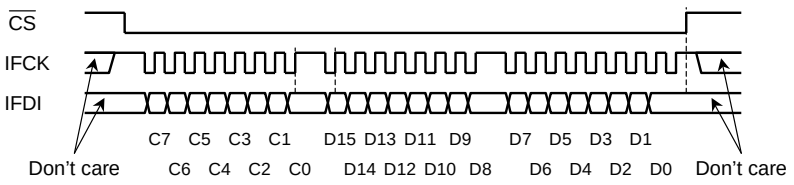
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.

The IFCK signal is the transmit/receive clock.

The IFDI signal is the data. The TC94A04AFG/AFDG loads the IFDI signal on the IFCK signal rising edge.

When $\overline{CS}$ = "H", the IFCK and IFDI signals are don't care.

2.1.1 Setting Resisters



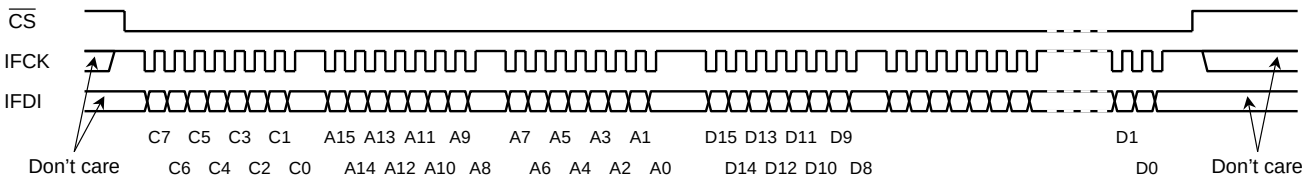
Cn: COMMAND
Dn: Data

The registers are set by command using the IFDI signals.

The first byte is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB.

Data are loaded the rising edge of the IFCK signal. Note that commands or data that must be switched, such as the RUN-MUTE command (command-44h) or the IFF flag (command-4Ah), must be synchronized with the SYNC signal and loaded on that signal.

2.1.2 Setting RAM (sequential)



Cn: COMMAND
An: ADDRESS
Dn: Data

The RAMs are set by command data using the IFDI signal.

The first byte is a command, which differs for each RAM. The next two bytes contain the start address for the RAM written.

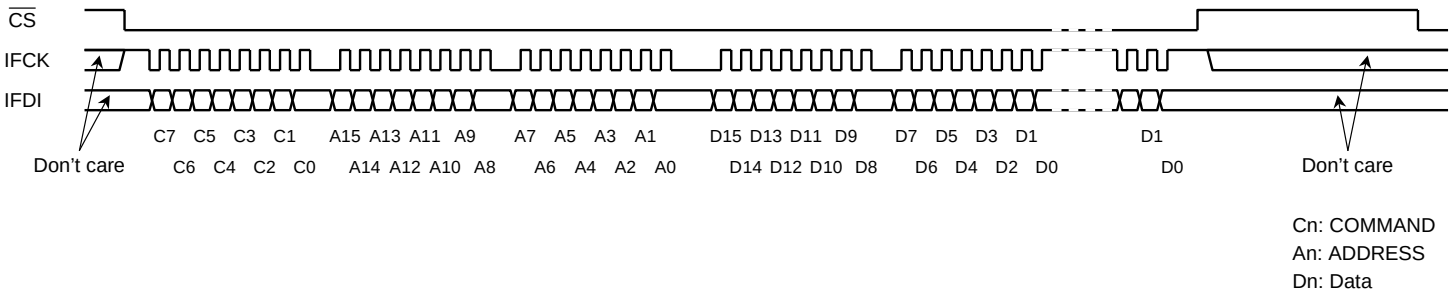
The length of the data field following the RAM address bytes is 2 × n bytes. The address is automatically incremented by 1.

During program running, 1 word of data is written at a time in internal RAM synchronizing with a SYNC signal.

Therefore, when performing continuously two or more write to word, unless it applies more than 1/fs [sec] per 1 word and it sets up, taking in of data is not performed correctly.

At the time of program STOP, it is written in asynchronous.

2.1.3 Setting RAM (ACMP mode)



In ACMP mode, the TC94A04AFG/AFDG does not write data directly to coefficient RAM (CRAM) or offset RAM (OFRAM). In this mode, data must be written to the interface buffer RAM (IFB-RAM). Then, all the data are updated together in a period of 1 fs.

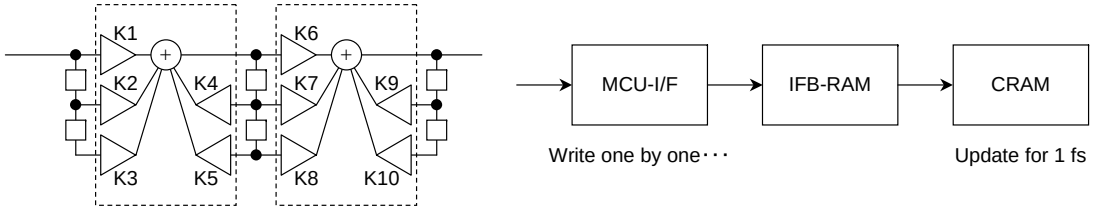
For example, if a signal flow filter is designed as in the following diagram, unless the K1 to K5 data are batch-updated, the circuit may resonate. The same applies to the K6 to K10 data.

Using ACMP mode can reduce the noise caused by updating coefficients while the TC94A04AFG/AFDG is operating.

IFB-RAM is 32-word memory. Therefore, data can be updated at one time in units of up to 32-words.

The length of the data field is $2 \times n$ bytes, where $n \leqq 32$.

In addition, operation at the time of transmitting other commands, before package rewriting of the data by ACMP mode was completed cannot be guaranteed. Please set up again after initializing by $\overline{\text{RST}}$ terminal or the initialization command.



2.2 I^2C Bus Mode

When I2CS = "H", data can be transmitted or received in I^2C bus mode.

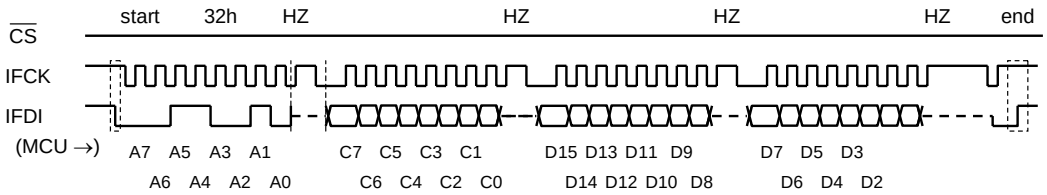
When the $\overline{CS}$ signal is Low, control from the microcontroller is enabled.

In I^2C mode, the $\overline{CS}$ signal can be used fixed to "L". The IFCK signal is the transmit/receive clock. The IFDI signal is the data.

The TC94A04AFG/AFDG loads the IFDI data on the IFCK signal rising edge.

When $\overline{CS}$ = "H", IFCK and IFD signal are don't care.

2.2.1 Setting Registers



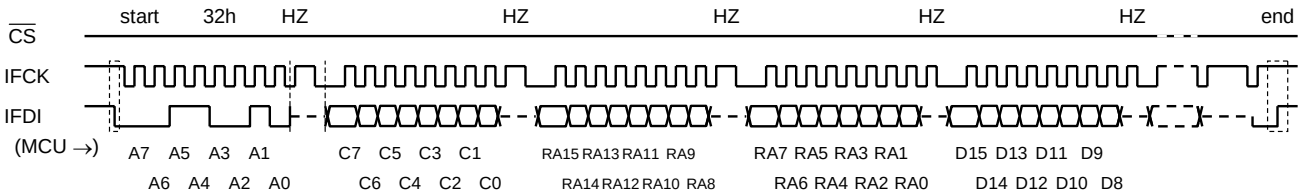
An: I^2C address
Cn: COMMAND
Dn: Data

The registers are set by command data using the IFDI signal.

The first byte after the I^2C address (= 32h) is a command, which differs for each register. The data sent after that are fixed to two bytes. Both command and data are sent starting from the MSB in I^2C format.

The data loaded internally every two bytes. Note that commands or data that must be switched on the SYNC signal, such as the RUN command (command-44h) or the IFF flag (command-4Ah), must be synchronized with the SYNC signal and loaded on that signal.

2.2.2 Setting RAM (sequential)



Cn: COMMAND
An: I^2C address
RAn: RAM-ADDRESS
Dn: Data

The RAMs are set by command data using the IFDI signal.

The first byte after the I^2C address (32h) is a command, which differs for each RAM. The next two bytes contain the start address for each RAM.

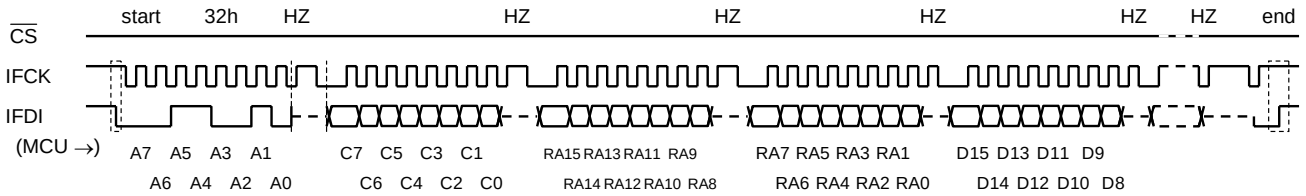
The length of the data field following the RAM address bytes is $2 \times n$ bytes. The address is automatically incremented by 1.

During program running, 1 word of data is written at a time in internal RAM synchronizing with a SYNC signal.

Therefore, when performing continuously two or more write to word, unless it applies more than 1/fs [sec] per 1 word and it sets up, taking in of data is not performed correctly.

At the time of program STOP, it is written in asynchronous.

2.2.3 Setting RAM (ACMP mode)



Cn: COMMAND
An: I^2C address
RAn: RAM-ADDRESS
Dn: Data

In ACMP mode, the TC94A04AFG/AFDG does not write data directly to coefficient RAM (CRAM) or offset RAM (OFRAM). In this mode, data must be written to the interface buffer RAM (IFB-RAM). Then, all the data are updated together in a period of 1 fs.

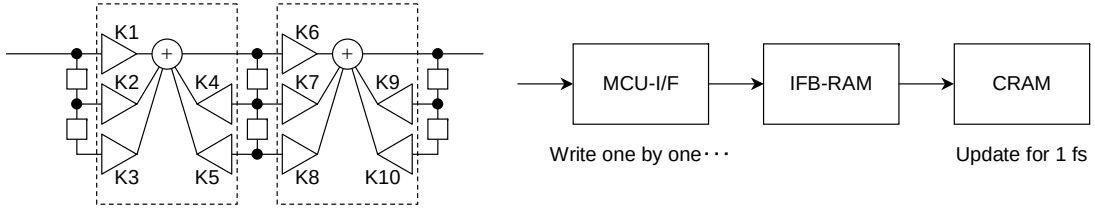
For example, if a signal flow filter is designed as in the following diagram, unless the K1 to K5 data are batch-updated, the circuit may resonate. The same applies to the K6 to K10 data.

Using ACMP mode can reduce the noise caused by updating coefficients while the TC94A04AFG/AFDG is operating.

IFB-RAM is 32-word memory. Therefore, data can be updated at one time in units of up to 32-words.

The length of the data field is $2 \times n$ bytes, where $n \leqq 32$.

In addition, operation at the time of transmitting other commands, before package rewriting of the data by ACMP mode was completed cannot be guaranteed. Please set up again after initializing by $\overline{RST}$ terminal or the initialization command.



3. Control Commands

The following table lists the control commands that can be used from the microcontroller.

3.1 Control-Command Table

Table 1 Control commands

Command	Code	R/W	Description	RAM Sequential	Transfer Sync/Async to SYNC Signal
TIMING	40h	W	Timing	—	Async
BOOT	41h		Self boot ROM start address	—	Async
DIN/AIN	42h		Setting digital/analog input	—	Async
DOUT/AOUT	43h		Setting digital/analog output	—	Async
RUN-MUTE	44h		Program execution, mute	—	Sync
MSEQ	45h		Sequential RAM	—	Sync: RUN, Async: STOP
CRAM	46h		CRAM	Enable	
CRAM-ACMP	47h		CRAM (ACMP mode)		Async
ORAM	48h		ORAM		Sync: RUN, Async: STOP
ORAM-ACMP	49h		ORAM (ACMP mode)		Async
IFF	4Ah		IFF setting	—	Sync
DE-EMPH	4Bh		De-emphasis	—	Sync
DAC-LR	4Ch		DAC output trim level (L/R-ch)	—	Sync
DAC-CS	4Dh		DAC output trim level (C/S-ch)	—	Sync
DF-ATT	4Eh		DF attenuator level (all ch)	—	Async
M-RST	4Fh		Initialization	—	Async

Note 4: The command which is “Sync” in the transfer Sync with Sync signal needs to set the $\overline{CS}$ = H section to a minimum of 1 fs more until it transmits the follwing command. (It need more than 22.68 μs at fs = 44.1 KHz.)

3.2 Control Commands Description

Each command explanation is shown below. *mark in each command explanation table shows the initial value at the time of reset.

Command-40h (0100 0000): TIMING (4400h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	SYPD	SYD1	SYD0	0	SYPA	SYA1	SYA0	0	SYPS	SYS1	SYS0	0	ELROS	EBC-OS1	EBC-OS0

Bit	Name	Description	Value	Operation
D15	—	Fixed to 0 (zero)	—	—
D14	SYPD	ASP digital block sync polarity switching	0	ASP program starts on falling edge
			1*	ASP program starts on rising edge
D13 D12	SYD [1:0]	ASP digital block SYNC signal input switching	0*	Signal after SYNC 1 fs output
			1	Signal after SYNC 2 fs output 2 fs (for 96 kHz sampling)
			2	SYNC pin
			3	ELRI/O pin
D11	—	Fixed to 0 (zero)	—	—
D10	SYPA	DF block sync polarity switching	0	DF-processing starts in a falling
			1*	DF-processing starts in a rising
D9 D8	SYA [1:0]	DF block sync input switching	0*	SYNC 1 fs output
			1	SYNC 2 fs output
			2	Reserved
			3	Reserved
D7	—	Fixed to 0 (zero)	—	—
D6	SYPS	SYNC circuit input polarity switching (SYNC reference signal)	0*	Reference input = L Lch
			1	Reference input = H Lch
D5 D4	SYS [1:0]	SYNC circuit input switching (SYNC reference signal)	0*	Internal divided results
			1	SYNC pin
			2	ELRI/O pin
			3	Output ELRI/O pin input divided by 2 (for 96 kHz sampling)
D3	—	Fixed to 0 (zero)	—	—
D2	ELROS	Select the clock at the time of ELRI/O output	0*	1 fs (Internal fs)
			1	2 fs (Internal fs × 2)
D1 D0	EBCOS [1:0]	Select the clock at the time of EBCI/O output	0*	32 fs (Internal fs × 32)
			1	64 fs (Internal fs × 64)
			2	128 fs (Internal fs × 128)
			3	Reserved

Command-41h (0100 0001): BOOT (0000h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	BTA8	BTA7	BTA6	BTA5	BTA4	BTA3	BTA2	BTA1	BTA0

Bit	Name	Description	Value	Operation
D15 to D7	—	Fixed to 0 (zero)	—	—
D8 to D0	BTA [8:0]	Self-boot ROM start address	000h to 1FEh	Starts self-boot operation from specified address

Command-42h (0100 0010): DIN/AIN (0100h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CHSI 1	CHSI 0	VS	AUTO	AIS4	AIS3	AIS2	AIS1	ZDE	SIS	ISLT1	ISLT0	IBCS1	IBCS0	IFMT1	IFMT0

Bit	Name	Description	Value	Operation
D15 D14	CHSI [1:0]	Serial input (SI) switching	0*	Analog 2 ch input
			1	Digital 4 ch input (2 ch input by the program is possible)
			2	Digital 6 ch input
			3	Analog and Digital MIX mode
D13	VS	Switching threshold of input pin [SYNC, ELRI/O, EBCI/O, DIN2, DIN1, DIN0]	0*	CMOS level
			1	TTL level
D12	AUTO	Auto mute (analog input)	0*	Mute OFF
			1	Mute ON
D11 D10 D9 D8	AIS [4:1]	Switching analog input	0 to Fh (1*)	AIS4: LIN4/RIN4 pin, AIS3: LIN3/RIN3 pin, AIS2: LIN2/RIN2 pin, AIS1: LIN1/RIN1 pin Select channel, it was set as “1”. (output from OUTL/OUTR) MIX between channels is also possible.
D7	ZDE	Digital-input zero-level detection mute function	0*	Mute OFF
			1	Mute ON
D6	SIS	Serial input	0*	Master (synchronizes with internal clock (output from ELRI/O, EBCI/O pin))
			1	Slave (synchronizes with external clock (input from ELRI/O, EBCI/O pin))
D5 D4	ISLT [1:0]	Number of serial input slots	0*	16 slots (bit clock = 32 fs)
			1	20 slots (bit clock = 40 fs)
			2	24 slots (bit clock = 48 fs)
			3	32 slots (bit clock = 64 fs)
D3 D2	IBCS [1:0]	Serial input bit length	0*	16 bits
			1	18 bits
			2	20 bits
			3	24 bits
D1 D0	IFMT [1:0]	Serial input format	0*	Pads from the beginning
			1	Pads from the end
			2	I2S format
			3	

Command-43h (0100 0011): DOUT/AOUT (0080h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	HSMP	0	0	SIOS	SOS	CHSO 1	CHSO 0	OSLT 1	OSLT 0	OBCS 1	OBCS 0	OFMT 1	OFMT 0

Bit	Name	Description	Value	Operation
D15 to D13	—	Fixed to 0 (zero)	—	—
D12	HSMP	Switching high sampling of analog output	0*	Normal rate
			1	High sampling rate
D11 D10	—	Fixed to 0 (zero)	—	—
D9	SIOS	Switching input/output of ELRI/O, EBCI/O pin	0*	Input
			1	Output
D8	SOS	Serial output	0*	Master (synchronizes with internal clock (output from EBLRI/O, EBCI/O pin))
			1	Slave (synchronizes with external clock (input from EBLR/O, EBCI/O pin))
D7 D6	CHSO [1:0]	Serial output switching	0	DOUT pin ← SIR0
			1	DOUT pin ← SIR1
			2*	DOUT pin ← SIR2
			3	Reserved
D5 D4	OSLT [1:0]	Number of serial input slots	0*	16 slots
			1	20 slots
			2	24 slots
			3	32 slots
D3 D2	OBCS [1:0]	Serial output bit length	0*	16 bits
			1	18 bits
			2	20 bits
			3	24 bits
D1 D0	OFMT [1:0]	Serial output format	0*	Pads from the beginning
			1	Pads from the end
			2	I2S format
			3	

Command-44h (0100 0100): RUN-MUTE (1F0Fh*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RUN	0	0	AD MUT	IMUTE	OMU TE2	OMU TE1	OMU TE0	0	0	0	0	ERDET	ZST	SYRC	SYRO

Bit	Name	Description	Value	Operation
D15	RUN	ASP program execution	0*	Stops program
			1	Runs program
D14 D13	—	Fixed to 0 (zero)	—	—
D12	ADMUT	ADC mute	0	Mute OFF
			1*	Mute ON
D11	IMUTE	ASP block input mute	0	Mute OFF
			1*	Mute ON
D10	OMUTE2	ASP block output mote (SIR2 register mute)	0	Mute OFF
			1*	Mute ON
D9	OMUTE1	ASP block output mute (SIR1 register mute)	0	Mute OFF
			1*	Mute ON
D8	OMUTE0	ASP block output mute (SIR0 register mute)	0	Mute OFF
			1*	Mute ON
D7 to D4	0	Fixed to 0 (zero)	—	—
D3	ERDET	Error detection	0	Disable
			1*	Enable
D2	ZST	Switches to access CROM using Log-Linear adjustment	0	2-cycle access
			1*	1-cycle access
D1	SYRC	Set CP at each SYNC	0	Does not reset
			1*	Reset
D0	SYRO	Set OFP at each SYNC	0	Does not reset
			1*	Reset

Command-45h (0100 0101): MSEQ

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	MSA2	MSA1	MSA0

Bit	Name	Description	Value	Operation
D15 to D3	—	Fixed to 0 (zero)	—	—
D2 to D0	MSA [2:0]	Module sequential RAM first address	0h to 7h	The address of the head to write in is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	MSEQ 9	MSEQ 8	MSEQ 7	MSEQ 6	MSEQ 5	MSEQ 4	MSEQ 3	MSEQ 2	MSEQ 1	MSEQ 0

Bit	Name	Description	Value	Operation
D15 to D10	—	Fixed to 0 (zero)	—	—
D9 to D0	MSEQ [9:0]	Module sequential RAM data	000h to 3FFh	The data written in module sequence RAM are set up.

Data are sent continuously after transmitting the module sequence RAM head address (2 bytes). Enable a sequential write to RAM.
45h-MSEQ RAM address (2 bytes)-data (2 bytes)-data (2 bytes)-····· data (2 bytes)
(module sequential RAM: 8 words)

Command-46h (0100 0110): CRAM

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	CRAM A8	CRAM A7	CRAM A6	CRAM A5	CRAM A4	CRAM A3	CRAM A2	CRAM A1	CRAM A0

Bit	Name	Description	Value	Operation
D15 to D9	—	Fixed to 0 (zero)	—	—
D8 to D0	CRAMA [8:0]	CRAM (coefficient RAM) head address	000h to 17Fh	CRAM address of the head at the time of writing in by 46h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRAM D15	CRAM D14	CRAM D13	CRAM D12	CRAM D11	CRAM D10	CRAM D9	CRAM D8	CRAM D7	CRAM D6	CRAM D5	CRAM D4	CRAM D3	CRAM D2	CRAM D1	CRAM D0

Bit	Name	Description	Value	Operation
D15 to D0	CRAMD [15:0]	CRAM data	7FFFh to 8000h	Set CRAM data (two-complement-form formula)

The data written in continuously are sent after transmitting CRAM head address (2 bytes).
Enable a sequential write to RAM.
46h-CRAM address (2 bytes)-data (2 bytes)-data (2 bytes)·····data (2 bytes)
(CRAM: 384 words)

Command-47h (0100 0111): CRAM-ACMP

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	CRAM A8	CRAM A7	CRAM A6	CRAM A5	CRAM A4	CRAM A3	CRAM A2	CRAM A1	CRAM A0

Bit	Name	Description	Value	Operation
D15 to D9	—	Fixed to 0 (zero)	—	—
D8 to D0	CRAMA [8:0]	CRAM (coefficient RAM) head address	000h to 17Fh	CRAM address of the head at the time of writing in by 47h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CRAM D15	CRAM D14	CRAM D13	CRAM D12	CRAM D11	CRAM D10	CRAM D9	CRAM D8	CRAM D7	CRAM D6	CRAM D5	CRAM D4	CRAM D3	CRAM D2	CRAM D1	CRAM D0

Bit	Name	Description	Value	Operation
D15 to D0	CRAMD [15:0]	CRAM data	7FFFh to 8000h	Set CRAM data (two-complement-form formula)

It is CRAM write-in command which used the address compare mode. A maximum of 32 words is written at once.

The data written in continuously are sent after transmitting CRAM head address (2 bytes).

Enable a sequential write to RAM.

47h-CRAM address (2 bytes)-data (2 bytes)-data (2 bytes)‥‥‥‥‥‥‥‥‥‥data (2 bytes)

(CRAM: 384 word)

Command-48h (0100 1000): ORAM

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	ORAM A3	ORAM A2	ORAM A1	ORAM A0

Bit	Name	Description	Value	Operation
D15 to D4	—	Fixed to 0 (zero)	—	—
D3 to D0	ORAMA [3:0]	ORAM (offset RAM) head address	0h to Fh	ORAM address of the head at the time of writing in by 48h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	ORAM D10	ORAM D9	ORAM D8	ORAM D7	ORAM D6	ORAM D5	ORAM D4	ORAM D3	ORAM D2	ORAM D1	ORAM D0

Bit	Name	Description	Value	Operation
D15 to D11	—	Fixed to 0 (zero)	—	—
D10 to D0	ORAMD [10:0]	ORAM data	000 to 7FFh	Set ORAM data

It is ORAM write-in command which used the address compare mode.
The data written in continuously are sent after transmitting ORAM head address (2 bytes).
Enable a sequential write to RAM.
48h-ORAM address (2 bytes)-data (2 bytes)-data (2 bytes)-·····data (2 bytes)
(ORAM: 16 words)

Command-49h (0100 1001): ORAM-ACMP

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	ORAM A3	ORAM A2	ORAM A1	ORAM A0

Bit	Name	Description	Value	Operation
D15 to D4	—	Fixed to 0 (zero)	—	—
D3 to D0	ORAMA [3:0]	ORAM (offset RAM) head address	0h to Fh	ORAM address of the head at the time of writing in by 48h command is set up.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	ORAM D10	ORAM D9	ORAM D8	ORAM D7	ORAM D6	ORAM D5	ORAM D4	ORAM D3	ORAM D2	ORAM D1	ORAM D0

Bit	Name	Description	Value	Operation
D15 to D11	—	Fixed to 0 (zero)	—	—
D10 to D0	ORAMD [10:0]	ORAM data	000 to 7FFh	Set ORAM data

The data written in continuously are sent after transmitting ORAM head address (2 bytes).
Enable a sequential write to RAM.
49h-CRAM address (2 bytes)-data (2 bytes)-data (2 bytes)‥‥‥‥‥‥‥‥‥‥data (2 bytes)
(ORAM: 16 words)

Command-4Ah (0100 1010): IFF (0000h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	IFF2	IFF1	IFF0

Bit	Name	Description	Value	Operation
D15 to D4	—	Fixed to 0 (zero)	—	—
D3	IFF2	Set IFFn (n = 2, 1, 0)	0*	IFFn = 0
			1	IFFn = 1

Command-4Bh (0100 1011): DE-EMPH (0000h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	DEMP 1	DEMP 0

Bit	Name	Description	Value	Operation
D15 to D2	—	Fixed to 0 (zero)	—	—
D1 D0	DEMP [1:0]	Set de-emphasis	0*	De-emphasis Off
			1	fs = 32 kHz
			2	fs = 44.1 kHz
			3	fs = 48 kHz

Command-4Ch (0100 1100): DAC-LR (1F1Fh*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ATTL 4	ATTL 3	ATTL 2	ATTL 1	ATTL 0	0	0	0	ATTR 4	ATTR 3	ATTR 2	ATTR 1	ATTR 0

Bit	Name	Description	Value	Operation
D15 to D13	—	Fixed to 0 (zero)	—	—
D12 to D8	ATTL [4:0]	DAC L-ch attenuator value	00h to 1Fh*	Code : 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB) : 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh
D7 to D5	—	Fixed to 0 (zero)	—	—
D4 to D0	ATTR [4:0]	DAC R-ch attenuator value	00h to 1Fh*	Code : 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB) : 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh

Command-4Dh (0100 1101): DAC-CS (1F1Fh*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	ATTC 4	ATTC 3	ATTC 2	ATTC 1	ATTC 0	0	0	0	ATTS 4	ATTS 3	ATTS 2	ATTS 1	ATTS 0

Bit	Name	Description	Value	Operation
D15 to D13	—	Fixed to 0 (zero)	—	—
D12 to D8	ATTC [4:0]	DAC C-ch attenuator value	00h to 1Fh*	Code : 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB) : 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh
D7 to D5	—	Fixed to 0 (zero)	—	—
D4 to D0	ATTS [4:0]	DAC-Sch attenuator value	00h to 1Fh*	Code : 00h 01h 02h ··· 18h 19h ··· 1Fh ATT (dB) : 0 –1 –2 –24 ca.–60 ca.–60 Initial value: 1Fh

Command-4Eh (0100 1110): DF-ATT (007Fh*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0

Bit	Name	Description	Value	Operation
D15 to D7	—	Fixed to 0 (zero)	—	—
D6 to D0	ATL [6:0]	DF attenuator value	00h to 7Fh*	Initial value: 7Fh (level = –∞) LEVEL = 20 × log (ATL/128)

Code	ATL	Level
00h	7Fh	0.00dB
01h	7Eh	–0.14dB
02h	7Dh	–0.21dB
to	to	to
0Dh	72h	–1.01dB
1Ah	65h	–2.06dB
25h	5Ah	–3.06dB
to	to	to
3Fh	40h	–6.02dB
to	to	to
7Dh	02h	–36.12dB
7Eh	01h	–42.14dB
7Fh	00h	–∞

Command-4Fh (0100 1111): M-RST (0000h*)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MRST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Name	Description	Value	Operation
D15	MRST	Initialization from the micro controller command	0*	Does not initialize
			1	Initializes (set to initial value (0*))
D14 to D0	—	Fixed to 0 (zero)	—	—

4. Self-Boot Function Description

4.1 Self-Boot Function

The TC94A04AFG/AFDG supports a self-boot function for setting coefficients and offsets.

As Figure 1 shows, the data are set via the microcontroller interface circuit.

First saving the data to be set via the microcontroller in the self-boot ROM (SBROM) allows various modes to be set later. The microcontroller interface circuit supports two format: I^2C and the original mode. However, the boot must be executed in Standard Transmission.

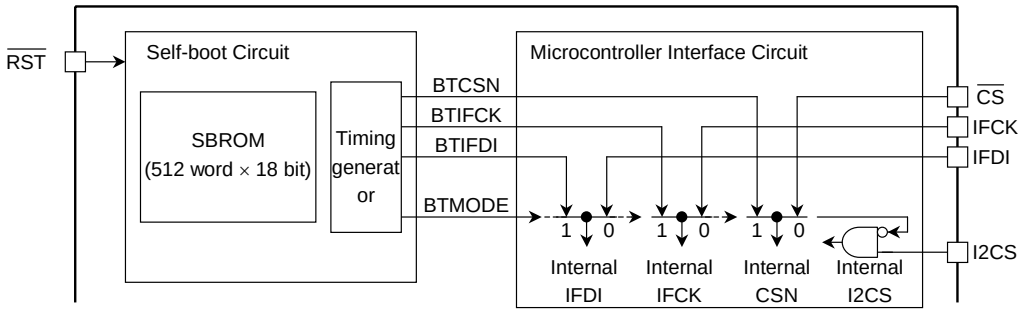


Figure 1 Self-Boot System

All the command inputs from the exterior are disregarded during a boot term.

4.2 Boot ROM Format

The following shows the breakdown of the 18 bits.

00	Data that are being sent
01	Command
10	Final data (after the data are sent, the $\overline{CS}$ signal set to “H”).
11	Jump address (jump to any address in the boot-ROM)

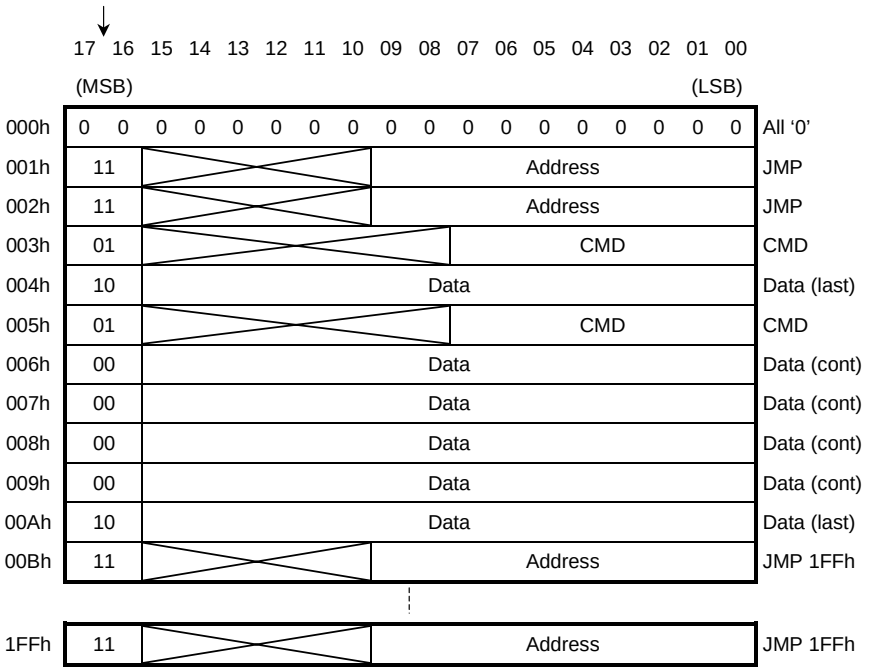


Figure 2 Boot ROM Format and Example

Note 5: Boot mode completes when the address reaches 1FFh, the maximum value. Therefore, for the final address (1FFh), write JMP 1FFh (data = 301FFh).

Note 6: For the head address (000h), write (00000).

Note 7: Please do not set a command of fs synchronous taking in to the address: 1FEh (RUN-MUTE/IFF/DE-EMPH/DAC-LR/DAC-CS etc.).

4.3 Self-Boot Operation

Self-boot operation supports two modes: one for use at reset and for setting the microcontroller.

4.3.1 Self-Boot Operation at Reset

To enter this mode, set the $\overline{RST}$ pin to High or send initialized command. The 2048 fs period (46.4 ms when fs = 44.1 kHz) after a reset release is wait period. The boot operation starts at the end of this period.

Relationship between fs and Wait Period

fs	Wait Period	Boot Time (maximum)
32 kHz	64.0 ms	16.0 ms
44.1 kHz	46.4 ms	11.6 ms
48 kHz 96 kHz	42.7 ms	10.7 ms

Starting address is fixed to 001h. If the jump address to application to execute at the time of a boot is specified to be 0001h, at the time of a reset, the initial value of application will be set up automatically.

When you do not boot at the time of a reset, please set JMP (1FFh: data = 301FFh) as 001h.

4.3.2 Self-Boot Operation When Setting Microcontroller

In this mode, the microcontroller can specify any address and the boot operation starts from that address.

The BOOT pin can be set to either High or Low. Setting the self-boot ROM start address using the BOOT command (command: 41h) from the microcontroller starts the boot operation with no wait. The boot operation when set from the microcontroller is the same as the self-boot operation at reset except that the boot operation can start from any address.

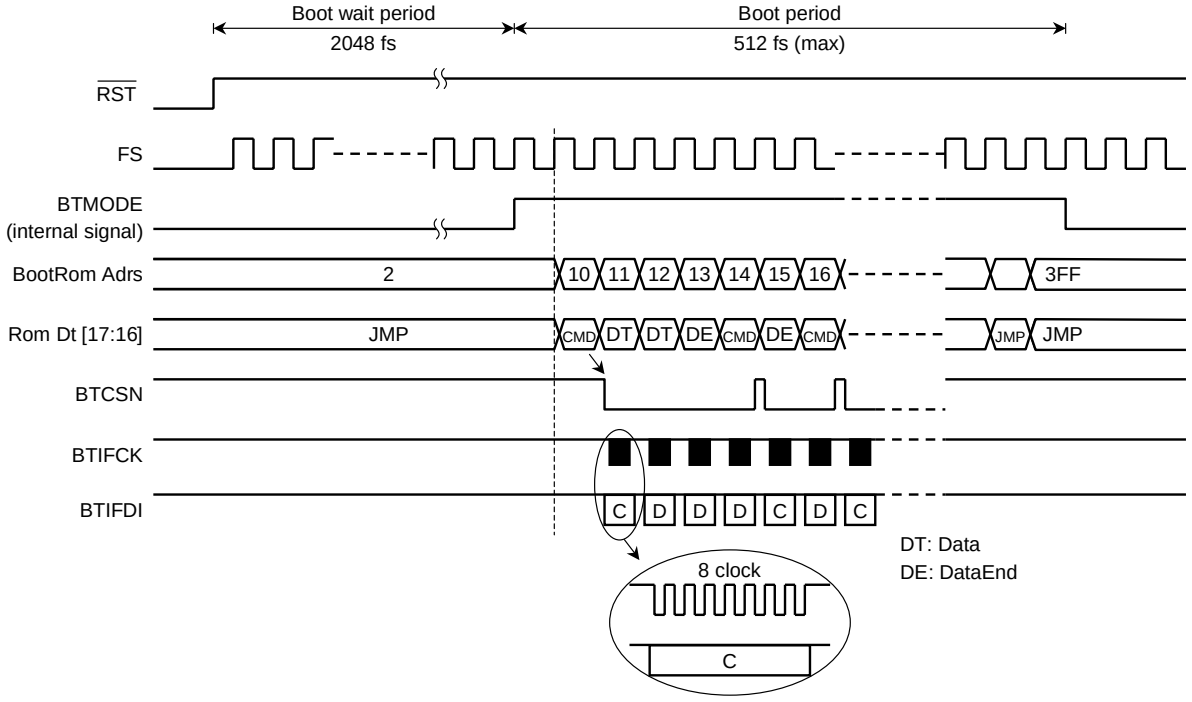


Figure 3 Boot Timing Chart (at reset)

5. Cautions on Use

5.1 Initial Reset

After a power-supply injection, once at least, please set up a required register after applying reset which makes $\overline{\text{RST}}$ terminal "L" level and making the value of an internal register decide.

5.2 The Cautions at the Time of Using ACMP (address compare mode)

In rewriting coefficient data and offset data using ACMP mode, please do not use it the following condition.

5.2.1 Please Do Not Transmit the Following Command before Completing Rewriting of Data.

Please do not send the following command before completing rewriting of data of CRAM or ORAM. Please check that waiting the term after rewriting has been completed until it transmits the following was carried out.

5.2.2 Please Do Not Include Data of an Intact Address.

Please do not include coefficient data of offset data of address which are not used by the program under execution, into transmitting data. When data of an intact address is contained, operation in ACMP mode cannot de ended. If the following command is transmitted in this state, RAM data will become unfixed also by the command with the command unrelated to CRAM or ORAM.

It needs to reset and all data needs to be re-set up to interrupt before completing rewriting of data in the rewriting processing.

5.2.3 Please Do Not Use the 0th Street of CRAM Address.

5.3 Please Do Not Perform Continuation Transmission over the 0th Address.

The transmission over the 0th address may incorrect-operate.

For example, when writing in 17Fh from 178h and 000h from 007h of CRAM, it must transmit in two steps.

5.4 Please Do Not Set-Up a Soft Reset Command as the Data of Boot ROM.

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{DD}	−0.3 to 6.0	V
Input voltage		V_{in}	−0.3 to V_{DD} + 0.3	V
Power dissipation	TC94A04AFG	P_D	1538 (Note 8)	mW
	TC94A04AFDG		1538	
Operating temperature		T_{opr}	−40 to 75	°C
Storage temperature		T_{stg}	−55 to 150	°C

Note 8: Power dissipation of TC94A04AFG is reference value when assembled chip on PCB. (normally, PD is 1250 mW.)

Electrical Characteristics
(unless otherwise specified, Ta = 25°C, $V_{DD} = V_{DX} = V_{DR} = V_{DA12} = V_{DA23} = V_{DALR}$ = 5.0 V)

DC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating power supply voltage	V_{DD}	—	Ta = −40 to 75°C	4.75	5.0	5.25	V
Operating frequency range	f_{opr}	—	511 step mode	12	33.8	37	MHz
Operating power supply current	I_{DD}	—	f_{opr} = 36.864 MHz 511 Step mode	—	135	146	mA

Clock Pins (XI, XO)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage (1)	"H" level	V_{IH1}	—	XI pin		V_{DD} × 0.7	—	V_{DD} + 0.3	V
	"L" level	V_{IL1}				—	—	V_{DD} × 0.7	
Output voltage (1)	"H" level	V_{OH1}	—	I_{OH} = −3.0 mA	XO pin	V_{DD} − 0.5	—	—	V
	"L" level	V_{OL1}		I_{OL} = 5.0 mA		—	—	0.5	

Input Pins

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Input voltage (2)	"H" level	V_{IH2}	—	(Note 9) (CMOS input), (Note 10)		$V_{DD} \times 0.8$	—	—	V
	"L" level	V_{IL2}				—	—	$V_{DD} \times 0.2$	
Input voltage (3)	"H" level	V_{IH3}	—	(Note 9) (TTL input)		$V_{DD} \times 0.5$	—	—	V
	"L" level	V_{IL3}				—	—	$V_{DD} \times 0.2$	
Input leakage current	"H" level	I_{IH2}	—	$V_{IN} = V_{DD}$	(Note 9), (Note 10), (Note 11)	—	—	10	μA
	"L" level	I_{IL2}		$V_{IN} = 0$ V		−10	—	—	

Note 9: SYNC, ELRI/O, EBCI/O, DIN0 to 2

Note 10: $\overline{CS}$, IFCK, IFDI, I2CS, TST0, TST1

Note 11: XI

Output Pins

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Output voltage (2)	"H" level	V_{OH2}	—	$I_{OH} = -2.0$ mA	(Note 12)	$V_{DD} - 0.5$	—	—	V
	"L" level	V_{OL2}		$I_{OL} = 2.0$ mA	(Note 12), (Note 14)	—	—	0.5	
Output voltage (3)	"L" level	V_{OL3}	—	$I_{OL} = 4.0$ mA	(Note 13)	—	—	0.5	V
Output open leakage current		I_{OZ4}	—	$V_{OH} = V_{DD}$	(Note 12), (Note 14)	—	—	±10	μA

Note 12: DOUT, IFDO (normally output)

Note 13: IFDI (I^2C mode output)

Note 14: IFOK, $\overline{ERR}$ (open drain output)

AC Characteristics

AD Converter: LIN1 to LIN4, RIN1 to RIN4 Pins

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Maximum input signal level	V_{in}	—	Input level that ADC output at full-scale digital output (Note 15)	1.27	1.33	—	Vrms
Input impedance	Z_{in}	—	Each of LIN1 to LIN4, RIN1 to RIN4 pins	—	19	—	kΩ
S/(N + D) ratio	S/N_{a1}	—	A-Weight, X'tal: 36.864 MHz (Note 15)	87	95	—	dB
	S/N_{a2}	—	CCIR-ARM, X'tal: 36.864 MHz (Note 15)	83	91	—	dB
THD + N	THD_a	—	20 kHz LPF, X'tal: 36.864 MHz (Note 15)	—	−82	−70	dB
Cross-talk	CT_a	—	20 kHz LPF, Lch → Rch/Rch → Lch, X'tal: 36.864 MHz (Note 15)	—	−80	−72	dB
Dynamic range	DR_a	—	A-Weight, X'tal: 36.864 MHz (Note 15)	83	90	—	dB

Note 15: One input pin selected of four selector of each channels.

Selector Output: OUTL, OUTR Pins

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output signal level	V_{out}	—	1 kHz, 1.122 Vrms input (Note 15)	0.9	1.0	1.12	Vrms
Output impedance	Z_{out}	—	OUTL/OUTR pins	—	0.5	—	kΩ
S/(N + D) ratio	S/N_s	—	A-Weight	93	104	—	dB
THD + N	THD_s	—	20 kHz LPF	—	−94	−80	dB
Cross-talk	CT_s	—	OUTL → OUTR/ OUTR → OUTL	—	−88	−80	dB

Note 15: One input pin selected of four selectors of each channels.

DA Converter

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output signal level	A_o	—	Output voltage at full-scale digital input	1.22	1.27	1.37	Vrms
S/N ratio	S/N_d	—	A-Weight, X'tal: 36.864 MHz	90	98	—	dB
THD + N	THD_d	—	20 kHz LPF, X'tal: 36.864 MHz	—	−86	−75	dB
Cross-talk	CT_d	—	20 kHz LPF, X'tal: 36.864 MHz	—	−95	−83	dB
Dynamic range	DR_d	—	A-Weight, X'tal: 36.864 MHz	87	95	—	dB

Timing

Clock Input Pin (XI)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock cycle	t_{XI}	—	—	27	—	—	ns
Clock “H” cycle width	t_{XIH}	—	—	—	13.5	—	ns
Clock “L” cycle width	t_{XIL}	—	—	—	13.5	—	ns

Reset Pin ($\overline{RST}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Standby time	t_{RRS}	—	—	10	—	—	ms
Reset pulse width	t_{WRS}	—	—	1.0	—	—	μs

Audio Serial Interface (EBCI/O, ELRI/O, DIN0 to 2, DOUT)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
ELRI/O hold time (ELRI/O input)		t_{LIH}	—	Unless than fs = 48 kHz, EBCI/O input: Unless than 64 fs	−75	—	75	ns
DIN 0, 1, 2 setup time		t_{SDI}	—		50	—	—	ns
DIN 0, 1, 2 hold time		t_{HDI}	—		50	—	—	ns
EBCI/O clock cycle	(ELRI/O input)	t_{EBCI}	—		150	—	—	ns
EBCI/O clock “H” cycle width		t_{EBIH}	—		75	—	—	ns
EBCI/O clock “L” clock width		t_{EBIL}	—		75	—	—	ns
ELRI/O output delay time (ELRI/O output)		t_{LOH}	—	C_L = 30 pF	0	—	60	ns
DOUT output delay time (1)		t_{DO1}	—	C_L = 30 pF	—	—	35	ns
DOUT output delay time (2)		t_{DO2}	—	C_L = 30 pF	—	—	35	ns

Microcontroller Interface

(1) Standard transmission mode ($\overline{CS}$, IFCK, IFDI, IFDO)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Standby time	t_{STB}	—	—	1.0	—	—	μs
$\overline{CS}$ ↓-IFCK ↓ setup time	t_{CCD}	—	—	0.2	—	—	μs
IFCK "L" cycle width	t_{WLC}	—	—	0.25	—	—	μs
IFCK "H" cycle width	t_{WHC}	—	—	0.25	—	—	μs
IFCK ↑- $\overline{CS}$ ↑ setup time	t_{CKC}	—	—	0.25	—	—	μs
$\overline{CS}$ "H" cycle width	t_{WCS}	—	(Note 16)	0.5	—	—	μs
IFDI-IFCK ↑ setup time	t_{SCD}	—	—	0.2	—	—	μs
IFCK ↑-IFDI holed time	t_{HCD}	—	—	0.2	—	—	μs
IFCK ↓-IFDO propagation delay time	t_{DDO}	—	C_L = 30 pF	—	—	0.2	μs

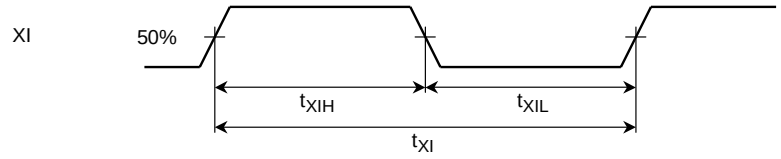
Note 16: The command which is "Sync" in the transfer Sync with Sync signal of a 14 page table 1 control command table needs to set the $\overline{CS}$ = H section to a minimum of 1 fs more until it transmits the follwing command. (It needs more than 22.68 μs at fs = 44.1 KHz.)

(2) I^2C mode ($\overline{CS}$, IFCK, IFDI)

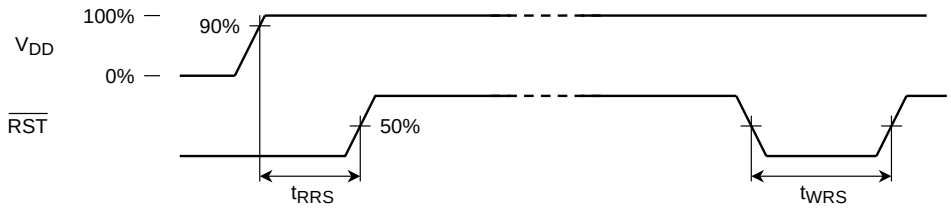
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
IFCK clock frequency	t_{IFCK}	—	C_L = 400 pF	0	—	400	kHz
IFCK "H" cycle width	t_H	—	C_L = 400 pF	0.6	—	—	μs
IFCK "L" cycle width	t_L	—	C_L = 400 pF	1.3	—	—	μs
Data setup time	t_{DS}	—	C_L = 400 pF	0.1	—	—	μs
Data hold time	t_{DH}	—	C_L = 400 pF	0	—	—	μs
Transmission start condition hold time	t_{SCH}	—	C_L = 400 pF	0.6	—	—	μs
Repeat transmission start setup time	t_{SCS}	—	C_L = 400 pF	0.6	—	—	μs
Transmission end condition setup time	t_{ECS}	—	C_L = 400 pF	0.6	—	—	μs
Data transmission interval	t_{BUF}	—	C_L = 400 pF	1.3	—	—	μs
I^2C rising time	t_R	—	C_L = 400 pF	—	—	0.3	μs
I^2C falling time	t_F	—	C_L = 400 pF	—	—	0.3	μs

AC Characteristic Measurement Point

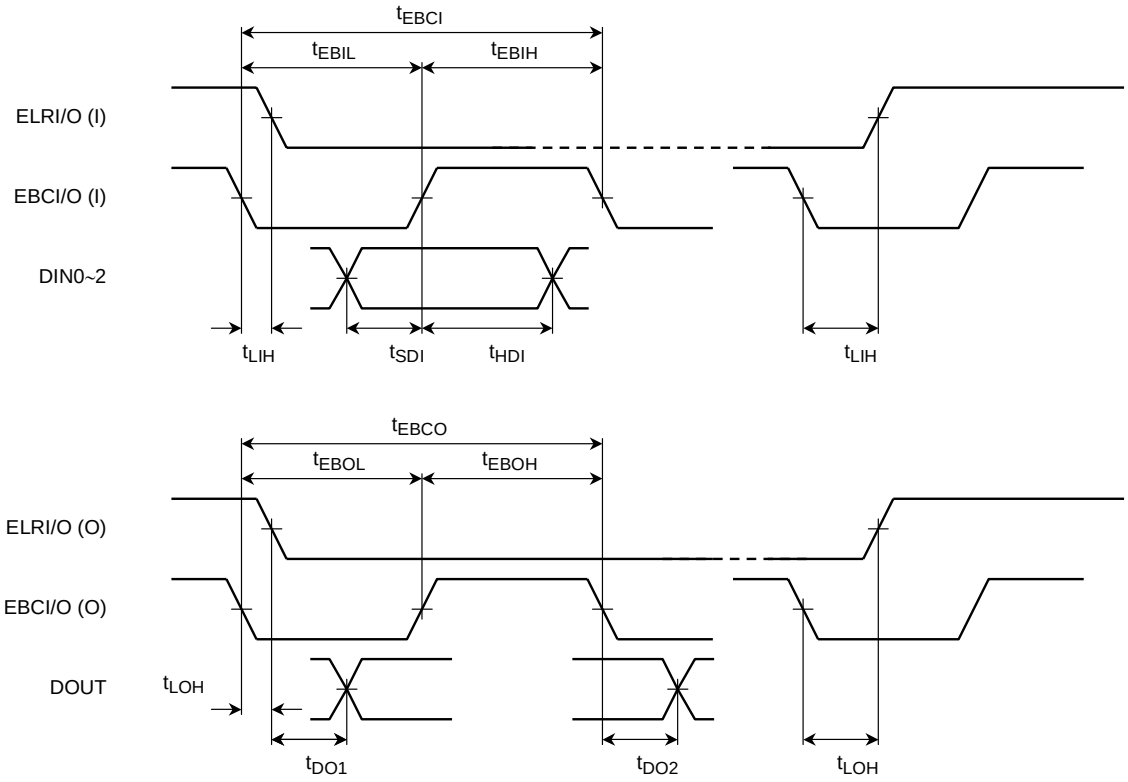
(1) Clock pin (XI)



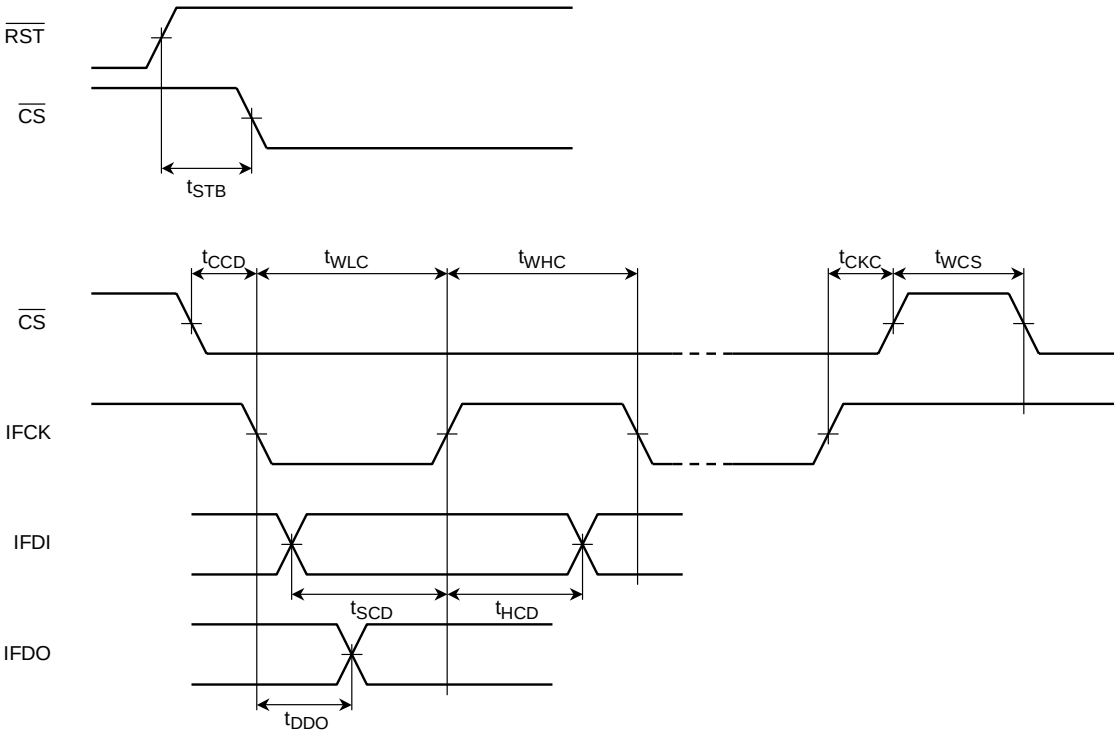
(2) Reset



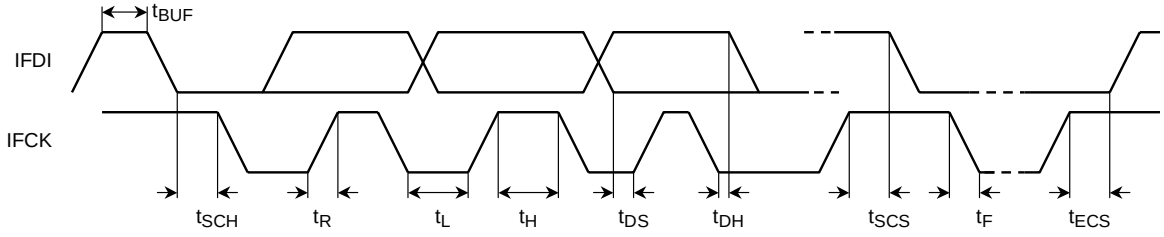
(3) Audio serial interface (ELRI/O, EBCI/O, DIN0 to 2, DOUT)



(4) Microcontroller interface in standard transmission mode ($\overline{CS}$, IFCK, IFDI, IFDO)

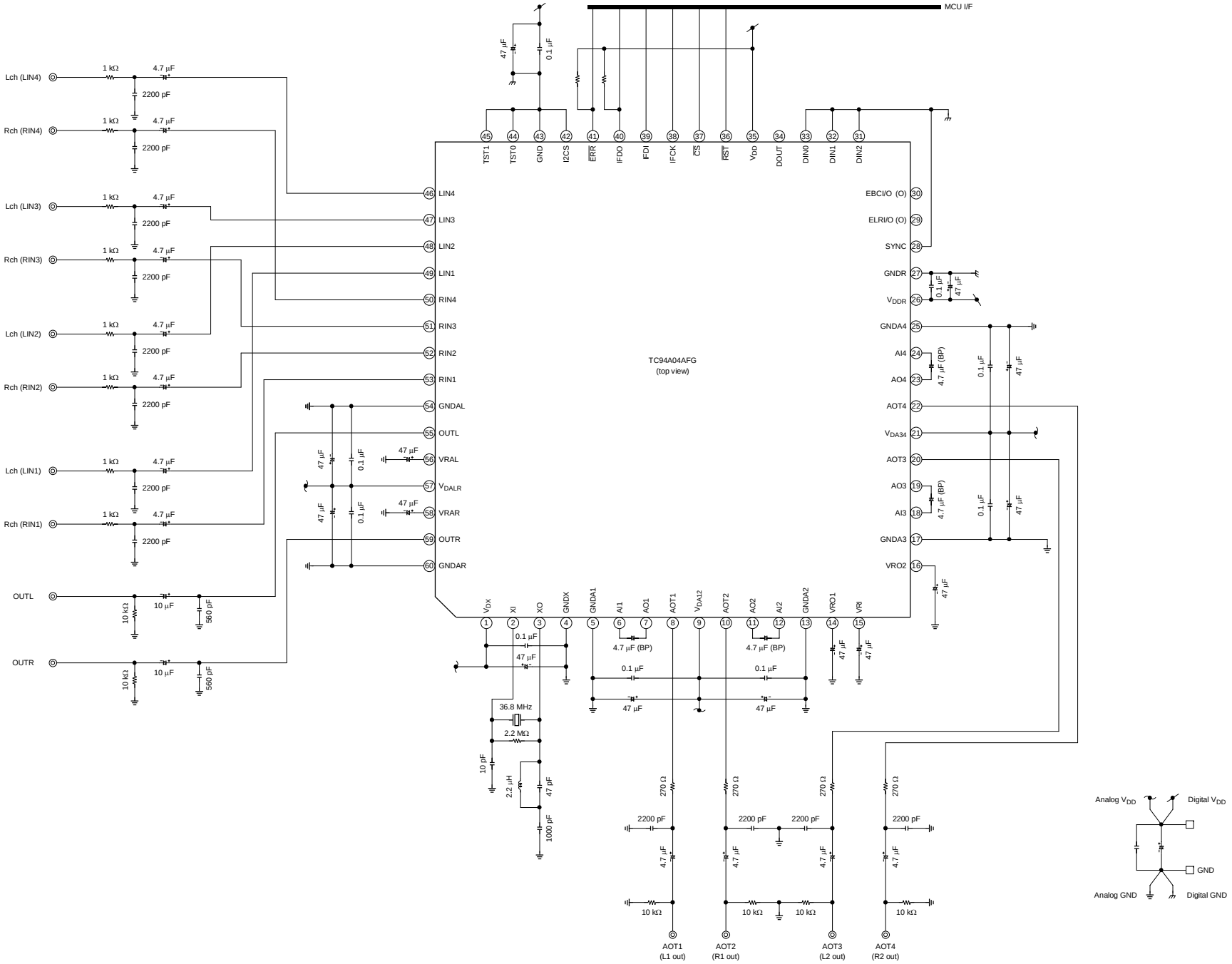


(5) Microcontroller interface in I^2C mode (IFCK, IFDI)



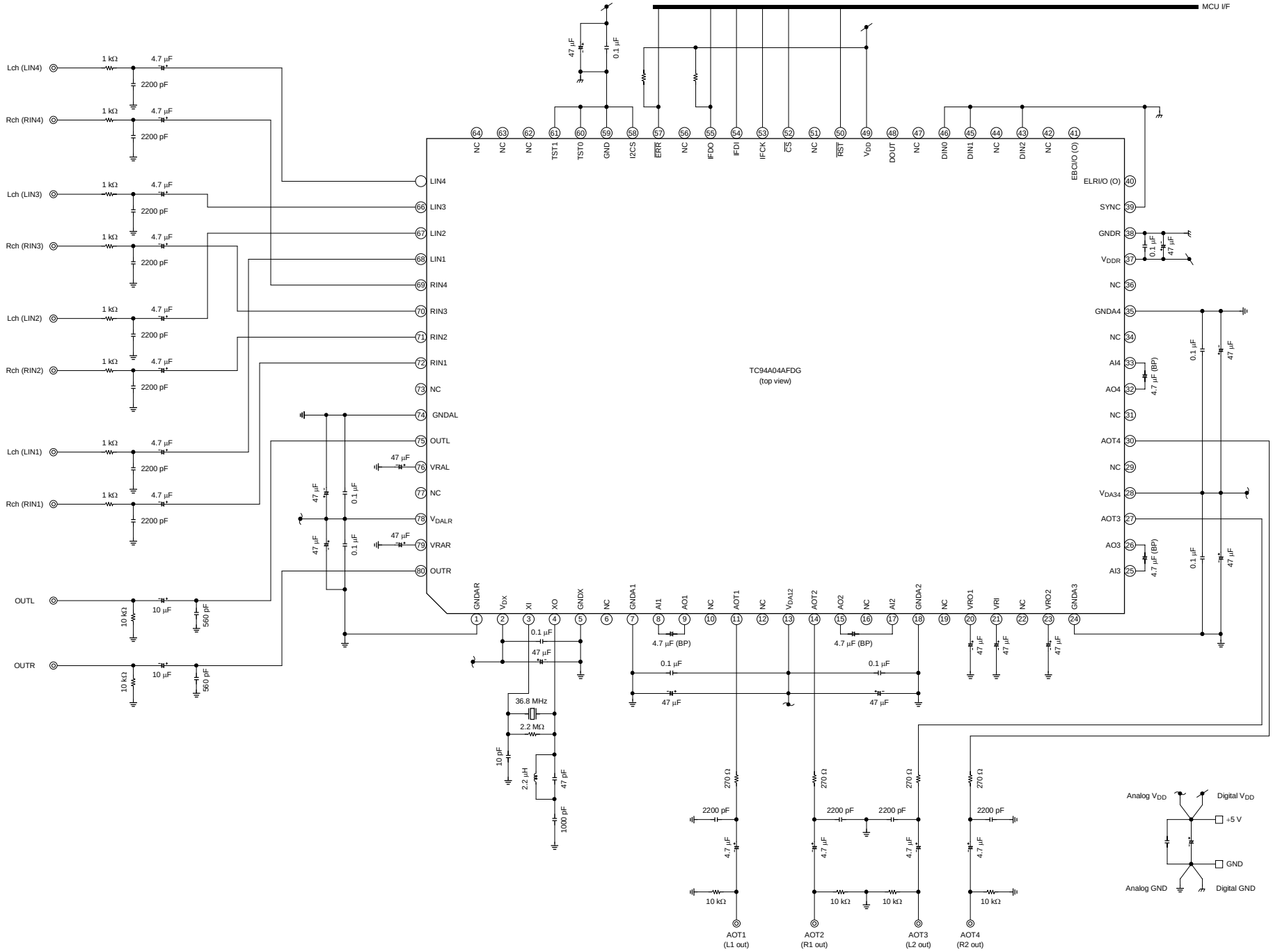
Peripheral Circuit Example 1

The circuit below is an example circuit only. The operation of this circuit is not guaranteed by Toshiba.



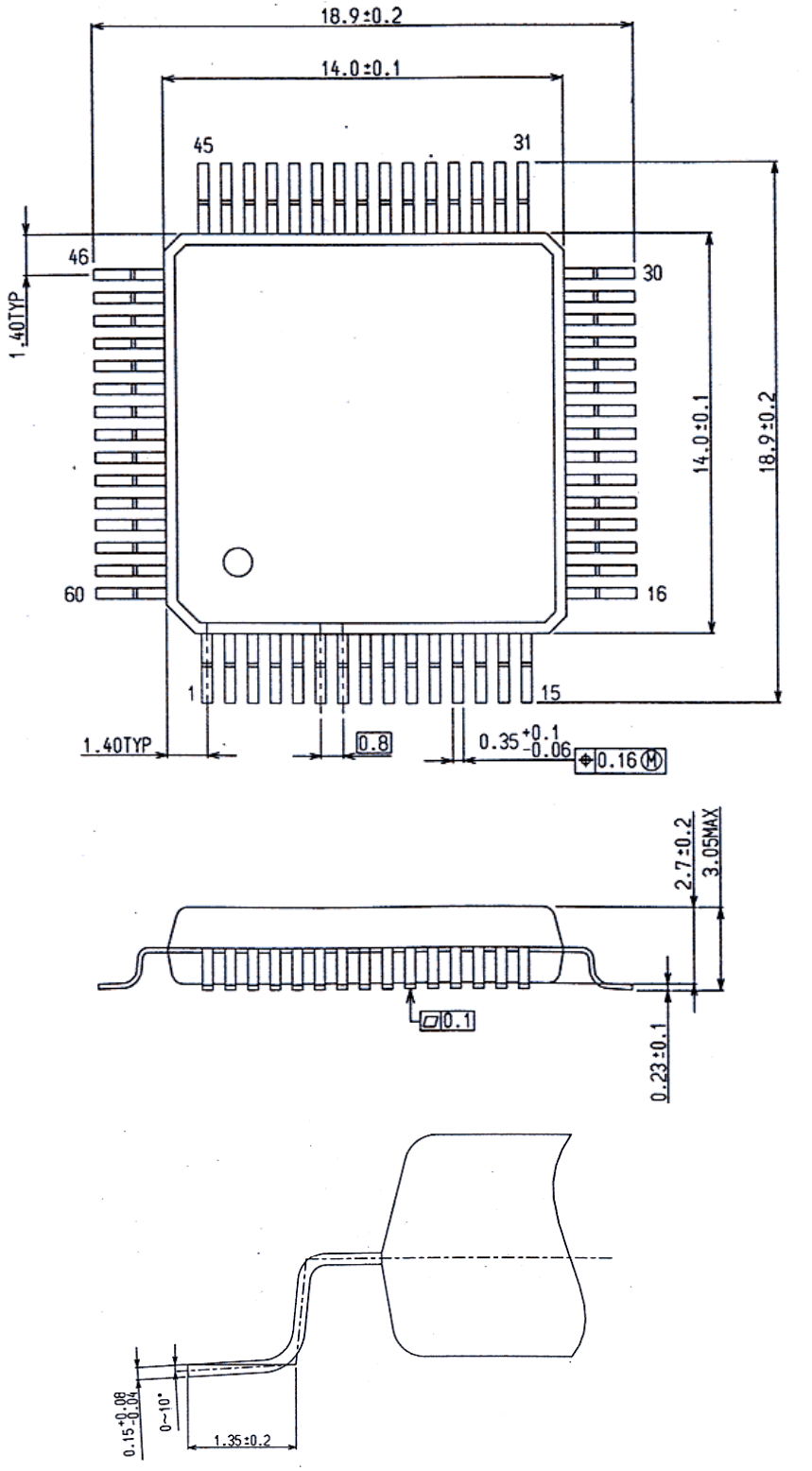
Peripheral Circuit Example 2

The circuit below is an example circuit only. The operation of this circuit is not guaranteed by Toshiba.



Package Dimensions

P-QFP60-1414-0.80N Unit: mm

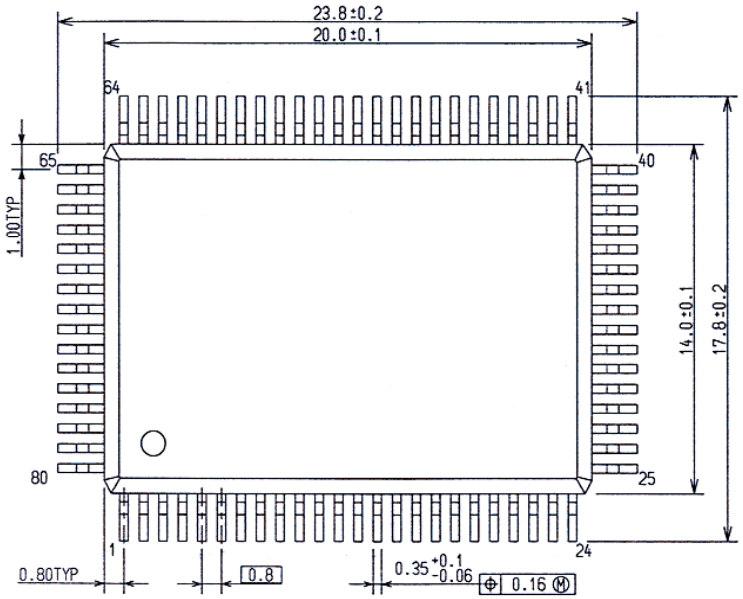


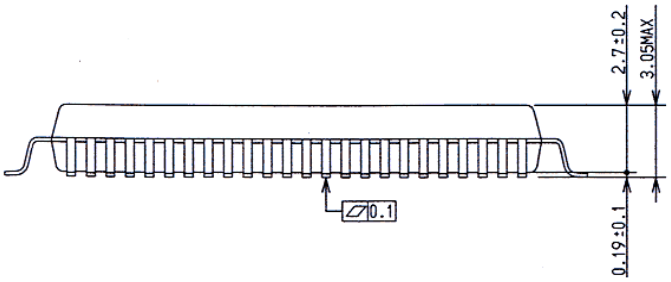
(Note) Palladium plate

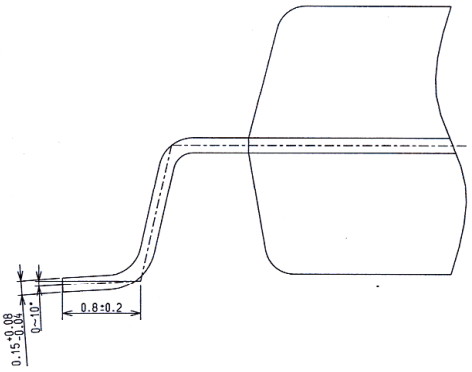
Weight: 1.08 g (typ.)

Package Dimensions

P-QFP80 -1420-0.80M Unit: mm







(Note) Palladium plate

Weight: 1.57 g (typ.)

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030619EBA

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