4.5Ω 300MHz Bandwidth Dual SPDT Analog Switch

UM4717 *CSP10 1.90×1.40*
UM4717Q *QFN10 1.80×1.40*

General Description

The UM4717/UM4717Q low-voltage, low on-resistance (R_{ON}), dual single-pole/double-throw (SPDT) analog switch operates from a single +1.8V to +5.5V supply. The device is designed for USB 1.1/2.0 and audio switching applications.

The UM4717 features two 4.5Ω R_{ON}(max) SPDT switches with 1.2Ω flatness and 0.3Ω matching between channels, while the UM4717Q features two 6Ω R_{ON}(max) SPDT switches with 1.8Ω flatness and 0.6Ω matching between channels. The switch offers break-before-make switching (1ns) with t_{ON}<80ns and t_{OFF}<40ns at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply.

The UM4717 is packaged in a chip-scale package (CSP), occupies only a 1.90mm ×1.40mm area and has a 4×3 bump array with a bump pitch of 0.50mm. The UM4717Q is packaged in a 1.80mm ×1.40mm QFN10 package, both significantly reducing the required PC board area.

Applications

- USB 1.1/2.0 Signal Switching Circuits
- Battery-Operated Equipment
- Audio/Video-Signal Routing
- Headphone Switching
- Low-Voltage Data-Acquisition Systems
- Sample-and-Hold Circuits
- Cell Phones
- PDAs

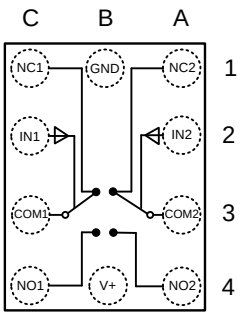
Features

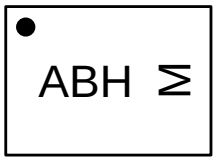
- 2ns (Max) Differential Skew
- -3dB Bandwidth: 300MHz
- Low 15pF On-Channel Capacitance
- Single-Supply Operation from +1.8V to +5.5V
- Typical R_{ON}(max) with +3V Supply: 4.5Ω (UM4717), 6Ω (UM4717Q)
- Rail-to-Rail Signal Handling
- High Off-Isolation: -50dB (10MHz)
- Low Crosstalk: -70dB (10MHz)
- Low Distortion: 0.03%
- +1.8V CMOS-Logic Compatible
- < 0.5nA Leakage Current at +25℃

Pin Configurations

Top View

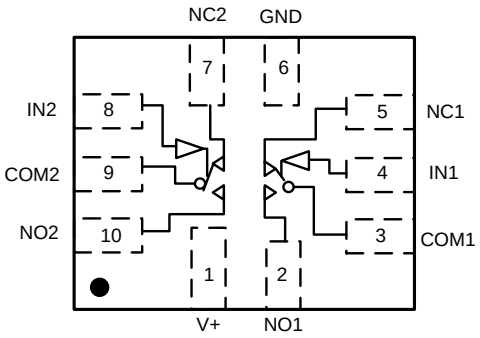
(Top View)

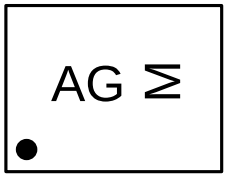




M: Month Code
UM4717
CSP10 1.90×1.40

(Top View)





M: Month Code
UM4717Q
QFN10 1.80×1.40

Ball Mapping for UM4717

C	B	A	
NC1	GND	NC2	1
IN1		IN2	2
COM1		COM2	3
NO1	V+	NO2	4

Transparent Top View

Pin Description

Pin		Name	Function
UM4717	UM4717Q		
A1	7	NC2	Analog Switch 2-Normally Closed Terminal
A2	8	IN2	Analog Switch 2-Digital Control Input
A3	9	COM2	Analog Switch 2-Common Terminal
A4	10	NO2	Analog Switch 2-Normally Open Terminal
B1	6	GND	Ground Connection
B4	1	V_+	Positive Supply Voltage
C1	5	NC1	Analog Switch 1-Normally Closed Terminal
C2	4	IN1	Analog Switch 1-Digital Control Input
C3	3	COM1	Analog Switch 1-Common Terminal
C4	2	NO1	Analog Switch 1-Normally Open Terminal

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM4717	CSP10 1.90×1.40	ABH	3000pcs/7 Inch Tape & Reel
UM4717Q	QFN10 1.80×1.40	AG	3000pcs/7 Inch Tape & Reel

Function Table

IN_	NO_	NC_
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Symbol	Parameter		Limit	Unit
V_+	Supply Voltage		-0.3 to +6.0	V
V_S	DC Switch Voltage (Note 1)		-0.3 to (V_++0.3)	
IN_	DC IN Voltage		-0.3 to +6.0	
I_O	Continuous Current (COM_, NO_, NC_)		±100	mA
I_P	Peak Current (Pulsed at 1ms, 10% Duty Cycle)		±200	
T_O	Operating Temperature Range		-40 to +85	℃
T_J	Junction Temperature		+150	
T_{STG}	Storage Temperature Range		-65 to +150	
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		+300	
T_{Bump}	Bump Temperature (Soldering)	Infrared (15s)	+220	
		Vapor Phase (60s)	+215	
P_D	Continuous Power Dissipation @ +70℃		909	mW
ESD	ESD Method 3015.7		＞2000	V

Note 1: Signals on COM_, NO_, or NC_ exceeding V_+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Electrical Characteristics (Single +3V Supply)

(V_+=+2.7V to +3.6V, T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_+=+3.0V, T_A=+25℃) (Notes 2, 3)

Symbol	Parameter	Test Conditions		Temp	Limits (–40℃ to 85℃)			Unit
					Min	Typ	Max	
DC Electrical Characteristics								
$V_{COM_}$ $V_{NO_}$ $V_{NC_}$	Analog Signal Range			Full	0		V_+	V
V_+	Power Supply Range			Full	1.8		5.5	V
I_+	Supply Current	V_+=+5.5V, V_{IN}=0V or V_+		Full			1	μA
$I_{COM_(ON)}$	COM_On Leakage Current (Note 4)	V_+=+3.6V, $V_{COM_}$=0.3V, 3.3V; $V_{NO_}$ or $V_{NC_}$=0.3V, 3.3V, or Floating		Room Full	-1 -2	+0.01	+1 +2	nA
I_{OFF}	OFF State Leakage Current (Note 4)	V_+=+3.6V, $V_{COM_}$=0.3V, 3.3V; V_{NO} or V_{NC} =3.3V, 0.3V		Room Full	-0.5 -1	+0.01	+0.5 +1	nA
V_{IH}	Input High Voltage			Full	1.6			V
V_{IL}	Input Low Voltage			Full			0.5	V
I_{IN}	Input Leakage Current	V_+=+3.6V, $V_{IN_}$=0 or 5.5V		Full	-100		+100	nA
R_{ON}	On-Resistance (Note 4)	V_+=+2.7V, $I_{COM_}$=10mA; $V_{NO_}$ or $V_{NC_}$=1.5V	UM4717	Room		3.0	4.5	Ω
				Full			5	
			UM4717Q	Room		4.5	6	
				Full			7	
ΔR_{ON}	On Resistance Match Between Channels (Notes 4, 5)	V_+=+2.7V, $I_{COM_}$=10mA; $V_{NO_}$ or $V_{NC_}$=1.5V	UM4717	Room		0.1	0.3	Ω
				Full			0.4	
			UM4717Q	Room		0.5	0.6	
				Full			0.9	
R_{FLAT}	On Resistance Flatness (Note 6)	V_+=+2.7V, $I_{COM_}$=10mA; $V_{NO_}$ or $V_{NC_}$= 1.0V, 1.5V, 2.0V	UM4717	Room		0.6	1.2	Ω
				Full			1.5	
			UM4717Q	Room		1.5	1.8	
				Full			2.0	

Note 2: The parts are 100% tested at +25℃ only, and guaranteed by design over the specified temperature range.

Note 3: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

Note 4: Guaranteed by design.

Note 5: $\Delta R_{ON}=R_{ON(MAX)}-R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Between any two switches.

Electrical Characteristics (Single +3V Supply) (Continued)

(V_+=+2.7V to +3.6V, T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_+=+3.0V, T_A=+25℃) (Notes 2, 3)

Symbol	Parameter	Test Conditions	Temp	Limits (–40℃ to 85℃)			Unit
				Min	Typ	Max	
AC Electrical Characteristics							
t_{ON}	Turn-On Time	$V_{NO_}$, $V_{NC_}$=1.5V; R_L=300Ω, C_L=35pF, Figure 1; V_{IH}=1.5V, V_{IL}=0V	Room Full		40	80 100	ns
t_{OFF}	Turn-Off Time	$V_{NO_}$, $V_{NC_}$=1.5V; R_L=300Ω, C_L=35pF, Figure 1; V_{IH}=1.5V, V_{IL}=0V	Room Full		20	40 50	ns
t_{BBM}	Break Before Make Time (Note 4)	$V_{NO_}$, $V_{NC_}$=1.5V; R_L=300Ω, C_L=35pF, Figure 2	Room Full	1	8		ns
t_{SKEW}	Skew (Note 4)	R_S=39Ω, C_L=50pF, Figure 3	Full		0.15	2	ns
Q_{INJ}	Charge Injection	C_L=1.0nF, Figure 4 V_{GEN}=1.5V, R_{GEN}=0Ω	Room		5		pC
V_{ISO}	Off Isolation	f=10MHz; $V_{NO_}$, $V_{NC_}$=1V_{P-P}; R_L=50Ω, C_L=5pF, Figure 5	Room		-50		dB
		f=1MHz; $V_{NO_}$, $V_{NC_}$=1V_{P-P}; R_L=50Ω, C_L=5pF, Figure 5			-70		
V_{CT}	Crosstalk (Note 7)	f=10MHz; $V_{NO_}$, $V_{NC_}$=1V_{P-P}; R_L=50Ω, C_L=5pF, Figure 5	Room		-70		dB
		f=1MHz; $V_{NO_}$, $V_{NC_}$=1V_{P-P}; R_L=50Ω, C_L=5pF, Figure 5			-90		
BW	-3dB Bandwidth	Signal=0dBm, R_L=50Ω, C_L=5pF, Figure 5	Room		300		MHz
THD	Total Harmonic Distortion	R_L=600Ω, $V_{COM_}$=2V_{P-P}	Room		0.03		%
Capacitance							
$C_{NO_(OFF)}$ $C_{NC_(OFF)}$	NO_, NC_ Off Capacitance	f=1MHz, Figure 6	Room		9		pF
$C_{(ON)}$	Switch On Capacitance	f=1MHz, Figure 6	Room		15		pF

Note 2: The parts are 100% tested at +25℃ only, and guaranteed by design over the specified temperature range.

Note 3: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

Note 4: Guaranteed by design.

Note 5: $\Delta R_{ON}=R_{ON(MAX)}-R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Between any two switches.

Electrical Characteristics (Single +5V Supply)

(V_+=+4.2V to +5.5V, T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_+=+5.0V, T_A=+25℃) (Notes 2, 3)

Symbol	Parameter	Test Conditions		Temp	Limits (–40℃ to 85℃)			Unit
					Min	Typ	Max	
DC Electrical Characteristics								
$V_{COM_}$ $V_{NO_}$ $V_{NC_}$	Analog Signal Range			Full	0		V_+	V
V_+	Power Supply Range			Full	1.8		5.5	V
I_+	Supply Current	V_+=+5.5V, $V_{IN_}$=0V or V_+		Full			1	μA
$I_{COM_(ON)}$	COM_On Leakage Current (Note 4)	V_+=+5.5V, $V_{COM_}$=1.0V, 4.5V; $V_{NO_}$ or $V_{NC_}$=1.0V, 4.5V, or Floating		Room Full	-1 -2	+0.01	+1 +2	nA
I_{OFF}	OFF State Leakage Current (Note 4)	V_+=+5.5V, $V_{COM_}$=1.0V, 4.5V; V_{NO} or V_{NC} =1.0V, 4.5V		Room Full	-0.5 -1	+0.01	+0.5 +1	nA
V_{IH}	Input High Voltage			Full	2.3			V
V_{IL}	Input Low Voltage			Full			0.8	V
I_{IN}	Input Leakage Current	V_+=+5.5V, $V_{IN_}$=0 or V_+		Full	-100		+100	nA
R_{ON}	On-Resistance (Note 4)	V_+=+4.2V, $I_{COM_}$=10mA; $V_{NO_}$ or $V_{NC_}$=3.5V	UM4717	Room		1.7	3	Ω
				Full			3.5	
			UM4717Q	Room		2.5	3.5	
				Full			4	
ΔR_{ON}	On Resistance Match Between Channels (Notes 4, 5)	V_+=+4.2V, $I_{COM_}$=10mA; $V_{NO_}$ or $V_{NC_}$= 3.5V	UM4717	Room		0.1	0.3	Ω
				Full			0.4	
			UM4717Q	Room		0.5	0.6	
				Full			0.9	
R_{FLAT}	On Resistance Flatness (Note 6)	V_+=+4.2V, $I_{COM_}$=10mA; $V_{NO_}$ or $V_{NC_}$=1.0V, 2.0V, 3.5V	UM4717	Room		0.4	1.2	Ω
				Full			1.5	
			UM4717Q	Room		0.9	1.2	
				Full			1.5	

Note 2: The parts are 100% tested at +25℃ only, and guaranteed by design over the specified temperature range.

Note 3: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a maximum.

Note 4: Guaranteed by design.

Note 5: $\Delta R_{ON}=R_{ON(MAX)}-R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 7: Between any two switches.

Electrical Characteristics (Single +5V Supply) (Continued)

(V_+=+4.2V to +5.5V, T_A=T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_+=+5.0V, T_A=+25℃) (Notes 2, 3)

Symbol	Parameter	Test Conditions	Temp	Limits (–40℃ to 85 ℃)			Unit
				Min	Typ	Max	
AC Electrical Characteristics							
t_{ON}	Turn-On Time	$V_{NO_}$, $V_{NC_}$=3.0V; R_L=300Ω, C_L=35pF, Figure 1;	Room Full		30	80 100	ns
t_{OFF}	Turn-Off Time	$V_{NO_}$, $V_{NC_}$=3.0V; R_L=300Ω, C_L=35pF, Figure 1;	Room Full		20	40 50	ns
t_{BBM}	Break Before Make Time (Note 4)	$V_{NO_}$, $V_{NC_}$=3.0V; R_L=300Ω, C_L=35pF, Figure 2	Room Full	1	8		ns
t_{SKEW}	Skew (Note 4)	R_S=39Ω, C_L=50pF, Figure 3	Full		0.15	2	ns
Q_{INJ}	Charge Injection	C_L=1.0nF, Figure 4 V_{GEN}=1.5V, R_{GEN}=0Ω	Room		9		pC
V_{ISO}	Off Isolation	f=10MHz; $V_{NO_}$, $V_{NC_}$=$1V_{P-P}$; R_L=50Ω, C_L=5pF, Figure 5	Room		-50		dB
		f=1MHz; $V_{NO_}$, $V_{NC_}$=$1V_{P-P}$; R_L=50Ω, C_L=5pF, Figure 5			-70		
V_{CT}	Crosstalk (Note 7)	f=10MHz; $V_{NO_}$, $V_{NC_}$=$1V_{P-P}$; R_L=50Ω, C_L=5pF, Figure 5	Room		-70		dB
		f=1MHz; $V_{NO_}$, $V_{NC_}$=$1V_{P-P}$; R_L=50Ω, C_L=5pF, Figure 5			-90		
BW	-3dB Bandwidth	Signal=0dBm, R_L=50Ω, C_L=5pF, Figure 5	Room		300		MHz
THD	Total Harmonic Distortion	R_L=600Ω, $V_{COM_}$=$2V_{P-P}$	Room		0.03		%
Capacitance							
$C_{NO_(OFF)}$ $C_{NC_(OFF)}$	NO_, NC_ Off Capacitance	f=1MHz, Figure 6	Room		9		pF
$C_{(ON)}$	Switch On Capacitance	f=1MHz, Figure 6	Room		15		pF

Note 2: The parts are 100% tested at +25℃ only, and guaranteed by design over the specified temperature range.

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Note 4: Guaranteed by design.

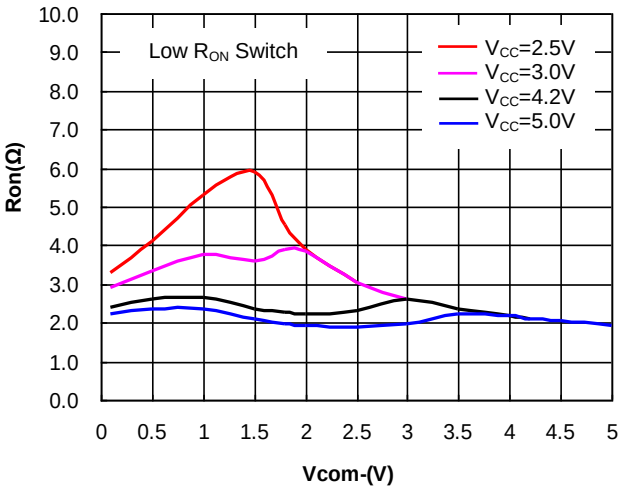
Note 5: $\Delta R_{ON}=R_{ON(MAX)}-R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

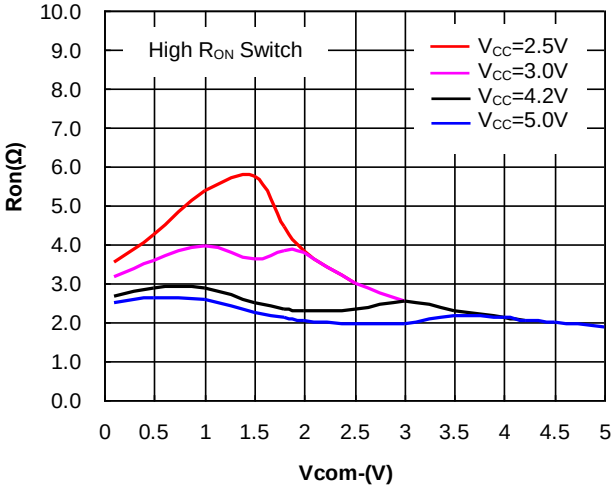
Note 7: Between any two switches.

Typical Operating Characteristics

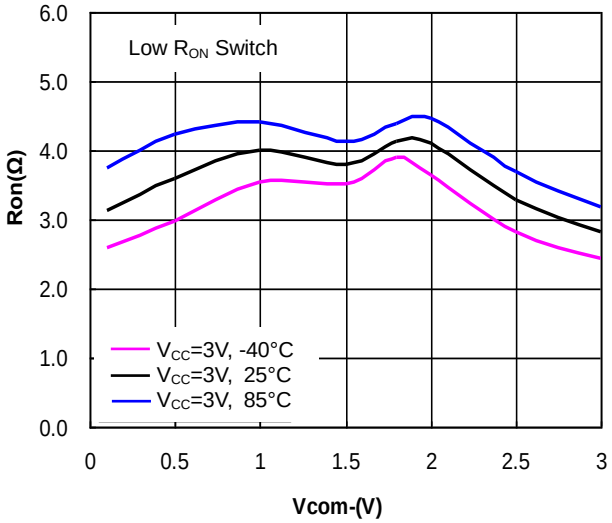
On Resistance vs. COM_Voltage



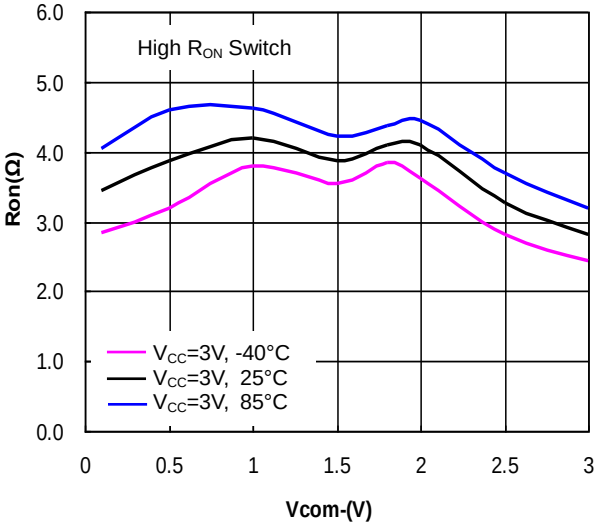
On Resistance vs. COM_Voltage



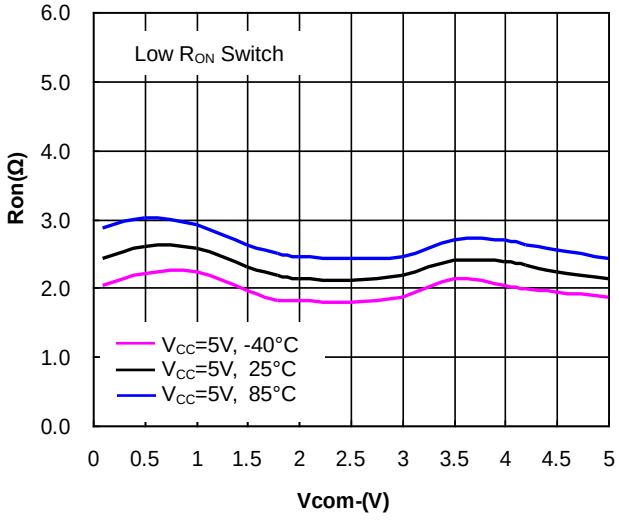
On Resistance vs. COM_Voltage



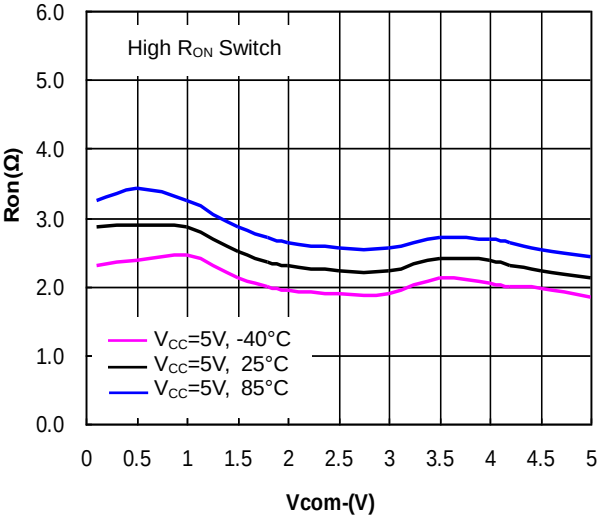
On Resistance vs. COM_Voltage



On Resistance vs. COM_Voltage

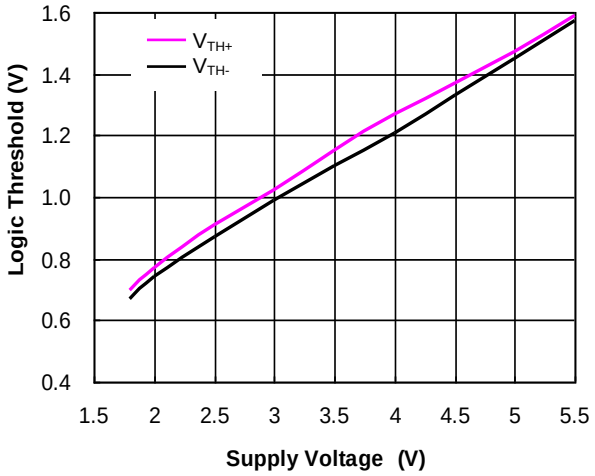


On Resistance vs. COM_Voltage

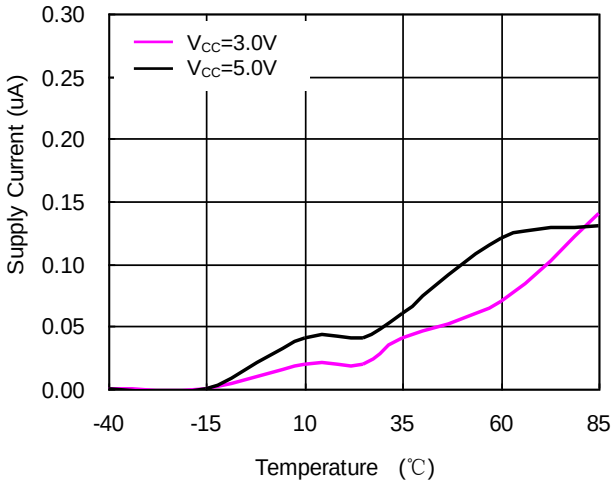


Typical Operating Characteristics (Continued)

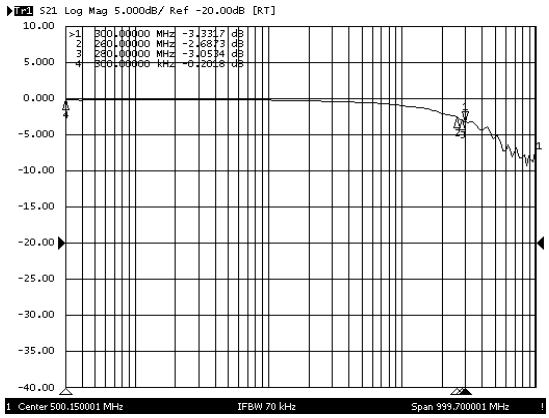
Logic Threshold vs. Supply Voltage



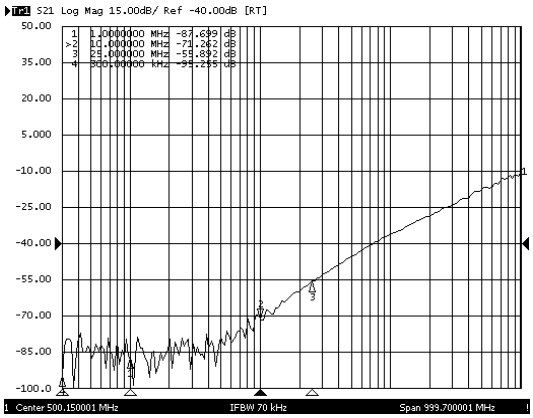
Supply Current vs. Temperature



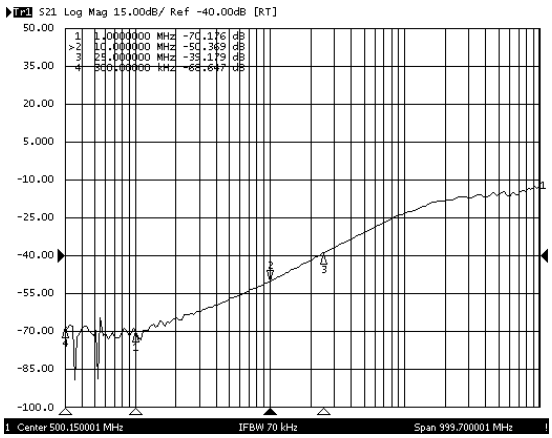
Bandwidth



Crosstalk



Off Isolation



Detailed Description

The UM4717/UM4717Q high-speed, low-voltage, low on-resistance (R_{ON}), dual SPDT analog switch operates from a single +1.8V to +5.5V supply. The switch features break-before-make switching operation and fast switching speeds (t_{ON}=80ns (max), t_{OFF}=40ns (max)).
The switch has low 15pF on-channel capacitance, which allows for 12Mbps switching of the data signals for USB 1.0/1.1 applications. The UM4717/UM4717Q is designed to switch D_+ and D_- USB signals with a guaranteed skew of less than 2ns (see Figure 4) as measured from 50% of the input signal to 50% of the output signal.

Applications Information

Digital Control Inputs

The UM4717/UM4717Q logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN_ can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving the control logic inputs rail-to-rail minimizes power consumption. For a +3V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Analog Signal Levels

The on-resistance of the UM4717/UM4717Q changes very little for analog input signals across the entire supply voltage range (see the Typical Operating Characteristics). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Power-Supply Sequencing and Over-Voltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V_+ before applying analog signals, especially if the analog signal is not current-limited.

Test Circuits

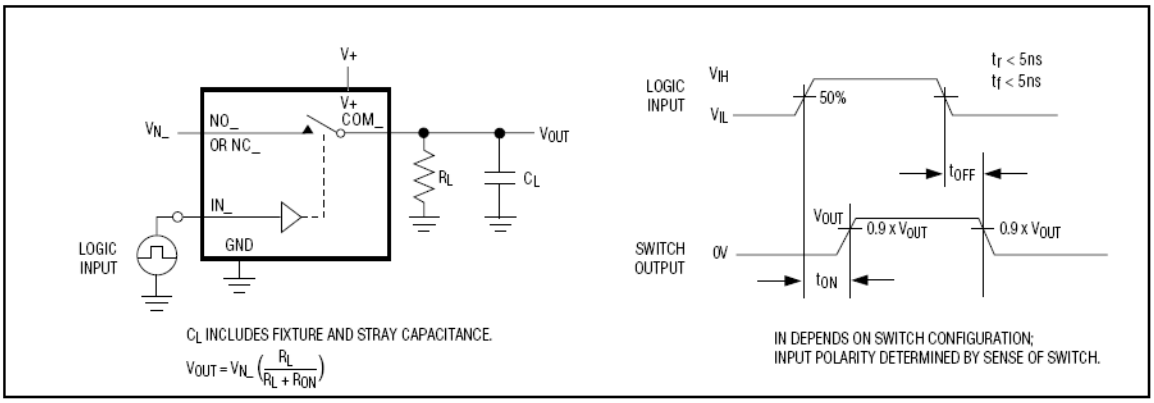


Figure 1. Switching Time

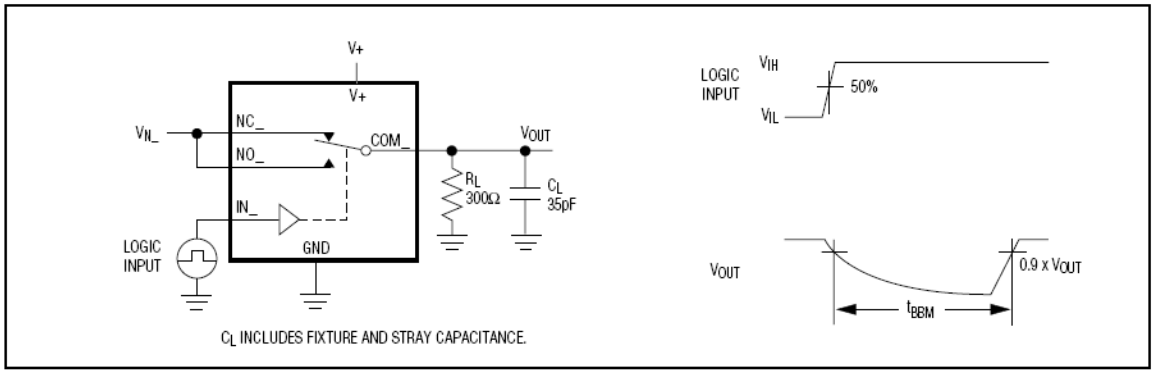


Figure 2. Break-Before-Make Interval

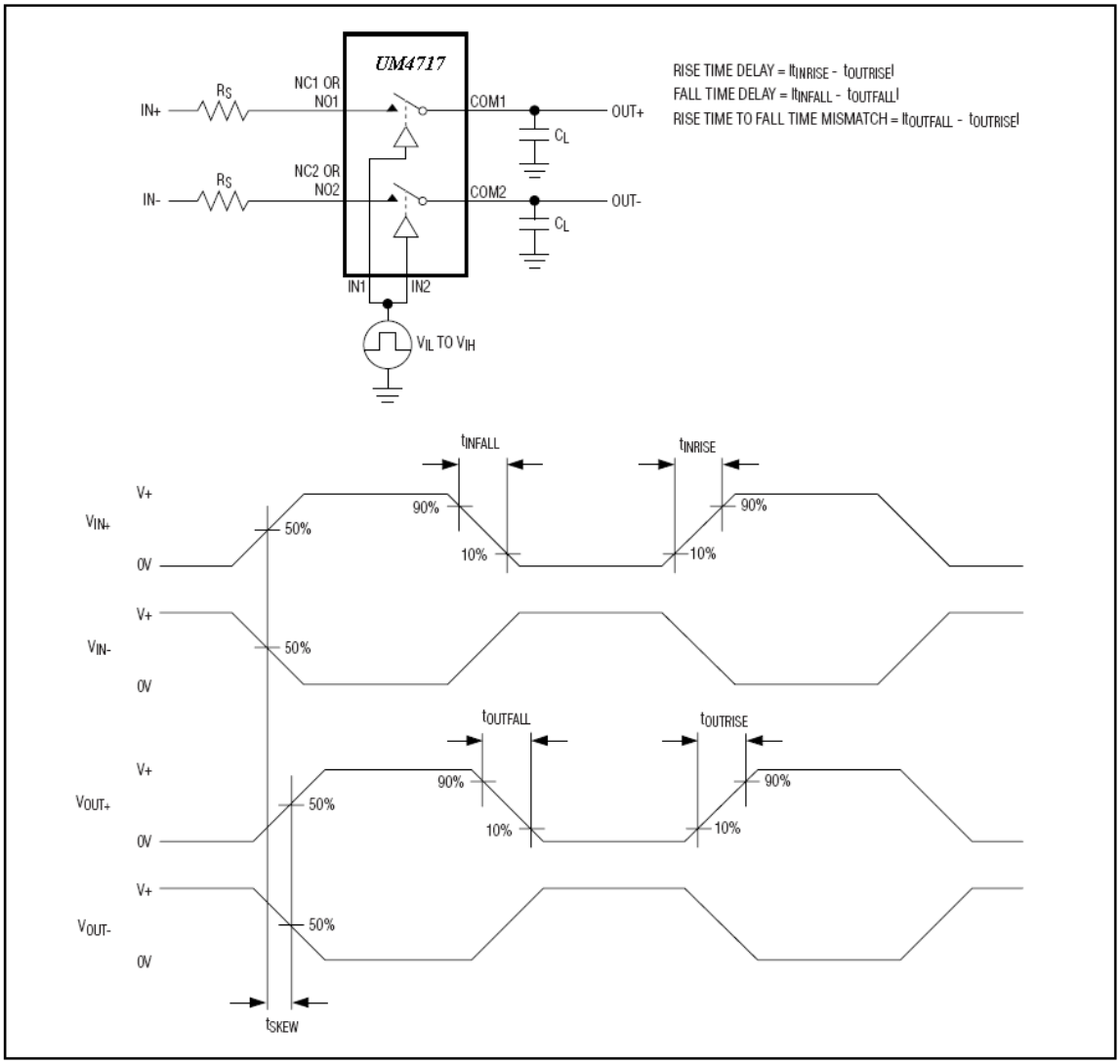


Figure 3. Output Signal Skew

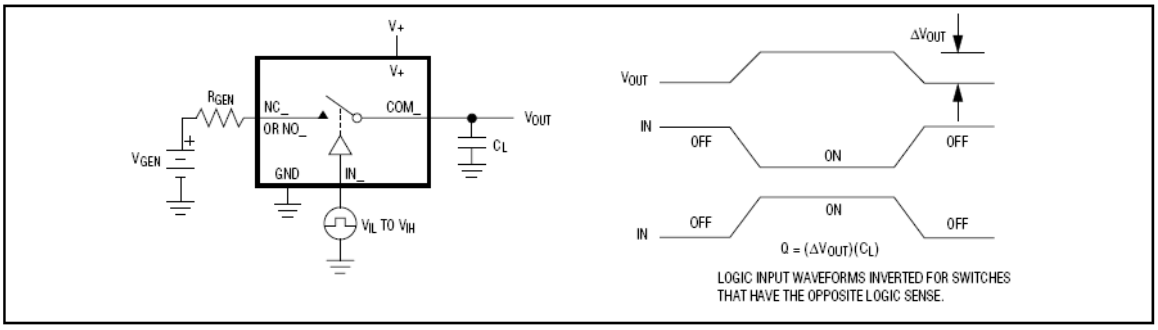


Figure 4. Charge Injection

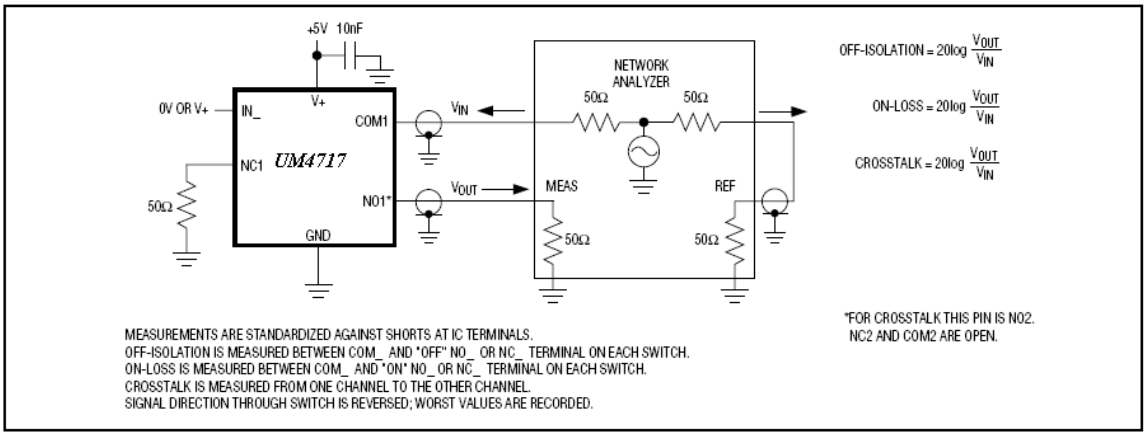


Figure 5. On-Loss, Off-Isolation, and Crosstalk

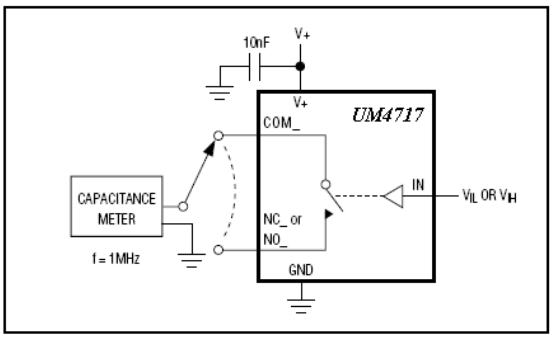
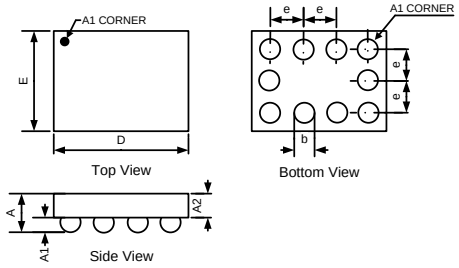


Figure 6. Channel Off/On-Capacitance

Package Information

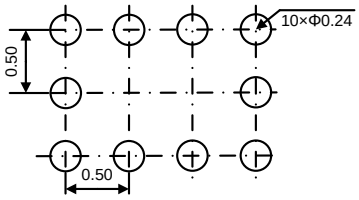
UM4717: CSP10 1.90×1.40

Outline Drawing



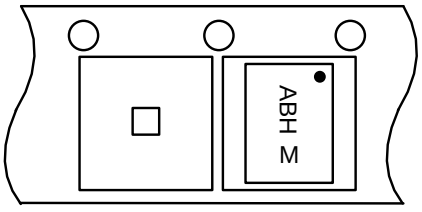
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.68	-	-	0.027
A1	0.21	0.231	0.24	0.0083	0.0091	0.0094
A2	0.40	0.41	0.42	0.015	0.016	0.017
b	0.27	0.30	0.32	0.011	0.012	0.013
D	1.82	-	1.90	0.072	-	0.075
E	1.32	-	1.40	0.052	-	0.055
e	0.50TYP			0.020TYP		

Land Pattern



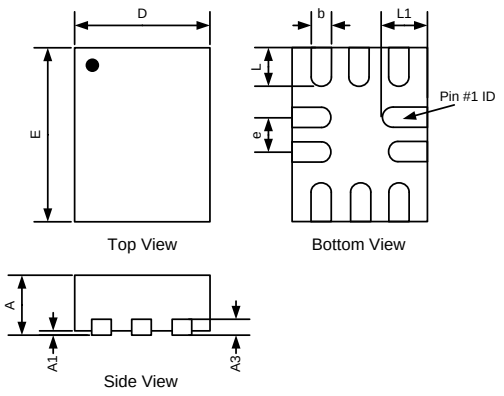
NOTES:
1. Bump is Lead Free Sn/Ag/Cu.
2. Unit: mm.
3. Non-solder mask defined copper landing pad.
4. Laser Mark on silicon die back; back-lapped.

Tape and Reel Orientation



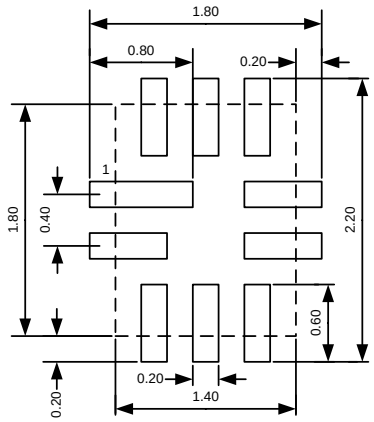
UM4717Q: QFN10 1.80×1.40

Outline Drawing



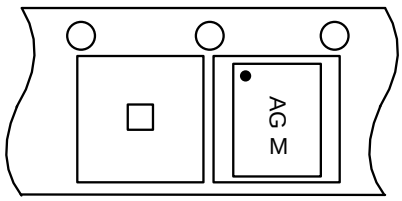
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15REF			0.006REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.35	1.40	1.45	0.053	0.055	0.057
E	1.75	1.80	1.85	0.069	0.071	0.073
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.40	0.50	0.60	0.016	0.020	0.024

Land Pattern



NOTES:
1. Compound dimension: 1.80×1.40;
2. Unit: mm
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



GREEN COMPLIANCE

Union Semiconductor is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.
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http://www.union-ic.com/index.aspx?cat_code=RoHSDeclaration

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