AN-9750

High-Power Factor Flyback Converter for LED Driver with FL7732 PSR Controller

Introduction

This highly integrated PWM controller, FL7732, provides several features to enhance the performance of low-power flyback converters. The proprietary topology enables simplified circuit design for LED lighting applications. By using single-stage topology with primary-side regulation, a LED lighting board can be implemented with few external components and minimized cost, without requiring an input bulk capacitor and feedback circuitry. To implement high power factor and low THD, constant on-time control utilizes an external capacitor connected at the COMI pins.

Precise constant-current control regulates accurate output current across changes in input voltage and output voltage. The operating frequency is proportionally changed by the output voltage to guarantee DCM operation with higher efficiency and simple design. FL7732 provides protection functions such as open-LED, short-LED and over-temperature protection. The current-limit level is automatically reduced to minimize the output current and protect external components in short-LED condition.

This application note presents practical design consideration for an LED driver employing Fairchild Semiconductor PWM PSR controller FL7732. It includes designing the transformer, selecting the components, and implementing constant current regulation. The step-by-step design procedure helps engineers design a power supply. The design procedure is verified through an experimental prototype converter. Figure 1 shows the typical application circuit of primary-side controlled flyback converter using FL7732 created in the design example.

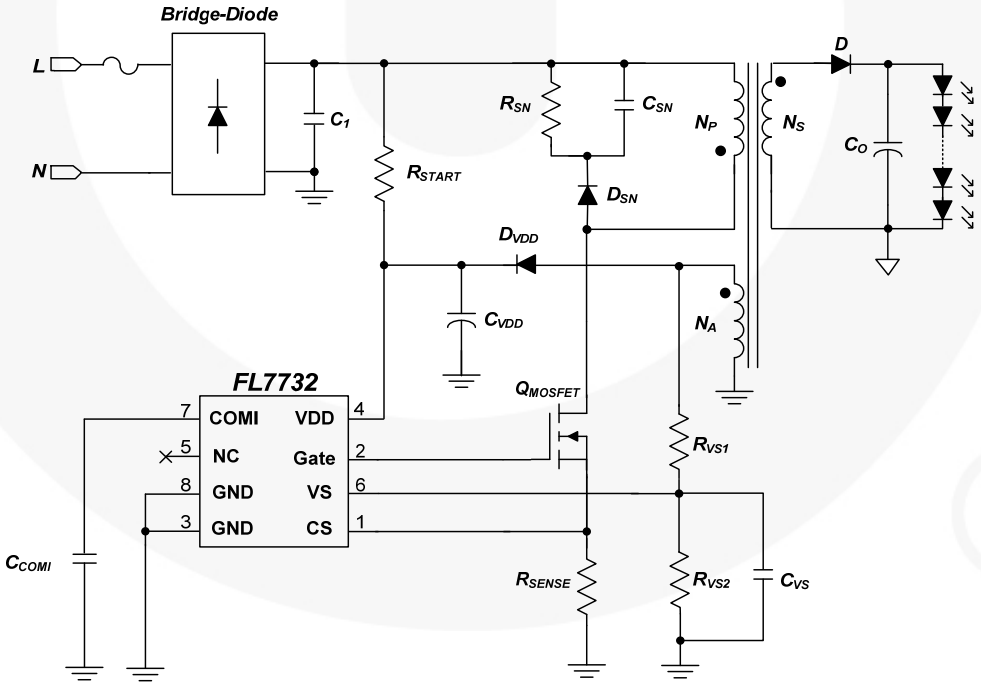

Figure 1. Typical Application Circuit

Basic Operation

Generally, Discontinuous Conduction Mode (DCM) operation is preferred for primary-side regulation because it allows better output regulation. The operation principles of DCM flyback converter are as follows:

Mode I

During the MOSFET turn-on time (t_{ON}), input voltage ($V_{IN.pk}$) is applied across the primary-side inductor (L_m). Then, drain current (I_{DS}) of the MOSFET increases linearly from zero to the peak value (I_{pk}), as shown in Figure 2. During this time, the energy is drawn from the input and stored in the inductor.

Mode II

When the MOSFET (Q) is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on.

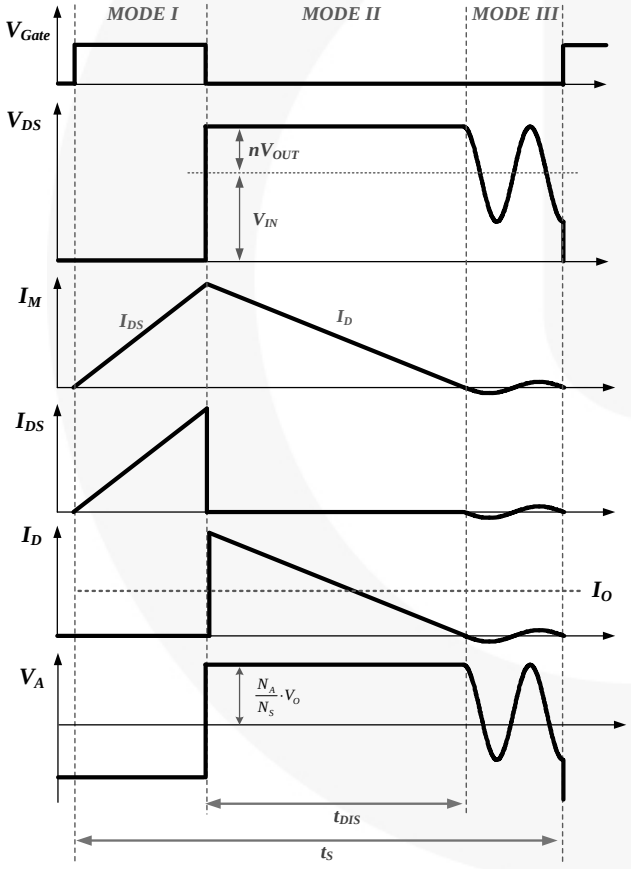

Figure 2. Basic Function of DCM Mode Flyback

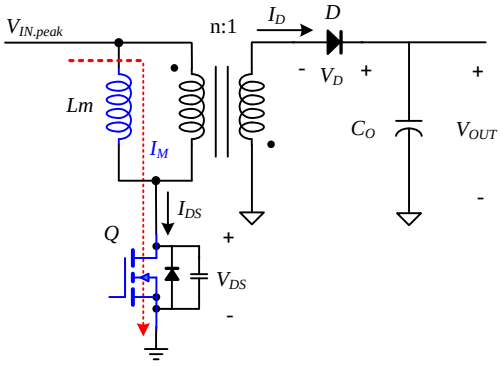

Figure 3. Mode I: Q[ON], D[OFF]

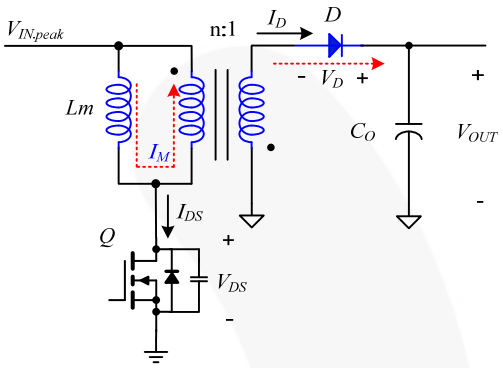

Figure 4. Mode II: Q[OFF], D[ON]

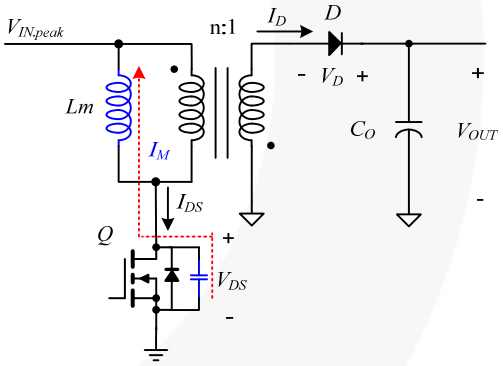

Figure 5. Mode III: Q[OFF], D[OFF]

While the diode is conducting, output voltage (V_{OUT}), together with diode forward-voltage drop (V_F), is applied across the secondary-side inductor and diode current (I_D) decreases linearly from the peak value ($I_{pk} \cdot N_P/N_S$) to zero. At the end of inductor current discharge time (t_{DIS}), all energy stored in the inductor has been delivered to the output.

Mode III

When the diode current reaches zero, the transformer auxiliary winding voltage begins to oscillate by the resonance between the primary-side inductor (L_m) and the effective capacitor loaded across MOSFET (Q).

Constant Current Regulation

The output current (I_O) can be estimated by using the peak drain current (I_{pk}) of MOSFET and discharging time (t_{DIS}) of inductor current because output current (I_O) is same as the average of the diode current (I_D) in steady state. The output current estimator identifies the peak value of the drain current with a peak-detection circuit and calculates the output current using the inductor discharging time and switching period (t_S). This output information is compared with an internal precise reference to generate error voltage (V_{COMI}), which determines the duty cycle of the MOSFET in Constant Current Mode. With Fairchild's innovative TRUECURRENT® technique, the constant output current can be precisely controlled.

$$I_O = \frac{1}{2} \cdot \frac{t_{DIS}}{t_S} \cdot V_{CS} \cdot \frac{N_P}{N_S} \cdot \frac{1}{R_{SENSE}} \quad (1)$$

TRUECURRENT® calculation makes a precise output current prediction.

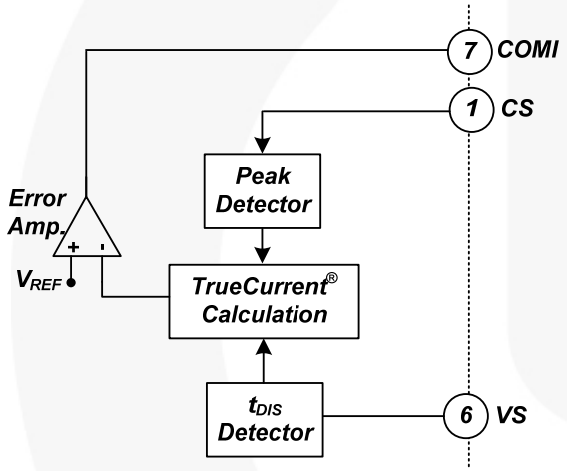

Figure 6. Detection for TRUECURRENT® Calculation

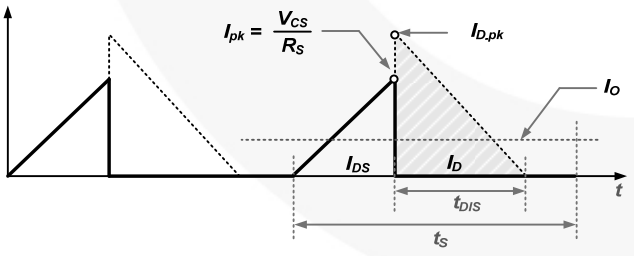

Figure 7. TRUECURRENT® Calculation Principle

Linear Frequency Control

As mentioned above, DCM should be guaranteed for high power factor in flyback topology. To maintain DCM in the wide range of output voltage, frequency is linearly changed by the output voltage in linear frequency control. Output voltage is detected by the auxiliary winding and resistive divider connected to the VS pin, as shown in Figure 7.

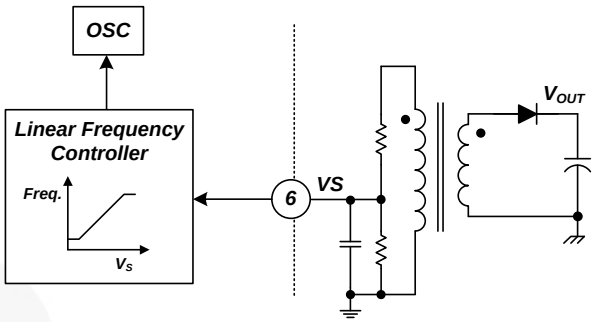

Figure 8. Linear Frequency Control

When output voltage decreases, secondary diode conduction time is increased and the linear frequency control lengthens the switching period, which retains DCM operation in the wide output voltage range, as shown in Figure 8. The frequency control also lowers primary rms current with better power efficiency in full-load condition.

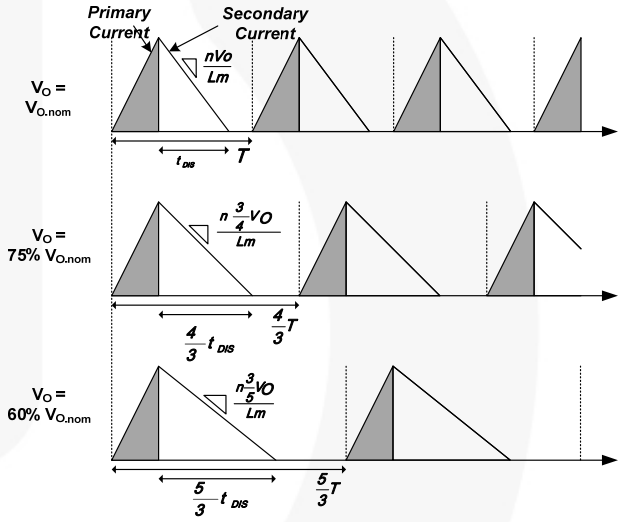

Figure 9. Primary and Secondary Current

BCM Control

The end of secondary diode conduction time is possibly over a switching period set by linear frequency control. In this case, FL7732 doesn't allow CCM and the operation mode changes from DCM to BCM. Therefore, FL7732 originally eliminates sub-harmonic distortion in CCM.

Protections

The FL7732 have several self-protection functions, such as over-voltage protection, over-temperature protection, and pulse-by-pulse current limit. All the protections are implemented as Auto-Restart Mode.

Open-LED Protection

FL7732 protects external components, such as diode and capacitor at secondary side, in open-LED condition. During switch-off, the V_{DD} capacitor is charged up to the auxiliary winding voltage, which is applied as the reflected output voltage. Because the V_{DD} voltage has output voltage information, the internal voltage comparator at the V_{DD} pin can trigger output over-voltage protection (OVP), as shown in Figure 9. When at least one LED is open-circuited, output load impedance becomes very high and output capacitor is quickly charged up to V_{OVP} x N_S / N_A. Then switching is shut down and the V_{DD} block goes into "Hiccup Mode" until the open-LED condition is removed, as shown in Figure 10.

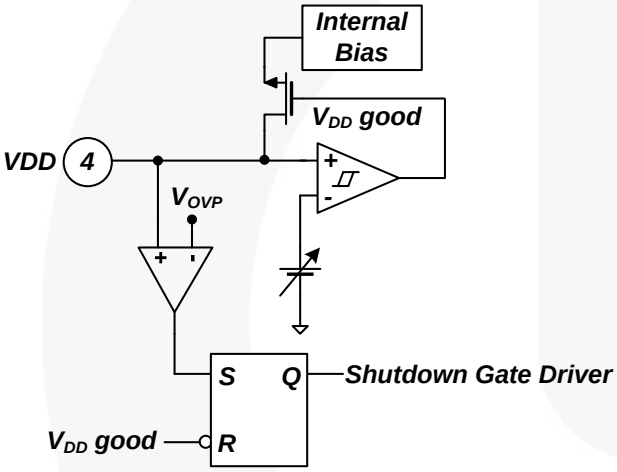

Figure 10. Internal OVP Block

Under Voltage Lockout (UVLO)

The turn-on and turn-off thresholds are fixed internally at 16V and 7.5V, respectively. During startup, the V_{DD} capacitor must be charged to 16V. The V_{DD} capacitor continues to supply V_{DD} until power can be delivered from the auxiliary winding of the main transformer. V_{DD} is not allowed to drop below 7.5V during this startup process. This UVLO hysteresis window ensures that V_{DD} capacitor properly supplies V_{DD} during startup.

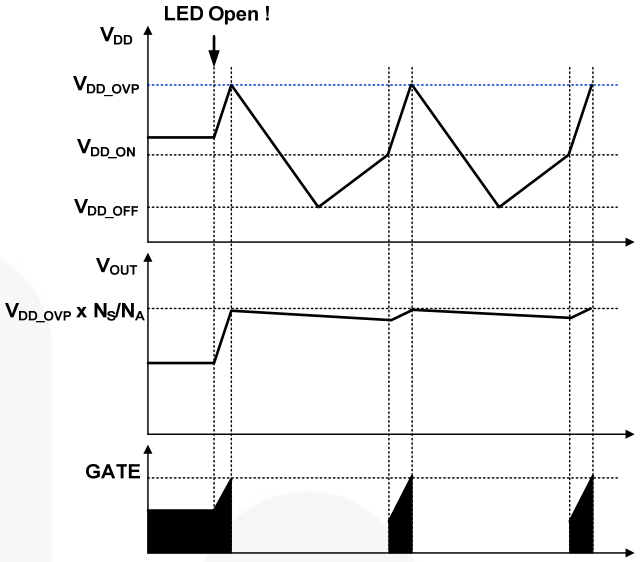

Figure 11. Waveforms at Open-LED Condition

Short-LED Protection (OCP)

In case of short-LED condition, the switching MOSFET and secondary diode are usually stressed by the high powering current. However, FL7732 changes the OCP level in the short LED condition. When V_S voltage is lower than 0.4V, OCP level changes to 0.2V from 0.7V, as shown in Figure 12 so that powering is limited and external components current stress is relieved.

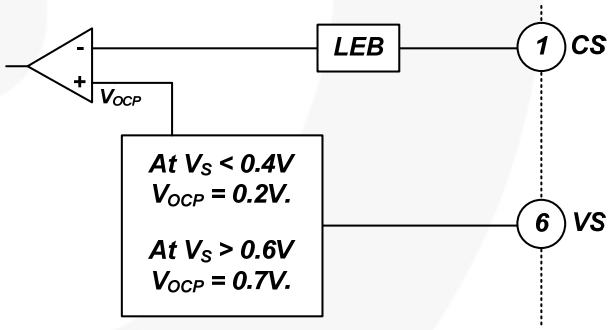

Figure 12. Internal OCP Block

Figure 13 shows operational waveforms at short-LED condition. Output voltage is quickly lowered to 0V right after the LED-short event. Then, the reflected auxiliary voltage is also 0V making V_S voltage less than 0.4V. 0.2V OCP level limits primary-side current and V_{DD} hiccups up and down in between UVLO hysteresis.

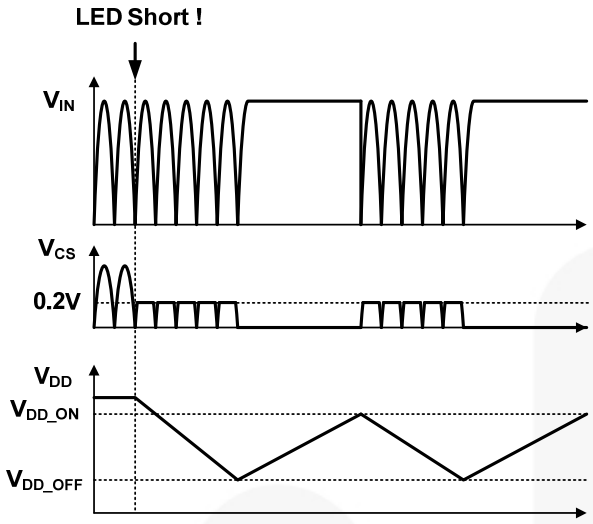

Figure 13. Waveforms at Short-LED Condition

At short-LED condition, V_S is low due to low output voltage. Then, OCP level is changed to 0.2V to reduce output current.

Over-Voltage Protection (OVP)

The OVP prevents damage in over-voltage conditions. If the V_{DD} voltage exceeds 23V at open-loop feedback condition, the OVP is triggered and the PWM switching is disabled. At open-LED condition, V_{DD} reaches V_{DD_OVP}. Then, auto-restart sequence causes a delay, limiting output voltage.

Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output if the junction temperature exceeds 150°C. There is hysteresis of 10°C.

Design Procedure

In this section, a design procedure a of single-stage flyback using FL7732 is presented using the schematic of Figure 1 as a reference. An offline LED driver with 16.8W (24V/0.7A) output has been selected as a design example. The design specifications are as follows:

- Input voltage range: 90 ~ 264V_{AC} and 50 ~ 60Hz
- Nominal output voltage and current: 24V/0.7A
- Minimum efficiency: 87%
- Maximum switching frequency: 65kHz

Step 1. Inductor Selection (L_m)

FL7732 operates with constant turn-on and turn-off time, as shown Figure 14. When MOSFET turn-on time (t_{ON}) and switching period (t_S) are constant, I_{IN} is proportional to V_{IN} and can implement high power factor.

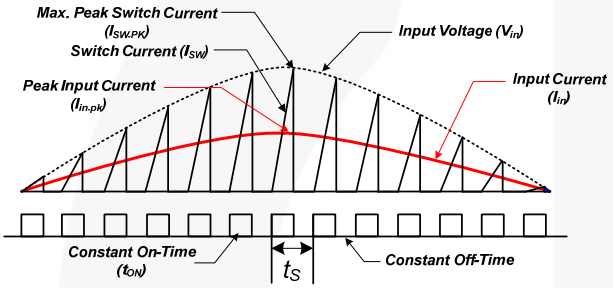

Figure 14. Theoretical Waveform

The single-stage flyback using FL7732 is assumed to operate in DCM due to constant t_{ON} and t_S. Input voltage is applied across the magnetizing inductance (L_m) during t_{ON}, charging the magnetic energy in L_m. Therefore, the maximum peak switch current ($I_{SW.pk}$) of MOSFET occurs at peak point of line voltage, as shown Figure 14. The peak input current ($I_{IN.pk}$) is also shown at the peak input voltage of one line cycle. Once the maximum t_{ON} is decided, $I_{SW.pk}$ of MOSFET is obtained at the minimum line input voltage and full-load condition as:

$$I_{SW.pk} = \frac{t_{ON} \cdot V_{IN.\min pk}}{L_m} \quad (2)$$

where $V_{IN.min.pk}$ and t_{ON} are the peak input voltage and the maximum turn-on time at the minimum line input voltage, respectively.

Using equation 2, the peak input current is obtained by:

$$I_{IN.pk} = \frac{1}{2} \cdot (t_{ON}) \left(\frac{V_{IN.\min.pk}}{Lm} \cdot t_{ON} \right) \cdot f_S \quad (3)$$

then $I_{IN.pk}$ and $V_{IN.min.pk}$ can be expressed as:

$$I_{IN.pk} = \sqrt{2} \cdot I_{IN.rms} \quad (4)$$

$$V_{IN.\min.pk} = \sqrt{2} \cdot V_{IN.rms} \quad (5)$$

where the $I_{IN.rms}$ and $V_{IN.rms}$ are rms line input current and voltage, respectively.

t_{ON} is required to calculate reasonable L_m value. With Equation (2) ~ (5), the turn-on time, t_{ON}, is obtained as:

$$t_{ON}^{\ 2} = \frac{2L_m \cdot I_{IN.rms}}{V_{IN.rms} \cdot f_s} \quad (6)$$

The input power is given as:

$$P_{IN} = I_{IN.rms} \cdot \frac{P_O}{\eta} \quad (7)$$

With Equation (6) and (7), the L_m value is obtained as:

$$Lm = \frac{\eta \cdot (V_{IN.rms})^2 \cdot f_s \cdot t_{ON}^{\ 2}}{2P_O} \quad (8)$$

(Design Example) Since the minimum input voltage is 90V_{AC}, the maximum t_{ON} occurs at full-load condition. Assuming the maximum t_{ON} is 7.4μs at 65kHz of the maximum frequency, the magnetizing inductance is obtained as:

$$L_m = \frac{0.87 \times 90^2 \times 65 \times 10^3 \times (7.4 \times 10^{-6})^2}{2 \times 16.8} = 743\mu H$$

The maximum peak current of MOSFET at nominal output power is calculated as:

$$I_{SW.pk} = \frac{7.4 \times 10^{-6} \times \sqrt{2} \times 90}{743 \times 10^{-6}} = 1.26A$$

Step 2. Sensing Resistor and n_{PS} Selection

Since FL7732 adopts TRUECURRENT® Calculation method to regulate constant output current (I_O), as defined in equation 1. The output current is proportional to turn ratio n_{ps} between the primary and secondary windings of the transformer and inversely proportional to sensing resistor (R_S). The FL7732 also implements cycle-by-cycle current limitation by detecting V_{CS} to protect system from output short or overload. Therefore, V_{CS} level to handle rated system power without the current limitation should be considered. It is typical to set the cycle-by-cycle limit level (typical: 0.67V) at 20~30% higher than CS peak voltage ($V_{CS.pk}$) at full-load condition. MOSFET peak current ($I_{SW.pk}$) is converted into $V_{CS.pk}$ as:

$$V_{CS.pk} = I_{SW.pk} \cdot R_S \quad (9)$$

According to Equation (1), the transformer turn ratio is determined by the sensing resistor and nominal output current as:

$$n_{ps} = 10.5 \times I_O \times R_S \quad (10)$$

where:

$$\frac{1}{2} \cdot \frac{t_{DIS}}{t_S} \cdot V_{CS} = \frac{1}{10.5} \quad (11)$$

(Design Example) Once $V_{CS,pk}$ is set as 0.5V, the sensing resistor value is obtained as:

$$R_S = \frac{V_{CS.pk}}{I_{SW.PK}} = \frac{0.5}{1.26} = 0.396$$

$$n_{ps} = 10.5 \times 0.7 \times 0.396 = 2.91$$

Step 3. n_{AS} Selection

When V_{DD} voltage is 23V, FL7732 stops switching operation due to over-voltage protection (OVP). So n_{AS} can be determined as follows:

$$n_{AS} = \frac{V_{DD.OVP}}{V_{O.OVP}} = \frac{23}{V_{O.OVP}} \quad (12)$$

where (n_{AS}=N_A/N_S) is the turns ratio the of secondary to auxiliary of transformer. Therefore, $V_{O.OVP}$ can be set by changing the n_{AS} value.

(Design Example) Once output over-voltage level is set as 30V, n_{AS} is obtained as:

$$n_{AS} = \frac{23}{30} = 0.77$$

Step 4. Resistor Selection (R_{VS1} and R_{VS2})

The first consideration for R_{VS1} and R_{VS2} selection is that V_S is 2.35V at the end of diode current conduction time to operate at maximum switching frequency at rated power. The second consideration is V_S blanking, as explained below. The output voltage is detected by auxiliary winding and a resistive divider connected to the VS pin, as shown in Figure 7. However, in a single-stage flyback without DC link capacitor, auxiliary winding voltage cannot be clamped to reflected output voltage due to the small L_m current, which induces V_S voltage sensing error. Then, frequency decreases rapidly at the zero-crossing point of line voltage, which can cause flicker. To maintain constant frequency over the whole sinusoidal line voltage, FL7732 has V_S blanking to disable sampling of V_S voltage at less than a particular line voltage by sensing the auxiliary winding.

Considering the maximum switching frequency at rated power and V_S blanking level, R_{VS1} and R_{VS2} are obtained as:

$$R_{VS} = \frac{(V_O + V_F) n_{AS} - V_{VS \cdot \max}}{V_{VS \cdot \max}} \quad (13)$$

$$R_{VS1} = r_{VS} \cdot R_{VS2} \quad (14)$$

where $V_{VS.max}$ is the V_S value to set the maximum switching frequency for constant output current in rated power and V_F is secondary diode forward voltage.

$$R_{VS2} = \frac{1}{100 \times 10^{-6}} \times (0.545 + \frac{0.545 + V_{IN\,bnk} \cdot n_{AP}}{R_{VS}}) \quad (15)$$

where $V_{IN.bnk}$ *and* n_{AP} are the blanking level of input voltage and the turn ratio of auxiliary to primary, respectively. The n_{AP} can be calculated as the ratio of n_{AS} to n_{PS}.

(Design Example) The voltage divider network is determined as:

$$R_{VS} = \frac{(24 + 0.7) \times 0.77 - 2.35}{2.35} = 7.06$$

Once $\boldsymbol{V_{IN.bnk}}$ level is set to 50V, R_{VS2} is obtained as.

$$R_{VS2} = \frac{1}{100 \times 10^{-6}} \times (0.545 + \frac{0.545 + 50 \times \frac{0.77}{2.91}}{7.06}) = 24.86k\Omega$$

Then R_{VS1} is determined to be $175.5k\Omega$.

It is recommended to place a bypass capacitor of 10 ~ 30pF closely between the VS pin and the GND pin to bypass the switching noise and keep the accuracy of the V_S sensing for CC regulation. The value of the capacitor affects constant-current regulation. If a high value of V_S capacitor is selected, the discharge time t_{DIS} becomes longer and the output current is lower, compared to small V_S capacitor.

Step 5. Design the Transformer

The number of primary turns is determined by Faraday's law. $N_{p,min}$ is fixed by the peak value of the minimum line input voltage across the primary winding and the maximum on time. The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_{p,\min} = \frac{V_{IN.\min.pk} \cdot t_{ON}}{B_{sat} \cdot A_e} \quad (16)$$

where A_e is the cross-sectional area of the core in m^2 and B_{sat} is the saturation flux density in Tesla.

Since the saturation flux density decreases as the temperature rises, the high-temperature characteristics should be considered when it is used in an enclosed case.

(Design Example) An RM8 core is selected for the transformer and the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_{p,\min} = \frac{\sqrt{2} \cdot 90 \times 7.4 \times 10^{-6}}{0.27 \times 64 \times 10^{-6}} = 54.5T$$

Considering the tolerance of the transformer and high ambient temperature, N_P should be selected with a margin about 5% ~ 10% to avoid core saturation:

$$N_p = 54.5 \times 1.1 = 59.95T$$

Once the turn number of the primary side (N_P) is determined as 60T, the turn number of the secondary side (N_S) is obtained by:

$$N_S = 60 \div 2.91 = 20.5T$$

Once the turn number of the secondary side (N_S) is determined as 20T, the auxiliary winding turns (N_A) is obtained by:

$$N_A = 20 \times 0.77 = 15.4T$$

N_A is determined to be 15T.

Step 6. Calculate the Voltage and Current of the Switching Devices

Primary-Side MOSFET: The voltage stress of the MOSFET was discussed when determining the transformer turns ratio. Assuming the drain voltage overshoot is the same as the reflected output voltage, the maximum drain voltage is given as:

$$V_{DS(\max)} = V_{IN.\max.pk} + \frac{N_P}{N_S}(V_o + V_F) + V_{OS} \quad (17)$$

where $V_{in.max.pk}$ is the maximum line peak voltage.

The rms current ($I_{SW.rms}$) though the MOSFET is given as:

$$I_{SW.rms} \approx I_{pk} \cdot \sqrt{\frac{t_{ON} \cdot f_S}{6}} \quad (18)$$

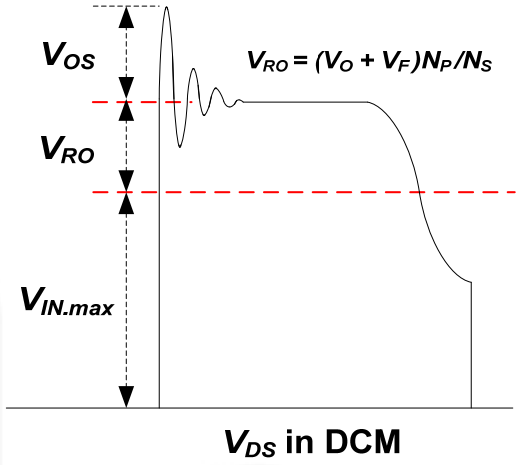

Figure 15. Drain Voltage of MOSFET

(**Design Example**) Assuming that drain voltage overshoot is the same as the reflected output voltage, the maximum drain voltage across the MOSFET is calculated as:

$$V_{DS(\max)} = 374 + \frac{60}{20} \times (24 + 0.7) \times 2 = 522V$$

The rms current though the MOSFET is

$$I_{SW.rms} \approx 1.26 \times \sqrt{\frac{7.4 \times 0.065}{6}} = 0.357A$$

Secondary-Side Diode: The maximum reverse voltage and rms current of the rectifier diode are obtained as:

$$V_D = V_O + \frac{N_S}{N_P} \cdot V_{in.\max.pk} \quad (19)$$

$$I_{D.rms} \approx I_{SW.rms} \times \sqrt{\frac{V_{in.\min.pk}}{2 \times V_{RO}}} \cdot \frac{N_P}{N_S} \quad (20)$$

(**Design Example**) The diode voltage and current are obtained as:

$$V_D = 24 + \frac{20}{60} \times 374 = 148.7V$$

$$I_{D.rms} \approx 0.357 \times \sqrt{\frac{127}{2 \times 74.1}} \cdot \frac{60}{20} = 0.991A$$

Step 7. Design RCD Snubber in Primary Side

When the power MOSFET is turned off, there is a high-voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of the device. Therefore, it is necessary to use an additional network to clamp the voltage. The RCD snubber circuit and its waveform are shown in Figure 16 and Figure 17, respectively. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode (D_{SN}) once the MOSFET drain voltage exceeds the cathode voltage of snubber diode. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle. The snubber capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable for these reasons.

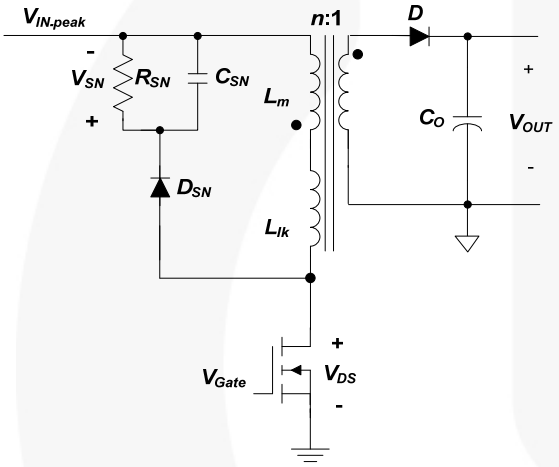

Figure 16. Snubber Circuit

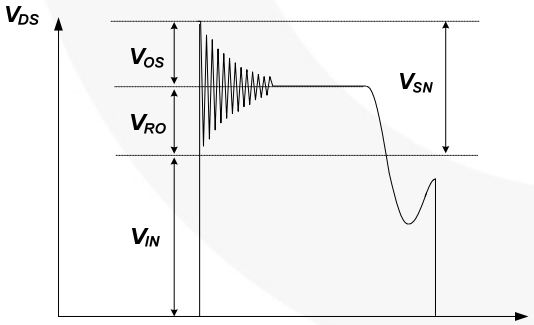

Figure 17. Snubber Waveforms

Snubber capacitor voltage at full-load condition is given as:

$$V_{SN} = V_{RO} + V_{OS} \tag{21}$$

The power dissipated in the snubber network is obtained as:

$$P_{SN} = \frac{V_{SN}^{\ 2}}{R_{SN}} = \frac{1}{2} L_{lk} \cdot I_{PK}^{\ 2} \cdot \frac{V_{SN}}{V_{SN} - V_{RO}} \cdot f_S \tag{22}$$

where L_{lk} is leakage inductance, V_{SN} is the snubber capacitor voltage at full load, and R_{SN} is the snubber resistor.

The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted. Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_S} \tag{23}$$

In general, 5 ~ 20% ripple of the selected capacitor voltage is reasonable. In this snubber design, neither the lossy discharge of the inductor nor stray capacitance is considered.

(**Design Example**) Since the voltage overshoot of drain voltage has been determined to be the same as the reflected output voltage, the snubber voltage is:

$$V_{SN} = V_{RO} + V_{OS} = 150V$$

The leakage inductance is measured as 10μH. Then the loss in snubber networking is given as:

$$P_{SN} = \frac{1}{2} 10 \times 10^{-6} \times 1.26^2 \times \frac{150}{150 - 75} \times 65 \times 10^3 = 1.03W$$

$$R_{SN} = \frac{150^2}{1.03} = 21.84k\Omega$$

To allow 7% ripple on the snubber voltage (150V):

$$C_{SN} = \frac{150}{0.07 \times 150 \times 21.84 \cdot 10^3 \times 65 \cdot 10^3} = 10.06nF$$

Lab Notes

1. Before modifying or soldering/desoldering the power supply, discharge the primary capacitors through the external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high-voltage during the process. This device is sensitive to electrostatic discharge (ESD). To improve the yield, the production line should be ESD protected as required by ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1 standards.
2. In case of LED-short condition, V_{DD} voltage charged at V_{DD} capacitor should touch V_{DD} off level rapidly to stop switching. Therefore, V_{DD} capacitor value is recommended under 22µF.

Schematic of Design example

Figure 18 shows the schematic of the 16.8W LED driver design example. RM8 core is used for the transformer. Figure 19 shows the transformer information.

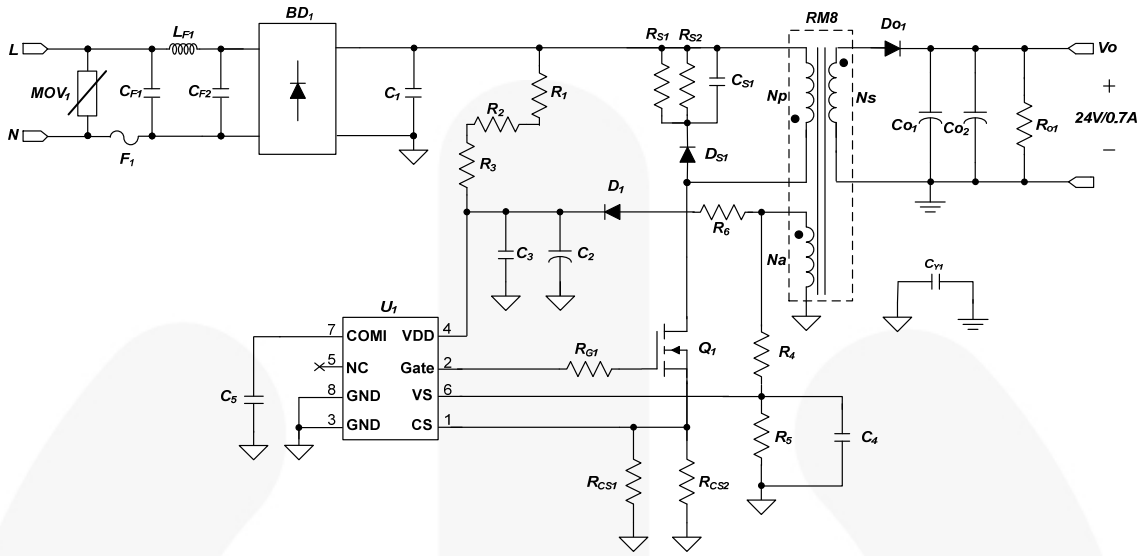

Figure 18. Schematic of the FL7732 17W Design Example

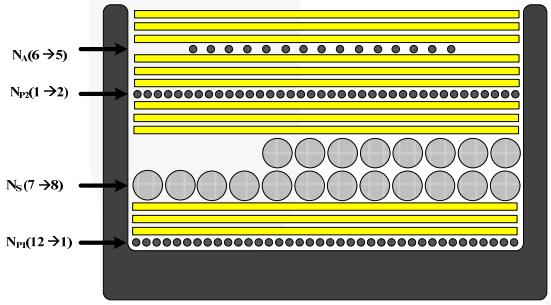

Figure 19. Transformer Winding Structure

No.	Winding	Pin (S → F)	Wire	Turns	Winding Method
1	NP1	12 → 1	0.25φ	30 Ts	Solenoid Winding
2	Insulation: Polyester Tape t = 0.025mm, 3-Layer				
3	NS	7- → 8	0.5φ (TIW)	20 Ts	Solenoid Winding
4	Insulation: Polyester Tape t = 0.025mm, 3-Layer				
5	NP2	1 → 2	0.25φ	30 Ts	Solenoid Winding
6	Insulation: Polyester Tape t = 0.025mm, 3-Layer				
7	NA	6 → 5	0.25φ	15 Ts	Solenoid Winding
8	Insulation: Polyester Tape t = 0.025mm, 3-Layer				

	Pin	Specification	Remark
Inductance	12– 2	750μH ± 10%	60kHz, 1V
Leakage	1– 2	6μH	60kHz, 1V Short All Output Pins

Bill of Materials

Item No.	Part Reference	Part Number	Qty	Description	Manufacturer
1	BD1	DF06S	1	1.5A/600V Bridge Diode	Fairchild
2	CF1	MPX AC275V 104K	1	104/AC275V X-Capacitor	Carli
3	CF2	MPX AC275V 473K	1	473/AC275V X-Capacitor	Carli
4	CS1	C1206C103KDRACTU	1	103/1kV SMD Capacitor 3216	Kemet
5	CY1	SCFz2E472M10BW	1	472/250V Y-Capacitor	Samwha
6	CO1,CO2	KMG 470µF/35V	2	470uF/35V Electrolytic Capacitor	Samyoung
7	C1	MPE 630V104K 14S	1	104/630V MPE Film Capacitor	Sungho
8	C2	KMG 22µF/50V	1	22uF/35V Electrolytic Capacitor	Samyoung
9	C3	C0805C104K5RACTU	1	104/50V SMD Capacitor 2012	Kemet
10	C4	C0805C200J5GACTU	1	200/50V SMD Capacitor 2012	Kemet
11	C5	C0805C225Z3VACTU	1	225/25V SMD Capacitor 2012	Kemet
12	DS1	RS1M	1	1000V/1A Ultra Fast Recovery Diode	Fairchild
13	Do1	ES3D	1	200V/3A, Fast Rectifier	Fairchild
14	D1	1N4003	1	200V/1A, General Purpose Rectifier	Fairchild
15	F1	SS-5-1A	1	250V/1A Fuse	Bussmann
16	LF1	R10402KT00	1	4mH Inductor, 10Ø	Bosung
17	MOV1	SVC 471 D-07A	1	Metal Oxide Varistor	Samwha
18	Q1	FDD5N60NZ	1	600V/4A, N-Channel MOSFET	Fairchild
19	RG1, R6	RC1206JR-0710L	2	10Ω SMD Resistor 3216	Yageo
20	RS1,RS2	RC1206JR-07100KL	2	100kΩ SMD Resistor 3216	Yageo
21	RCS1,RCS2	RC1206JR-071RL	2	1Ω SMD Resistor 3216	Yageo
22	RCS3	RC1206JR-072R4L	1	2.4Ω SMD Resistor 3216	Yageo
23	RO1	RC1206JR-0720KL	1	20KΩ SMD Resistor 3216	Yageo
24	R4	RC1206JR-07150KL	1	150KΩ SMD Resistor 3216	Yageo
25	R1,R2,R3	RC1206JR-0768KL	3	68KΩ SMD Resistor 3216	Yageo
26	R5	RC1206JR-0724KL	1	24KΩ SMD Resistor 3216	Yageo
27	T1	RM8 Core	1	12pin, Transformer	TDK
28	U1	FL7732M_F116	1	Main PSR Controller	Fairchild

Related Datasheets

FL7732 — Single-Stage PFC Primary-Side-Regulation Offline LED Driver

Reference Designs — http://www.fairchildsemi.com/referencedesign/