OPA810 Low-Power, Rail-to-Rail Input/Output, FET-Input Operational Amplifier

1 Features

- Gain-bandwidth product: 70 MHz
- Small-signal bandwidth: 125 MHz
- Slew rate: 192 V/µs
- Wide supply range: 4.75 V to 27 V
- Low noise:
  - Input voltage noise: 6 nV/√Hz (f = 500 kHz)
  - Input current noise: 5 fA/√Hz (f = 10 kHz)
- Rail-to-rail input and output:
  - FET input stage: 2-pA input bias current (typical)
  - High linear output current: 75 mA
- Input offset: ±1.5 mV (maximum)
- Offset drift: ±1.5 µV/°C (typical)
- Low power: 3.7 mA/channel
- Extended temperature operation: –40°C to +125°C
- Dual-channel version: OPA2810

2 Applications

- Wideband photodiode transimpedance amplifiers
- Analog input/output modules
- Impedance measurements
- Power analyzers and meters
- High-Z voltage and current measurements
- Multichannel sensor interfaces
- Level shifting and buffering
- Optoelectronic drivers

3 Description

The OPA810 is a single-channel, field-effect transistor (FET)-input, voltage-feedback operational amplifier with low input bias current. The OPA810 is unity-gain stable with a small-signal, unity-gain bandwidth of 125 MHz, and offers excellent DC precision and dynamic AC performance at a low quiescent current (I_Q) of 3.7 mA per channel (typical). The OPA810 is fabricated on Texas Instrument's proprietary, high-speed SiGe BiCMOS process and achieves significant performance improvements over comparable FET-input amplifiers at similar levels of quiescent power. With a gain-bandwidth product (GBWP) of 70 MHz, slew rate of 192 V/µs, and low-noise voltage of 6 nV/√Hz, the OPA810 is well suited for use in a wide range of high-fidelity data acquisition and signal processing applications.

The OPA810 is characterized to operate over a wide supply range of 4.75 V to 27 V, and features rail-to-rail inputs and outputs. The OPA810 amplifier delivers 75 mA of linear output current, suitable for driving optoelectronics components and analog-to-digital converter (ADC) inputs or buffering digital-to-analog converter (DAC) outputs into heavy loads.

The OPA810 is available in an 8-pin SOIC package and is rated over the extended industrial temperature range of –40°C to +125°C. The OPA2810 is a dual-channel variant of this device, available in 8-pin SOIC, SOT23, and VSSOP packages.

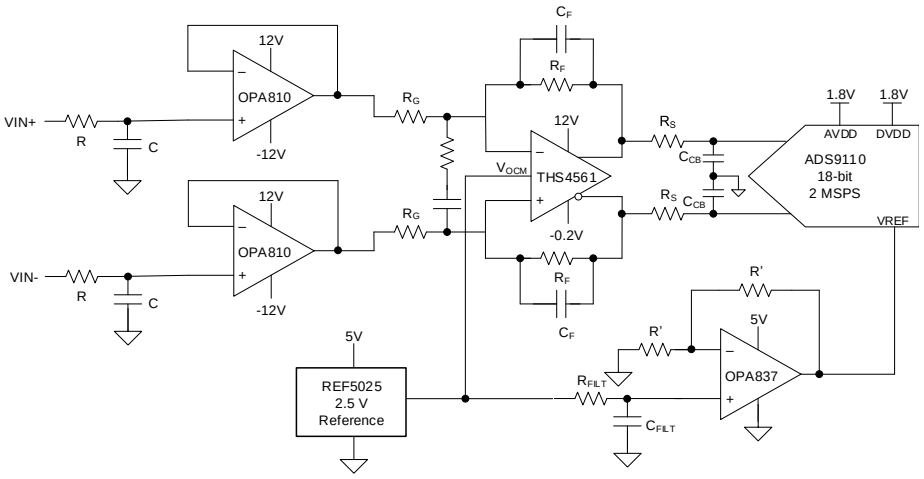
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA810	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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High-Z Input Data Acquisition Front-End



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2019	*	Initial release.

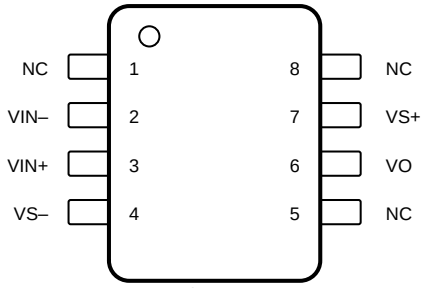
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5 Device Comparison Table

DEVICE	$V_{S\pm}$ (V)	I_Q/CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA810	±12	3.7	70	192	6	Unity-gain stable FET input
THS4631	±15	13	210	900	7	Unity-gain stable FET input
OPA656	±6	14	230	290	7	Unity-gain stable FET input
OPA818	±6.5	27.7	2700	1400	2.2	Gain of 7 stable FET input
OPA659	±6	32	350	2550	8.9	Unity-gain stable FET input

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
NC	1	–	No internal connection
VIN–	2	I	Inverting input pin
VIN+	3	I	Noninverting input pin
VS–	4	P	Negative power supply pin
NC	5	–	No internal connection
VO	6	O	Output pin
VS+	7	P	Positive power supply pin
NC	8	–	No internal connection

(1) I = input, O = output, and P = power.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage (total bipolar supplies)(2)			±14	V
V_{IN}	Input voltage		$V_{S–}$ – 0.5	V_{S+} + 0.5	V
$V_{IN,Diff}$	Differential input voltage(3)			±7	V
I_I	Continuous input current			±10	mA
I_O	Continuous output current(4)	T_A = –40℃ to +85℃		±40	mA
		T_A = 125℃		±12	mA
P_D	Continuous power dissipation		See *Thermal Information*		
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_S is the total supply voltage given by $V_S = V_{S+} – V_{S–}$.
(3) Equal to the lower of ±7 V or total supply voltage.
(4) Long-term continuous output current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	4.75		27	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA810 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics: 10 V

Test conditions unless otherwise noted: T_A = 25°C, V_{S+} = 5 V, $V_{S–}$ = –5 V, R_L = 1 kΩ, input and output are biased to midsupply(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
AC PERFORMANCE							
SSBW	Small-signal bandwidth	G = 1, V_O = 20 mV_{PP}, R_F = 0 Ω		120		MHz	C
		G = 1, V_O = 20 mV_{PP}, R_F = 0 Ω, C_L = 10 pF		125			C
		G = –1, V_O = 20 mV_{PP}		60			C
LSBW	Large-signal bandwidth	G = 2, V_O = 2 V_{PP}		38		MHz	C
GBWP	Gain-bandwidth product	G = 11, V_O = 20 mV_{PP}		70		MHz	C
	Bandwdith for 0.1-dB flatness	G = 2, V_O = 20 mV_{PP}		13		MHz	C
SR	Slew rate (20%-80%)(3)	G = 2, V_O = –2-V to 2-V step		192		V/µs	C
	Settling time to 0.1%	G = 2, V_O = 2-V step		47		ns	C
		G = 2, V_O = 8-V step		65			C
	Settling time to 0.001%	G = 2, V_O = 2-V step		330		ns	C
		G = 2, V_O = 8-V step		230			C
HD2	Second-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–118		dBc	C
		f = 1 MHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–99			C
HD3	Third-order harmonic distortion	f = 100 kHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–134		dBc	C
		f = 1 MHz, R_L = 1 kΩ, V_O = 2 V_{PP}		–104			C
e_n	Input-referred voltage noise	f = 500 kHz, flatband		6		nV/√Hz	C
e_i	Input-referred current noise	f = 10 kHz		5		fA/√Hz	C
z_O	Closed-loop output impedance	f = 100 kHz		0.007		Ω	C
DC PERFORMANCE							
A_{OL}	Open-loop voltage gain	f = DC, V_O = ±2.5 V	108	120		dB	A
V_{OS}	Input offset voltage			0.1	1.5	mV	A
	Input offset voltage drift	T_A = –40°C to +125°C		1.5		µV/°C	B
	Input bias current			2	20	pA	A
	Input offset current			1	20	pA	A
CMRR	Common-mode rejection ratio	f = DC, V_{CM} = –3 V to 1 V	83	100		dB	A
INPUT							
	Allowable input differential voltage			±7		V	C
	Common-mode input impedance	In closed-loop configuration		12 || 2.5		GΩ||pF	C
	Differential input capacitance	In open-loop configuration		0.5		pF	C
	Most positive input voltage	ΔV_{OS} < 5 mV(4)	V_{S+} + 0.2	V_{S+} + 0.3		V	A
	Most negative input voltage	ΔV_{OS} < 5 mV(4)	$V_{S–}$ – 0.2	$V_{S–}$ – 0.3		V	A
	Most positive input voltage for main-JFET stage			V_{S+} – 2.5		V	C
OUTPUT							
V_{OCRH}	Output voltage range high	R_L = 667 Ω	V_{S+} – 0.18	V_{S+} – 0.11		V	A
V_{OCRL}	Output voltage range low	R_L = 667 Ω		$V_{S–}$ + 0.08	$V_{S–}$ + 0.15	V	A

(1) For AC specifications, G = 2 V/V, R_F = 1 kΩ and C_L = 4.7 pF (unless otherwise noted).
(2) Test levels (all values set by characterization and simulation): (A) 100% tested at 25°C, overtemperature limits by characterization and simulation; (B) Not tested in production, limits set by characterization and simulation; (C) Typical value only for information.
(3) Lower of the measured positive and negative slew rate.
(4) Change in input offset from its value when input is biased to midsupply.

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Electrical Characteristics: 10 V (continued)

Test conditions unless otherwise noted: T_A = 25°C, V_{S+} = 5 V, $V_{S–}$ = –5 V, R_L = 1 kΩ, input and output are biased to midsupply(1).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
$I_{O(max)}$	Linear output drive (sourcing and sinking)	V_O = 2.65 V, R_L = 51 Ω, ΔV_{OS} < 1 mV	52	75		mA	A
I_{SC}	Output short-circuit current	t_{Delay} = 5 ms		100		mA	B
C_L	Capacitive load drive	< 3-dB peaking, R_S = 0 Ω		10		pF	C
POWER SUPPLY							
V_S	Operating voltage		4.75		27	V	A
I_Q	Quiescent current per channel		3.125	3.7	4.05	mA	A
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(5)	82	100		dB	A
AUXILIARY CMOS INPUT STAGE							
	Gain-bandwidth product	V_{CM} = (V_{S+}) – 1 V		27		MHz	C
	Open-loop voltage gain	V_{CM} = (V_{S+}) – 1 V, f = DC, ΔV_O = 4 V	80	100		dB	A
	Input-referred voltage noise	V_{CM} = V_{S+} – 1V, f = 1 MHz		21		nV/√Hz	C
	Input offset voltage	V_{CM} = V_{S+} – 1.5 V, no load			4	mV	A
	Input bias current	V_{CM} = V_{S+} – 1.5 V		2	20	pA	A

(5) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

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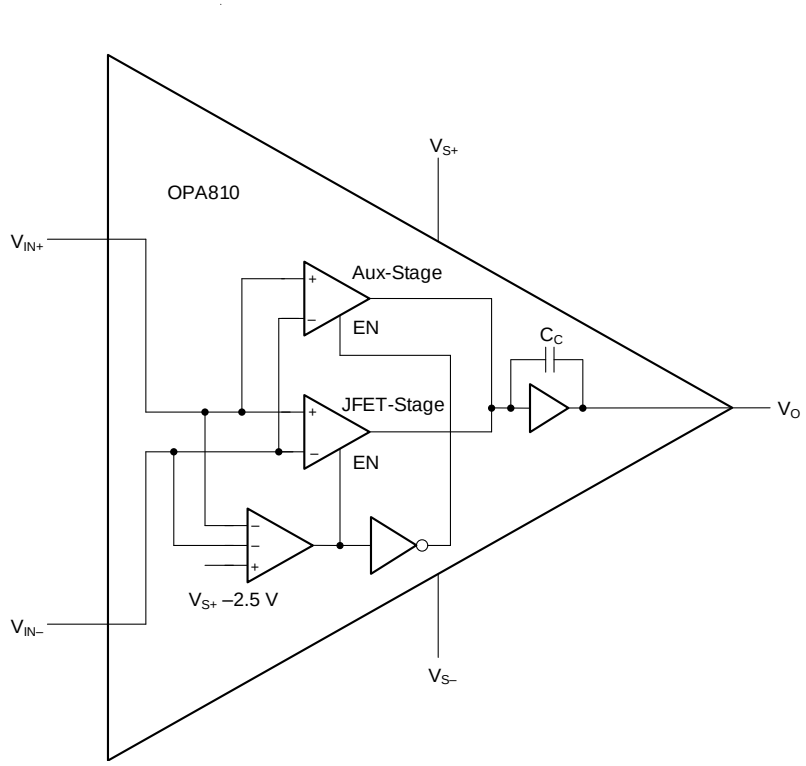
8 Detailed Description

8.1 Overview

The OPA810 is a single-channel, field-effect transistor (FET)-input, unity-gain stable, voltage-feedback operational amplifier with extremely low input bias current across its common-mode input voltage range. The OPA810, characterized to operate over a wide supply range of 4.75 V to 27 V, has a small-signal, unity-gain bandwidth of 125 MHz and offers both excellent DC precision and dynamic AC performance at low quiescent power. The OPA810 is fabricated on Texas Instrument's proprietary, high-speed SiGe BiCMOS process and achieves significant performance improvements over comparable FET-input amplifiers at similar levels of quiescent power. With a gain-bandwidth product (GBWP) of 70 MHz, extremely high slew rate (190 V/µs), and low noise (6 nV/√Hz), the OPA810 is ideal in a wide range of data acquisition and signal processing applications. The OPA810 includes input clamps to allow maximum input differential voltage of up to 7 V, making the device suitable for use with multiplexers and for processing signals with fast transients. The device achieves these benchmark levels of performance while consuming a typical quiescent current (I_Q) of 3.7 mA per channel.

The OPA810 can source and sink large amounts of current without degradation in its linearity performance. The wide bandwidth of the OPA810 implies that the device has low output impedance across a wide frequency range, thereby allowing the amplifier to drive capacitive loads up to 10 pF without requiring output isolation. This device is suitable for a wide range of data acquisition, test and measurement front-end buffer, impedance measurement, power analyzer, wideband photodiode transimpedance, and signal processing applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 OPA810 Architecture

The OPA810 features a true high-impedance input stage including a JFET differential-input pair main stage and a CMOS differential-input auxiliary (aux) stage operational within 2.5 V of the positive supply voltage. The bias current is limited to a maximum of 20 pA throughout the common-mode input range of the amplifier. The *Functional Block Diagram* section provides a block diagram representation for the input stage of the OPA810. The amplifier exhibits superior performance for high-speed signals (distortion, noise, and input offset voltage)

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Feature Description (continued)

while the aux stage enables rail-to-rail inputs and prevents phase reversal. The OPA810 also includes input clamps that enable the maximum input differential voltage of up to 7 V (lower of 7 V and total supply voltage). This architecture offers significantly greater differential input voltage capability as compared to one to two times the diode forward voltage drop maximum rating in standard amplifiers, and makes this device suitable for use with multiplexers and processing of signals with fast transients. The input bias currents are also clamped to maximum 300 µA, which does not load the previous driver stage or require current-limiting resistors (except when limiting current through the input ESD diodes when input common-mode voltages are greater than the supply voltages). This feature also enables the use of one of the channels as a comparator in systems that require an amplifier and a comparator for signal gain and fault detection, respectively. For the lowest offset, distortion, and noise performance, limit the common-mode input voltage to the main JFET-input stage (greater than 2.5 V away from the positive supply).

As Figure 1 shows, an amplifier phase margin reduces and becomes unstable when driving a capacitive load (C_L) at its output. Using a series resistor (R_S) between the amplifier output and load capacitance introduces a zero that cancels the pole formed by the amplifier output impedance and C_L in the open-loop transfer function. The OPA810 drives capacitive loads of up to 10 pF without causing instability. Using a series resistor for larger load capacitance values is recommended.

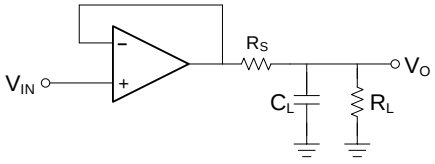


Figure 1. OPA810 Driving Capacitive Load

8.3.2 ESD Protection

As Figure 2 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous input and output currents. The differential input clamps only limit the bias current when the input common-mode voltages are within the supply voltage range, whereas current-limiting series resistors must be added at the inputs if common-mode voltages higher than the supply voltages are possible. Keep these resistor values as low as possible because using high values degrades noise performance and frequency response.

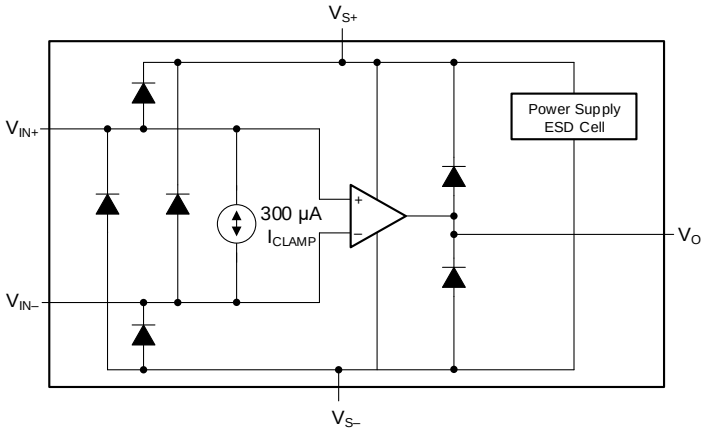


Figure 2. Internal ESD Protection

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8.4 Device Functional Modes

8.4.1 Split-Supply Operation (±2.375 V to ±13.5 V)

To facilitate testing with common lab equipment, the OPA810 can be configured to allow for split-supply operation (see the *OPA2810DGK Evaluation Module* user guide). This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers, and other lab equipment reference the inputs and outputs to ground. Figure 3 depicts the OPA810 configured as a noninverting amplifier and Figure 4 illustrates the OPA810 configured as an inverting amplifier. For split-supply operation referenced to ground, the power supplies V_{S+} and V_{S-} are symmetrical around ground and V_{REF} is at GND. Split-supply operation is preferred in systems where the signals swing around ground because of the ease-of-use; however, the system requires two supply rails.

8.4.2 Single-Supply Operation (4.75 V to 27 V)

Many newer systems use a single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA810 can be used with a single supply (with the negative supply set to ground) with no change in performance if the input and output are biased within the linear operation of the device. To change the circuit from split supply to a balanced, single-supply configuration, level shift all voltages by half the difference between the power-supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of PSRR are minimized because the low-supply rail is grounded. See the *Single-Supply Op Amp Design Techniques* application report for examples of single-supply designs.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Amplifier Gain Configurations

The OPA810 is a classic voltage-feedback amplifier with each channel having two high-impedance inputs and a low-impedance output. Standard application circuits (as shown in Figure 3 and Figure 4) include the noninverting and inverting gain configurations. The DC operating point for each configuration is level-shifted by the reference voltage V_{REF} that is typically set to midsupply in single-supply operation. V_{REF} is often connected to ground in split-supply applications.

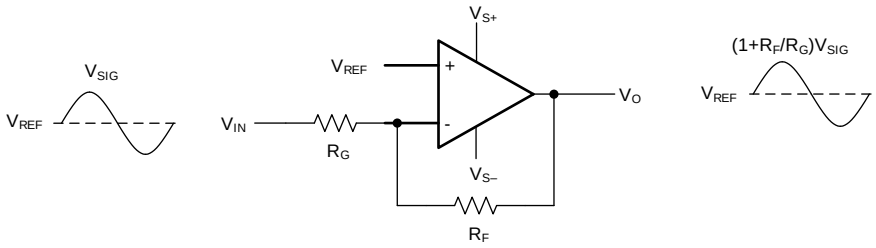


Figure 3. Noninverting Amplifier

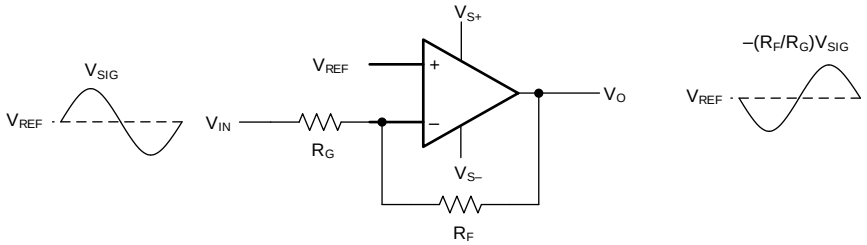


Figure 4. Inverting Amplifier

Equation 1 shows the closed-loop gain of an amplifier in a noninverting configuration.

$$V_O = V_{IN}\left(1+\frac{R_F}{R_G}\right)+V_{REF} \quad (1)$$

Equation 2 shows the closed-loop gain of an amplifier in an inverting configuration.

$$V_O = V_{IN}\left(-\frac{R_F}{R_G}\right)+V_{REF} \quad (2)$$

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9.2 Typical Applications

9.2.1 Transimpedance Amplifier

The high GBWP and low input voltage and current noise for the OPA810 make the device an ideal wideband transimpedance amplifier for moderate to high transimpedance gains.

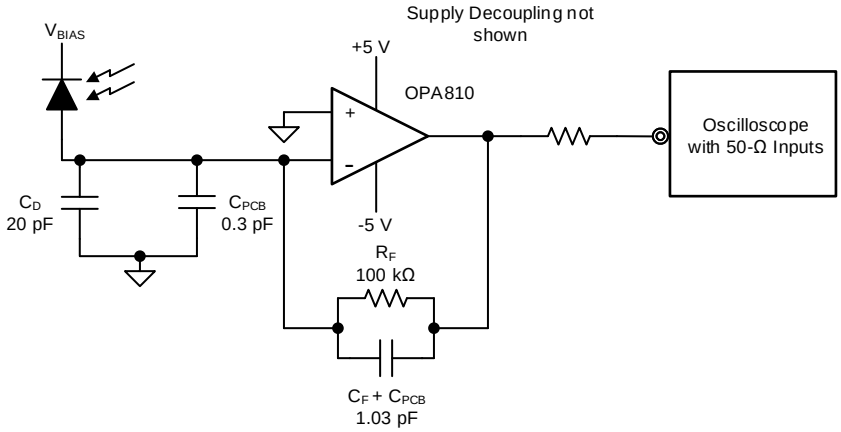


Figure 5. Wideband, High-Sensitivity, Transimpedance Amplifier

9.2.1.1 Design Requirements

Table 1 lists the design requirements for a high-bandwidth, high-gain transimpedance amplifier circuit.

Table 1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Target bandwidth	> 2 MHz
Transimpedance gain	100 kΩ
Photodiode capacitance	20 pF

9.2.1.2 Detailed Design Procedure

Designs that require high bandwidth from a large area detector with relatively high transimpedance gain benefit from the low input voltage noise of the OPA810. This input voltage noise is peaked up over frequency by the diode source capacitance, and can (in many cases) become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage (V_{BIAS}) applied, the desired transimpedance gain, R_F, and the GBWP for the OPA810 (70 MHz). Figure 5 shows a transimpedance circuit with the parameters as described in Table 1. With these three variables set (and including the parasitic input capacitance for the OPA810 and the printed circuit board (PCB) added to C_D), the feedback capacitor value (C_F) can be set to control the frequency response. The *Transimpedance Considerations for High-Speed Amplifiers* application report discusses using high-speed amplifiers for transimpedance applications. Set the feedback pole according to Equation 3 in order to achieve a maximally-flat second-order Butterworth frequency response:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBWP}{4\pi R_F C_D}} \tag{3}$$

The input capacitance of the amplifier is the sum of the common-mode and differential capacitance (2.5 + 0.5) pF. The parasitic capacitance from the photodiode package and the PCB is approximately 0.3 pF. Using gives a total input capacitance of C_D = 23.3 pF. From Equation 3, set the feedback pole at 1.55 MHz. Setting the pole at 1.55 MHz requires a total feedback capacitance of 1.03 pF.

Equation 4 shows the approximate –3-dB bandwidth of the transimpedance amplifier circuit:

$$f_{-3dB} = \sqrt{GBWP / (2\pi R_F C_D)} Hz \tag{4}$$

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Equation 4 estimates a closed-loop bandwidth of 2.19 MHz. Figure 6 and Figure 7 show the loop-gain magnitude and phase plots from the TINA-TI simulations of the transimpedance amplifier circuit of Figure 5. The 1/β gain curve has a zero from R_F and C_{IN} at 70 kHz and a pole from R_F and C_F cancelling the 1/β zero at 1.5 MHz, resulting in a 20-dB per decade rate-of-closure at the loop-gain crossover frequency (the frequency where A_{OL} equals 1/β), ensuring a stable circuit. A phase margin of 62° is obtained with a closed-loop bandwidth of 3 MHz and a 100-kΩ transimpedance gain.

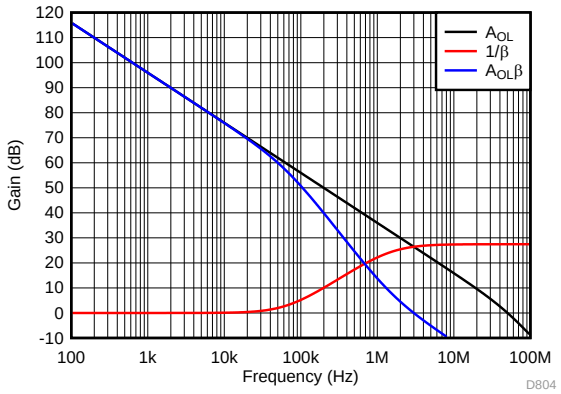


Figure 6. Loop-Gain Magnitude vs Frequency for the Transimpedance Amplifier Circuit of Figure 5

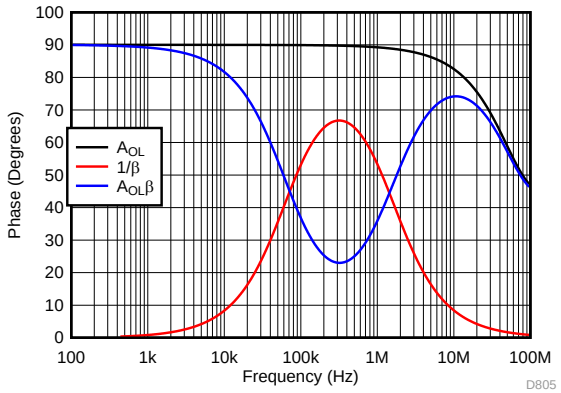


Figure 7. Loop-Gain Phase vs Frequency for the Transimpedance Amplifier Circuit of Figure 5

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9.2.2 Multichannel Sensor Interface

High-Z input amplifiers are particularly useful when interfaced with sensors that have relatively high output impedance. Such multichannel systems usually interface these sensors with the signal chain through a multiplexer. Figure 8 shows one such implementation using an amplifier for the interface with each sensor, and driving into an ADC through a multiplexer. An alternate circuit, shown in Figure 9, can use a single higher GBWP and fast-settling amplifier at the output of the multiplexer. This architecture gives rise to large signal transients when switching between channels, where the settling performance of the amplifier and maximum allowed differential input voltage limits signal chain performance and amplifier reliability, respectively.

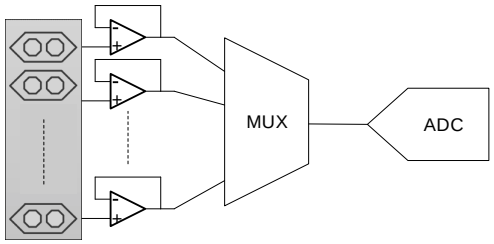


Figure 8. Multichannel Sensor Interface Using Multiple Amplifiers

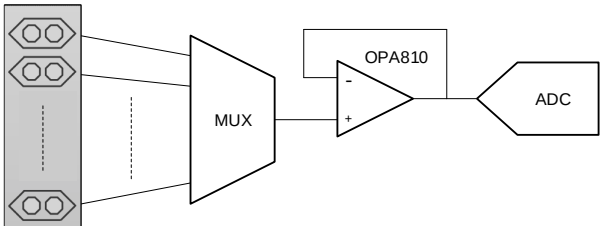


Figure 9. Multichannel Sensor Interface Using a Single Higher GBWP Amplifier

Figure 10 shows the output voltage and input differential voltage when a 8-V step is applied at the noninverting terminal of the OPA810 configured as a unity-gain buffer of Figure 9.

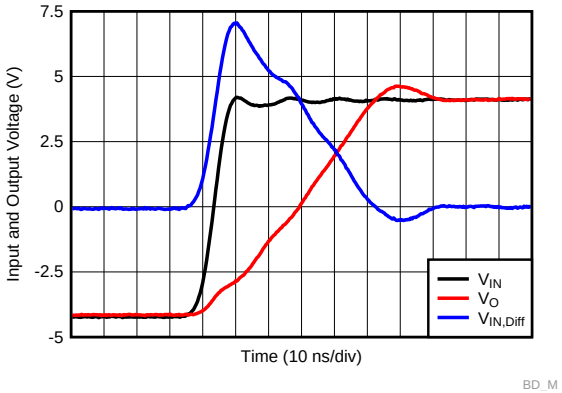


Figure 10. Large-Signal Transient Response Using the OPA810

Because of the fast input transient, the amplifier is slew-limited and the inputs cease to track each other (a maximum $V_{IN,Diff}$ of 7 V is shown in Figure 10) until the output reaches its final value and the negative feedback loop is closed. For standard amplifiers with a 0.7-V to 1.5-V maximum $V_{IN,Diff}$ rating, current-limiting resistors must be used in series with the input pins to protect the device from irreversible damage, which also limits the device frequency response. The OPA810 has built-in input clamps that allow the application of as much as 7 V of $V_{IN,Diff}$, with no external resistors required and no damage to the device or a shift in performance specifications. Such an input-stage architecture, coupled with its fast settling performance, makes the OPA810 a good fit for multichannel sensor multiplexed systems.

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10 Power Supply Recommendations

The OPA810 is intended for operation on supplies ranging from 4.75 V to 27 V. The OPA810 can be operated on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors resulting from the –PSRR term can be minimized. Typically, AC performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1") from the power-supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF, supply-decoupling capacitor at the device supply pins. For single-supply operation, only the positive supply has these capacitors. When a split supply is used, use these capacitors from each supply to ground. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA810 requires careful attention to board layout parasitics and external component types. The OPA2810EVM can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. **Minimize parasitic capacitance** to any AC ground for all signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, this capacitance can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, open a window around the signal I/O pins in all ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1") from the power-supply pins to high-frequency, 0.01-µF decoupling capacitors. At the device pins, do not allow the ground and power plane layout to be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These capacitors can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the high-frequency performance of the OPA810.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 10 kΩ, this parasitic capacitance can add a pole or zero close to the GBWP of 70 MHz and subsequently affects circuit operation. Keep resistor values as low as possible and consistent with load driving considerations. Lowering the resistor values keeps the resistor noise terms low, and minimizes the effect of parasitic capacitance, however lower resistor values increase the dynamic power consumption because R_F and R_G become part of the amplifiers output load network. Transimpedance applications (see the *Transimpedance Amplifier* section) can use whatever feedback resistor is required by the application as long as the feedback compensation capacitor is set considering all parasitic capacitance terms on the inverting node.
4. **Connections to other wideband devices** on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S for sufficient phase margin and stability. Low parasitic capacitive loads (< 10 pF) may not need an R_S because the OPA810 is nominally compensated to operate with a 10-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed with increase in signal gain (increasing the unloaded phase margin). If a long trace is

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Layout Guidelines (continued)

required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and a higher impedance environment improves distortion. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA810 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device—this total effective impedance must be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value to obtain sufficient phase margin and stability. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, the signal attenuates because of the voltage divider formed by the series output into the terminating impedance.

5. **Take care to design the PCB layout for optimal thermal dissipation.** For the extreme case of 125°C operating ambient, using the approximate 134.8°C/W for the SOIC package, and an internal power of 24-V supply × 4.5-mA 125°C supply current gives a maximum internal power dissipation of 108 mW. This power gives a 15°C increase from ambient to junction temperature. Load power adds to this value and this dissipation must also be calculated to determine the worst-case safe operating point.
6. **Socketing a high-speed device such as the OPA810 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can almost make achieving a smooth, stable frequency response impossible. Best results are obtained by soldering the OPA810 onto the board.

11.2 Layout Example

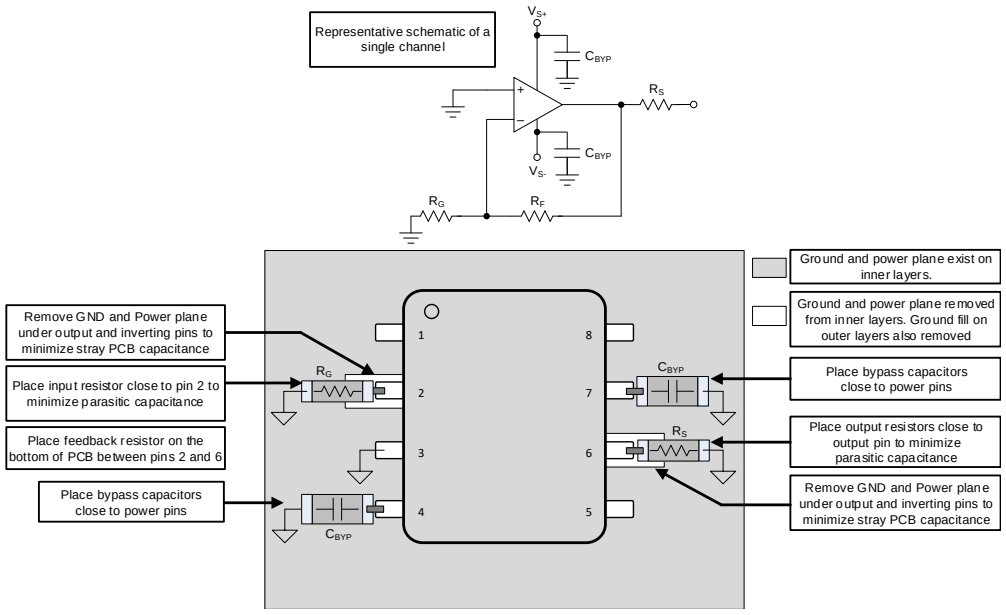


Figure 11. Layout Recommendation

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA2810 Dual-Channel, 27-V, Rail-to-Rail Input/Output FET-Input Operational Amplifier* data sheet
- Texas Instruments, *OPA2810DGK Evaluation Module* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report
- Texas Instruments, *Transimpedance Considerations for High-Speed Amplifiers* application report
- Texas Instruments, *Blog: What you need to know about transimpedance amplifiers – part 1*
- Texas Instruments, *Blog: What you need to know about transimpedance amplifiers – part 2*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps* application report
- Texas Instruments, *TINA model and simulation tool*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA810IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	810	
OPA810IDT	PREVIEW	SOIC	D	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	810	
XOPA810IDT	ACTIVE	SOIC	D	8	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

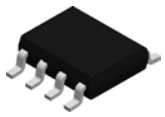
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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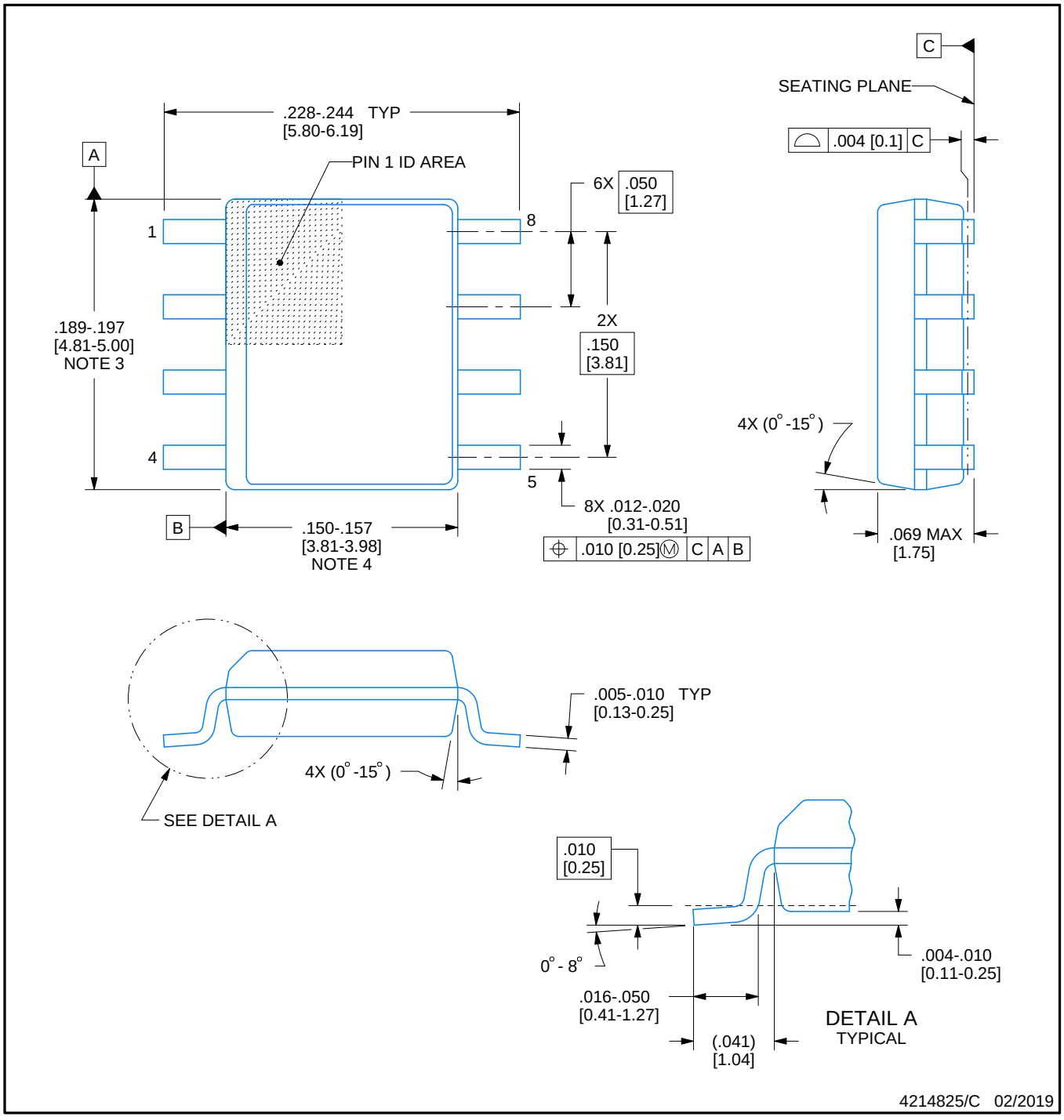


PACKAGE OUTLINE

D0008A

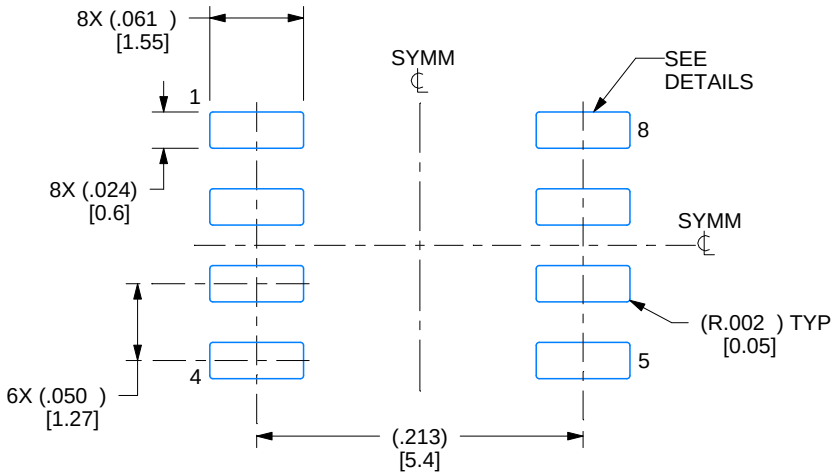
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

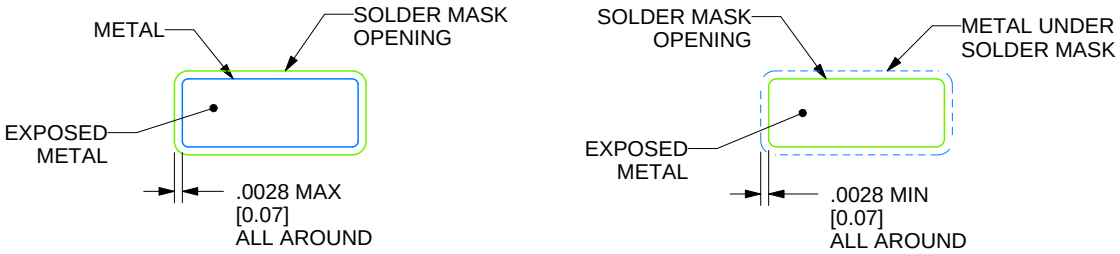


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

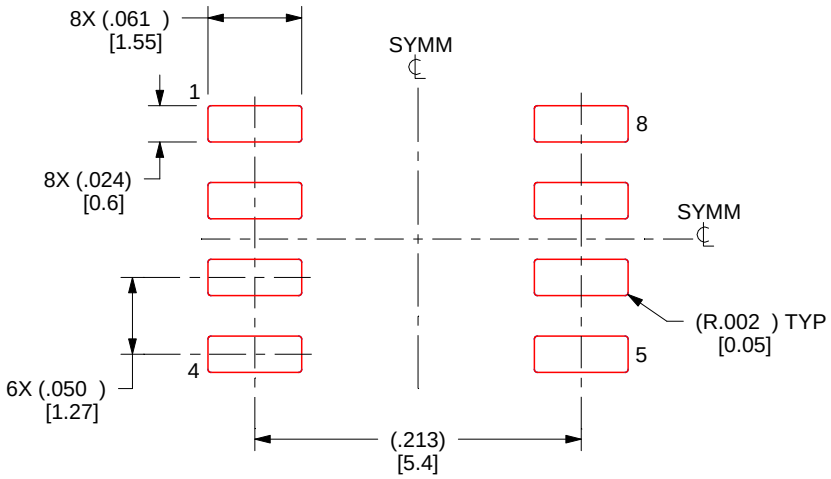
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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