

IP4776CZ38

Fully integrated HDMI interface with level shifter, ESD and backdrive protection

Rev. 6 — 7 January 2011 **Product data sheet**

1. General description

The IP4776CZ38 is designed for HDMI host-interface protection. The IP4776CZ38 includes level shifting for the DDC channels and backdrive protection for HDMI as well as high-level ESD protection diodes for the TMDS signal lines.

The level shifting function is required when the receiver operates at a supply voltage lower than the external devices to protect the I/Os against overvoltages. The IP4776CZ38 contains four N-channel MOSFETs to provide this level shifting function.

Furthermore, all TMDS intra-pairs are protected by a special diode configuration offering an ultra low line capacitance of 0.7 pF only. These diodes provide protection to downstream components from ESD voltages up to ±8 kV contact according to the IEC 61000-4-2, level 4 standard.

2. Features and benefits

- Pb-free and RoHS compliant, Dark Green
- Integrated high-level ESD protection, level shifting and backdrive protection
- All TMDS lines with integrated rail-to-rail clamping diodes with downstream ESD protection of ±8 kV according to IEC 61000-4-2, level 4 standard
- Matched 0.5 mm trace spacing
- Bidirectional level shifting N-channel FETs provided for DDC clock and data channels
- TMDS lines with ≤ 0.05 pF matching of capacitance between the TMDS pairs
- Ultra low line capacitance of 0.7 pF per channel
- HDMI 1.3 compliant
- Backdrive protection
- 38-pin TSSOP lead-free package

3. Applications

- The IP4776CZ38 is designed for HDMI receiver and transmitter port protection, level shifting and backdrive protection e.g.:
  - TV
  - Graphics card
  - Set-top box
  - DVD
  - Digital media adapter
  - Game console

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4776CZ38	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1

5. Functional diagram

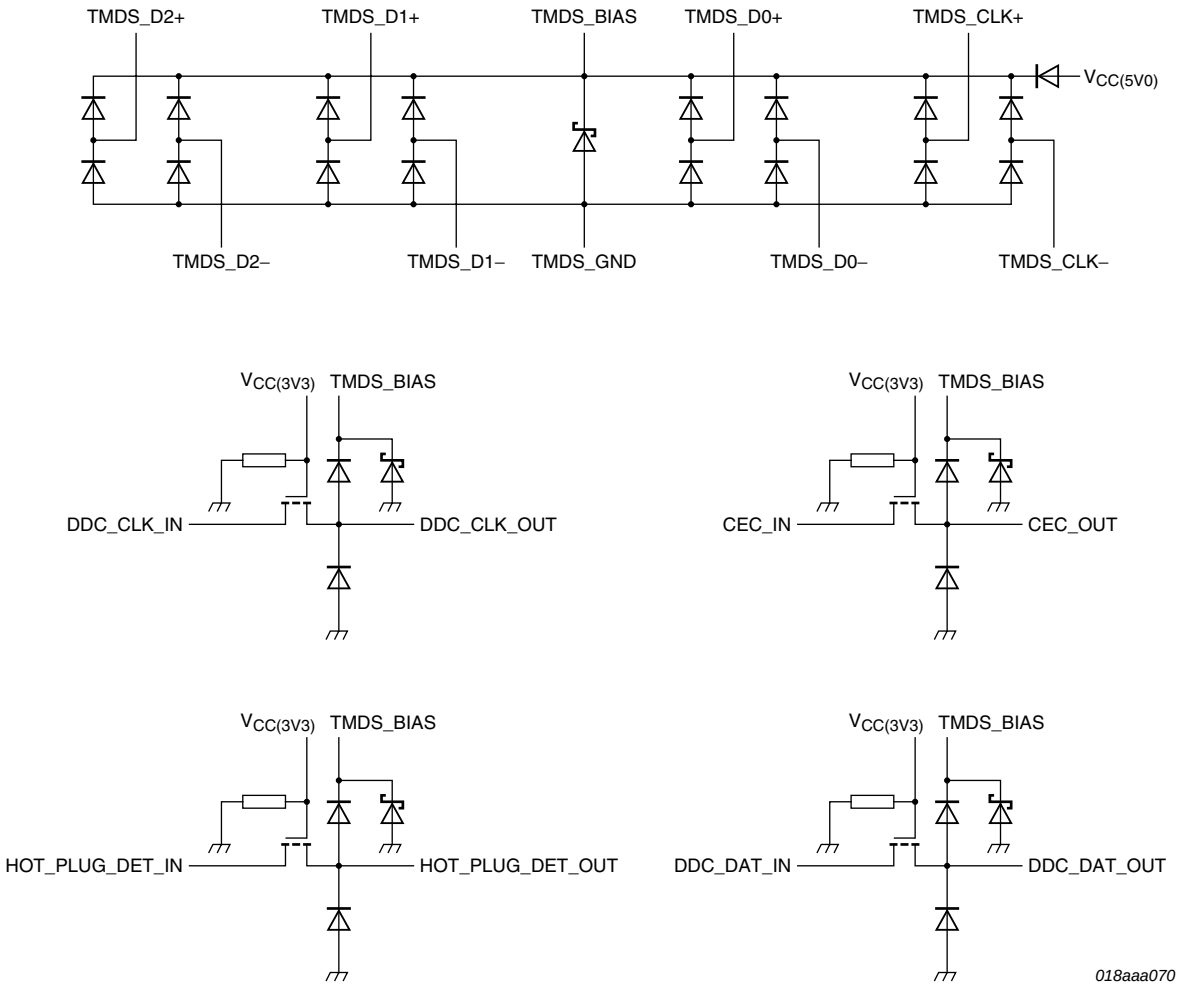


Fig 1. Functional diagram

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6. Pinning information

6.1 Pinning

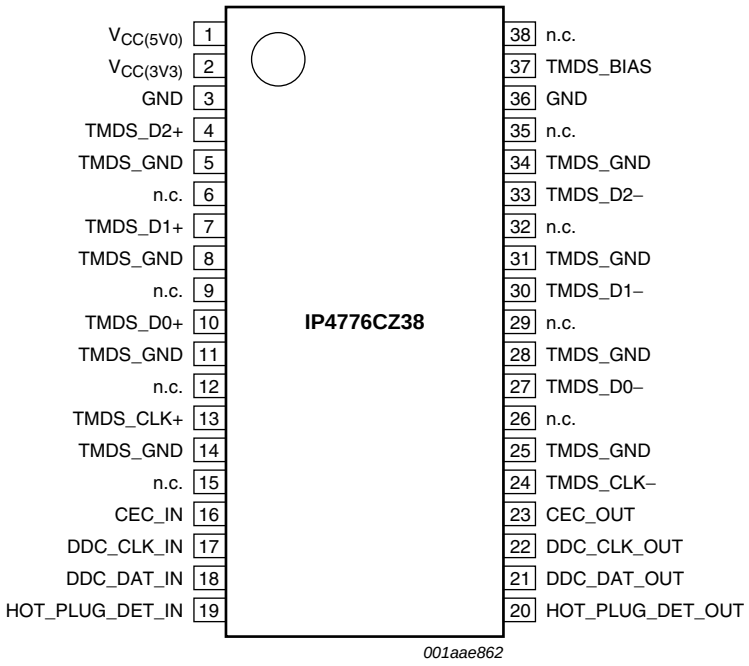


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(5V0)}$	1	supply voltage
$V_{CC(3V3)}$	2	bias supply voltage for the level shifters
GND	3	ground reference[1]
TMDS_D2+	4	D2+ TMDS ESD protection[2]
TMDS_GND	5	ground reference[1]
n.c.	6	not connected[2]
TMDS_D1+	7	D1+ TMDS ESD protection[2]
TMDS_GND	8	ground reference[1]
n.c.	9	not connected[2]
TMDS_D0+	10	D0+ TMDS ESD protection[2]
TMDS_GND	11	ground reference[1]
n.c.	12	not connected[2]
TMDS_CLK+	13	CLK+ TMDS ESD protection[2]
TMDS_GND	14	ground reference[1]
n.c.	15	not connected[2]

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Table 2. Pin description *...continued*

Symbol	Pin	Description
CEC_IN	16	CEC input[3]
DDC_CLK_IN	17	DDC clock input[3]
DDC_DAT_IN	18	DDC data input[3]
HOT_PLUG_DET_IN	19	hot plug detection input[3]
HOT_PLUG_DET_OUT	20	hot plug detection output[4]
DDC_DAT_OUT	21	DDC data output[4]
DDC_CLK_OUT	22	DDC clock output[4]
CEC_OUT	23	CEC output[3]
TMDS_CLK–	24	CLK– TMDS ESD protection[2]
TMDS_GND	25	ground reference[1]
n.c.	26	not connected[2]
TMDS_D0–	27	D0– TMDS ESD protection[2]
TMDS_GND	28	ground reference[1]
n.c.	29	not connected[2]
TMDS_D1–	30	D1– TMDS ESD protection[2]
TMDS_GND	31	ground reference[1]
n.c.	32	not connected[2]
TMDS_D2–	33	D2– TMDS ESD protection[2]
TMDS_GND	34	ground reference[1]
n.c.	35	not connected[2]
GND	36	ground reference[1]
TMDS_BIAS	37	bias for TMDS ESD protection and bias for level shifter output ESD protection. This pin must be connected to a 0.1 μF capacitor.
n.c.	38	not connected

[1] Pins GND and TMDS_GND are internally connected.

[2] This pin always has to be connected to the pin on the opposite location of the IC via a PCB track to guarantee correct functionality; see Figure 3, Figure 4 and Figure 5.

[3] $V_{CC(3V3)}$ referenced logic level in.

[4] $V_{CC(5V0)}$ referenced logic level out.

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7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			GND – 0.5	5.5	V
V_I	input voltage	at input pins		GND – 0.5	5.5	V
V_{ESD}	electrostatic discharge voltage	signal pins; IEC 61000-4-2, level 4	[1]			
		contact	[2]	–8	+8	kV
		air discharge	[2]	–15	+15	kV
		all other pins; MIL-STD-883 Method 3015 (human body model)				
		contact		–2	+2	kV
		air discharge		–2	+2	kV
T_{stg}	storage temperature			–55	+125	°C

[1] Signal pins:
TMDS_D2+, TMDS_D2–, TMDS_D1+, TMDS_D1–, TMDS_D0+, TMDS_D0–,
TMDS_CLK+, TMDS_CLK–,
CEC_OUT,
DDC_DAT_OUT,
DDC_CLK_OUT,
HOT_PLUG_DET_OUT.

[2] This measurement is performed with a 0.1 μF external capacitor on pin TMDS_BIAS.

8. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature		–40	-	+85	°C

9. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{CC(5V0)}$	supply current (5.0 V)	$V_{CC(5V0)}$ = 5.0 V		-	-	130	μA
$I_{CC(3V3)}$	supply current (3.3 V)	$V_{CC(3V3)}$ = 3.3 V		-	1	5	μA
$I_{bck(out-VCC5V0)}$	back current from output / TMDS pins to $V_{CC(5V0)}$	signal pins; powered down; $V_{CC(5V0)} < V_{O(ch)}$	[1]	-	0.1	0.5	μA
V_{BRzd}	Zener diode breakdown voltage	I = 1 mA		6	-	9	V
$I_{L(r)}$	reverse leakage current	per TMDS channel; V_I = 3.0 V		-	-	1	μA
V_F	forward voltage			-	0.7	-	V
$C_{ch(TMDS)}$	TMDS channel capacitance	$V_{CC(5V0)}$ = 5 V; f = 1 MHz; V_{bias} = 2.5 V	[2]	-	0.7	-	pF

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Table 5. Characteristics *...continued*

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta C_{ch(TMDS)}$	TMDS channel capacitance difference	$V_{CC(5V0)}$ = 5 V; f = 1 MHz; V_{bias} = 2.5 V	[2]	-	0.05	-	pF
$C_{ch(mutual)}$	mutual channel capacitance	between signal pin and pin n.c.; $V_{CC(5V0)}$ = 0 V; f = 1 MHz; V_{bias} = 2.5 V	[2]	-	0.07	-	pF
$C_{I(ch-GND)(levsh)}$	level shifting input capacitance from channel to ground	$V_{CC(5V0)}$ = 0 V; f = 1 MHz; V_{bias} = 2.5 V	[2]	-	4	6	pF
R_{dyn}	dynamic resistance	I = 1 A; IEC 61000-4-5/9					
		positive transient		-	2.4	-	Ω
		negative transient		-	1.3	-	Ω
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	V_{ESD} = 8 kV	[3]	-	8	-	V
ΔV_{on}	on-state voltage drop	$V_{CC(3V3)}$ = 2.5 V; V_S = GND; I_{DS} = 3 mA	[4]	-	85	140	mV

[1] Signal pins:
TMDS_D2+, TMDS_D2–, TMDS_D1+, TMDS_D1–, TMDS_D0+, TMDS_D0–,
TMDS_CLK+, TMDS_CLK–,
CEC_OUT,
DDC_DAT_OUT,
DDC_CLK_OUT,
HOT_PLUG_DET_OUT.

[2] This parameter is guaranteed by design.

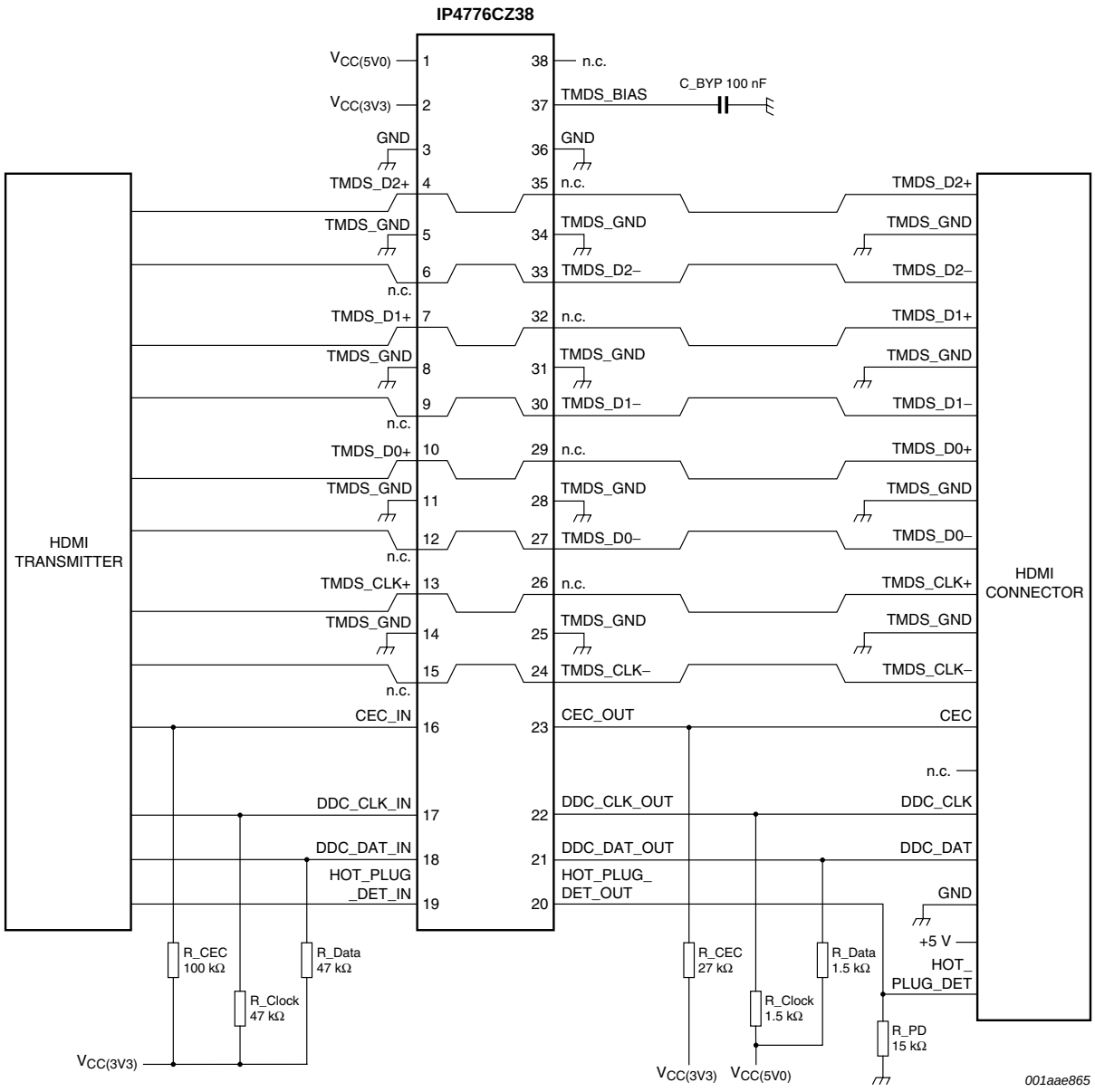
[3] This measurement is performed with a 0.1 μF external capacitor on pin TMDS_BIAS.

[4] For level shifting N-FET.

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10. Application information



Use tapered tracks to connect adjacent TMDS+ and TMDS– pins with the opposite n.c. pins; see Figure 5.

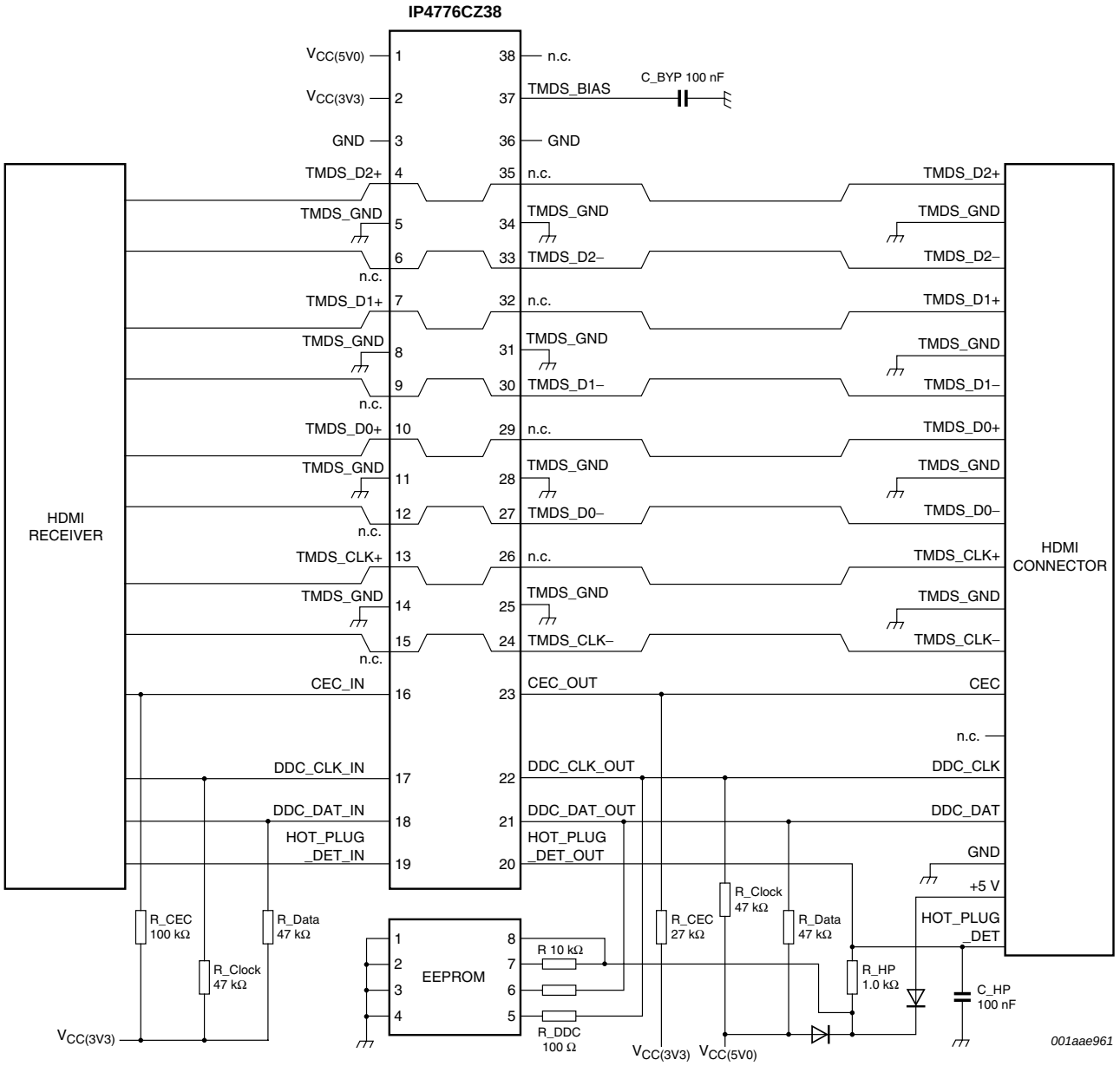
Use tapered tracks to connect adjacent TMDS+ and TMDS– pins with the HDMI connector; see Figure 5.

Use tapered tracks to connect adjacent TMDS+ and TMDS– pins with the HDMI transmitter; see Figure 5.

Fig 3. HDMI transmitter application layout diagram

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Use tapered tracks to connect adjacent TMDS+ and TMDS– pins with the opposite n.c. pins; see Figure 5.

Use tapered tracks to connect adjacent TMDS+ and TMDS– pins with the HDMI connector; see Figure 5.

Use tapered tracks to connect adjacent TMDS+ and TMDS– pins with the HDMI receiver; see Figure 5.

Fig 4. HDMI receiver application layout diagram

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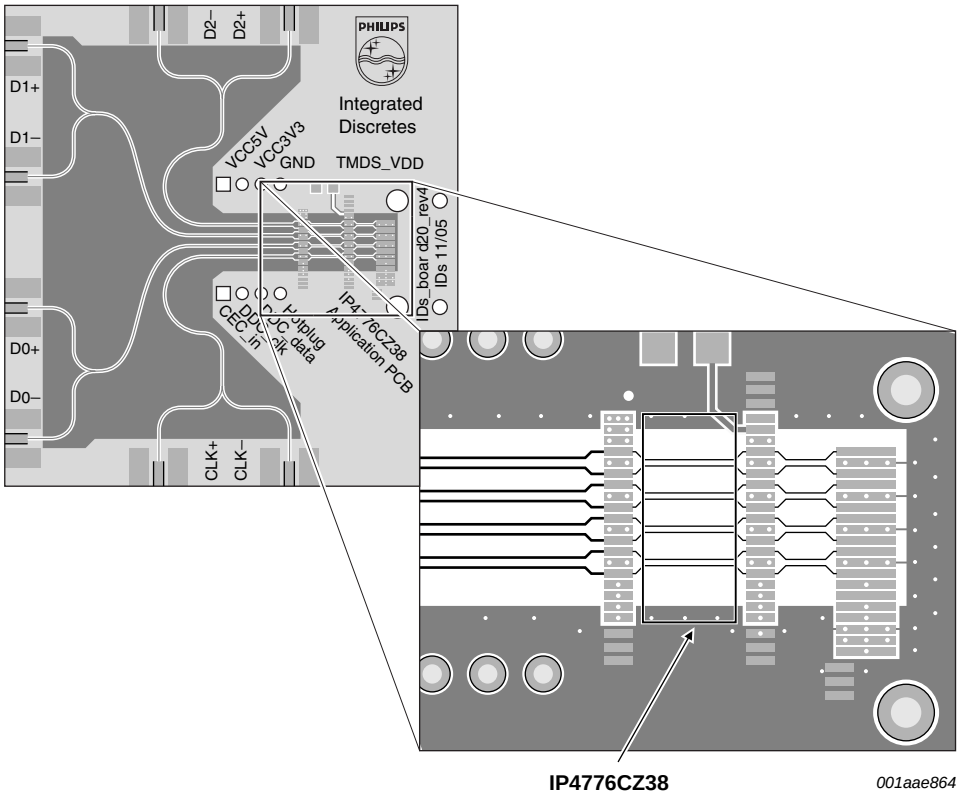


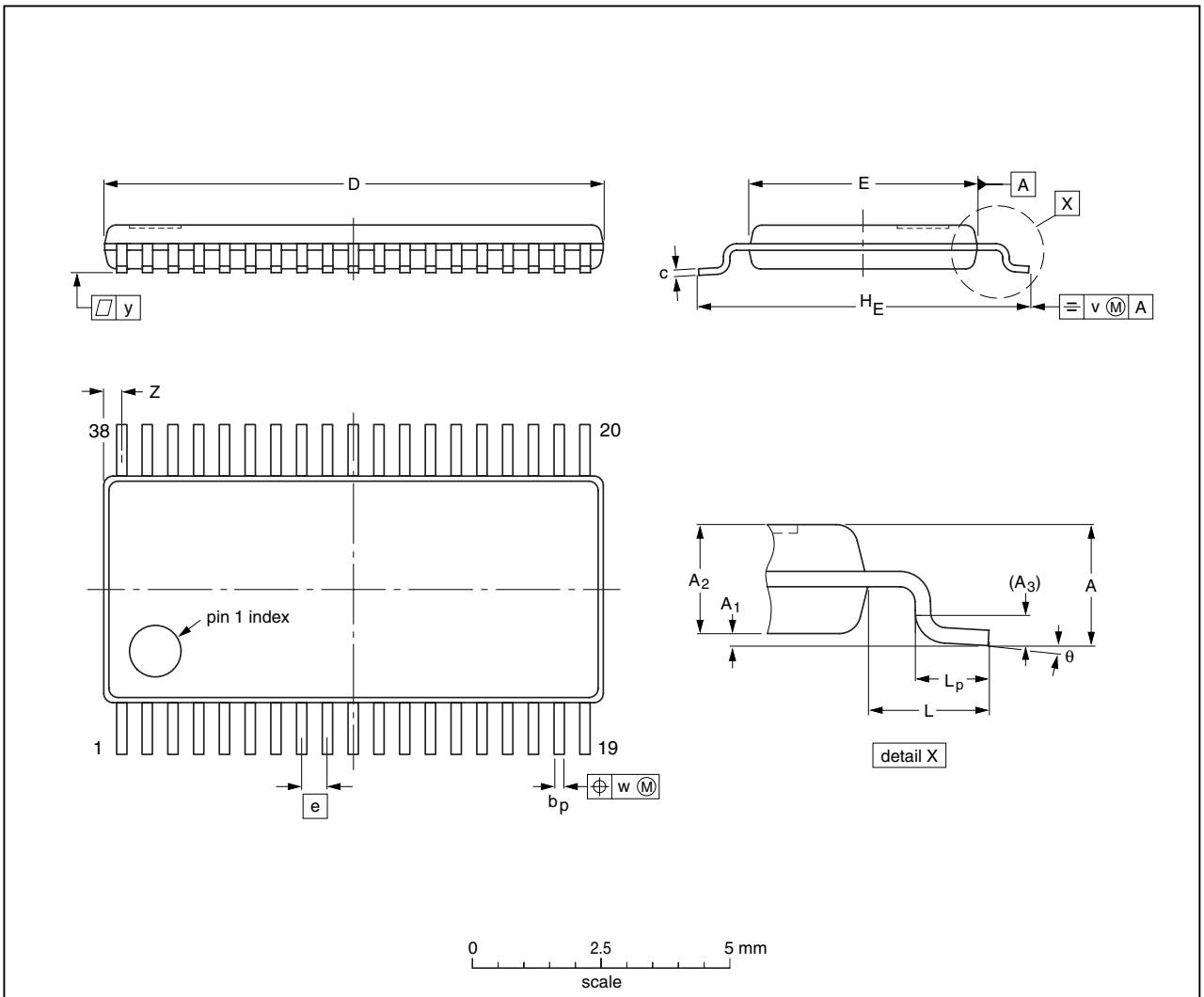
Fig 5. Layout proposal of printed-circuit board

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11. Package outline

TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm **SOT510-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.27 0.17	0.20 0.09	9.8 9.6	4.5 4.3	0.5	6.4	1	0.7 0.5	0.2	0.08	0.08	0.49 0.21	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT510-1		MO-153				~~03-02-18~~ 05-11-02

Fig 6. Package outline SOT510-1 (TSSOP38)

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12. Abbreviations

Table 6. Abbreviations

Acronym	Description
CEC	Consumer Electronics Control
DDC	Data Display Channel
DVD	Digital Video Disk
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HDM	High-Definition Multimedia
HDMI	High-Definition Multimedia Interface
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed-Circuit Board
RoHS	Restriction of the use of certain Hazardous Substances
TMDS	Transition Minimized Differential Signaling

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13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4776CZ38 v.6	20110107	Product data sheet	-	IP4776CZ38 v.5
Modifications:	• Figure 1: corrected			
IP4776CZ38 v.5	20100706	Product data sheet	-	IP4776CZ38 v.4
IP4776CZ38 v.4	20070612	Product data sheet	-	IP4776CZ38 v.3
IP4776CZ38 v.3	20070125	Product data sheet	-	IP4776CZ38 v.2
IP4776CZ38 v.2	20060918	Product data sheet	-	IP4776CZ38 v.1
IP4776CZ38 v.1	20060714	Product data sheet	-	-

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14. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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16. Contents

1	**General description**	**1**
2	**Features and benefits**	**1**
3	**Applications**	**1**
4	**Ordering information**	**2**
5	**Functional diagram**	**2**
6	**Pinning information**	**3**
6.1	Pinning	3
6.2	Pin description	3
7	**Limiting values**	**5**
8	**Recommended operating conditions**	**5**
9	**Characteristics**	**5**
10	**Application information**	**7**
11	**Package outline**	**10**
12	**Abbreviations**	**11**
13	**Revision history**	**12**
14	**Legal information**	**13**
14.1	Data sheet status	13
14.2	Definitions	13
14.3	Disclaimers	13
14.4	Trademarks	14
15	**Contact information**	**14**
16	**Contents**	**15**

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