JAN. 2000

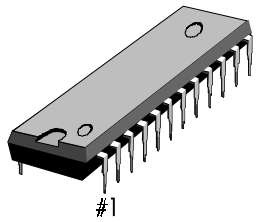
DATA SHEET

S5D2501F

OVERVIEW

The S5D2501F is used to display some characters or symbols on a screen of monitor. Basically, the operation is to control the internal memory on chip and generate the R,G,B signals for some characters or symbols. The R,G,B signals are synchronized with the horizontal sync. Then the R,G,B signals are mixed with the main video signal in the Video Amp IC.
The font data for characters or symbols are stored in the internal ROM. This stored data are accessed and controlled by the control data from a micro controller. The control data are transmitted through the I^2C bus. All timing control signals including the system clock are synchronized with the horizontal sync. Therefore there is a PLL circuitry on chip.

24-DIP-300



FEATURES

- Build in 1K-byte SRAM
- 464 ROM fonts (448 standard fonts + 16 Multi-color fonts)
- Full Screen Memory Architecture
- Wide range PLL available (15 kHz — 120 kHz)
- Programmable vertical height of character
- Programmable vertical and horizontal positioning
- Character color selection up to 16 different colors
- Programmable background color (Up to 16 colors)
- Character blinking, bordering and shadowing
- Color blinking
- Character scrolling
- Fade-in and fade-out
- Row to row spacing control
- Window outline and shadowing
- Box drawing
- Character sizing up to four times
- 8 PWM DAC channels with 8-bit resolution
- 96 MHz pixel frequency from on-chip PLL
- I2C Protocol Data Transmission (Slave Address : BAH)
- OSD Vertical Bouncing Auto Detect / Correction
- Back Raster Blanking (Row Control)

ORDERING INFORMATION

Device	Package	Operating Temperature
S5D2501F	24-DIP-300	0°C — 70°C

BLOCK DIAGRAM

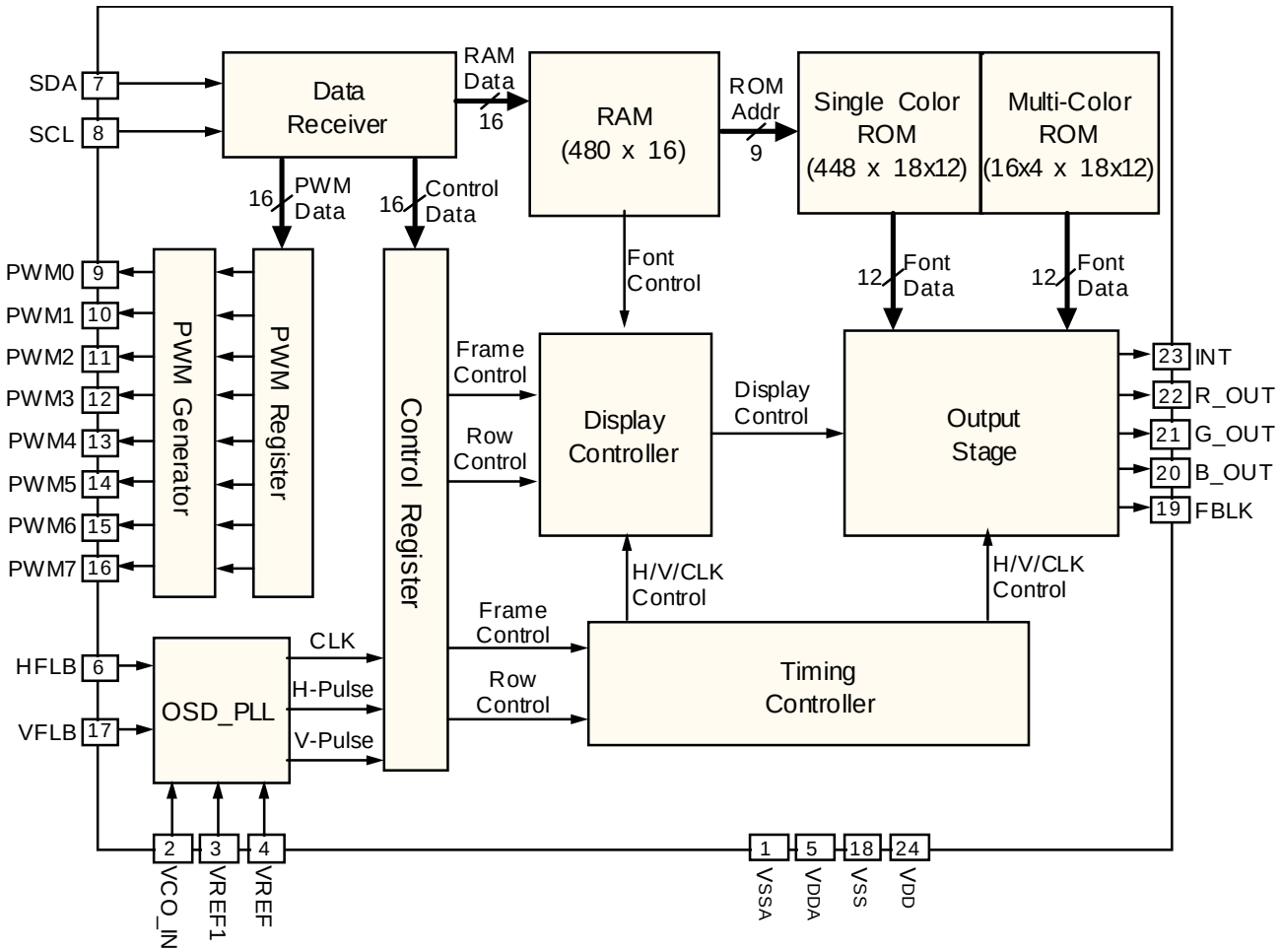


Figure 1. Functional Block Diagram

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PIN CONFIGURATIONS

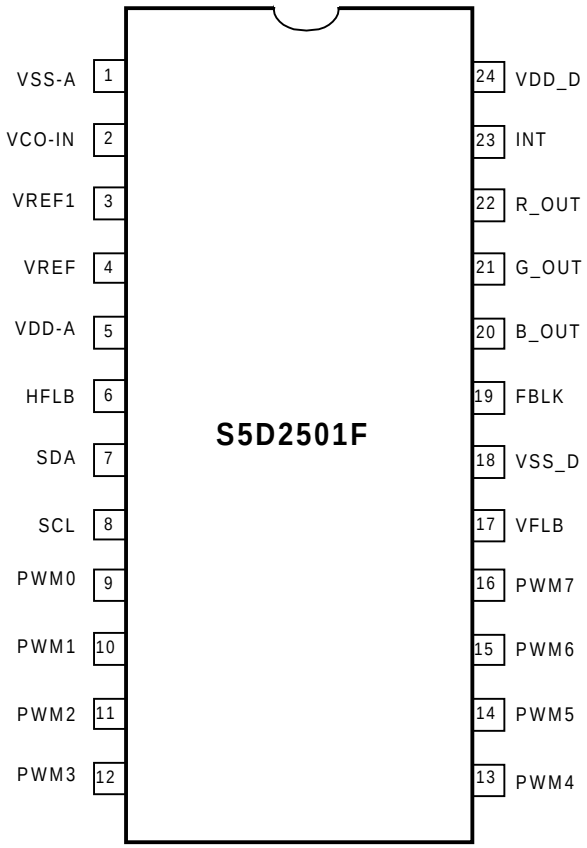


Figure 2. Pin Configurations

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin No.	Signal	Active	I/O	Description
1	VSS_A	-	-	Ground (Analog Part)
2	VCO_IN	-	Input	This voltage is generated at the external loop filter and goes into the input stage of the VCO.
3	VREF1	-	Input	1.26 V DC Voltage from the Bandgap Reference. Connected to ground through a resistor to make internal reference current (Typical 36 kΩ for 27μA)
4	VREF	-	Input	Bandgap Reference Voltage (Typical 1.26 V)
5	VDD_A	-	-	+5 V Supply Voltage for Analog Part
6	HFLB	Low	Input	Horizontal Flyback Signal
7	SDA	-	In/Out	Serial Data (I^2C)
8	SCL	-	In/Out	Serial Clock (I^2C)
9	PWM 0	-	Output	PWM DAC 0 Output
10	PWM 1	-	Output	PWM DAC 1 Output
11	PWM 2	-	Output	PWM DAC 2 Output
12	PWM 3	-	Output	PWM DAC 3 Output
13	PWM 4	-	Output	PWM DAC 4 Output
14	PWM 5	-	Output	PWM DAC 5 Output
15	PWM 6	-	Output	PWM DAC 6 Output
16	PWM 7	-	Output	PWM DAC 7 Output
17	VFLB	Low	Input	Vertical Flyback Signal
18	VSS_D	-	-	Ground for Digital Part
19	FBLK	-	Output	Fast Blank Signal
20	B_OUT	-	Output	Video Signal Output (B)
21	G_OUT	-	Output	Video Signal Output (G)
22	R_OUT	-	Output	Video Signal Output (R)
23	INT	-	Output	Intensity Signal Output
24	VDD_D	-	-	+5 V Supply Voltage for Dogital Part

ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value			Unit
		Min.	Typ.	Max.	
Maximum Supply Voltage	VDD	-	-	6.5	V
Input Voltage	V_I	-	-	5.25	V
Operating Temperature Range	T_{OPR}	-20	-	70	°C
Storage Temperature Range	T_{STG}	-40		125	°C
Power Dissipation	P_D	-	-	1200	mW

NOTE: PKG Thermal Resistance : 64.2 °C/W

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

(Ta = 25 °C, V_{DD} = 5 V)

Table 2. DC Electrical Characteristics

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.75	5.00	5.25	V
Supply Current (No load on any output)	I_{DD}	-	-	25	mA
Input Voltage	V_{IH}	$0.8V_{DD}$	-	-	V
	V_{IL}	-	-	V_{SS} + 0.4	V
Output Voltage (Iout = ±1mA)	V_{OH}	$0.8V_{DD}$	-	-	V
	V_{OL}	-	-	V_{SS} + 0.4	V
Input Leakage Current	I_{IL}	-10	-	10	µA
VCO Input Voltage	V_{VCO}		2.5		V

OPERATION TIMINGS

Table 3. Operation Timings

Parameters (Conditions)	Symbol	Min.	Typ.	Max.	Unit
Output Signal R/G/B_OUT, INT, FBLK (Ta = 25°C V_{DDA} = V_{DD} = 5 V , C_{LOAD} = 30pF)					
Rise Time	t_R	-	-	6	nsec
Fall Time	t_F	-	-	6	nsec
Input Signal HFLB, VFLB					
Horizontal Flyback Signal Frequency	f_{HFLB}	-	-	120	kHz
Vertical Flyback Signal Frequency	f_{VFLB}	-	-	200	Hz
I^2C Interface SDA, SCL (Refer to Figure 3)					
SCL Clock Frequency	f_{SCL}	-	-	300	kHz
Hold Time for start condition	t_{hs}	500	-	-	ns
Set Up Time for stop condition	t_{sus}	500	-	-	ns
Low Duration of clock	t_{low}	400	-	-	ns
High Duration of clock	t_{high}	400	-	-	ns
Hold Time for data	t_{hd}	0	-	-	ns
Set Up Time for data	t_{sud}	500	-	-	ns
Time between 2 access	t_{ss}	500	-	-	ns
Fall Time of SDA	t_{fSDA}	-	-	20	ns
Rise Time of both SCL and SDA	t_{rSDA}	-	-	-	ns

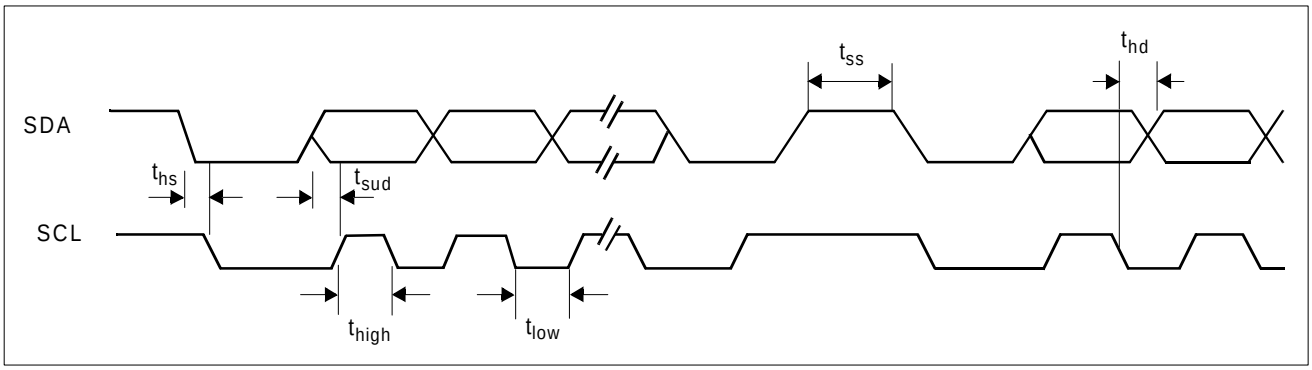


Figure 3. I^2C Bus Timing Diagram

FUNCTIONAL DESCRIPTIONS

Data Transmission to the S5D2501F

According to the I^2C protocol, the S5D2501F receives the data from a micro controller. The SDA line and the SCL line are shown in Figure 4. As shown in Figure 4, after the starting pulse, the slave address with R/W* bit and an acknowledge are transmitted in sequence, an internal register address of the S5D2501F is followed. The first 8-bit byte is the upper 8bits of the register address. The lower 8bits of the register address are followed after the second acknowledge. There is a data transmission format and are two address bit patterns in the S5D2501F as following. The slave address of the S5D2501F is BAH(in hexadecimal).

Data Transmission Format

Row Address -> Column Address -> Data Byte N -> Data Byte N+1 -> Data Byte N+2 -> ....

Address Bit Pattern for Display Registers Data

(a) Row Address Bit Pattern R3 - R0: Valid Data for Row Address

A15	A14	A13	A12	A11	A10	A9	A8
X	X	X	X	R3	R2	R1	R0

(b) Column Address Bit Pattern C4 - C0: Valid Data for Column Address

A7	A6	A5	A4	A3	A2	A1	A0
X	X	X	C4	C3	C2	C1	C0

After addressing, data bytes are followed as the above data transmission format. The Figure 4 describes the data transmission with the I^2C bus protocol.

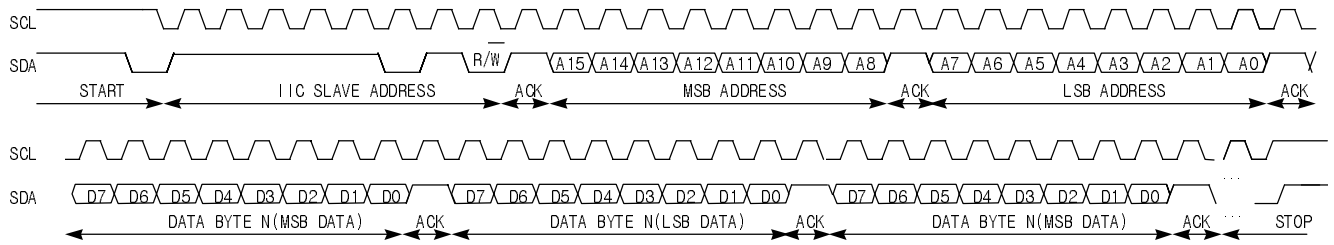


Figure 4. (a) SDA line and SCL line (Write Operation)

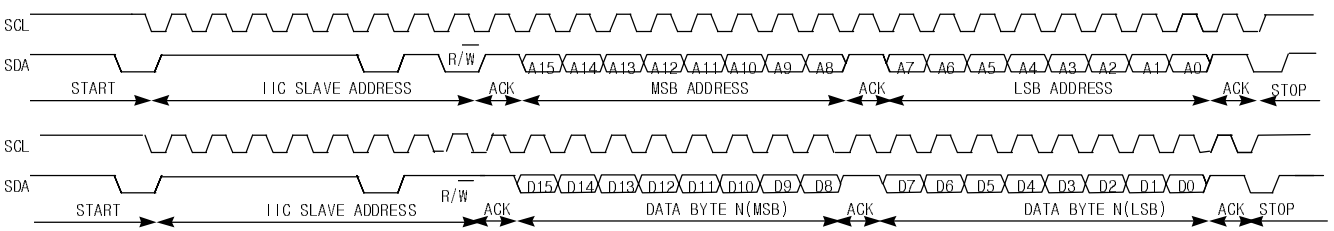


Figure 4. (b)SDA line and SCL line (Read Operation)

Memory Map

The display RAM is addressed with the row and column number in sequence. The display RAM consists of four register groups: Character & Attribute Registers, Row Attribute Registers, Frame Control Registers and PWM Control Registers. As the display area in a monitor screen is 30 columns by 15 rows, the related Character & Attribute Registers are also 30 columns by 15 rows. Each register contains a character address and an attribute corresponding to display location on a monitor screen. And one register is composed of 16 bits. The lower 9 bits select characters out of 464 ROM fonts. The upper 7 bits are assigned to give a character attribute to a selected font. Row Attribute Registers occupy the 31th column of Display RAM and provide the row attribute of a blank mode, raster color, raster color intensity, character color intensity, horizontal character size, vertical character size.
Frame Control Registers and PWM Control Registers are located at the 16th row.
The content of each register is described in Figure 5 and following register set.

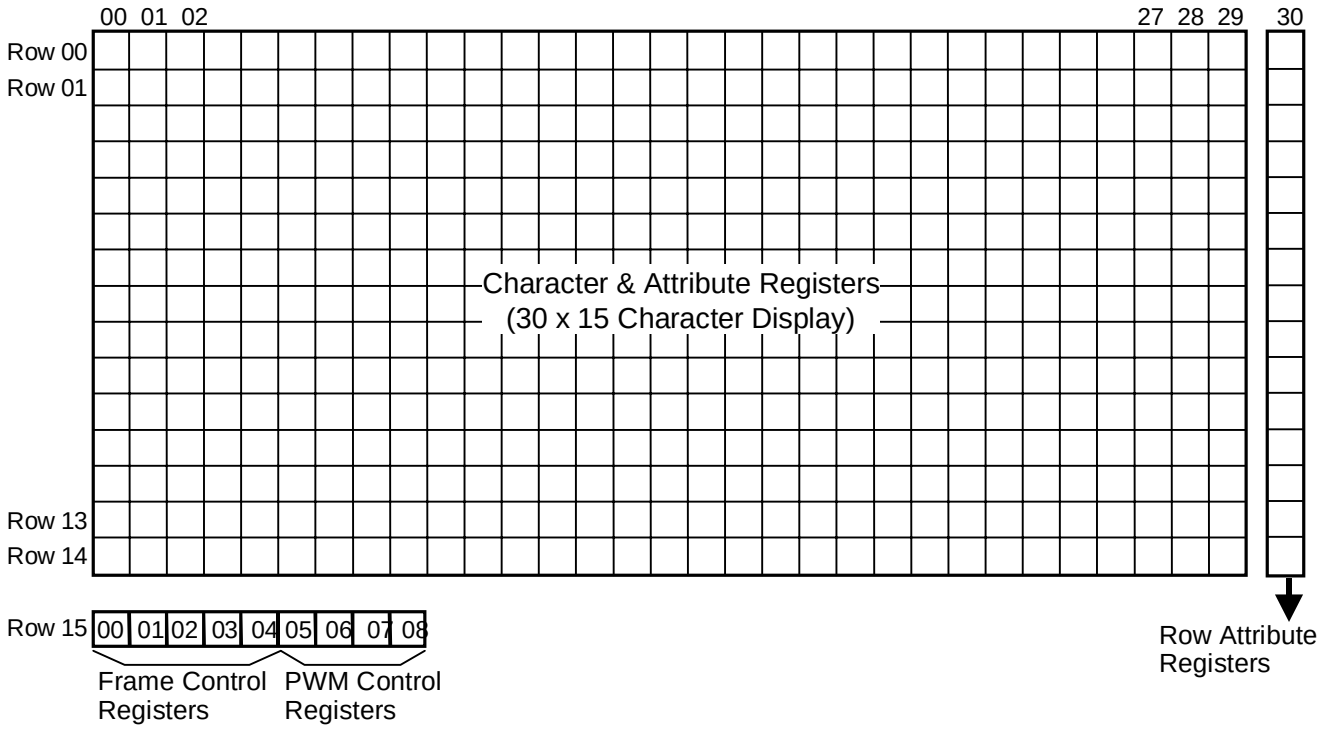


Figure 5. Memory Map of Display Registers

ROM Fonts

S5D2501F is able to supply 464 ROM fonts for describing an OSD icon. So a multi-language OSD icon can be generated. 448 fonts of 464 ROM fonts are standard fonts and 16 fonts are multi-color fonts as following figure. The standard font $000 is reserved for blank data.
Each multi-color font consists of 4-color attribute ROM fonts as following figure.

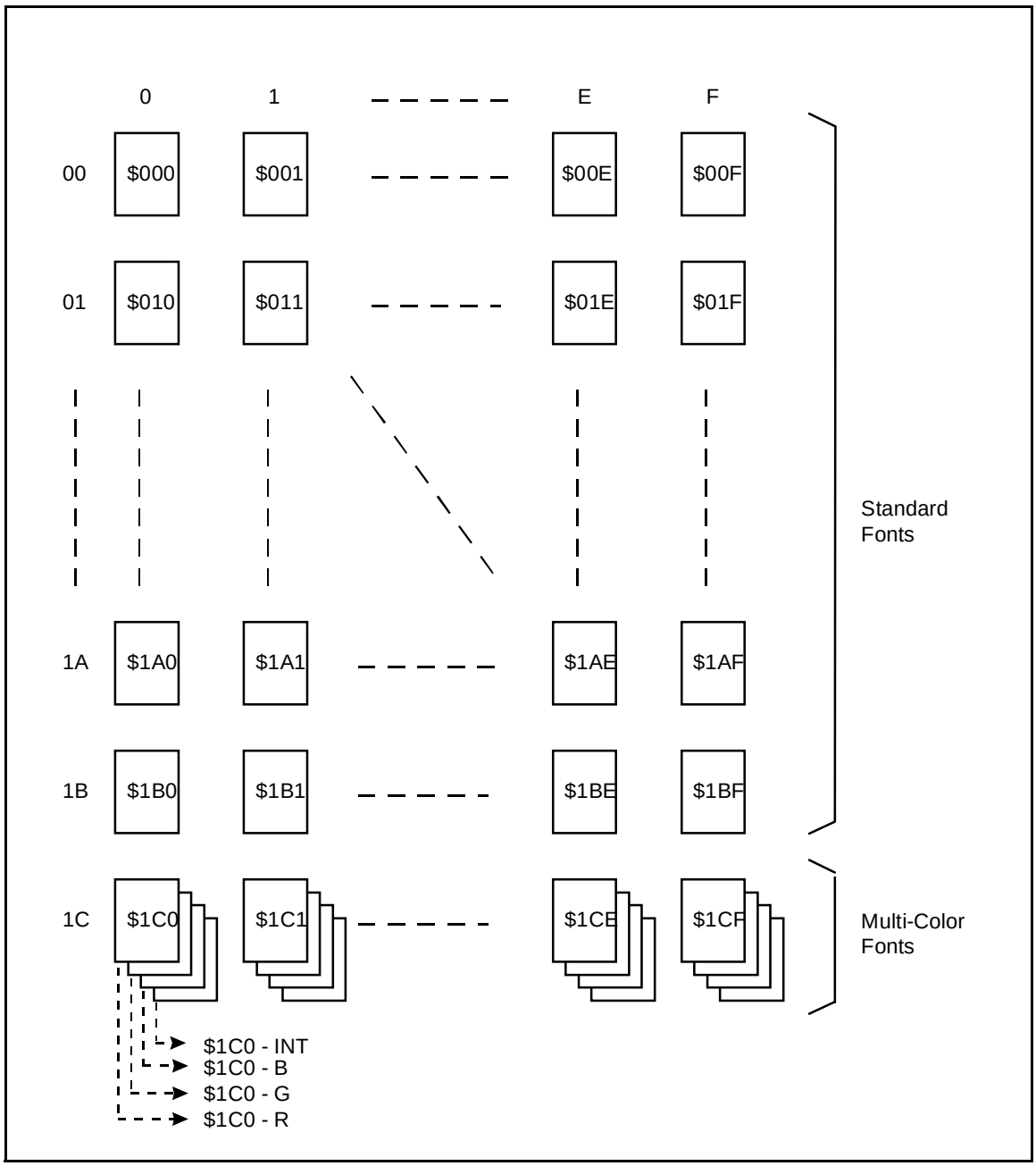
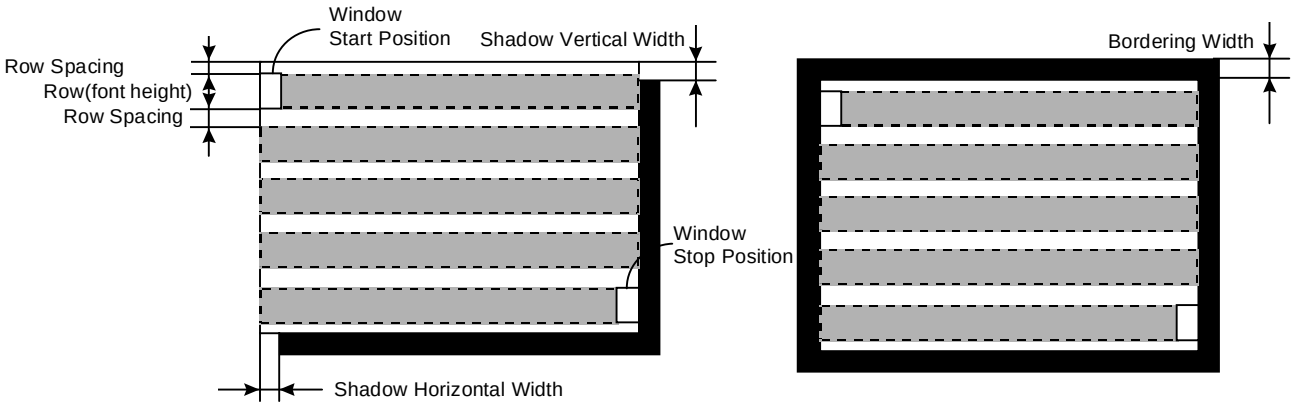


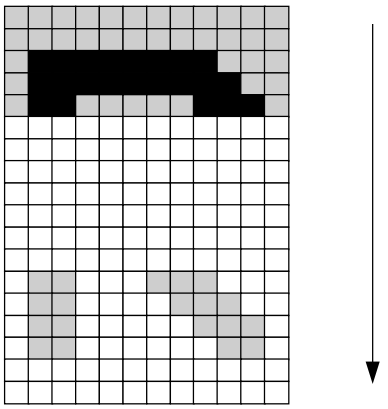
Figure 6. Array of ROM Fonts

Window , Window Shadowing and Bordering

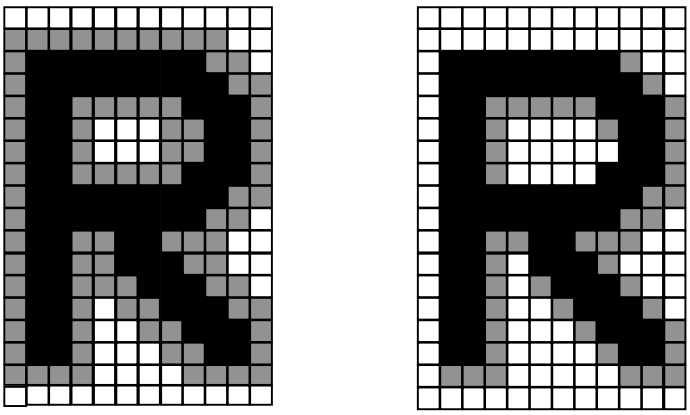


Scroll

The scrolling function is to display or erase a character slowly from the top line to the bottom. The scrolling time is controlled by 'ScrT'bit of the frame control registers. If 'ScrT' bit is high, then the time is 1 sec. Otherwise, 0.5 sec.



Character Bordering & Shadowing



Character Height Control

Two examples of the height-controlled character are shown in the following figure. The height control is performed by repeating some lines. The repeating line-number comes from the equation below.

[# of the repeating lines = 2 + N $\times$ M] ,
where N = 1,2,3,... and M = round{14÷(CH[5:0]-18)}.

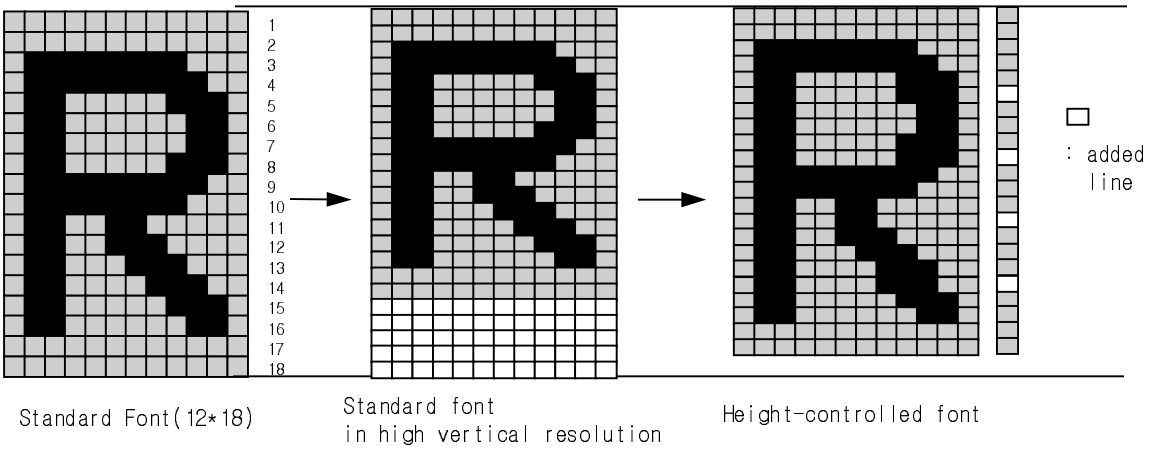
If the M value is less than or equal to 1, all the lines of the standard font are repeated once or more. This is described as following.

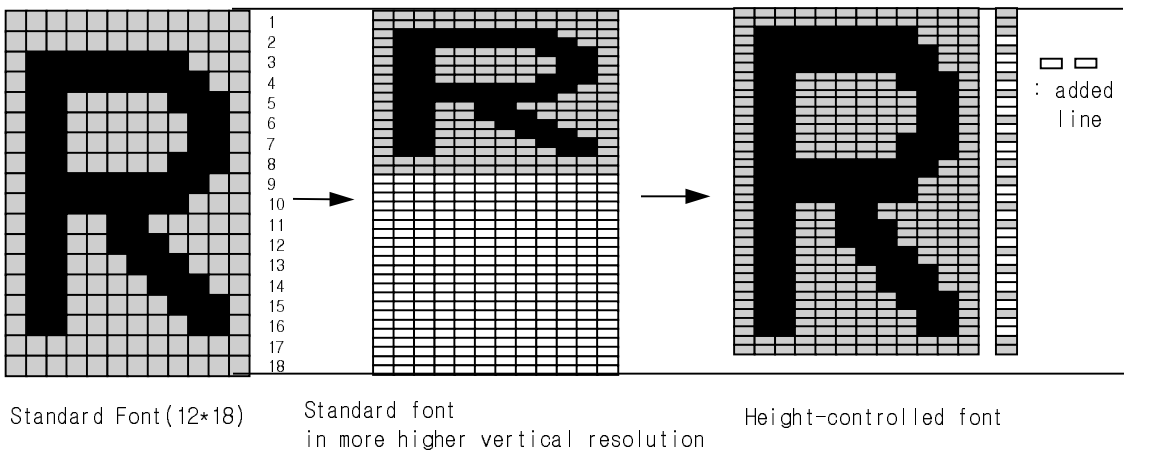
(i) If CH[5:0] is greater than 32, and less than or equal to 46 (32 < CH[5:0] ≤ 46),
then all lines are repeated once or twice. The lines repeated twice are selected by the following equation.
[# of the repeating lines = 2 + N $\times$ M] ,
where N = 1,2,3,... and M= round{14÷(CH[5:0]-32)}.

(ii) If CH[5:0] is greater than 46, and less than or equal to 60 (46 < CH[5:0] ≤ 60),
then all lines are repeated twice or three times. The lines repeated three times are selected by the following equation.
[# of the repeating lines = 2 + N $\times$ M] ,
where N = 1,2,3,... and M= round{14÷(CH[5:0]-46)}.

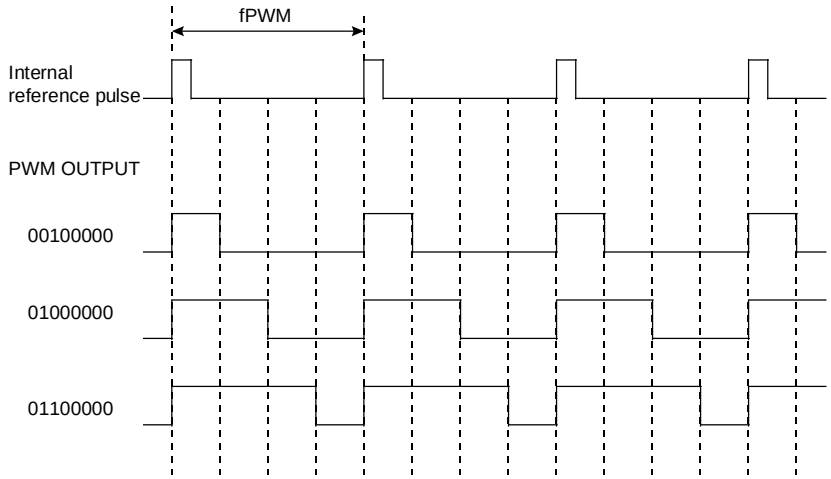
iii) If CH[5:0] is greater than 60, and less than or equal to 64 (60 < CH[5:0] ≤ 64),
then all lines are repeated three or four times. The lines repeated four times are selected by the following equation.
[# of the repeating lines = 2 + N $\times$ M] ,
where N = 1,2,3,... and M= round{14÷(CH[5:0]-60)}.

The repeating line-number is limited to 16.


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
: added line
Standard Font(12*18)
Standard font in high vertical resolution
Height-controlled font


1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
: added line
Standard Font(12*18)
Standard font in more higher vertical resolution
Height-controlled font

PWM OUTPUT



The frequency of PWM signal (fPWM) is dependent on the horizontal flyback signal frequency and horizontal mode (320dots/line, ...) as shown in the following table.

Horizontal Mode	320 dots/line (f_{PWM})	480 dots/line (f_{PWM})	640 dots/line (f_{PWM})	800 dots/line (f_{PWM})
15kHz < Hf < 20kHz	(320/256) * Hf	(480/256) * Hf	(640/256) * Hf	(800/256) * Hf
20kHz < Hf < 35kHz				(800/256) * (Hf/2)
35kHz < Hf < 50kHz			(640/256) * (Hf/2)	
50kHz < Hf < 65kHz		(480/256) * (Hf/2)		
65kHz < Hf < 80kHz				(800/256) * (Hf/4)
80kHz < Hf < 95kHz	(320/256) * (Hf/2)		(640/256) * (Hf/4)	
95kHz < Hf < 110kHz				
110kHz < Hf < 120kHz				

FRAME CONTROL & TIMING

Figure 7 shows the composition of display frame with the OSD characters.

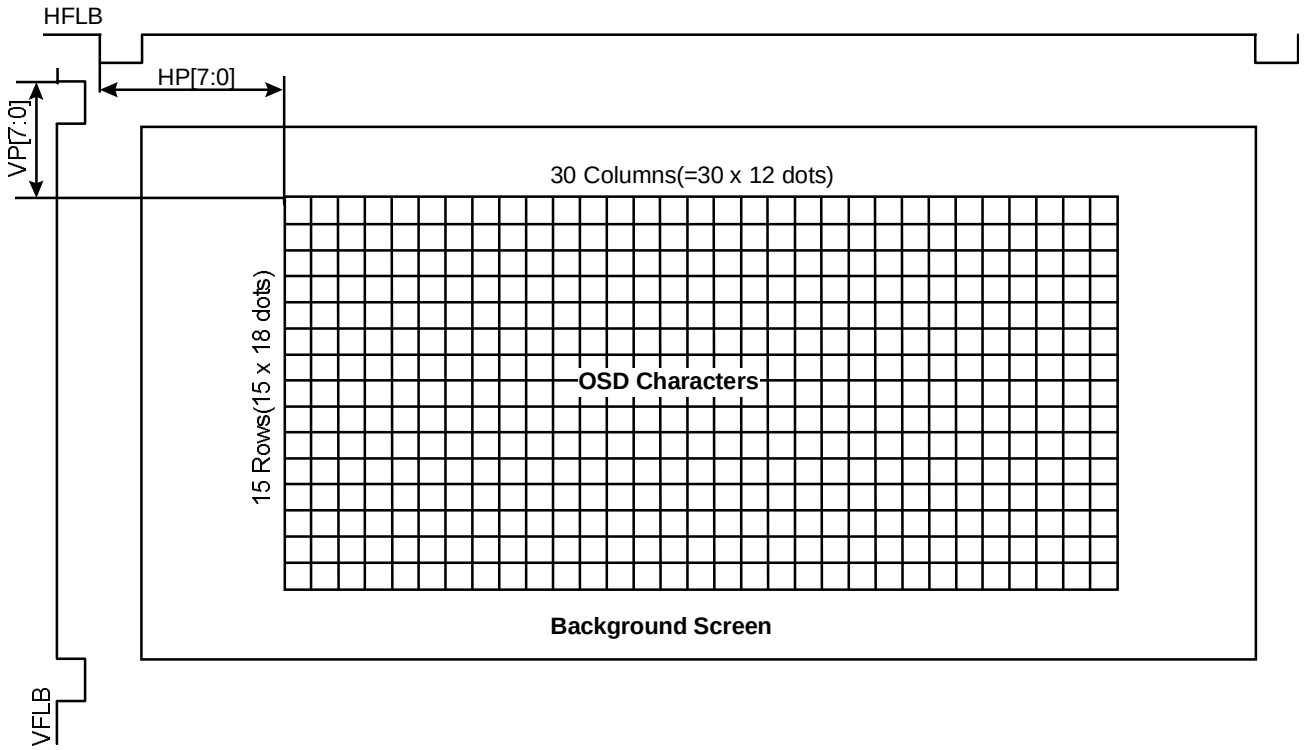


Figure 7. Frame Composition with the OSD Characters

User can determine the dot frequency by the equation of H freq. x the number of horizontal resolution.
And the number of horizontal resolution is determined by the bit9 - 8 (dot 1,dot 0) of the frame Control registers-1.
If dot 0 = “0”, dot 1 = “0”, then the dot frequency is calculated by the equation of H freq. × 320. If the H freq. = 15 kHz, then the dot frequency is 15 kHz × 320 = 4.8 MHz.
If dot 0 = “1”, dot 1 = “1” and the horizontal frequency is 120 kHz, then the dot frequency is 120 kHz × 800 = 96 MHz. 96 MHz is the maximum clock frequency in this processor.

REGISTER DESCRIPTION

◆ **Character & Attribute Register : Row00~14, Column00~29**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
BINV	BOX1	BOX0	B	G	R	Blink/FINT	C8	C7	C6	C5	C4	C3	C2	C1	C0
← Character Attribute →							← Character Code(464 Fonts) →								

◆ **Row Attribute Register : Row00~14, Column30**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	BREN	INTE	CBli	BOXE	BORD	SHA	RB	RG	RR	RINT	CINT	HZ1	HZ0	VZ1	VZ0
							← Raster Color →			← Intensity →		← Character Size →			

◆ **Frame Control Register 0 : Row15, Column00**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	Fde	FdeT	VPOL	HPOL	WC	WBOR	WSHA	-	Erase	EN	ScrI	ScrT	Bli1	Bli0	BliT

◆ **Frame Control Register 1 : Row15, Column01**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
CP1	CP0	FpII	HF2	HF1	HF0	dot1	dot0	-	FBLK	CH5	CH4	CH3	CH2	CH1	CH0
← PLL Control →										← Character Height Control →					

◆ **Frame Control Register 2 : Row15, Column02**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
← Horizontal Start Position →								← Vertical Start Position →							

◆ **Frame Control Register 3 : Row15, Column03**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
RS2	RS1	RS0	RSB	RSG	RSR	RSI	STR3	STR2	STR1	STR0	STC4	STC3	STC2	STC1	STC0
← Row Space →			← Row Space Color →				← Window Start Position →								

◆ **Frame Control Register 4 : Row15, Column04**

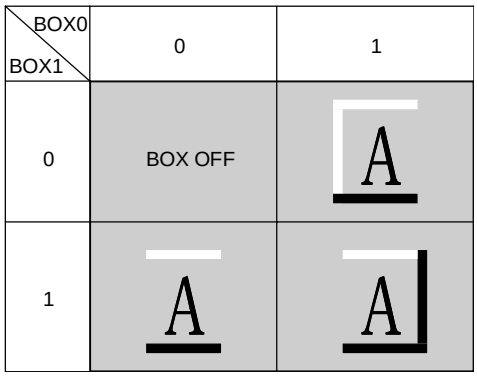
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
-	BW1	BW0	HW1	HW0	VW1	VW0	SPR3	SPR2	SPR1	SPR0	SPC4	SPC3	SPC2	SPC1	SPC0
							← Window Stop Position →								

◆ **PWM Registers : Row15, Column05~08**

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
MSB							LSB	MSB							LSB
← Channel 2/4/6/8 →								← Channel 1/3/5/7 →							

'-' ; Don't care bit

Table 4. Register Description

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="4">Character & Attribute Register (Row 00—14, Column 00—29)</td><td>C8—C0
(Bit 8—0)</td><td>Character Code Address of 464 ROM Fonts.</td></tr>
<tr><td>Blink
(Bit 9)</td><td>Character Blinking.
Set this bit to activate the blinking effect. The blinking period is set by the 'Bli T' bit and the duty is selected by the 'Bli 0' and 'Bli 1' bits. If ‘INTE’ bit is high, this bit controls the font intensity combined with ‘INTE’, ’RINT’ and ‘CINT’ as following table.
<table>
<tr><th>INTE</th><th>Blink</th><th>RINT</th><th>CINT</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>-</td><td>-</td><td>Normal</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>-</td><td>Blink</td></tr>
<tr><td>1</td><td>0</td><td>-</td><td>-</td><td>Normal</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Character Intensity</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Raster Intensity</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Character & Raster Intensity</td></tr>
</table></td></tr>
<tr><td>B,G,R
(Bit C—A)</td><td>Character Color is determined by these bits.
8 colors can be selected and the color intensity of a character is given by 'CINT' bit of Row Attribute Regisers.
So you can select up to 16 colors. If a multi-color font is selected, this bits must be set to all 0's.</td></tr>
<tr><td>BOX 1,
BOX0
(Bit E, D)</td><td>Character Box Drawing.
The combinations of this two bits generate four different box drawing modes as following. The following example is the case that box dawing is activated with the font 'A'.


* Bit F — D (RB/RG/RR) is also used for raster color by setting the 'BOXE' bit low. Raster color of a font is determined by this bits if the 'BOXE' bit is low. Priority of raster color selected here is higher than that of row attribute.</td></tr>
</table>

Table 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td>Character & Attribute Register</td><td>BINV
(Bit F)</td><td>Box Inversion.
The box drawing activated by the bit E and D is changed to white box from black and conversely.</td></tr>
<tr><td rowspan="7">Row Attribute Register
(Row 00 — 14, Column 30)</td><td>VZ1,VZ0
(Bit 1, 0)</td><td>Vertical Character Size Control.
Vertical character size is determined by the combinations of this two bits as following table.
<table><tr><th>VZ1</th><th>VZ0</th><th>Vertical Character Size</th></tr><tr><td>0</td><td>0</td><td>1X</td></tr><tr><td>0</td><td>1</td><td>2X</td></tr><tr><td>1</td><td>0</td><td>3X</td></tr><tr><td>1</td><td>1</td><td>4X</td></tr></table></td></tr>
<tr><td>HZ1,HZ0
(Bit 3, 2)</td><td>Horizontal Character Size Control.
The horizontal character size is determined by the combinations of this two bits as following table.
<table><tr><th>HZ1</th><th>HZ0</th><th>Horizontal Character Size</th></tr><tr><td>0</td><td>0</td><td>1X</td></tr><tr><td>0</td><td>1</td><td>2X</td></tr><tr><td>1</td><td>0</td><td>3X</td></tr><tr><td>1</td><td>1</td><td>4X</td></tr></table></td></tr>
<tr><td>CINT
(Bit 4)</td><td>Character Color Intensity.
If INTE, Blink and this bit is set, the color intensity of characters in the same row is high.</td></tr>
<tr><td>RINT
(Bit 5)</td><td>Raster Color Intensity.
If INTE, Blink and this bit is set, the color intensity of rasters in the same row is high</td></tr>
<tr><td>RB,RG,RR
(Bit 8—6)</td><td>Raster Color is determined by these bits.
8 colors can be selected and the color intensity of a character is given by 'RINT' bit of Row Attribute Registers.
So you can select up to 16 colors.</td></tr>
<tr><td>SHA
(BIT 9)</td><td>Character Shadowing.
Set this bit to activate characters shadowing.</td></tr>
<tr><td>BORD
(Bit A)</td><td>Character Bordering.
Set this bit to activate characters bordering.</td></tr>
</table>

Table 4. Register Description (Continued)

Registers	Bits	Description
Row Attribute Register	BOXE (Bit B)	BOX Enable. If this bit is set, Bit F-D in the Character & Attribute Registers are used for the box-drawing function. Otherwise,those are used for raster color of a font. Even though the raster color attribute is given by Bit 8-6 in the row attribute registers, the priority of Bit F-D in the character & attribute registers is higher.
	CBli (Bit C)	Color Blink Enable. If this bit is high, color blinking effect is activated. The color effect is to repeat color inversion between character and raster. Color blinking time and the duty is controlled byBil T, Bil 1 and Bli 0.
	INTE (Bit D)	Intensity Enable. If this bit and Blink bit(CHARACTER ATTRIBUTE) is high, character and raster intensity can be controlled.
	BREN (Bit E)	Back Raster Enable. If this bit is high and back raster color is black, back raster color is blank.
	Bit F	Reserved

Table 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="15">Frame Control Register 0
(Row 15, Column 00)</td><td>Bli T
(Bit 0)</td><td>Blink Time Control.
If this bit is high, the blink time is 0.5 sec. Otherwise, 1 sec.</td></tr>
<tr><td>Bli 1,Bli 0
(Bit 2,1)</td><td>Blinking Duty Control.
The blinking duty is controlled by the combination of this two bits as following.
<table><tr><th>Bli 1</th><th>Bli 0</th><th>Blinking Duty</th></tr><tr><td>0</td><td>0</td><td>Blink Off</td></tr><tr><td>0</td><td>1</td><td>Duty 25%</td></tr><tr><td>1</td><td>0</td><td>Duty 50%</td></tr><tr><td>1</td><td>1</td><td>Duty 75%</td></tr></table></td></tr>
<tr><td>ScrT
(Bit 3)</td><td>Scroll Time Control.
If this bit is high, the scroll time is 1 sec. Otherwise, 0.5 sec.</td></tr>
<tr><td>Scrl
(Bit 4)</td><td>Scroll Enable.
The scroll display is activated by setting this bit high.</td></tr>
<tr><td>EN
(Bit 5)</td><td>OSD Enable.
The character display is controlled by this bit. If this bit is high, OSD is enable. Otherwise, disable.</td></tr>
<tr><td>Erase
(Bit 6)</td><td>RAM Erasing.
RAM data are erased by setting this bit.</td></tr>
<tr><td>WSHA
(Bit 8)</td><td>Window Shadowing.
Set this bit to activate window shadowing.</td></tr>
<tr><td>WBOR
(Bit 9)</td><td>Window Bordering.
Set this bit to activate window bordering.</td></tr>
<tr><td>WC
(Bit A)</td><td>White/black selection of window border and shadow.
If this bit is high, the color of window border and shadow is white. Otherwise, black.</td></tr>
<tr><td>HPOL
(Bit B)</td><td>Polarity of Horizontal Fly Back Signal. Positive 1, Negative 0</td></tr>
<tr><td>VPOL
(Bit C)</td><td>Polarity of Vertical Fly Back Signal. Positive 1, Negative 0</td></tr>
<tr><td>FdeT
(Bit D)</td><td>Fade-in and fade-out Time Control.
If this bit is high, the time is 1 sec. Otherwise, 0.5 sec.</td></tr>
<tr><td>Fde
(Bit E)</td><td>Fade-in and fade-out Enable.
The fade-in and fade-out effect is activated by setting this bit high.</td></tr>
<tr><td>Bit F</td><td>Reserved.</td></tr>
</table>

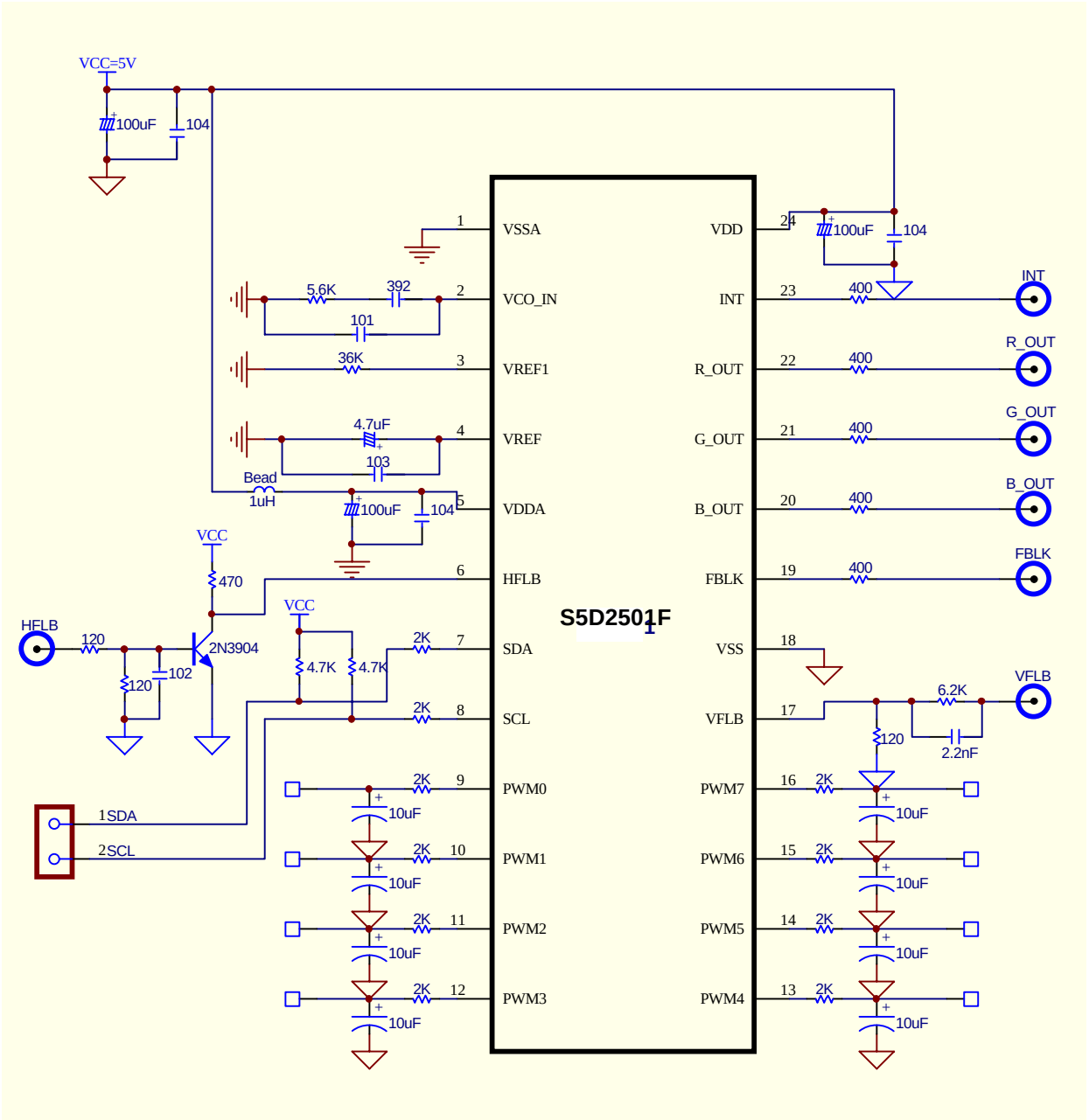
Table 4. Register Description (Continued)

<table>
<tr><th>Registers</th><th>Bits</th><th>Description</th></tr>
<tr><td rowspan="5">Frame Control Register 1
(Row 15, Column 01)</td><td>CH5—CH0
(Bit 5—0)</td><td>Character Height Control.
The vertical character size is determined by the bit 'VZ1' and VZ0'.
This six bits are available to get a proper character height by setting a binary value. According to the value made by this six bits, the character height is determined.
If the value is 32, the number of vertical pixel of character font is 32.
Eventually, the character height is expanded from 18 to 63.
The binary vlaue must be greater than 18.</td></tr>
<tr><td>FBLK
(Bit 6)</td><td>It determines the configuration of FBLK output pin.
When it is clear, FBLK pin outputs high during displaying characters or rasters. Otherwise,FBLK pin outputs high only during displaying characters.</td></tr>
<tr><td>dot 1,dot 0
(Bit 9,8)</td><td>This two bits determine the number of dots per horizontal line.
Refer to following table.
<table>
<tr><th>dot 1</th><th>dot 0</th><th>No. of Dots</th></tr>
<tr><td>0</td><td>0</td><td>320 dots/line</td></tr>
<tr><td>0</td><td>1</td><td>480 dots/line</td></tr>
<tr><td>1</td><td>0</td><td>640 dots/line</td></tr>
<tr><td>1</td><td>1</td><td>800 dots/line</td></tr>
</table></td></tr>
<tr><td>HF2—HF0
(Bit C—A)</td><td>These three bits decide horizontal frequency range (region).
Please refer to Application Note for more information.</td></tr>
<tr><td>FPLL
(Bit D)</td><td>If this bit is high, the VCO block of OSD_PLL operates on full range (4 MHz - 96 MHz).</td></tr>
<tr><td>Frame Control Register 1
(Row 15, Column 01)</td><td>CP 1,CP 0
(Bit F,E)</td><td>This bit controls charge pump output current.
<table>
<tr><th>CP 1</th><th>CP 0</th><th>Charge Pump Current</th></tr>
<tr><td>0</td><td>0</td><td>0.75mA</td></tr>
<tr><td>0</td><td>1</td><td>1 mA</td></tr>
<tr><td>1</td><td>0</td><td>1.25mA</td></tr>
<tr><td>1</td><td>1</td><td>1.5 mA</td></tr>
</table></td></tr>
<tr><td rowspan="2">Frame Control Register 2
(Row 15, Column 02)</td><td>VP7—VP0
(Bit 7—0)</td><td>Vertical Start Position Control.
It means the top margin height from the V-sync reference edge.
(= VP[7:0] $\times$ 4)</td></tr>
<tr><td>HP7—HP0
(Bit F—8)</td><td>Horizontal Start Position Control.
It means the horizontal display delay from the H-sync reference edge to the 1'st pixel position of characters. (= HP[7:0] $\times$ 6)</td></tr>
</table>

Table 4. Register Description (Continued)

Registers	Bits	Description
Frame Control Register 3 (Row 15, Column 02)	STC 4 —STC 0	Window Start Column Position. It means the column address that window starts from.
	STR 3 —STR 0	Window Start Row Position. It means the row address that window starts from.
	RSI	Row Space Color Intensity.
	RSR,RSG, RSB	Row Space Color Attribute.
	RS2—RS0 (Bit F—D)	Row Space. It means the line number between a character row and the next row. The defaut value is 0. (line number for spacing = RS[2:0] $\times$ 2)
Frame Control Register 4 (Row 15, Column 04)	SPC 4— SPC 0	Window Stop Column Position. It means the column address that window stops on.
	SPR 3— SPR 0	Window Stop Row Position. It means the row address that window stops on.
	VW 1, 0	Vertical width of window shadowing.
	HW 1, 0	Horizontal width of window shadowing.
	BW 1, 0	Width of window bordering.
PWM Registers (Row 15, Column 05 - 08)	Bit 7— 0	This 8-bit value decides the output duty cycle and waveforms of PWM for channel 1,3,5 and 7.
	Bit F—8	This 8-bit value decides the output duty cycle and waveforms of PWM for channel 2,4,6 and 8.

APPLICATION CIRCUIT



SAMSUNG ELECTRONICS