

#### Features

- ESD protection for two lines with bi-direction
- Provide transient protection for each line to IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact) IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 20A (8/20µs)
- 0402 small DFN package saves board space
- Protect two I/O lines or two power lines
- Fast turn-on and low clamping voltage
- Suitable for, **6.3V and below**, operating voltage applications
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part

## Applications

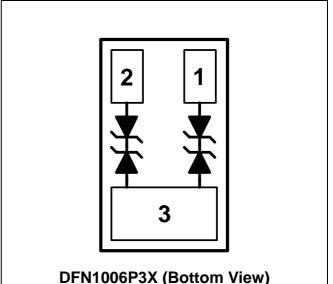
- Power supply protection
- Data and I/O lines protection
- Panels
- Portable devices
- Consumer electronics
- Notebooks, desktops, and servers
- Peripherals

## Description

AZ5946-02F is a design which includes two bi-directional ESD rated clamping cells to protect two power lines, or two control lines, or two low-speed data lines in an electronic system. The AZ5946-02F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning. AZ5946-02F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines, control lines or data lines, protecting any downstream components.

AZ5946-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm$ 15kV air,  $\pm$ 8kV contact discharge).

# Circuit Diagram / Pin Configuration



# Specifications

Absolute Maximum Ratings ( $T_A$ = 25°C, unless otherwise specified)				
Parameter	Symbol	Rating	Unit	
Peak Pulse Current (t <sub>p</sub> =8/20µs)	I <sub>PP</sub> (Note 1)	20	А	
Operating Voltage (Pin-1, -2 to pin-3)	V <sub>DC</sub>	±6.5	V	
ESD per IEC 61000-4-2 (Air)	V <sub>ESD-1</sub>	±30	kV	
ESD per IEC 61000-4-2 (Contact)	$V_{ESD-2}$	±30	κv	
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C	
Operating Temperature	T <sub>OP</sub>	-55 to +125	°C	
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C	

Electrical Characteristics						
Parameter	Symbol	Condition	Тур	Max	Unit	
Reverse Stand-Off Voltage	V <sub>RWM</sub>	T= 25°C.	-6.3		6.3	V
Reverse Leakage Current	I <sub>Leak</sub>	$V_{RWM} = \pm 6.3 V$ , T= 25°C.	$V_{RWM} = \pm 6.3 V, T = 25^{\circ}C.$ 1			μΑ
Reverse Breakdown Voltage	$V_{BV}$	I <sub>BV</sub> = 1mA, T= 25°C.	6.6		9	V
Surge Clamping Voltage (Note 1)	V <sub>CL-surge</sub>	$I_{PP} = 5A$ , $t_p = 8/20\mu s$ , pin-1, -2 to pin-3, T= 25°C.		8.4		V
		I <sub>PP</sub> = 20A, t <sub>p</sub> = 8/20μs, pin-1, -2 to pin-3, T= 25°C.		11.5		V
ESD Clamping Voltage (Note 2)	V <sub>CL-ESD</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), contact mode, pin-1, -2 to pin-3, T= 25°C.		9		V
ESD Dynamic Turn-on Resistance	R <sub>dynamic</sub>	IEC 61000-4-2 0~+8kV, contact mode, pin-1, -2 to pin-3, T= 25°C.		0.09		Ω
Channel Input Capacitance	C <sub>IN</sub>	$V_R = 0V$ , f = 1MHz, pin-1, -2 to pin-3, T= 25°C.		35	45	pF

Note 1: The Peak Pulse Current measured conditions:  $t_p = 8/20\mu s$ , 20hm source impedance.

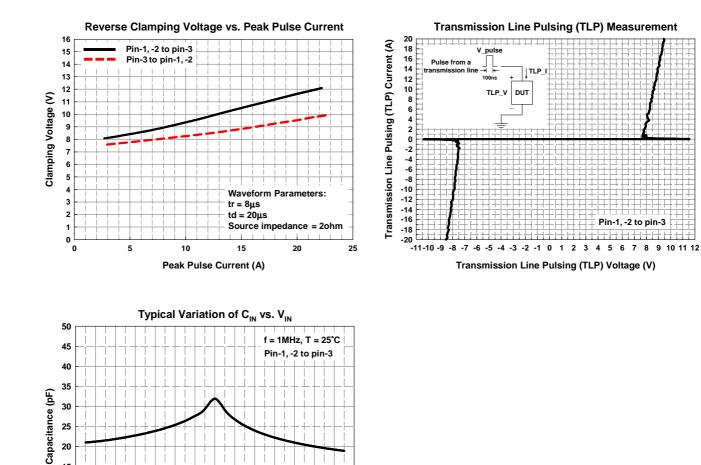
Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions:  $Z_0 = 50\Omega$ ,  $t_p = 100$ ns,  $t_r = 1$ ns.



# **Typical Characteristics**

15 10 5 0 -7 -6 -5 -4 -3 -2



0

-1 Input Voltage (V)

2 3 4 5 6 7



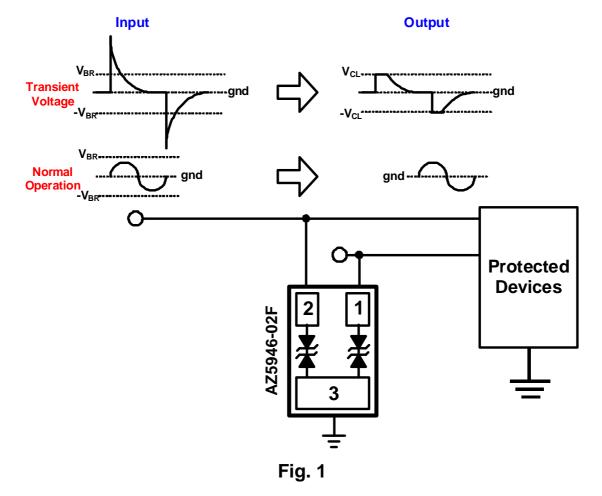
#### **Application Information**

The AZ5946-02F is designed to protect two lines against system ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5946-02F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin-1 and pin-2, respectively. The pin-3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5946-02F should be kept as short as possible.

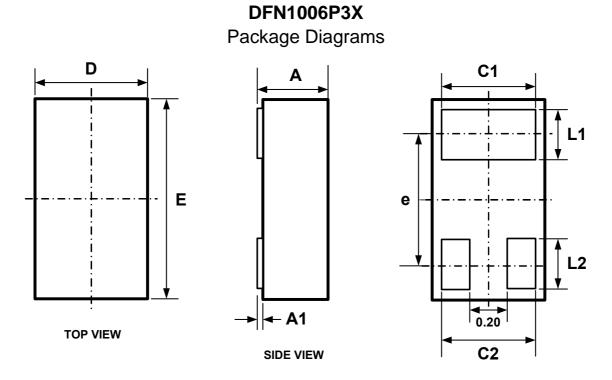
In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5946-02F.
- Place the AZ5946-02F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.





## **Mechanical Details**



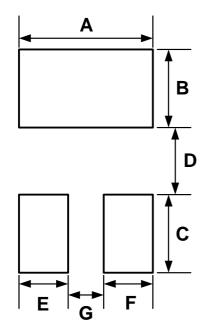
**BOTTOM VIEW** 

#### Package Dimensions

Symbol	Millimeters			Inches		
Symbol	Min.	Nom.	Max.	Min.	Nom.	Max.
E	0.95	1.00	1.05	0.037	0.039	0.041
D	0.55	0.60	0.65	0.022	0.024	0.026
Α	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
C1	0.45	0.50	0.55	0.018	0.020	0.022
C2	0.45	0.50	0.55	0.018	0.020	0.022
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012
е	0.65 BSC				0.026BSC	



## Land Layout

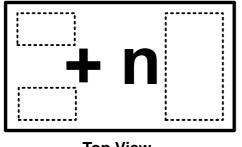


Dimensions					
Index	Index Millimeter Inches				
A	0.600	0.024			
В	0.350	0.014			
С	0.350	0.014			
D	0.300	0.012			
E	0.225	0.009			
F	0.225	0.009			
G	0.150	0.006			

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

# Marking Code



Top View n= device code

Part Number	Marking Code
AZ5946-02F.R7GR (Green part)	n

Note. Green means Pb-free, RoHS, and Halogen free compliant.



# **Ordering Information**

PN#	Material	Туре	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5946-02F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels=48,000/box	6 boxes=288,000/carton

#### **Revision History**

Revision	Modification Description
Revision 2019/11/05	Formal Release.