RX5001

315.00 MHz Hybrid Receiver

- ***Designed for Short-Range Wireless Control and Data Communications***
- ***Supports RF Data Transmission Rates Up to 115.2 kbps***
- ***3 V, Low Current Operation plus Sleep Mode***
- ***Stable, Easy to Use, Low External Parts Count***
- ***Complies with Directive 2002/95/EC (RoHS)***

The RX5001 hybrid receiver is ideal for short-range wireless control and data applications where robust operation, small size, low power consumption and low cost are required. The RX5001 employs RFM's amplifier-sequenced hybrid (ASH) architecture to achieve this unique blend of characteristics. All critical RF functions are contained in the hybrid, simplifying and speeding design-in. The RX5001 is sensitive and stable. A wide dynamic range log detector, in combination with digital AGC and a compound data slicer, provide robust performance in the presence of on-channel interference or noise. Two stages of SAW filtering provide excellent receiver out- of-band rejection. The RX5001 generates virtually no RF emissions, facilitating compliance with FCC Part 15 and similar regulations.



SM-20L Case

Rating	Value	Units
Power Supply and All Input/Output Pins	-0.3 to +4.0	V
Non-Operating Case Temperature	-50 to +100	°C
Soldering Temperature (10 seconds / 5 cycles max.)	260	°C

Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	f_o		314.80		315.20	MHz
Modulation Types				OOK & ASK		
Data Rate					115.2	kbps
Receiver Performance, High Sensitivity Mode						
Sensitivity, 2.4 kbps, 10-3 BER, AM Test Method		1		-109		dBm
Sensitivity, 2.4 kbps, 10-3 BER, Pulse Test Method		1		-103		dBm
Current, 2.4 kbps (R_{PR} = 330 K)		2		3.0		mA
Sensitivity, 19.2 kbps, 10-3 BER, AM Test Method		1		-105		dBm
Sensitivity, 19.2 kbps, 10-3 BER, Pulse Test Method		1		-99		dBm
Current, 19.2 kbps (R_{PR} = 330 K)		2		3.1		mA
Sensitivity, 115.2 kbps, 10-3 BER, AM Test Method		1		-101		dBm
Sensitivity, 115.2 kbps, 10-3 BER, Pulse Test Method		1		-95		dBm
Current, 115.2 kbps				3.8		mA
Receiver Performance, Low Current Mode						
Sensitivity, 2.4 kbps, 10-3 BER, AM Test Method		1		-104		dBm
Sensitivity, 2.4 kbps, 10-3 BER, Pulse Test Method		1		-98		dBm
Current, 2.4 kbps (R_{PR} = 1100 K)		2		1.8		mA

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Electrical Characteristics (typical values given for 3.0 Vdc power supply, 25 °C)

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Receiver Out-of-Band Rejection, ±5% fo	$R_{\pm 5\%}$	3		80		dB
Receiver Ultimate Rejection	R_{ULT}	3		100		dB
Sleep Mode Current	I_S			0.7		µA
Power Supply Voltage Range	V_{CC}		2.2		3.7	Vdc
Power Supply Voltage Ripple					10	mV_{P-P}
Ambient Operating Temperature	T_A		-40		85	°C

Notes:

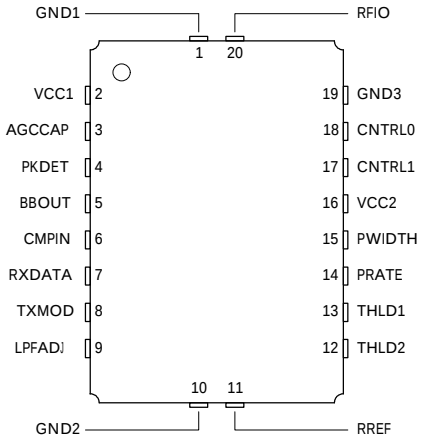
1. Typical sensitivity data is based on a 10^{-3} bit error rate (BER), using DC-balanced data. There are two test methods commonly used to measure OOK/ASK receiver sensitivity, the "100% AM" test method and the "Pulse" test method. Sensitivity data is given for both test methods. See Appendix 3.8 in the *ASH Transceiver Designer's Guide* for the details of each test method, and for sensitivity curves for a 2.2 to 3.7 V supply voltage range at five operating temperatures. The application/test circuit and component values are shown on the next page and in the *Designer's Guide*.

2. At low data rates it is possible to adjust the ASH pulse generator to trade-off some receiver sensitivity for lower operating current. Sensitivity data and receiver current are given at 2.4 kbps for both high sensitivity operation (R_{PR} = 330 K) and low current operation (R_{PR} = 1100 K).

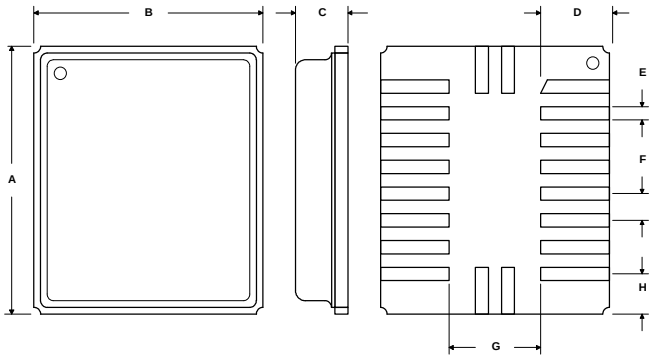
3. Data is given with the ASH radio matched to a 50 ohm load. Matching component values are given on the next page.

4. See Table 1 on Page 8 for additional information on ASH radio event timing.

ASH Transceiver Pin Out



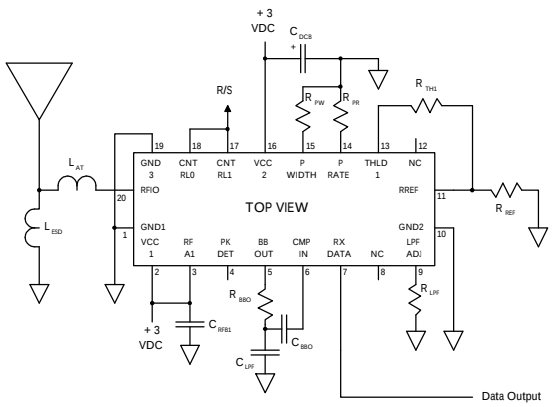
SM-20L Package Drawing



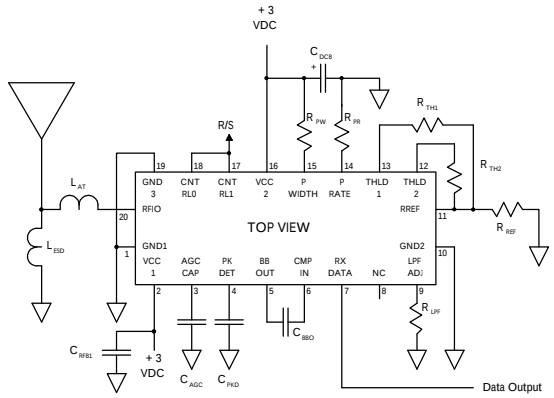
Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	10.795	10.922	11.049	.425	.430	.435
B	9.525	9.652	9.779	.375	.380	.385
C	1.778	1.905	2.032	.070	.075	.080
D	3.048	3.175	3.302	.120	.125	.130
E	0.381	0.508	0.635	.015	.020	.025
F	0.889	1.016	1.143	.035	.040	.045
G	3.175	3.302	3.429	.125	.130	.135
H	1.778	1.905	2.032	.070	.075	0.80

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ASH Receiver Application Circuit
OOK Configuration



ASH Receiver Application Circuit
ASK Configuration



Receiver Set-Up, 3.0 Vdc, -40 to +85 °C

Item	Symbol	OOK	OOK	ASK	Units	Notes
Nominal NRZ Data Rate	DR_{NOM}	2.4	19.2	115.2	kbps	see page 1& 2
Minimum Signal Pulse	SP_{MIN}	416.67	52.08	8.68	µs	single bit
Maximum Signal Pulse	SP_{MAX}	1666.68	208.32	34.72	µs	4 bits of same value
AGCCAP Capacitor	C_{AGC}	-	-	2200	pF	±10% ceramic
PKDET Capacitor	C_{PKD}	-	-	0.001	µF	±10% ceramic
BBOUT Capacitor	C_{BBO}	0.1	0.015	0.0027	µF	±10% ceramic
BBOUT Resistor	R_{BBO}	12	0	0	K	±5%
LPFAUX Capacitor	C_{LPF}	0.0047	-	-	µF	±5%
LPFADJ Resistor	R_{LPF}	300	100	15	K	±5%
RREF Resistor	R_{REF}	100	100	100	K	±1%
THLD2 Resistor	R_{TH2}	-	-	100	K	±1%, for 6 dB below peak
THLD1 Resistor	R_{TH1}	0	0	10	K	±1%, typical values
PRATE Resistor	R_{PR}	330	330	160	K	±5%
PWIDTH Resistor	R_{PW}	270 to GND	270 to GND	1000 to Vcc	K	±5%
DC Bypass Capacitor	C_{DCB}	4.7	4.7	4.7	µF	tantalum
RF Bypass Capacitor 1	C_{RFB1}	100	100	100	pF	±5% NPO
Antenna Tuning Inductor	L_{AT}	82	82	82	nH	50 ohm antenna
Shunt Tuning/ESD Inductor	L_{ESD}	33	33	33	nH	50 ohm antenna

CAUTION: Electrostatic Device. Observe precautions when handling.

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ASH Receiver Theory of Operation

Introduction

RFM's RX5000 series amplifier-sequenced hybrid (ASH) receivers are specifically designed for short-range wireless control and data communication applications. The receivers provide robust operation, very small size, low power consumption and low implementation cost. All critical RF functions are contained in the hybrid, simplifying and speeding design-in. The ASH receiver can be readily configured to support a wide range of data rates and protocol requirements. The receiver features virtually no RF emissions, making it easy to certify to short-range (unlicensed) radio regulations.

Amplifier-Sequenced Receiver Operation

The ASH receiver's unique feature set is made possible by its system architecture. The heart of the receiver is the amplifier- sequenced receiver section, which provides more than 100 dB of stable RF and detector gain without any special shielding or decoupling provisions. Stability is achieved by distributing the total RF gain over *time*. This is in contrast to a superheterodyne receiver, which achieves stability by distributing total RF gain over multiple frequencies.

Figure 1 shows the basic block diagram and timing cycle for an amplifier-sequenced receiver. Note that the bias to RF amplifiers RFA1 and RFA2 are independently controlled by a pulse generator, and that the two amplifiers are coupled by a surface acoustic wave (SAW) delay line, which has a typical delay of 0.5 µs.

An incoming RF signal is first filtered by a narrow-band SAW filter, and is then applied to RFA1. The pulse generator turns RFA1 ON for 0.5 µs. The amplified signal from RFA1 emerges from the SAW delay line at the input to RFA2. RFA1 is now switched OFF and RFA2 is switched ON for 0.55 µs, amplifying the RF signal further. The ON time for RFA2 is usually set at 1.1 times the ON time for RFA1, as the filtering effect of the SAW delay line stretches the signal pulse from RFA1 somewhat. As shown in the timing diagram, RFA1 and RFA2 are never on at the same time, assuring excellent receiver stability. Note that the narrow-band SAW filter eliminates sampling sideband responses outside of the receiver passband, and the SAW filter and delay line act together to provide very high receiver ultimate rejection.

Amplifier-sequenced receiver operation has several interesting characteristics that can be exploited in system design. The RF amplifiers in an amplifier-sequenced receiver can be turned on and off almost instantly, allowing for very quick power-down (sleep) and wake-up times. Also, both RF amplifiers can be off between ON sequences to trade-off receiver noise figure for lower average current consumption. The effect on noise figure can be modeled as if RFA1 is on continuously, with an attenuator placed in front of it with a loss equivalent to $10*\log_{10}$(RFA1 duty factor), where the duty factor is the average amount of time RFA1 is ON (up to 50%). Since an amplifier-sequenced receiver is inherently a sampling receiver, the overall cycle time between the start of one RFA1 ON sequence and the start of the next RFA1 ON sequence should be set to sample the narrowest RF data pulse at least 10 times. Otherwise, significant edge jitter will be added to the detected data pulse.

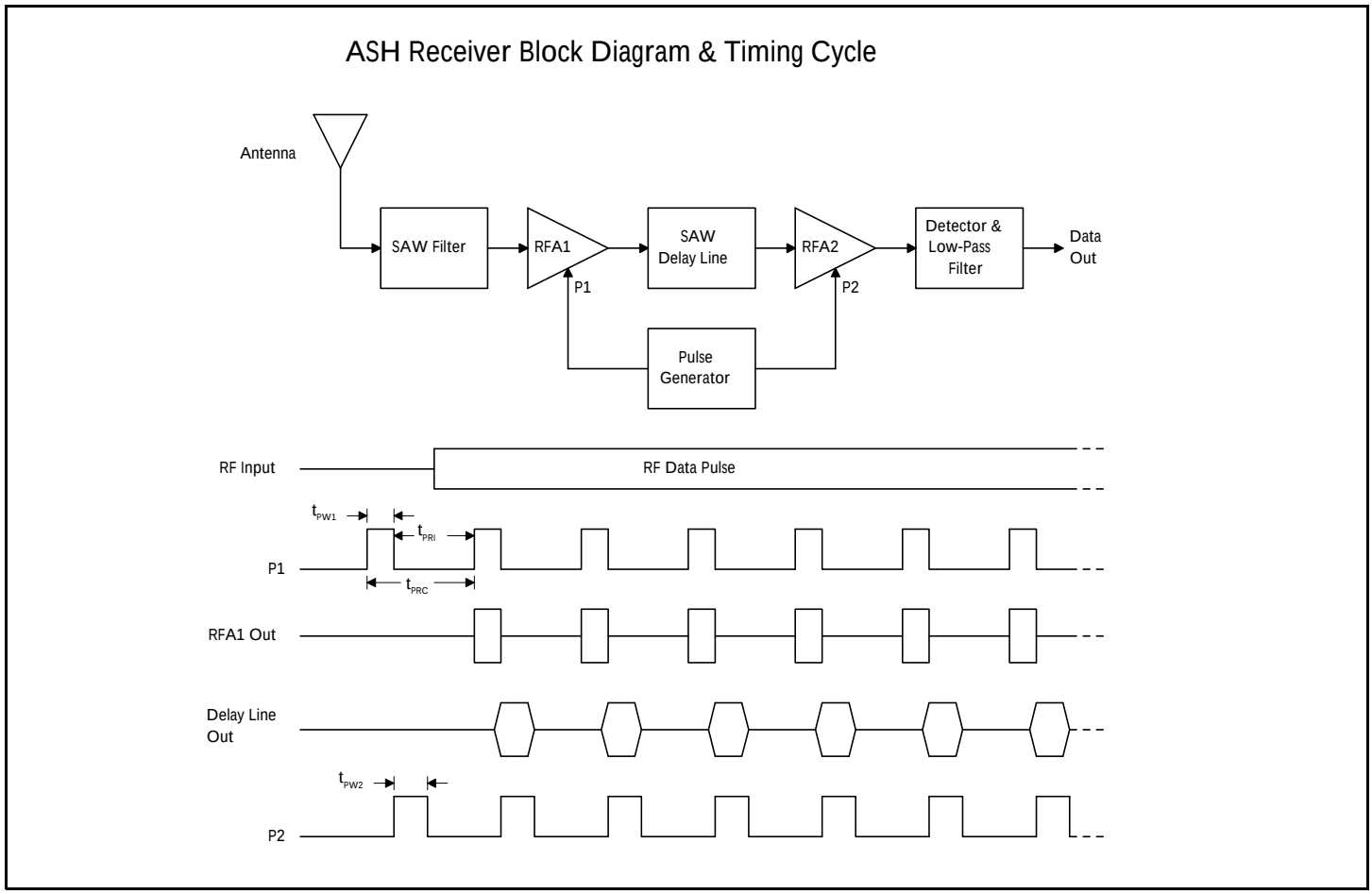


Figure 1

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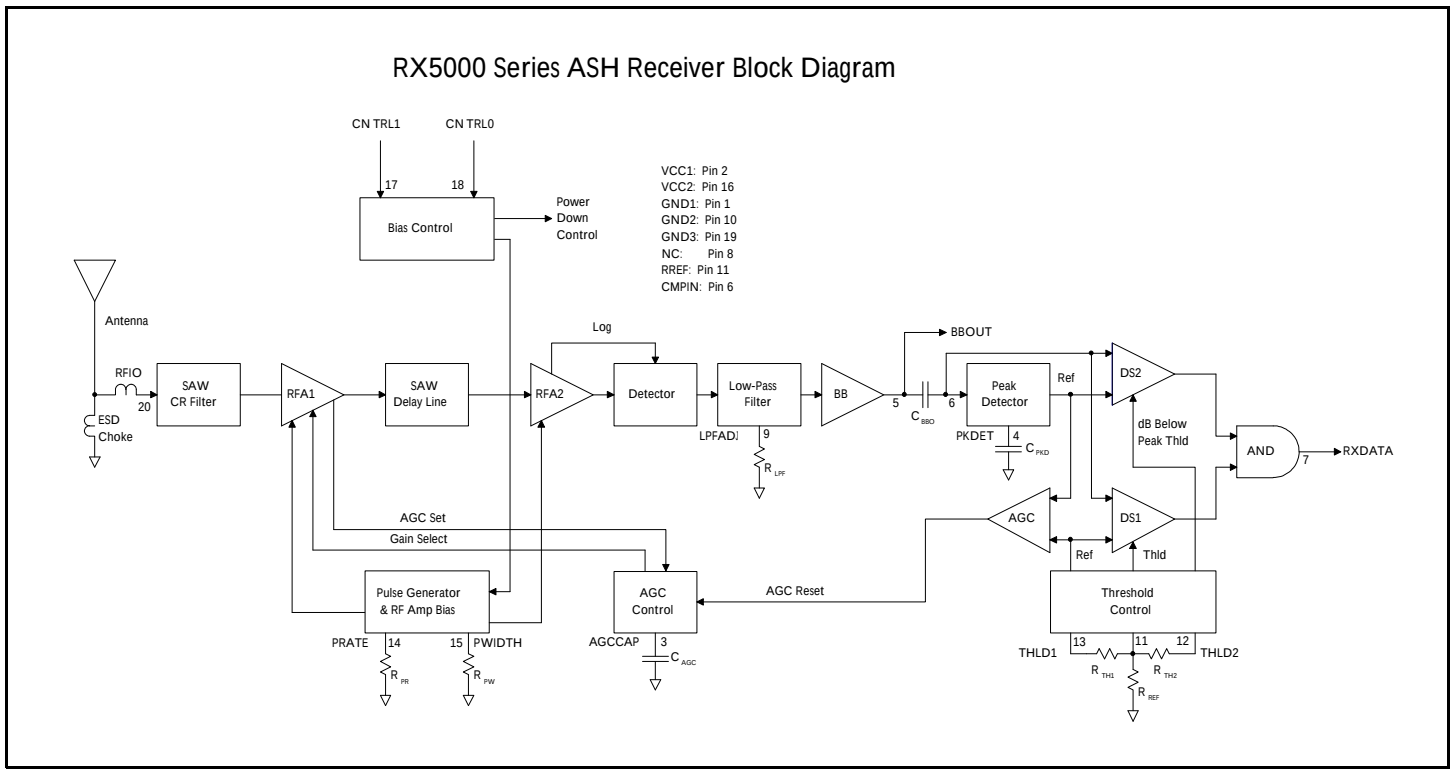


Figure 2

RX5000 Series ASH Receiver Block Diagram

Figure 2 is the general block diagram of the RX5000 series ASH receiver. Please refer to Figure 2 for the following discussions.

Antenna Port

The only external RF components needed for the receiver are the antenna and its matching components. Antennas presenting an impedance in the range of 35 to 72 ohms resistive can be satisfactorily matched to the RFIO pin with a series matching coil and a shunt matching/ESD protection coil. Other antenna impedances can be matched using two or three components. For some impedances, two inductors and a capacitor will be required. A DC path from RFIO to ground is required for ESD protection.

Receiver Chain

The output of the SAW filter drives amplifier RFA1. This amplifier includes provisions for detecting the onset of saturation (AGC Set), and for switching between 35 dB of gain and 5 dB of gain (Gain Select). AGC Set is an input to the AGC Control function, and Gain Select is the AGC Control function output. ON/OFF control to RFA1 (and RFA2) is generated by the Pulse Generator & RF Amp Bias function. The output of RFA1 drives the SAW delay line, which has a nominal delay of 0.5 µs.

The second amplifier, RFA2, provides 51 dB of gain below saturation. The output of RFA2 drives a full-wave detector with 19 dB of threshold gain. The onset of saturation in each section of RFA2 is detected and summed to provide a logarithmic response. This is added to the output of the full-wave detector to produce an overall detector response that is square law for low signal levels, and transitions into a log response for high signal levels. This combination provides excellent threshold sensitivity and more than 70 dB of detector dynamic range. In combination with the 30 dB of AGC range in RFA1, more than 100 dB of receiver dynamic range is achieved.

The detector output drives a gyrator filter. The filter provides a three-pole, 0.05 degree equiripple low-pass response with excellent group delay flatness and minimal pulse ringing. The 3 dB bandwidth of the filter can be set from 4.5 kHz to 1.8 MHz with an external resistor.

The filter is followed by a base-band amplifier which boosts the detected signal to the BBOUT pin. When the receiver RF amplifiers are operating at a 50%-50% duty cycle, the BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 685 mV. For lower duty cycles, the mV/dB slope and peak-to-peak signal level are proportionately less. The detected signal is riding on a 1.1 Vdc level that varies somewhat with supply voltage, temperature, etc. BBOUT is coupled to the CMPIN pin or to an external data recovery process (DSP, etc.) by a series capacitor. The correct value of the series capacitor depends on data rate, data run length, and other factors as discussed in the *ASH Transceiver Designer's Guide*.

When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and CMPIN by separate series coupling capacitors. The AGC reset function is driven by the signal applied to CMPIN.

When the receiver is placed in the power-down (sleep) mode, the output impedance of BBOUT becomes very high. This feature helps preserve the charge on the coupling capacitor to minimize data slicer stabilization time when the receiver switches out of the sleep mode.

Data Slicers

The CMPIN pin drives two data slicers, which convert the analog signal from BBOUT back into a digital stream. The best data slicer choice depends on the system operating parameters. Data slicer DS1 is a capacitively-coupled comparator with provisions for an adjustable threshold. DS1 provides the best performance at low signal-to-noise conditions. The

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threshold, or squelch, offsets the comparator's slicing level from 0 to 90 mV, and is set with a resistor between the RREF and THLD1 pins. This threshold allows a trade- off between receiver sensitivity and output noise density in the no-signal condition. For best sensitivity, the threshold is set to 0. In this case, noise is output continuously when no signal is present. This, in turn, requires the circuit being driven by the RXDATA pin to be able to process noise (and signals) continuously.

This can be a problem if RXDATA is driving a circuit that must "sleep" when data is not present to conserve power, or when it its necessary to minimize false interrupts to a multitasking processor. In this case, noise can be greatly reduced by increasing the threshold level, but at the expense of sensitivity. The best 3 dB bandwidth for the low-pass filter is also affected by the threshold level setting of DS1. The bandwidth must be increased as the threshold is increased to minimize data pulse-width variations with signal amplitude.

Data slicer DS2 can overcome this compromise once the signal level is high enough to enable its operation. DS2 is a "dB-below- peak" slicer. The peak detector charges rapidly to the peak value of each data pulse, and decays slowly in between data pulses (1:1000 ratio). The slicer trip point can be set from 0 to 120 mV below this peak value with a resistor between RREF and THLD2. A threshold of 60 mV is the most common setting, which equates to "6 dB below peak" when RFA1 and RFA2 are running a 50%-50% duty cycle. Slicing at the "6 dB-below-peak" point reduces the signal amplitude to data pulse-width variation, allowing a lower 3 dB filter bandwidth to be used for improved sensitivity.

DS2 is best for ASK modulation where the transmitted waveform has been shaped to minimize signal bandwidth. However, DS2 is subject to being temporarily "blinded" by strong noise pulses, which can cause burst data errors. Note that DS1 is active when DS2 is used, as RXDATA is the logical AND of the DS1 and DS2 outputs. DS2 can be disabled by leaving THLD2 disconnected. A non-zero DS1 threshold is required for proper AGC operation.

AGC Control

The output of the Peak Detector also provides an AGC Reset signal to the AGC Control function through the AGC comparator. The purpose of the AGC function is to extend the dynamic range of the receiver, so that the receiver can operate close to its transmitter when running ASK and/or high data rate modulation. The onset of saturation in the output stage of RFA1 is detected and generates the AGC Set signal to the AGC Control function. The AGC Control function then selects the 5 dB gain mode for RFA1. The AGC Comparator will send a reset signal when the Peak Detector output (multiplied by 0.8) falls below the threshold voltage for DS1.

A capacitor at the AGCCAP pin avoids AGC "chattering" during the time it takes for the signal to propagate through the low-pass filter and charge the peak detector. The AGC capacitor also allows the hold-in time to be set longer than the peak detector decay time to avoid AGC chattering during runs of "0" bits in the received data stream. Note that AGC operation requires the peak detector to be functioning, even if DS2 is not being used. AGC operation can be defeated by connecting the AGCCAP pin to Vcc. The AGC can be latched on once engaged by connecting a 150 kilohm resistor between the AGCCAP pin and ground in lieu of a capacitor.

Receiver Pulse Generator and RF Amplifier Bias

The receiver amplifier-sequence operation is controlled by the Pulse Generator & RF Amplifier Bias module, which in turn is controlled by the PRATE and PWIDTH input pins, and the Power Down (sleep) Control Signal from the Bias Control function.

In the low data rate mode, the interval between the falling edge of one RFA1 ON pulse to the rising edge of the next RFA1 ON pulse t_{PRI} is set by a resistor between the PRATE pin and ground. The interval can be adjusted between 0.1 and 5 µs. In the high data rate mode (selected at the PWIDTH pin) the receiver RF amplifiers operate at a nominal 50%-50% duty cycle. In this case, the start-to-start period t_{PRC} for ON pulses to RFA1 are controlled by the PRATE resistor over a range of 0.1 to 1.1 µs.

In the low data rate mode, the PWIDTH pin sets the width of the ON pulse t_{PW1} to RFA1 with a resistor to ground (the ON pulse width t_{PW2} to RFA2 is set at 1.1 times the pulse width to RFA1 in the low data rate mode). The ON pulse width t_{PW1} can be adjusted between 0.55 and 1 µs. However, when the PWIDTH pin is connected to Vcc through a 1 M resistor, the RF amplifiers operate at a nominal 50%-50% duty cycle, facilitating high data rate operation. In this case, the RF amplifiers are controlled by the PRATE resistor as described above.

Both receiver RF amplifiers are turned off by the Power Down Control Signal, which is invoked in the sleep mode.

Receiver Mode Control

The receiver operating modes – receive and power-down (sleep), are controlled by the Bias Control function, and are selected with the CNTRL1 and CNTRL0 control pins. Setting CNTRL1 and CNTRL0 both high place the unit in the receive mode. Setting CNTRL1 and CNTRL0 both low place the unit in the power-down (sleep) mode. CNTRL1 and CNTRL0 are CMOS compatible inputs. These inputs must be held at a logic level; they cannot be left unconnected.

Receiver Event Timing

Receiver event timing is summarized in Table 1. Please refer to this table for the following discussions.

Turn-On Timing

The maximum time t_{PR} required for the receive function to become operational at turn on is influenced by two factors. All receiver circuitry will be operational 5 ms after the supply voltage reaches 2.2 Vdc. The BBOUT-CMPIN coupling-capacitor is then DC stabilized in 3 time constants ($3*t_{BBC}$). The total turn-on time to stable receiver operation for a 10 ms power supply rise time is:

$t_{PR} = 15\ ms + 3*t_{BBC}$

Sleep and Wake-Up Timing

The maximum transition time from the receive mode to the power-down (sleep) mode t_{RS} is 10 µs after CNTRL1 and CNTRL0 are both low (1 µs fall time).

The maximum transition time t_{SR} from the sleep mode to the receive mode is $3*t_{BBC}$, where t_{BBC} is the BBOUT-CMPIN coupling-capacitor time constant. When the operating temperature is limited to 60 oC, the time required to switch from sleep to receive is dramatically less for short sleep times, as less charge leaks away from the BBOUT- CMPIN coupling capacitor.

AGC Timing

The maximum AGC engage time t_{AGC} is 5 µs after the reception of a -30 dBm RF signal with a 1 µs envelope rise time.

The minimum AGC hold-in time is set by the value of the capacitor at the AGCCAP pin. The hold-in time $t_{AGH} = C_{AGC}/19.1$, where t_{AGH} is in µs and C_{AGC} is in pF.

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Peak Detector Timing

The Peak Detector attack time constant is set by the value of the capacitor at the PKDET pin. The attack time $t_{PKA} = C_{PKD}/4167$, where t_{PKA} is in µs and C_{PKD} is in pF. The Peak Detector decay time constant $t_{PKD} = 1000*t_{PKA}$.

Pulse Generator Timing

In the low data rate mode, the interval t_{PRI} between the falling edge of an ON pulse to the first RF amplifier and the rising edge of the next ON pulse to the first RF amplifier is set by a resistor R_{PR} between the PRATE pin and ground. The interval can be adjusted between 0.1 and 5 µs with a resistor in the range of 51 K to 2000 K. The value of the R_{PR} is given by:

$R_{PR} = 404* t_{PRI} + 10.5$, where t_{PRI} is in µs, and R_{PR} is in kilohms

In the high data rate mode (selected at the PWIDTH pin) the receiver RF amplifiers operate at a nominal 50%-50% duty cycle. In this case, the period t_{PRC} from the start of an ON pulse to the first RF amplifier to the start of the next ON pulse to the first RF amplifier is controlled by the PRATE resistor over a range of 0.1 to 1.1 µs using a resistor of 11 K to 220 K. In this case R_{PR} is given by:

$R_{PR} = 198* t_{PRC} - 8.51$, where t_{PRC} is in µs and R_{PR} is in kilohms

In the low data rate mode, the PWIDTH pin sets the width of the ON pulse to the first RF amplifier t_{PW1} with a resistor R_{PW} to ground (the ON pulse width to the second RF amplifier t_{PW2} is set at 1.1 times the pulse width to the first RF amplifier in the low data rate mode). The ON pulse width t_{PW1} can be adjusted between 0.55 and 1 µs with a resistor value in the range of 200 K to 390 K. The value of R_{PW} is given by:

$R_{PW} = 404* t_{PW1} - 18.6$, where t_{PW1} is in µs and R_{PW} is in kilohms

However, when the PWIDTH pin is connected to Vcc through a 1 M resistor, the RF amplifiers operate at a nominal 50%-50% duty cycle, facilitating high data rate operation. In this case, the RF amplifiers are controlled by the PRATE resistor as described above.

LPF Group Delay

The low-pass filter group delay is a function of the filter 3 dB bandwidth, which is set by a resistor R_{LPF} to ground at the LPFADJ pin. The minimum 3 dB bandwidth $f_{LPF} = 1445/R_{LPF}$, where f_{LPF} is in kHz, and R_{LPF} is in kilohms.

The maximum group delay $t_{FGD} = 1750/f_{LPF} = 1.21*R_{LPF}$, where t_{FGD} is in µs, f_{LPF} in kHz, and R_{LPF} in kilohms.

Receiver Event Timing, 3.0 Vdc, -40 to +85 °C

Event	Symbol	Time	Min/Max	Test Conditions	Notes
Turn On to Receive	t_{PR}	$3*t_{BBC}$ + 15 ms	max	10 ms supply voltage rise time	time until receiver operational
Sleep to RX	t_{SR}	$3*t_{BBC}$	max	1 µs CNTRL0/CNTROL 1 rise times	time until receiver operational
RX to Sleep	t_{RS}	10 µs	max	1 µs CNTRL0/CNTROL 1 fall times	time until receiver is in power-down mode
AGC Engage	t_{AGC}	5 µs	max	1 µs rise time, -30 dBm signal	RFA1 switches from 35 to 5 dB gain
AGE Hold-In	t_{AGH}	$C_{AGC}/19.1$	min	CAGC in pF, t_{AGH} in µs	user selected; longer than t_{PKD}
PKDET Attack Time Constant	t_{PKA}	$C_{PKD}/4167$	min	C_{PKD} in pF, t_{PKA} in µs	user selected
PKDET Decay Time Constant	t_{PKD}	$1000*t_{PKA}$	min	t_{PKD} and t_{PKA} in µs	slaved to attack time
PRATE Interval	t_{PRI}	0.1 to 5 µs	range	low data rate mode	user selected mode
PWIDTH RFA1	t_{PW1}	0.55 to 1 µs	range	low data rate mode	user selected mode
PWIDTH RFA2	t_{PW2}	$1.1*t_{PW1}$	range	low data rate mode	user selected mode
PRATE Cycle	t_{PRC}	0.1 to 1.1 µs	range	high data rate mode	user selected mode
PWIDTH High (RFA1 & RFA2)	t_{PWH}	0.05 to 0.55 µs	range	high data rate mode	user selected mode
LPF Group Delay	t_{FGD}	$1750/f_{LPF}$	max	t_{FGD} in µs, f_{LPF} in kHz	user selected
LPF 3 dB Bandwidth	f_{LPF}	$1445/R_{LPF}$	min	f_{LPF} in kHz, R_{LPF} in kilohms	user selected
BBOUT-CMPIN Time Constant	t_{BBC}	$0.064*C_{BBO}$	min	t_{BBC} in µs, C_{BBO} in pF	user selected

Table 1

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Pin Descriptions

Pin	Name	Description
1	GND1	GND1 is the RF ground pin. GND2 and GND3 should be connected to GND1 by short, low-inductance traces.
2	VCC1	VCC1 is the positive supply voltage pin for the receiver base-band circuitry. VCC1 must be bypassed by an RF capacitor, which may be shared with VCC2. See the description of VCC2 (Pin 16) for additional information.
3	AGCCAP	This pin controls the AGC reset operation. A capacitor between this pin and ground sets the minimum time the AGC will hold-in once it is engaged. The hold-in time is set to avoid AGC chattering. For a given hold-in time t_{AGH}, the capacitor value C_{AGC} is: C_{AGC} = 19.1* t_{AGH}, where t_{AGH} is in µs and C_{AGC} is in pF A ±10% ceramic capacitor should be used at this pin. The value of C_{AGC} given above provides a hold-in time between t_{AGH} and 2.65* t_{AGH}, depending on operating voltage, temperature, etc. The hold-in time is chosen to allow the AGC to ride through the longest run of zero bits that can occur in a received data stream. The AGC hold-in time can be greater than the peak detector decay time, as discussed below. However, the AGC hold-in time should not be set too long, or the receiver will be slow in returning to full sensitivity once the AGC is engaged by noise or interference. The use of AGC is optional when using OOK modulation with data pulses of at least 30 µs. AGC operation can be defeated by connecting this pin to Vcc. Active or latched AGC operation is required for ASK modulation and/or for data pulses of less than 30 µs. The AGC can be latched on once engaged by connecting a 150 K resistor between this pin and ground, instead of a capacitor. AGC operation depends on a functioning peak detector, as discussed below. The AGC capacitor is discharged in the receiver power-down (sleep) mode.
4	PKDET	This pin controls the peak detector operation. A capacitor between this pin and ground sets the peak detector attack and decay times, which have a fixed 1:1000 ratio. For most applications, these time constants should be coordinated with the base-band time constant. For a given base-band capacitor C_{BBO}, the capacitor value C_{PKD} is: C_{PKD} = 0.33* C_{BBO} , where C_{BBO} and C_{PKD} are in pF A ±10% ceramic capacitor should be used at this pin. This time constant will vary between t_{PKA} and 1.5* t_{PKA} with variations in supply voltage, temperature, etc. The capacitor is driven from a 200 ohm “attack” source, and decays through a 200 K load. The peak detector is used to drive the “dB-below-peak” data slicer and the AGC release function. The AGC hold-in time can be extended beyond the peak detector decay time with the AGC capacitor, as discussed above. Where low data rates and OOK modulation are used, the “dB-below-peak” data slicer and the AGC are optional. In this case, the PKDET pin and the THLD2 pin can be left unconnected, and the AGC pin can be connected to Vcc to reduce the number of external components needed. The peak detector capacitor is discharged in the receiver power-down (sleep) mode.
5	BBOUT	BBOUT is the receiver base-band output pin. This pin drives the CMPIN pin through a coupling capacitor C_{BBO} for internal data slicer operation. The time constant t_{BBC} for this connection is: t_{BBC} = 0.064*C_{BBO} , where t_{BBC} is in µs and C_{BBO} is in pF A ±10% ceramic capacitor should be used between BBOUT and CMPIN. The time constant can vary between t_{BBC} and 1.8*t_{BBC} with variations in supply voltage, temperature, etc. The optimum time constant in a given circumstance will depend on the data rate, data run length, and other factors as discussed in the *ASH Transceiver Designer’s Guide*. A common criteria is to set the time constant for no more than a 20% voltage droop during SP_{MAX}. For this case: C_{BBO} = 70*SP_{MAX}, where SP_{MAX} is the maximum signal pulse width in µs and C_{BBO} is in pF The output from this pin can also be used to drive an external data recovery process (DSP, etc.). The nominal output impedance of this pin is 1 K. When the receiver RF amplifiers are operating at a 50%-50% duty cycle, the BBOUT signal changes about 10 mV/dB, with a peak-to-peak signal level of up to 685 mV. For lower duty cycles, the mV/dB slope and peak-to-peak signal level are proportionately less. The signal at BBOUT is riding on a 1.1 Vdc value that varies somewhat with supply voltage and temperature, so it should be coupled through a capacitor to an external load. A load impedance of 50 K to 500 K in parallel with no more than 10 pF is recommended. When an external data recovery process is used with AGC, BBOUT must be coupled to the external data recovery process and CMPIN by separate series coupling capacitors. The AGC reset function is driven by the signal applied to CMPIN. When the receiver is in power-down (sleep) mode, the output impedance of this pin becomes very high, preserving the charge on the coupling capacitor.
6	CMPIN	This pin is the input to the internal data slicers. It is driven from BBOUT through a coupling capacitor. The input impedance of this pin is 70 K to 100 K.
7	RXDATA	RXDATA is the receiver data output pin. This pin will drive a 10 pF, 500 K parallel load. The peak current available from this pin increases with the receiver low-pass filter cutoff frequency. In the power-down (sleep) mode, this pin becomes high impedance. If required, a 1000 K pull-up or pull-down resistor can be used to establish a definite logic state when this pin is high impedance. If a pull-up resistor is used, the positive supply end should be connected to a voltage no greater than Vcc + 200 mV.
8	NC	This pin may be left unconnected or may be grounded.

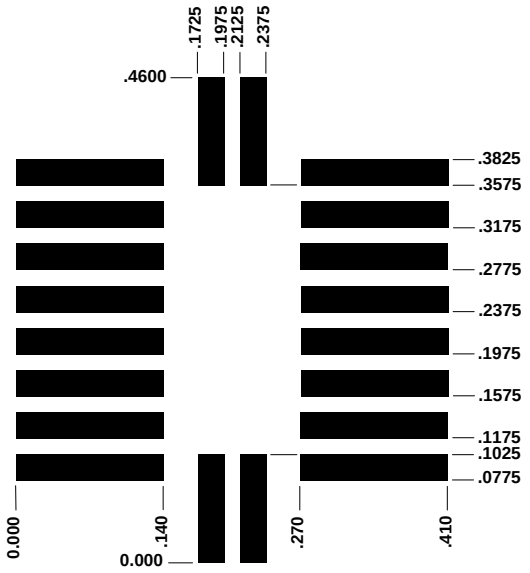
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Pin	Name	Description
9	LPFADJ	This pin is the receiver low-pass filter bandwidth adjust. The filter bandwidth is set by a resistor R_{LPF} between this pin and ground. The resistor value can range from 330 K to 820 ohms, providing a filter 3 dB bandwidth f_{LPF} from 4.5 kHz to 1.8 MHz. The resistor value is determined by: $R_{LPF} = 1445/ f_{LPF}$, where R_{LPF} is in kilohms, and f_{LPF} is in kHz A ±5% resistor should be used to set the filter bandwidth. This will provide a 3 dB filter bandwidth between f_{LPF} and 1.3* f_{LPF} with variations in supply voltage, temperature, etc. The filter provides a three-pole, 0.05 degree equiripple phase response. The peak drive current available from RXDATA increases in proportion to the filter bandwidth setting.
10	GND2	GND2 is an IC ground pin. It should be connected to GND1 by a short, low inductance trace.
11	RREF	RREF is the external reference resistor pin. A 100 K reference resistor is connected between this pin and ground. A ±1% resistor tolerance is recommended. It is important to keep the total capacitance between ground, Vcc and this node to less than 5 pF to maintain current source stability. If THLD1 and/or THDL2 are connected to RREF through resistor values less that 1.5 K, their node capacitance must be added to the RREF node capacitance and the total should not exceed 5 pF.
12	THLD2	THLD2 is the “dB-below-peak” data slicer (DS2) threshold adjust pin. The threshold is set by a 0 to 200 K resistor R_{TH2} between this pin and RREF. Increasing the value of the resistor decreases the threshold below the peak detector value (increases difference) from 0 to 120 mV. For most applications, this threshold should be set at 6 dB below peak, or 60 mV for a 50%-50% RF amplifier duty cycle. The value of the THLD2 resistor is given by: $R_{TH2} = 1.67*V$, where R_{TH2} is in kilohms and the threshold V is in mV A ±1% resistor tolerance is recommended for the THLD2 resistor. Leaving the THLD2 pin open disables the dB-below-peak data slicer operation.
13	THLD1	The THLD1 pin sets the threshold for the standard data slicer (DS1) through a resistor R_{TH1} to RREF. The threshold is increased by increasing the resistor value. Connecting this pin directly to RREF provides zero threshold. The value of the resistor depends on whether THLD2 is used. For the case that THLD2 is not used, the acceptable range for the resistor is 0 to 100 K, providing a THLD1 range of 0 to 90 mV. The resistor value is given by: $R_{TH1} = 1.11*V$, where R_{TH1} is in kilohms and the threshold V is in mV For the case that THLD2 is used, the acceptable range for the THLD1 resistor is 0 to 200 K, again providing a THLD1 range of 0 to 90 mV. The resistor value is given by: $R_{TH1} = 2.22*V$, where R_{TH1} is in kilohms and the threshold V is in mV A ±1% resistor tolerance is recommended for the THLD1 resistor. Note that a non-zero DS1 threshold is required for proper AGC operation.
14	PRATE	The interval between the falling edge of an ON pulse to the first RF amplifier and the rising edge of the next ON pulse to the first RF amplifier t_{PRI} is set by a resistor R_{PR} between this pin and ground. The interval t_{PRI} can be adjusted between 0.1 and 5 µs with a resistor in the range of 51 K to 2000 K. The value of R_{PR} is given by: $R_{PR} = 404* t_{PRI} + 10.5$, where t_{PRI} is in µs, and R_{PR} is in kilohms A ±5% resistor value is recommended. When the PWIDTH pin is connected to Vcc through a 1 M resistor, the RF amplifiers operate at a nominal 50%-50% duty cycle, facilitating high data rate operation. In this case, the period t_{PRC} from start-to-start of ON pulses to the first RF amplifier is controlled by the PRATE resistor over a range of 0.1 to 1.1 µs using a resistor of 11 K to 220 K. In this case the value of R_{PR} is given by: $R_{PR} = 198* t_{PRC} - 8.51$, where t_{PRC} is in µs and R_{PR} is in kilohms A ±5% resistor value should also be used in this case. Please refer to the *ASH Transceiver Designer’s Guide* for additional amplifier duty cycle information. It is important to keep the total capacitance between ground, Vcc and this pin to less than 5 pF to maintain stability.
15	PWIDTH	The PWIDTH pin sets the width of the ON pulse to the first RF amplifier t_{PW1} with a resistor R_{PW} to ground (the ON pulse width to the second RF amplifier t_{PW2} is set at 1.1 times the pulse width to the first RF amplifier). The ON pulse width t_{PW1} can be adjusted between 0.55 and 1 µs with a resistor value in the range of 200 K to 390 K. The value of R_{PW} is given by: $R_{PW} = 404* t_{PW1} - 18.6$, where t_{PW1} is in µs and R_{PW} is in kilohms A ±5% resistor value is recommended. When this pin is connected to Vcc through a 1 M resistor, the RF amplifiers operate at a nominal 50%-50% duty cycle, facilitating high data rate operation. In this case, the RF amplifier ON times are controlled by the PRATE resistor as described above. It is important to keep the total capacitance between ground, Vcc and this node to less than 5 pF to maintain stability. When using the high data rate operation with the sleep mode, connect the 1 M resistor between this pin and CNTRL1 (Pin 17), so this pin is low in the sleep mode.
16	VCC2	VCC2 is the positive supply voltage pin for the receiver RF section. This pin must be bypassed with an RF capacitor, which may be shared with VCC1. VCC2 must also be bypassed with a 1 to 10 µF tantalum or electrolytic capacitor.

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Pin	Name	Description
17	CNTRL1	CNTRL1 and CNTRL0 select the receiver modes. CNTRL1 and CNTRL0 both high place the unit in the receive mode. CNTRL1 and CNTRL0 both low place the unit in the power-down (sleep) mode. CNTRL1 is a high-impedance input (CMOS compatible). An input voltage of 0 to 300 mV is interpreted as a logic low. An input voltage of Vcc - 300 mV or greater is interpreted as a logic high. An input voltage greater than Vcc + 200 mV should not be applied to this pin. A logic high requires a maximum source current of 40 µA. Sleep mode requires a maximum sink current of 1 µA. This pin must be held at a logic level; it cannot be left unconnected.
18	CNTRL0	CNTRL0 is used with CNTRL1 to control the receiver modes. CNTRL0 is a high-impedance input (CMOS compatible). An input voltage of 0 to 300 mV is interpreted as a logic low. An input voltage of Vcc - 300 mV or greater is interpreted as a logic high. An input voltage greater than Vcc + 200 mV should not be applied to this pin. A logic high requires a maximum source current of 40 µA. Sleep mode requires a maximum sink current of 1 µA. This pin must be held at a logic level; it cannot be left unconnected.
19	GND3	GND3 is an IC ground pin. It should be connected to GND1 by a short, low inductance trace.
20	RFIO	RFIO is the receiver RF input pin. This pin is connected directly to the SAW filter transducer. Antennas presenting an impedance in the range of 35 to 72 ohms resistive can be satisfactorily matched to this pin with a series matching coil and a shunt matching/ESD protection coil. Other antenna impedances can be matched using two or three components. For some impedances, two inductors and a capacitor will be required. A DC path from RFIO to ground is required for ESD protection.

SM-20L PCB Pad Layout



Dimensions in inches

Note: Specifications subject to change without notice.

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