# MC100EP016A

# 3.3 V ECL 8-Bit Synchronous Binary Up Counter

ON Semiconductor®

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### Description

The MC100EP016A is a high−speed synchronous, presettable, cascadeable 8−bit binary counter. Architecture and operation are the same as the ECLinPS™ family MC100E016 with higher operating speed.

The counter features internal feedback to $\overline{TC}$ gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all−one state. When TCLD is HIGH, the TC feedback causes the counter to automatically reload upon TC = LOW, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

COUT and $\overline{COUT}$ provide differential outputs from a single, non−cascaded counter or divider application. COUT and $\overline{COUT}$ should not be used in cascade configuration. Only $\overline{TC}$ should be used for a counter or divider cascade chain output.

A differential clock input has also been added to improve performance.

The 100 Series contains temperature compensation.

### Features

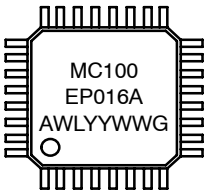
- 550 ps Typical Propagation Delay
- Operation Frequency > 1.3 GHz is 30% Faster than MC100EP016
- PECL Mode Operating Range: $V_{CC}$ = 3.0 V to 3.6 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range: $V_{CC}$ = 0 V with $V_{EE}$ = −3.0 V to −3.6 V
- Open Input Default State
- Safety Clamp on Clock Inputs
- Internal $\overline{TC}$ Feedback (Gated)
- Addition of COUT and $\overline{COUT}$
- 8−Bit
- Differential Clock Input
- $V_{BB}$ Output
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**MARKING DIAGRAM***



LQFP−32
FA SUFFIX
CASE 873A



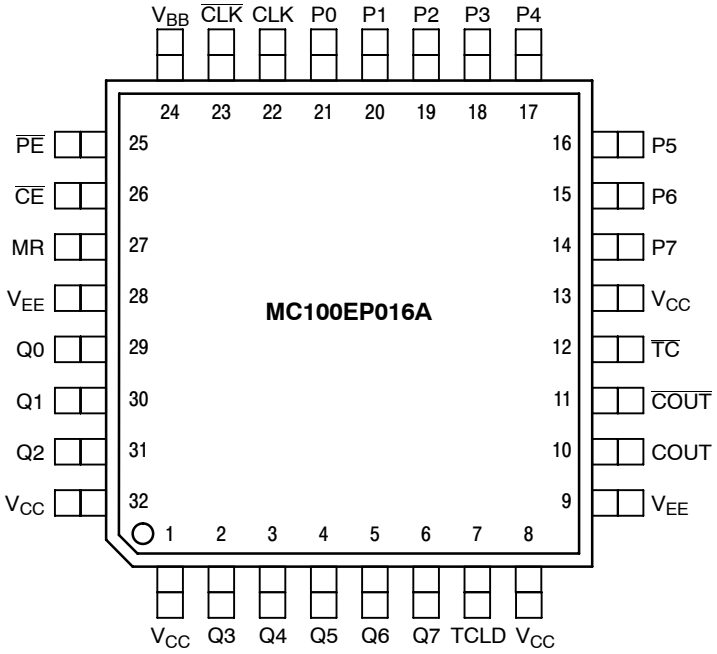

| | |
|---|---|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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Warning: All $V_{CC}$ and $V_{EE}$ pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 32−Lead LQFP Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| P0−P7* | ECL Parallel Data (Preset) Inputs |
| Q0−Q7 | ECL Data Outputs |
| $\overline{CE}$* | ECL Count Enable Control Input |
| $\overline{PE}$* | ECL Parallel Load Enable Control Input |
| MR* | ECL Master Reset |
| CLK*, $\overline{CLK}$* | ECL Differential Clock |
| $\overline{TC}$ | ECL Terminal Count Output |
| TCLD* | ECL TC−Load Control Input |
| COUT, $\overline{COUT}$ | ECL Differential Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |
| $V_{BB}$ | Reference Voltage Output |

* Pins will default LOW when left open.

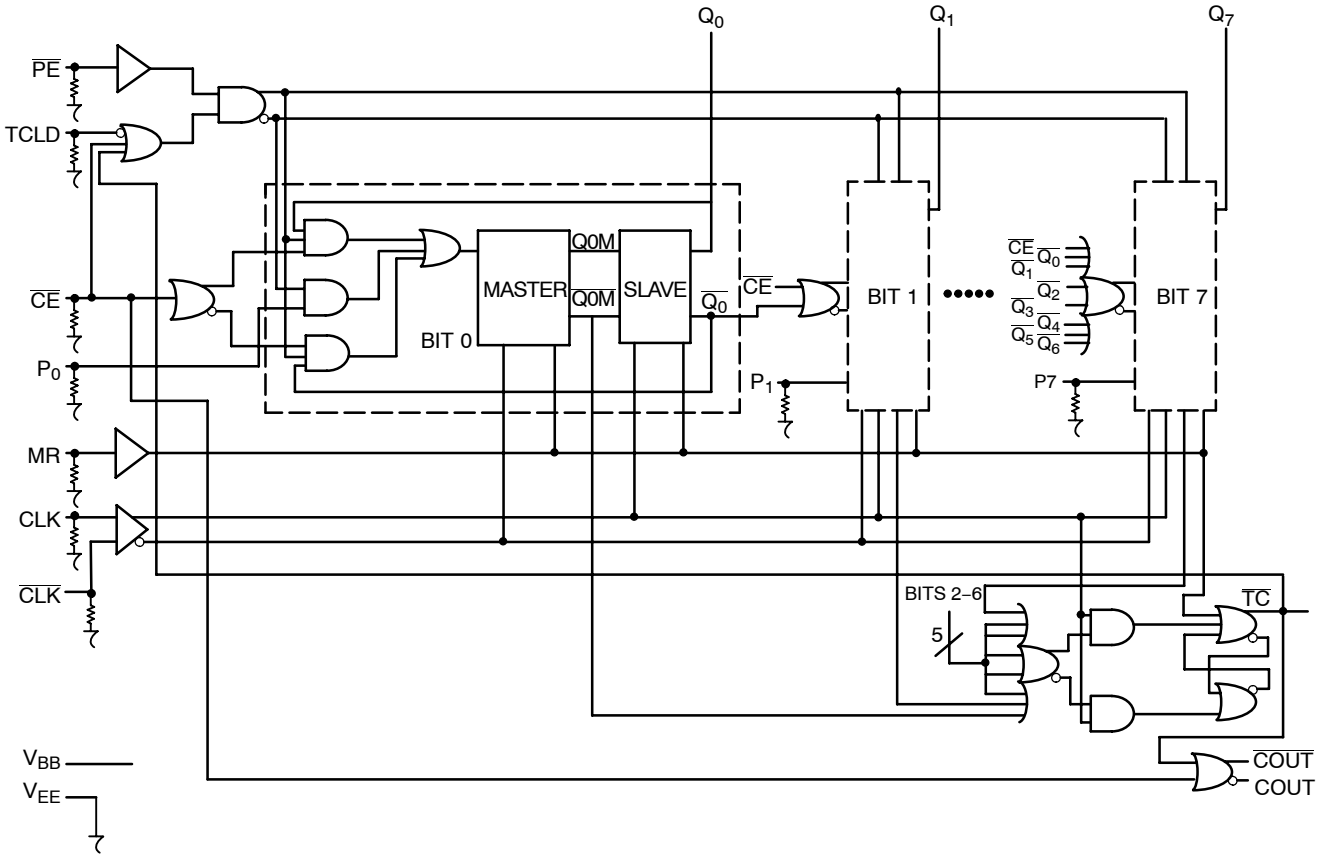
**Table 2. FUNCTION TABLES**

| $\overline{CE}$ | $\overline{PE}$ | TCLD | MR | CLK | FUNCTION |
|---|---|---|---|---|---|
| X | L | X | L | Z | Load Parallel (Pn to Qn) |
| L | H | L | L | Z | Continuous Count |
| L | H | H | L | Z | Count; Load Parallel on $\overline{TC}$ = LOW |
| H | H | X | L | Z | Hold |
| X | X | X | L | ZZ | Masters Respond, Slaves Hold |
| X | X | X | H | X | Reset (Qn : = LOW, $\overline{TC}$ : = HIGH) |

ZZ = Clock Pulse (High−to−Low)
Z = Clock Pulse (Low−to−High)

**Table 3. FUNCTION TABLE**

| Function | $\overline{PE}$ | $\overline{CE}$ | MR | TCLD | CLK | P7−P4 | P3 | P2 | P1 | P0 | Q7−Q4 | Q3 | Q2 | Q1 | Q0 | $\overline{TC}$ | $\overline{COUT}$ | COUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Load Count | L | X | L | X | Z | H | H | H | L | L | H | H | H | L | L | H | H | L |
| | H | L | L | L | Z | X | X | X | X | X | H | H | H | L | H | H | H | L |
| | H | L | L | L | Z | X | X | X | X | X | H | H | H | H | L | H | H | L |
| | H | L | L | L | Z | X | X | X | X | X | H | H | H | H | H | L | L | H |
| | H | L | L | L | Z | X | X | X | X | X | L | L | L | L | L | H | H | L |
| Load Hold | L | X | L | X | Z | H | H | H | L | L | H | H | H | L | L | H | H | L |
| | H | H | L | X | Z | X | X | X | X | X | H | H | H | L | L | H | H | L |
| | H | H | L | X | Z | X | X | X | X | X | H | H | H | L | L | H | H | L |
| Load on Terminal Count | H | L | L | H | Z | H | L | H | H | L | H | H | H | L | H | H | H | L |
| | H | L | L | H | Z | H | L | H | H | L | H | H | H | H | L | H | H | L |
| | H | L | L | H | Z | H | L | H | H | L | H | H | H | H | H | L | L | H |
| | H | L | L | H | Z | H | L | H | H | L | H | L | H | H | L | H | H | L |
| | H | L | L | H | Z | H | L | H | H | L | H | L | H | H | H | H | H | L |
| | H | L | L | H | Z | H | L | H | H | L | H | H | L | L | L | H | H | L |
| Reset | X | X | H | X | X | X | X | X | X | X | L | L | L | L | L | H | H | L |




Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

**Figure 2. 8-BIT Binary Counter Logic Diagram**

**Table 4. ATTRIBUTES**

| Characteristics | | Value | |
|---|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ | |
| Internal Input Pullup Resistor | | N/A | |
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 100 V<br>> 2 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb Pkg | Pb−Free Pkg |
| | LQFP−32 | Level 2 | Level 2 |
| Flammability Rating Oxygen Index: 28 to 34 | | UL 94 V−0 @ 0.125 in | |
| Transistor Count | | 1226 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

**Table 5. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 6 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −6 | V |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \leq V_{CC}$<br>$V_I \geq V_{EE}$ | 6<br>−6 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +70 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | 32 LQFP<br>32 LQFP | 74<br>61 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | Standard Board | 32 LQFP | 12 to 17 | °C/W |
| $T_{sol}$ | Wave Solder Pb<br>Pb−Free | | | 265<br>265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 6. 100EP DC CHARACTERISTICS, PECL** $V_{CC}$ = 3.3 V, $V_{EE}$ = 0 V (Note 2)

| Symbol | Characteristic | −40°C | | | 25°C | | | 70°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 130 | 170 | 210 | 130 | 177 | 210 | 130 | 180 | 210 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| $V_{BB}$ | Output Voltage Reference | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0 | | 3.3 | 2.0 | | 3.3 | 2.0 | | 3.3 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.3 V to −0.3 V.
3. All loading with 50 ohms to $V_{CC}$−2.0 volts.
4. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 7. 100EP DC CHARACTERISTICS, NECL** $V_{CC}$ = 0 V, $V_{EE}$ = −3.6 V to −3.0 V (Note 5)

| Symbol | Characteristic | −40°C | | | 25°C | | | 70°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | 130 | 170 | 210 | 130 | 177 | 210 | 130 | 180 | 210 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 6) | −1145 | −1020 | −895 | −1145 | −1020 | −895 | −1145 | −1020 | −895 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 6) | −1945 | −1820 | −1695 | −1945 | −1820 | −1695 | −1945 | −1820 | −1695 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | −1225 | | −880 | −1225 | | −880 | −1225 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | −1945 | | −1625 | −1945 | | −1625 | −1945 | | −1625 | mV |
| $V_{BB}$ | Output Voltage Reference | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | −1525 | −1425 | −1325 | mV |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | $V_{EE}$+2.0 | | 0.0 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with $V_{CC}$.
6. All loading with 50 ohms to $V_{CC}$−2.0 volts.
7. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 8. AC CHARACTERISTICS** $V_{EE}$ = −3.0 V to −3.6 V; $V_{CC}$ = 0 V or $V_{CC}$ = 3.0 V to 3.6 V; $V_{EE}$ = 0 V (Note 8)

| | | −40°C | | | 25°C | | | 70°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{COUNT}$ | Maximum Frequency<br>Count & Division Modes<br>Q, $\overline{TC}$, COUT/$\overline{COUT}$ | 1.3 | 1.5 | | 1.2 | 1.4 | | 1.2 | 1.3 | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay CLK to Q<br>MR to Q<br>CLK to $\overline{TC}$<br>MR to $\overline{TC}$<br>CLK to COUT/$\overline{COUT}$<br>MR to COUT/$\overline{COUT}$ | 350<br>400<br>350<br>400<br>475<br>450 | 511<br>550<br>511<br>555<br>705<br>720 | 650<br>700<br>650<br>700<br>850<br>850 | 400<br>400<br>400<br>400<br>500<br>500 | 550<br>570<br>550<br>570<br>745<br>760 | 700<br>750<br>700<br>750<br>900<br>900 | 480<br>450<br>480<br>520<br>550<br>570 | 610<br>630<br>610<br>635<br>825<br>830 | 780<br>820<br>780<br>820<br>1000<br>950 | ps |
| $t_S$ | Setup Time P0<br>P1 to P4<br>P5 to P7<br>$\overline{CE}$<br>$\overline{PE}$<br>TCLD | 400<br>300<br>250<br>500<br>500<br>550 | 240<br>140<br>80<br>320<br>315<br>355 | | 400<br>300<br>250<br>500<br>500<br>550 | 240<br>135<br>65<br>330<br>320<br>365 | | 400<br>300<br>250<br>500<br>500<br>550 | 245<br>125<br>55<br>340<br>325<br>380 | | ps |
| $t_H$ | Hold Time P0<br>P1 to P4<br>P5 to P7<br>$\overline{CE}$<br>$\overline{PE}$<br>TCLD | 100<br>50<br>150<br>600<br>625<br>525 | −145<br>−160<br>−105<br>380<br>465<br>320 | | 100<br>50<br>150<br>600<br>625<br>525 | −155<br>−170<br>−110<br>410<br>500<br>325 | | 100<br>50<br>150<br>600<br>625<br>525 | −170<br>−180<br>−115<br>450<br>535<br>340 | | ps |
| $t_{JITTER}$ | Clock Random Jitter<br>(RMS, 1000 Waveforms) | | 2.6 | 8.5 | | 2.5 | 8.0 | | 2.5 | 8.0 | ps |
| $t_{RR}$ | Reset Recovery Time | 400 | 195 | | 400 | 205 | | 400 | 220 | | ps |
| $t_{PW}$ | Minimum Pulse Width CLK<br>Minimum Pulse Width MR | 550<br>550 | 365<br>380 | | 550<br>550 | 365<br>380 | | 550<br>550 | 370<br>380 | | ps |
| $t_r$, $t_f$ | Output Rise/Fall Times<br>20% − 80% | 90 | 180 | 320 | 100 | 190 | 320 | 125 | 215 | 450 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to $V_{CC}$−2.0 V.

## Applications Information

### Cascading Multiple EP016A Devices

For applications which call for larger than 8-bit counters multiple EP016As can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of EP016A devices. Two EP016As can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 3 below pictorially illustrates the cascading of 4 EP016As to build a 32-bit high frequency counter. Note the EP01 gates used to OR the terminal count outputs of the lower order EP016As to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant EP016A is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an EP016A in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting EP016A devices from Figure 3 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for a cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output, the necessary setup time of the $\overline{CE}$ input, and the propagation delay through the OR gate controlling it (for 16–bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 3 shows EP01 gates used to control the count enable inputs, however, if the frequency of operation is slow enough, a LVECL OR gate can be used. Using the worst case guarantees for these parameters.

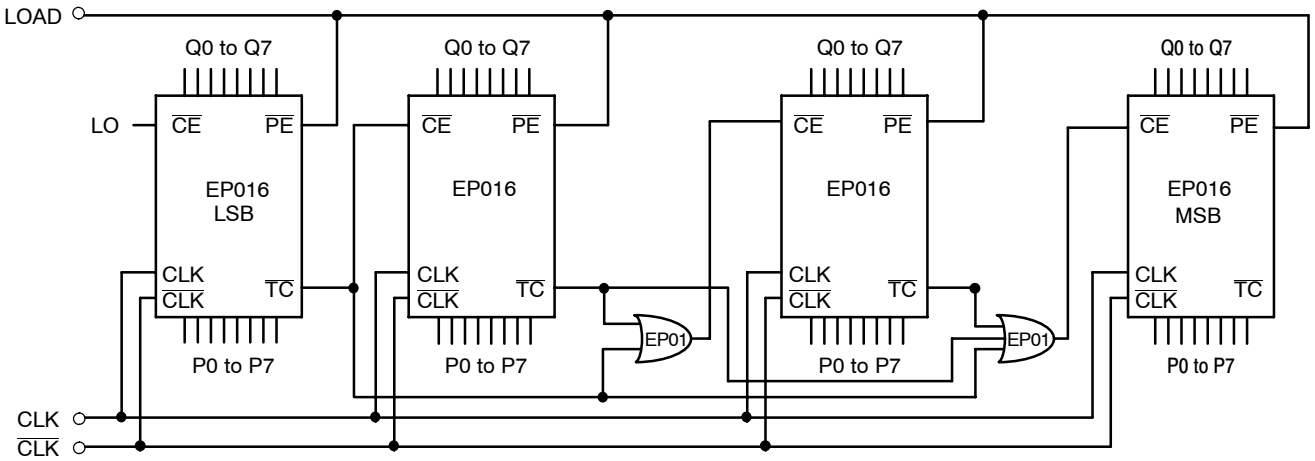



**Figure 3. 32-Bit Cascaded EP016A Counter**

Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

#### Programmable Divider

The EP016A has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 4 below illustrates the input conditions necessary for utilizing the EP016A as a programmable divider set up to divide by 113.

## Applications Information (continued)

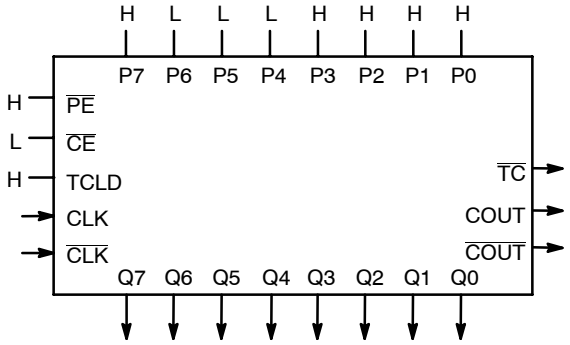



**Figure 4. Mod 2 to 256 Programmable Divider**

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = 256 − 113 = $8F_{16}$ = 1000 1111

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 4 will result in the waveforms of Figure 5. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016A and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

**Table 9. Preset Values for Various Divide Ratios**

| Divide Ratio | Preset Data Inputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| 2 | H | H | H | H | H | H | H | L |
| 3 | H | H | H | H | H | H | L | H |
| 4 | H | H | H | H | H | H | L | L |
| 5 | H | H | H | H | H | L | H | H |
| • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • |
| 112 | H | L | L | H | L | L | L | L |
| 113 | H | L | L | L | H | H | H | H |
| 114 | H | L | L | L | H | H | H | L |
| • | • | • | • | • | • | • | • | • |
| • | • | • | • | • | • | • | • | • |
| 254 | L | L | L | L | L | L | H | L |
| 255 | L | L | L | L | L | L | L | H |
| 256 | L | L | L | L | L | L | L | L |

A single EP016A can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple EP016As can be cascaded in a manner similar to that already discussed. When EP016As are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple EP016A divider chains.

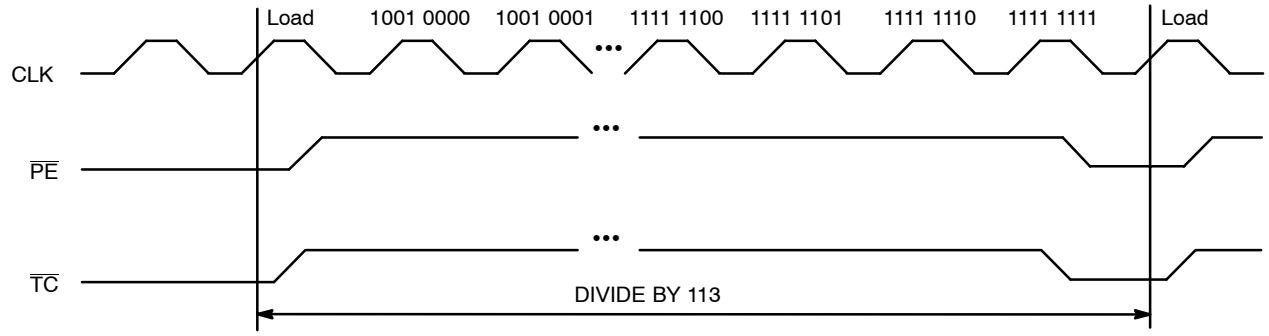



**Figure 5. Divide by 113 EP016A Programmable Divider Waveforms**

**Applications Information** (continued)

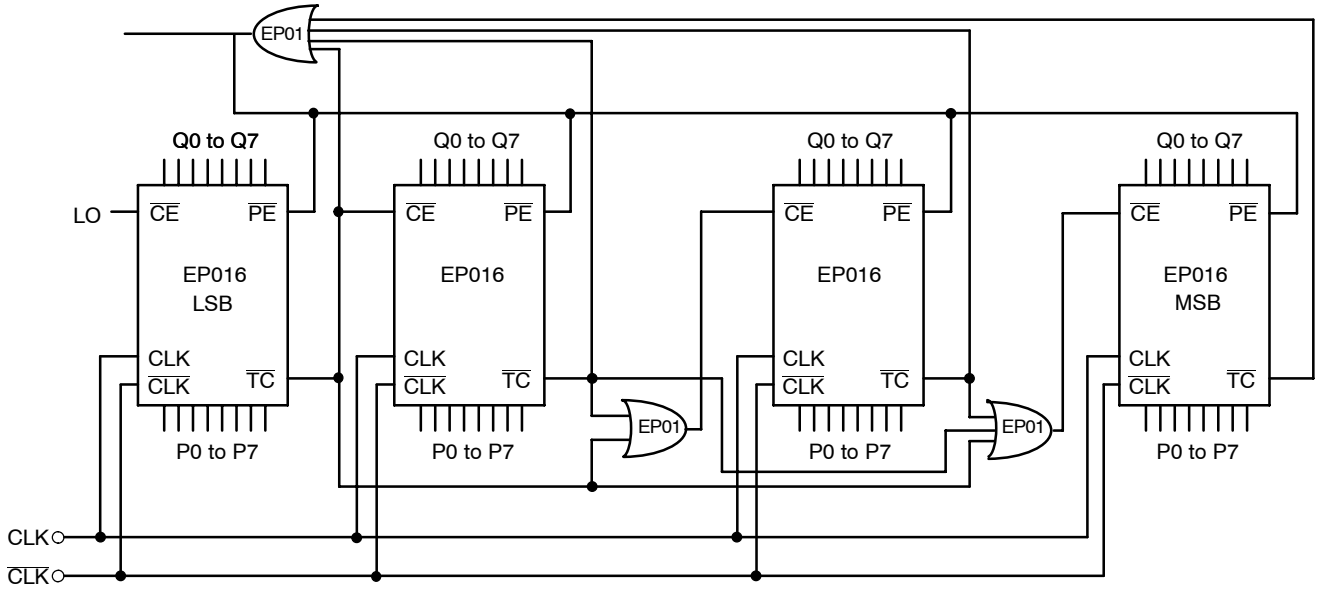



**Figure 6. 32-Bit Cascaded EP016A Programmable Divider**

Figure 6 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EP01 OR gates were used. For lower frequency applications a slower OR gate could replace the EP01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant EP016A must also feed the $\overline{CE}$ input of the most significant EP016A. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

**Maximizing EP016A Count Frequency**

The EP016A device produces 9 fast transitioning single ended outputs, thus $V_{CC}$ noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This $V_{CC}$ noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the $V_{CC}$ noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

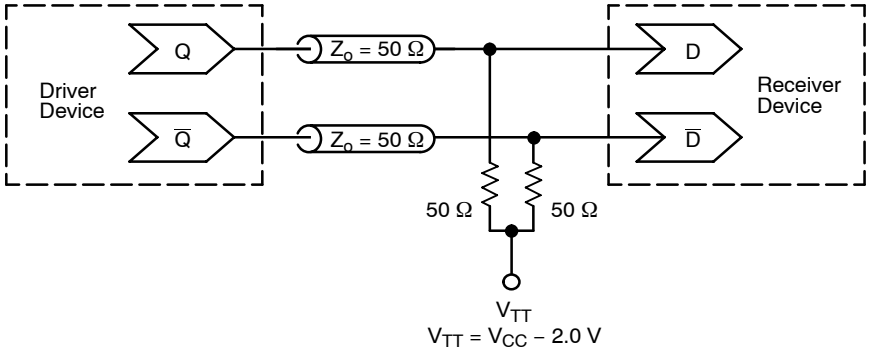



**Figure 7. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100EP016AFA | LQFP−32 | 250 Units / Tray |
| MC100EP016AFAG | LQFP−32 (Pb−Free) | 250 Units / Tray |
| MC100EP016AFAR2 | LQFP−32 | 2000 / Tape & Reel |
| MC100EP016AFAR2G | LQFP−32 (Pb−Free) | 2000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

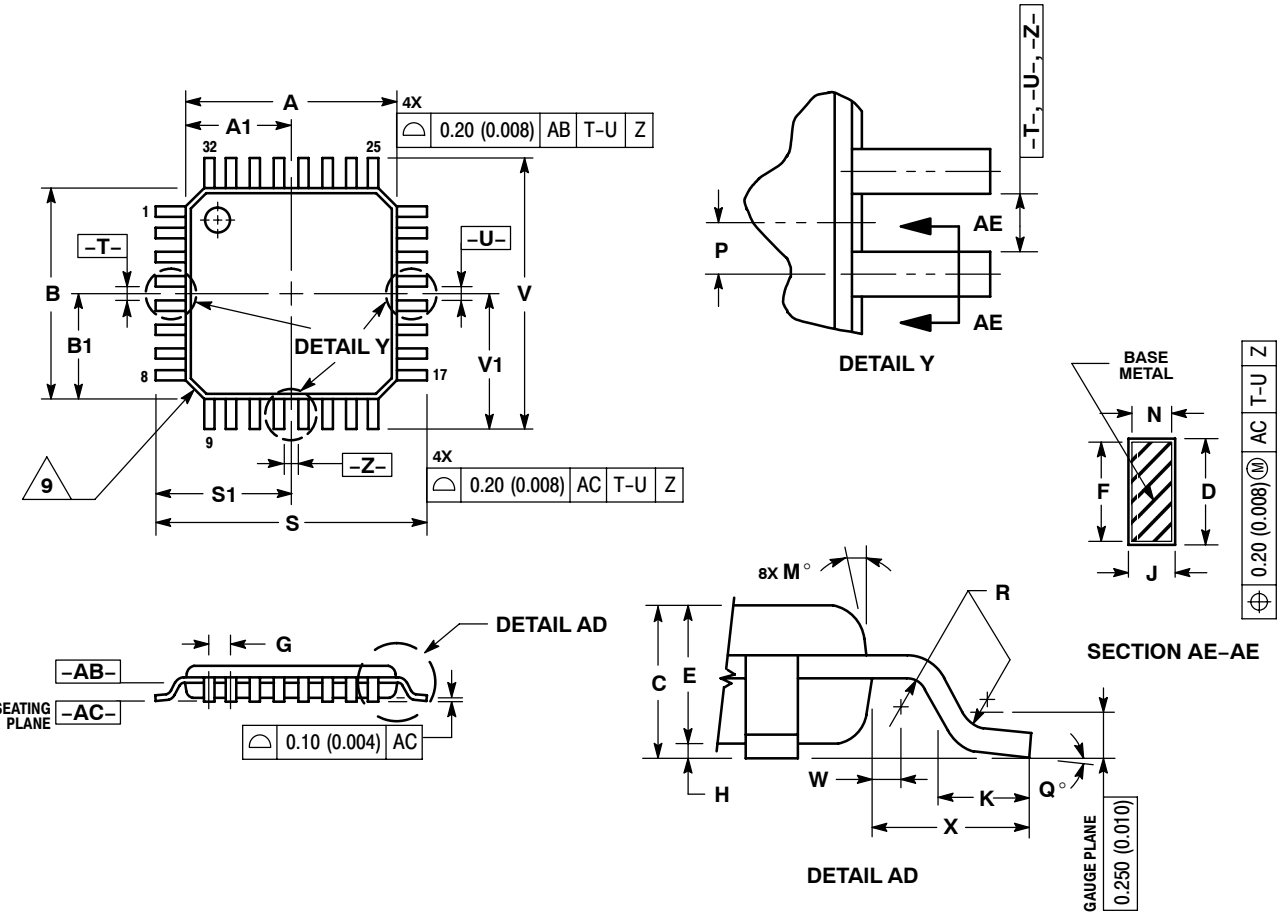
**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

## PACKAGE DIMENSIONS

**32 LEAD LQFP**
CASE 873A–02
ISSUE C




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