



Description

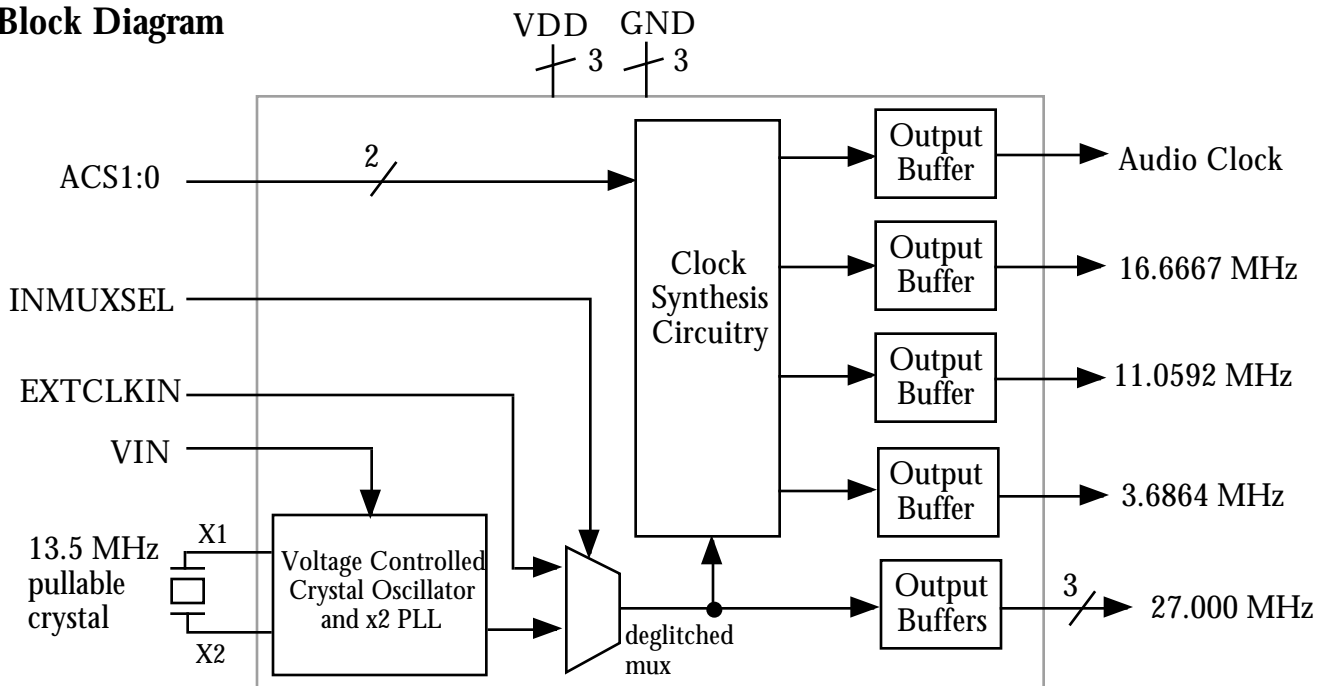
The MK2772-01 is a low cost, low jitter, high performance VCXO and clock synthesizer for set-top boxes. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3V input voltage to cause the output clocks to vary by ± 100 ppm. Using MicroClock's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz crystal input to produce multiple output clocks. All clocks are frequency locked to the 27.00MHz output (and to each other) with zero ppm error. The MK2772 includes a glitch-free multiplexer to switch input sources during operation.

MicroClock manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. Consult MicroClock to eliminate VCXOs, crystals and oscillators from your board.

Features

- Packaged in 20 pin SOIC
- Uses an inexpensive 13.5 MHz crystal
- On-chip VCXO (patented) with pull range of 200ppm (minimum)
- Ability to switch input sources "on-the-fly"
- VCXO tuning voltage of 0 to 3V
- Zero ppm synthesis error (patented) in all clocks. All exactly track 27MHz VCXO
- All clocks are frequency locked. All will vary the same amount (in ppm) as the VCXO
- Selectable Audio clock for 256x, 384x, and 512x.
- 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 5V operating voltage

Block Diagram





Pin Assignment

ACS1	1	20	ACS0
X2	2	19	EXTCLKIN
X1	3	18	27M
VDD	4	17	GND
VIN	5	16	27M
VDD	6	15	VDD
GND	7	14	GND
16.67M	8	13	27M
3.68M	9	12	11.06M
ACLK	10	11	INMUXSEL

Audio Clock Select

ACS1	ACS0	ACLK (MHz)
0	0	8.192
0	M	16.384
0	1	11.2896
M	0	16.9344
M	M	22.5792
M	1	18.432
1	0	12.288
1	M	24.576
1	1	5.6448

Input Source Select

INMUXSEL	27 MHz Input
0	EXTCLKIN
1	Internal VCXO

Pin Descriptions

Number	Name	Type	Description
1	ACS1	TI	Audio Clock Select 1. Determines ACLK frequency, as per table above.
2	X2	X	Crystal connection. Connect to a pullable 13.5 MHz crystal.
3	X1	X	Crystal connection. Connect to a pullable 13.5 MHz crystal.
4	VDD	P	Connect to +5V, and other VDDs.
5	VIN	VI	Voltage Input to VCXO. Zero to 3V signal which controls the frequency of the VCXO.
6	VDD	P	Connect to +5V.
7	GND	P	Connect to ground.
8	16.67M	O	16.6667 MHz processor clock output.
9	3.68M	O	3.6864 MHz clock output.
10	ACLK	O	Audio Clock Output determined by ACS1,0. Per table above.
11	INMUXSEL	I	Input Multiplexer Select. Selects either the internal VCXO/PLL output, or the clock on pin 19.
12	11.06M	O	11.0592 MHz clock output.
13	27M	O	27.00 MHz clock output.
14	GND	P	Connect to ground.
15	VDD	P	Connect to +5V.
16	27M	O	27.00 MHz clock output.
17	GND	P	Connect to ground.
18	27M	O	27.00 MHz clock output.
19	EXTCLKIN	I	External Clock Input. Connect an external 27 MHz clock to this pin for glitch free switching.
20	ACS0	TI	Audio Clock Select 0. Determines ACLK frequency, as per table above.

Key: I = Input, TI = tri-level input, VI = VCXO input, O = output, P = power supply connection, X = crystal connection

**Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless noted)					
Operating Voltage, VDD		4.75		5.25	V
Input High Voltage, VIH, X1 pin only		3.5	2.5		V
Input Low Voltage, VIL, X1 pin only			2.5	1.5	V
Input High Voltage, VIH	ACS1, ACS0	VDD-0.5			V
Input High Voltage, VIH	INMUXSEL	2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load, note 2		45		mA
Pull-up Resistor value	pin 11 only		250k		
Input Capacitance			7		pF
Frequency synthesis error	All clocks as shown		0	1	ppm
VIN, VCXO control voltage		0		3	V
AC CHARACTERISTICS (VDD = 5.0V unless noted)					
Input Crystal Frequency			13.50000		MHz
Input Crystal Accuracy				±30	ppm
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At 1.4V	40		60	%
Maximum Absolute Jitter, short term			300		ps
27 MHz output pullability, note 3	0V VIN 3V	±100			ppm

- Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With ACLK at 12.288 MHz.
3. With a recommended crystal.

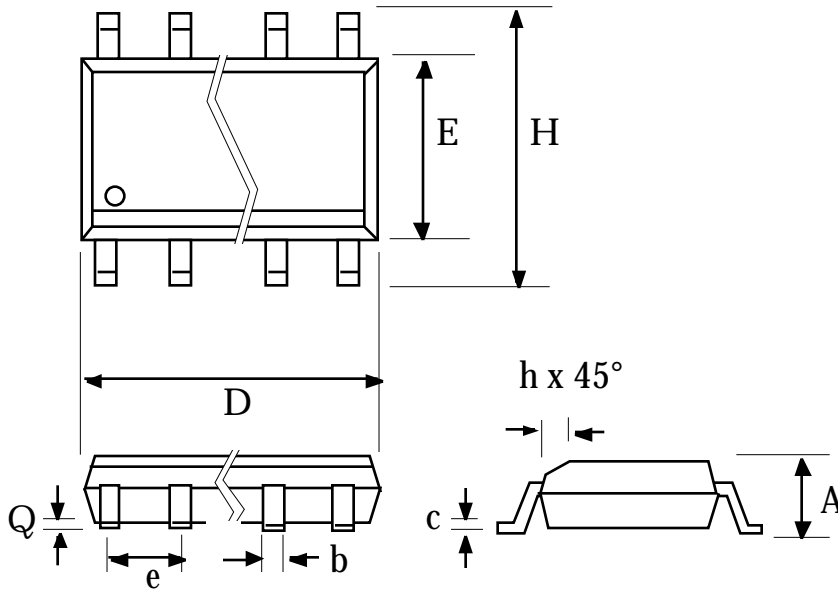
External Components/Crystal Selection

The MK2772-01 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF should be connected between VDD (pin 15) and GND (14), and between VDD (4) and GND (7), as close to the MK2772-01 as possible. A series termination resistor of 33 Ω may be used for each clock output. The input crystal must be connected as close to the chip as possible. The 13.5 MHz input crystal should be a parallel mode, pullable, AT cut with 14.0pF load capacitance. See Application Note MAN05 for more details on crystal selection and layout. Recommended crystal is from Ecliptek Corporation, P/N ECX-4665-13.500M. Contact Ecliptek at 714 433 1200tel, 714 433 1234fax.



Package Outline and Package Dimensions

20 pin SOIC



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.092	0.104	2.3368	2.6416
b	0.014	0.019	0.356	0.483
c	0.009	0.012	0.229	0.305
D	0.490	0.512	12.446	13.005
E	0.290	0.300	7.366	7.620
H	0.394	0.419	10.008	10.643
e	.050 BSC		1.27 BSC	
h		0.016		0.406
Q	0.003	0.011	0.076	0.279

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2772-01S	MK2772-01S	tubes	20 pin SOIC	0-70°C
MK2772-01STR	MK2772-01S	tape and reel	20 pin SOIC	0-70°C

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