ICL3225E, ICL3227E, ICL3245E

±15kV ESD Protected, +3V to +5.5V, 1µA, 1Mbps, RS-232 Transceivers with Enhanced Automatic Powerdown

FN4900
Rev 12.00
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The Intersil ICL3225E, ICL3227E, and ICL3245E devices are 3.0V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with manual and enhanced automatic powerdown functions, reduce the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 1Mbps are guaranteed at worst case load conditions. This family is fully compatible with 3.3V only systems, mixed 3.3V and 5.0V systems, and 5.0V only systems.

The ICL3245E is a 3-driver, 5-receiver device that provides a complete serial port suitable for laptop or notebook computers. It also includes a noninverting always-active receiver for “wake-up” capability.

These devices, feature an *enhanced automatic powerdown* function, which powers down the on-chip power supply and driver circuits. This occurs when all receiver and transmitter inputs detect no signal transitions for a period of 30s. These devices power back up automatically, whenever they sense a transition on any transmitter or receiver input.

Table 1 summarizes the features of the device represented by this datasheet, while Application Note AN9863 summarizes the features of each device comprising the ICL32xxE 3V family.

Related Literature

- For a full list of related documents, visit our website
  - ICL3225E, ICL3227E, and ICL3245E product pages

Features

- Pb-free (RoHS compliant)
- ESD protection for RS-232 I/O pins to ±15kV (IEC61000)
- Manual and enhanced automatic powerdown features
- Drop in replacements for MAX3225E, MAX3227E, MAX3245E
- RS-232 compatible with V_{CC} = 2.7V
- Meets EIA/TIA-232 and V.28/V.24 specifications at 3V
- Latch-up free
- On-chip voltage converters require only four external 0.1µF capacitors
- Guaranteed mouse driveability (ICL3245E)
- “Ready to Transmit” indicator output (ICL3225E/ICL3227E)
- Receiver hysteresis for improved noise immunity
- Guaranteed minimum data rate 1Mbps
- Low skew at transmitter/receiver input trip points 10ns
- Guaranteed minimum slew rate 24V/µs
- Wide power supply range . . . . . single +3V to +5.5V
- Low supply current in powerdown state 1µA

Applications

- Any system requiring RS-232 communication ports
  - Battery powered, hand-held, and portable equipment
  - Laptop computers, notebooks, palmtops
  - Modems, printers, and other peripherals
  - Digital cameras
  - Cellular/mobile phones

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF Tx.	NO. OF Rx.	NO. OF MONITOR Rx. (R_{OUTB})	DATA RATE (kbps)	Rx. ENABLE FUNCTION?	READY OUTPUT?	MANUAL POWER-DOWN?	ENHANCED AUTOMATIC POWERDOWN FUNCTION?
ICL3225E	2	2	0	1000	No	Yes	Yes	Yes
ICL3227E	1	1	0	1000	No	Yes	Yes	Yes
ICL3245E	3	5	1	1000	No	No	Yes	Yes

Ordering Information

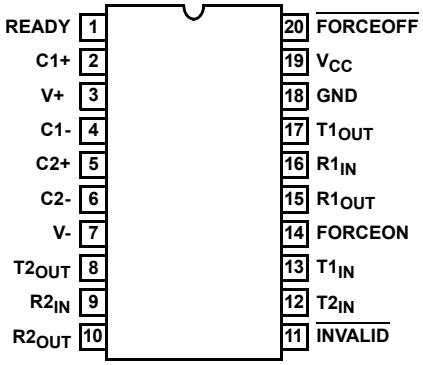
PART NUMBER (Notes 1, 2, 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ICL3225ECAZ	ICL3225ECAZ	0 to +70	20 Ld SSOP	M20.209
ICL3225ECPZ (No longer available, recommended replacement: ICL3225ECAZ) (Note 3)	3225ECPZ	0 to +70	20 Ld PDIP	E20.3
ICL3225EIAZ	ICL3225EIAZ	-40 to +85	20 Ld SSOP	M20.209
ICL3227ECAZA	3227ECAZ	0 to +70	16 Ld SSOP	M16.209
ICL3227EIAZA	3227EIAZ	-40 to +85	16 Ld SSOP	M16.209
ICL3245ECAZ	ICL3245ECAZ	0 to +70	28 Ld SSOP	M28.209
ICL3245ECBZ (No longer available, recommended replacement: ICL3245EIAZ)	ICL3245ECBZ	0 to +70	28 Ld SOIC	M28.3
ICL3245ECVZ (No longer available, recommended replacement: ICL3245EIAZ)	ICL3245ECVZ	0 to +70	28 Ld TSSOP	M28.173
ICL3245EIAZ	ICL3245EIAZ	-40 to +85	28 Ld SSOP	M28.209

NOTES:

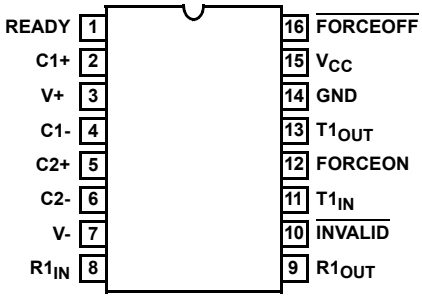
1. Add “-T” suffix for 1k unit tape and reel option. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.
4. For Moisture Sensitivity Level (MSL), see product information page for ICL3225E, ICL3227E, ICL3245E. For more information on MSL, see tech brief TB363.

Pin Configurations

ICL3225E (PDIP, SSOP)
TOP VIEW

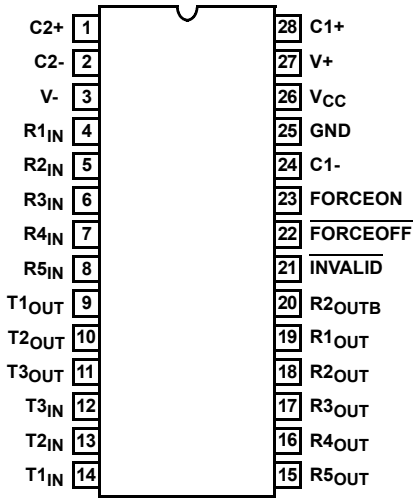


ICL3227E (SSOP)
TOP VIEW



Pin Configurations (Continued)

ICL3245E (SOIC, SSOP, TSSOP)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter Inputs.
T_{OUT}	±15kV ESD protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs.
R_{OUTB}	TTL/CMOS level, noninverting, always enabled receiver outputs.
$\overline{\text{INVALID}}$	Active low output that indicates if no valid RS-232 levels are present on any receiver input.
READY	Active high output that indicates when the ICL32xxE is ready to transmit (i.e., V- ≤ -4V).
$\overline{\text{FORCEOFF}}$	Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (see Table 2 on page 10).
FORCEON	Active high input to override automatic powerdown circuitry, thereby keeping transmitters active. ($\overline{\text{FORCEOFF}}$ must be high).

Typical Operating Circuits

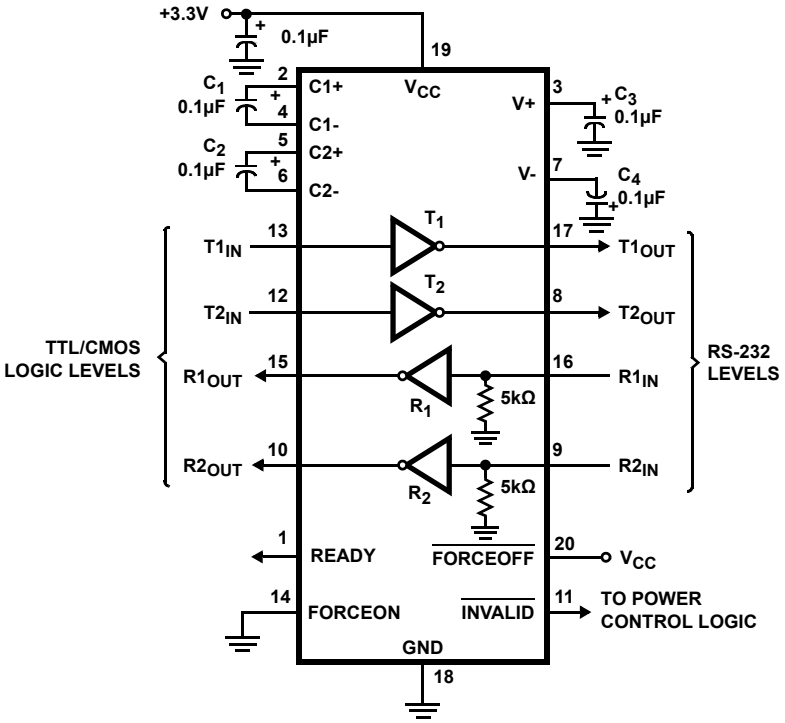


FIGURE 1. ICL3225E

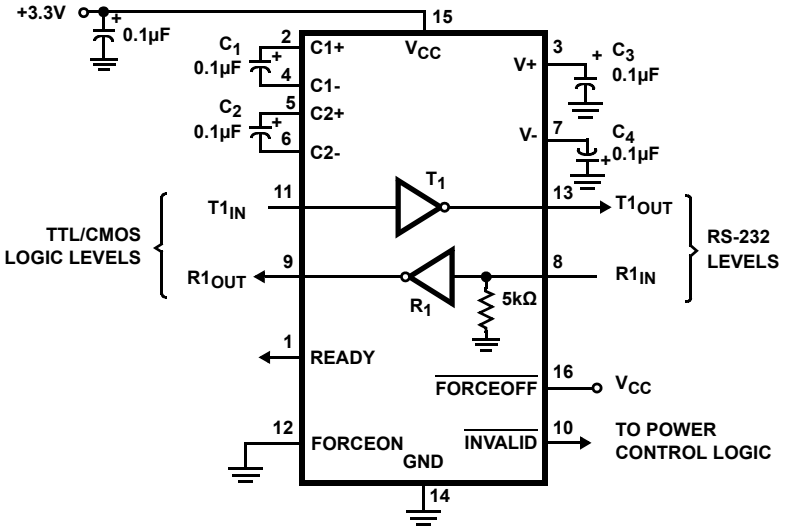


FIGURE 2. ICL3227E

Typical Operating Circuits (Continued)

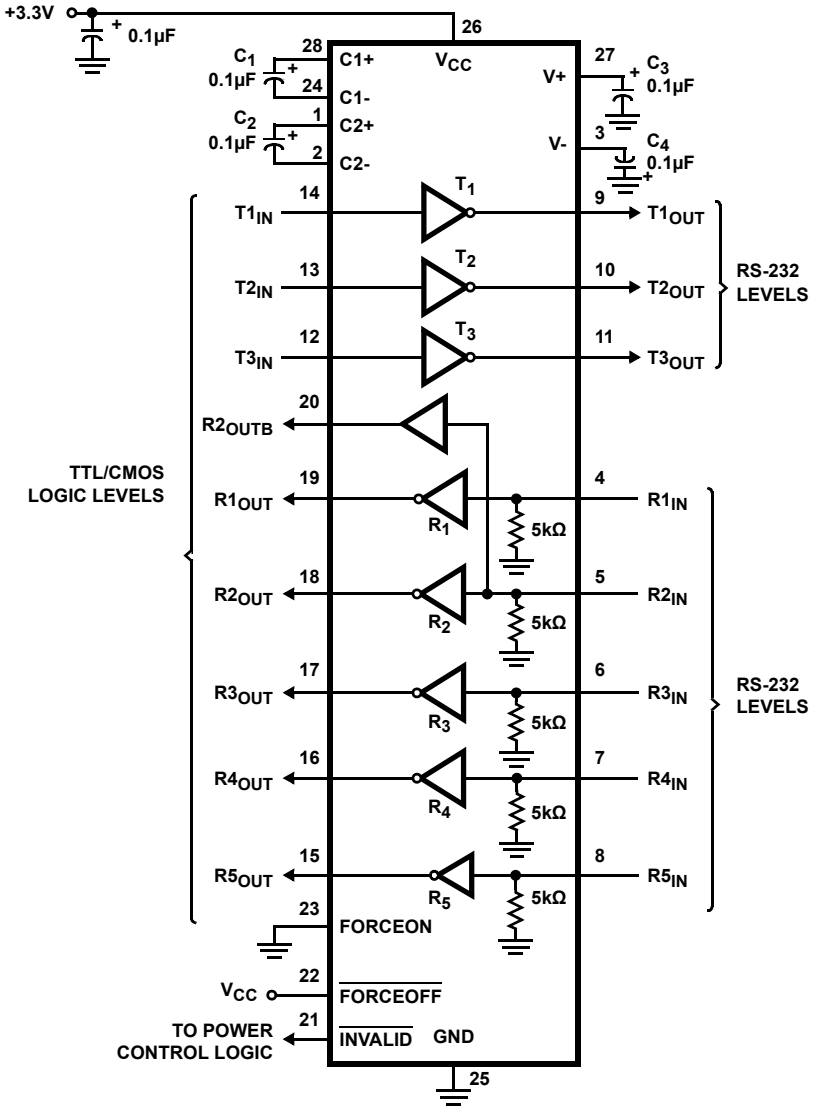


FIGURE 3. ICL3245E

Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V+ to Ground . . . . . -0.3V to 7V
V- to Ground . . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{FORCEOFF}$, FORCEON . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT}, $\overline{INVALID}$, READY . . . . . -0.3V to V_{CC} +0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
20 Ld PDIP Package*	80
28 Ld SOIC Package	75
16 Ld SSOP Package	145
20 Ld SSOP Package	135
28 Ld SSOP and TSSOP Packages	100

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile (SOIC, SSOP, TSSOP) . . . . . see TB493

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Operating Conditions

Temperature Range
ICL32xxEC . . . . . 0°C to +70°C
ICL32xxEI . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = +25°C

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
Supply Current, Automatic Powerdown	All R_{IN} open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		+25	-	1.0	10	µA
Supply Current, Powerdown	$\overline{FORCEOFF}$ = GND		+25	-	1.0	10	µA
Supply Current, Automatic Powerdown Disabled	All outputs unloaded, FORCEON = $\overline{FORCEOFF}$ = V_{CC}		+25	-	0.3	1.0	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$	V_{CC} = 3.3V	Full	2.0	-	-	V
		V_{CC} = 5.0V	Full	2.4	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$		Full	-	±0.01	±1.00	µA
Output Leakage Current	$\overline{FORCEOFF}$ = GND, ICL3245E only		Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} - 0.6	V_{CC} - 0.1	-	V
RECEIVER INPUTS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		+25	0.6	1.2	-	V
	V_{CC} = 5.0V		+25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		+25	-	1.5	2.4	V
	V_{CC} = 5.0V		+25	-	1.8	2.4	V
Input Hysteresis			+25	-	0.5	-	V
Input Resistance			+25	3	5	7	kΩ

Electrical Specifications

Test conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified.
Typicals are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
TRANSMITTER OUTPUTS							
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, transmitter output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, automatic powerdown or $\overline{FORCEOFF}$ = GND		Full	-	-	±25	µA
MOUSE DRIVEABILITY							
Transmitter Output Voltage (See Figure 14 on page 13)	$T1_{IN}$ = $T2_{IN}$ = GND, $T3_{IN}$ = V_{CC}, $T3_{OUT}$ loaded with 3kΩ to GND, $T1_{OUT}$ and $T2_{OUT}$ loaded with 2.5mA each		Full	±5	-	-	V
ENHANCED AUTOMATIC POWERDOWN (FORCEON = GND, FORCEOFF = VCC)							
Receiver Input Thresholds to $\overline{INVALID}$ High	See Figure 9 on page 11		Full	-2.7	-	2.7	V
Receiver Input Thresholds to $\overline{INVALID}$ Low	See Figure 9 on page 11		Full	-0.3	-	0.3	V
$\overline{INVALID}$, READY Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
$\overline{INVALID}$, READY Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} - 0.6	-	-	V
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay (t_{INVH})			+25	-	1	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low Delay (t_{INVL})			+25	-	30	-	µs
Receiver or Transmitter Edge to Transmitters Enabled Delay (t_{WU})	(Note 6)		25	-	100	-	µs
Receiver or Transmitter Edge to Transmitters Disabled Delay ($t_{AUTOPWDN}$)	(Note 6)		Full	15	30	60	sec
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, one transmitter switching	C_L = 1000pF	Full	250	-	-	kbps
		V_{CC} = 3V to 4.5V, C_L = 250pF	Full	1000	-	-	kbps
		V_{CC} = 4.5V to 5.5V, C_L = 1000pF	Full	1000	-	-	kbps
Receiver Propagation Delay	Receiver input to receiver output, C_L = 150pF	t_{PHL}	+25	-	0.15	-	µs
		t_{PLH}	+25	-	0.15	-	µs
Receiver Output Enable Time	Normal operation (ICL3245E only)		+25	-	200	-	ns
Receiver Output Disable Time	Normal operation (ICL3245E only)		+25	-	200	-	ns
Transmitter Skew	t_{PHL} - t_{PLH} (Note 7)		+25	-	25	-	ns
Receiver Skew	t_{PHL} - t_{PLH} (Note 7)		+25	-	50	-	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, measured from 3V to -3V or -3V to 3V, C_L = 150pF to 1000pF		+25	24	-	150	V/µs

Electrical Specifications

Test conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; unless otherwise specified. Typicals are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNIT
ESD PERFORMANCE							
RS-232 Pins (T_{OUT}, R_{IN})	Human body model		+25	-	±15	-	kV
	IEC61000-4-2 contact discharge		+25	-	±8	-	kV
	IEC61000-4-2 air gap discharge		+25	-	±15	-	kV
All Other Pins	ICL3245E	Human body model (HBM)	+25	-	±2	-	kV
		Charged Device Model (CDM)	+25	-	±1.5	-	kV
	ICL3225E, ICL3227E	Human body model (HBM)	+25	-	±4	-	kV
		Charged Device Model (CDM)	+25	-	±2	-	kV

NOTES:

6. An “edge” is defined as a transition through the transmitter or receiver input thresholds.
7. Skews are measured at the receiver input switching points (1.4V).

Detailed Description

These ICL32xxE interface ICs operate from a single +3V to +5.5V supply, guarantee a 1Mbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: The charge pump, the transmitters, and the receivers.

Charge Pump

Intersil's new ICL32xxE family utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions at V_{CC} = 3.3V. See the "Capacitor Selection", and Table 3 on page 13 for capacitor recommendations for other operating conditions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

Transmitter outputs disable and assume a high impedance state when the device enters the powerdown mode (see Table 2 on page 10). These outputs may be driven to ±12V when disabled.

All devices guarantee a 1Mbps data rate for full load conditions (3kΩ and 250pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 1.4Mbps. Transmitter skew is extremely low on these devices, and is specified at the receiver input trip points (1.4V), rather than the arbitrary 0V crossing point typical of other RS-232 families.

Transmitter inputs float if left unconnected, and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

Receivers

All the ICL32xxE devices contain standard inverting receivers, but only the ICL3245E receivers can tristate, via the $\overline{FORCEOFF}$ control line. Additionally, the ICL3245E includes a noninverting (monitor) receiver (denoted by the R_{OUTB} label) that is always active, regardless of the state of any control lines. Both receiver types convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 4) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

The ICL3245E inverting receivers disable during forced (manual) powerdown, but not during automatic powerdown (see Table 2). Conversely, the monitor receiver remains active even during manual powerdown making it extremely useful for Ring Indicator monitoring. Standard receivers driving powered down peripherals must be disabled to prevent current flow through the peripheral's protection diodes (see Figures 5 and 6). This renders them useless for wake-up functions, but the corresponding monitor receiver can be dedicated to this task as shown in Figure 6.

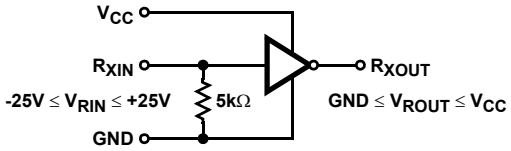


FIGURE 4. INVERTING RECEIVER CONNECTIONS

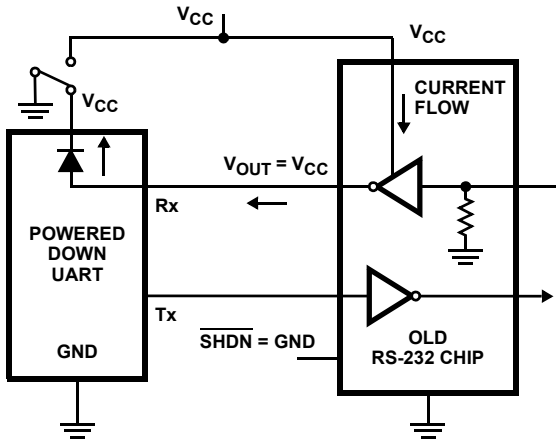


FIGURE 5. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

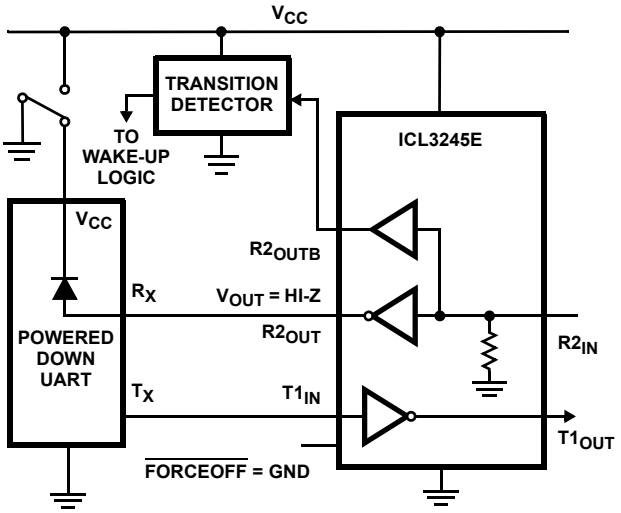


FIGURE 6. DISABLED RECEIVERS PREVENT POWER DRAIN

TABLE 2. POWERDOWN LOGIC TRUTH TABLE

RCVR OR XMTR EDGE WITHIN 30 SEC?	$\overline{\text{FORCEOFF}}$ INPUT	FORCEON INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	R_{OUTB} OUTPUTS (Note 8)	RS-232 LEVEL PRESENT AT RECEIVER INPUT?	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
ICL3225E, ICL3227E								
NO	H	H	Active	Active	N.A.	No	L	Normal Operation (Enhanced Auto Powerdown Disabled)
NO	H	H	Active	Active	N.A.	Yes	H	
YES	H	L	Active	Active	N.A.	No	L	Normal Operation (Enhanced Auto Powerdown Enabled)
YES	H	L	Active	Active	N.A.	Yes	H	
NO	H	L	High-Z	Active	N.A.	No	L	Powerdown Due to Enhanced Auto Powerdown Logic
NO	H	L	High-Z	Active	N.A.	Yes	H	
X	L	X	High-Z	Active	N.A.	No	L	Manual Powerdown
X	L	X	High-Z	Active	N.A.	Yes	H	
ICL322XE - $\overline{\text{INVALID}}$ DRIVING FORCEON AND $\overline{\text{FORCEOFF}}$ (EMULATES AUTOMATIC POWERDOWN)								
X	Note 9	Note 9	Active	Active	N.A.	Yes	H	Normal Operation
X	Note 9	Note 9	High-Z	Active	N.A.	No	L	Forced Auto Powerdown
ICL3245E								
NO	H	H	Active	Active	Active	No	L	Normal Operation (Enhanced Auto Powerdown Disabled)
NO	H	H	Active	Active	Active	Yes	H	
YES	H	L	Active	Active	Active	No	L	Normal Operation (Enhanced Auto Powerdown Enabled)
YES	H	L	Active	Active	Active	Yes	H	
NO	H	L	High-Z	Active	Active	No	L	Powerdown Due to Enhanced Auto Powerdown Logic
NO	H	L	High-Z	Active	Active	Yes	H	
X	L	X	High-Z	High-Z	Active	No	L	Manual Powerdown
X	L	X	High-Z	High-Z	Active	Yes	H	
ICL3245E - $\overline{\text{INVALID}}$ DRIVING FORCEON AND $\overline{\text{FORCEOFF}}$ (EMULATES AUTOMATIC POWERDOWN)								
X	Note 9	Note 9	Active	Active	Active	Yes	H	Normal Operation
X	Note 9	Note 9	High-Z	High-Z	Active	No	L	Forced Auto Powerdown

NOTES:

8. Applies only to the ICL3245E.
9. Input is connected to $\overline{\text{INVALID}}$ Output.

Powerdown Functionality

This 3V family of RS-232 interface devices requires a nominal supply current of 0.3mA during normal operation (not in powerdown mode). This is considerably less than the 5mA to 11mA current required of 5V RS-232 devices. The already low current requirement drops significantly when the device enters powerdown mode. In powerdown, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter outputs tristate. Inverting receiver outputs may or may not disable in powerdown; refer to Table 2 for details. This micro-power mode makes these devices ideal for battery powered and portable applications.

Software Controlled (Manual) Powerdown

These three devices allow the user to force the IC into the low power, standby state, and utilize a two pin approach where the FORCEON and $\overline{\text{FORCEOFF}}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{\text{FORCEOFF}}$ are both strapped high. To switch between active and powerdown modes, under logic or software control, only the $\overline{\text{FORCEOFF}}$ input need be driven. The FORCEON state isn't critical, as $\overline{\text{FORCEOFF}}$ dominates over FORCEON. Nevertheless, if strictly manual control over powerdown is desired, the user must strap FORCEON high to disable the enhanced automatic powerdown circuitry. ICL3245E inverting (standard) receiver outputs also disable when the device is in powerdown, thereby eliminating

the possible current path through a shutdown peripheral's input protection diode (see Figures 5 and 6).

Connecting $\overline{\text{FORCEOFF}}$ and FORCEON together disables the enhanced automatic powerdown feature, enabling them to function as a manual $\overline{\text{SHUTDOWN}}$ input (see Figure 7).

With any of the above control schemes, the time required to exit powerdown, and resume transmission is only 100µs.

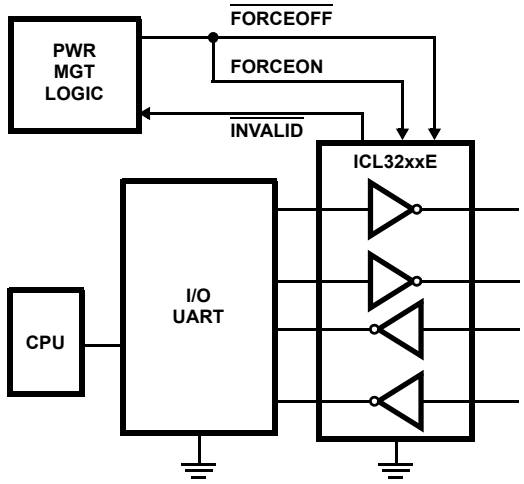


FIGURE 7. CONNECTIONS FOR MANUAL POWERDOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

When using both manual and enhanced automatic powerdown (FORCEON = 0), the ICL32xxE will not power up from manual powerdown until both $\overline{\text{FORCEOFF}}$ and FORCEON are driven high, or until a transition occurs on a receiver or transmitter input. Figure 8 illustrates a circuit for ensuring that the ICL32xxE powers up as soon as $\overline{\text{FORCEOFF}}$ switches high. The rising edge of the Master Powerdown signal forces the device to power up, and the ICL32xxE returns to enhanced automatic powerdown mode an RC time constant after this rising edge. The time constant isn't critical, because the ICL32xxE remains powered up for 30 seconds after the FORCEON falling edge, even if there are no signal transitions. This gives slow-to-wake systems (e.g., a mouse) plenty of time to start transmitting, and as long as it starts transmitting within 30 seconds both systems remain enabled.

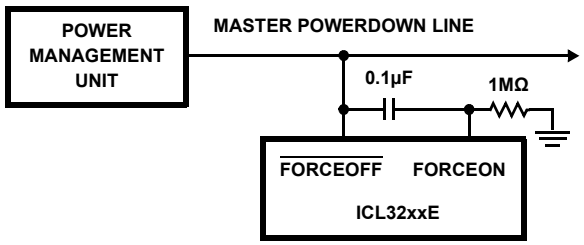


FIGURE 8. CIRCUIT TO ENSURE IMMEDIATE POWER UP WHEN EXITING FORCED POWERDOWN

$\overline{\text{INVALID}}$ Output

The $\overline{\text{INVALID}}$ output always indicates (see Table 2 on page 10) whether or not 30µs have elapsed with invalid RS-232 signals (see Figures 9 and 11) persisting on all of the receiver inputs, giving the user an easy way to determine when the interface block should power down. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{\text{INVALID}}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{\text{INVALID}}$ switches high, and the power management logic wakes up the interface block. $\overline{\text{INVALID}}$ can also be used to indicate the DTR or RING INDICATOR signal, as long as the other receiver inputs are floating, or driven to GND (as in the case of a powered down driver).

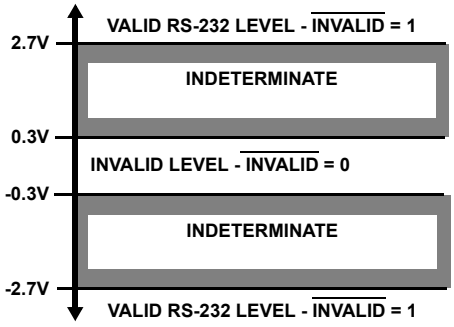


FIGURE 9. DEFINITION OF VALID RS-232 RECEIVER LEVELS

Enhanced Automatic Powerdown

Even greater power savings is available by using these devices, which feature an *enhanced automatic* powerdown function. When the enhanced powerdown logic determines that no transitions have occurred on any of the transmitter nor receiver inputs for 30 seconds, the charge pump and transmitters powerdown, thereby reducing supply current to 1µA. The ICL32xxE automatically powers back up whenever it detects a transition on one of these inputs. This automatic powerdown feature provides additional system power savings without changes to the existing operating system.

Enhanced automatic powerdown operates when the FORCEON input is low, and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic powerdown, but manual powerdown is always available via the overriding $\overline{\text{FORCEOFF}}$ input. Table 2 on page 10 summarizes the enhanced automatic powerdown functionality.

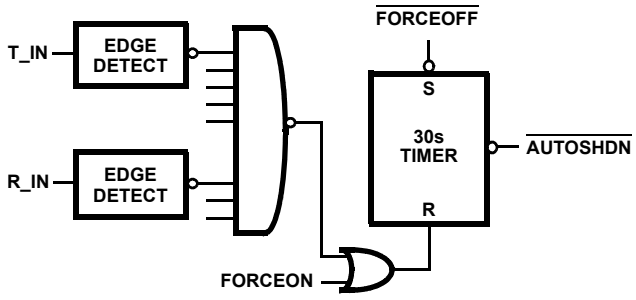


FIGURE 10. ENHANCED AUTOMATIC POWERDOWN LOGIC

Figure 10 illustrates the enhanced powerdown control logic. Note that once the ICL32xxE enters powerdown (manually or automatically), the 30 second timer remains timed out (set), keeping the ICL32xxE powered down until FORCEON transitions high, or until a transition occurs on a receiver or transmitter input.

The $\overline{\text{INVALID}}$ output signal switches low to indicate that invalid levels have persisted on all of the receiver inputs for more than 30µs (see Figure 11), but this has no direct effect on the state of the ICL32xxE (see the next sections for methods of utilizing $\overline{\text{INVALID}}$ to power down the device). $\overline{\text{INVALID}}$ switches high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic powerdown, or forced on), so it is also useful for systems employing manual powerdown circuitry.

The time to recover from automatic powerdown mode is typically 100µs.

Emulating Standard Automatic Powerdown

If enhanced automatic powerdown isn't desired, the user can implement the standard automatic powerdown feature (mimics the function on the ICL3221E/ICL3223E/ICL3243E) by connecting the $\overline{\text{INVALID}}$ output to the FORCEON and $\overline{\text{FORCEOFF}}$ inputs, as shown in Figure 12. After 30µs of invalid receiver levels, $\overline{\text{INVALID}}$ switches low and drives the ICL32xxE into a forced powerdown condition. $\overline{\text{INVALID}}$ switches high as soon as a receiver input senses a valid RS-232 level, forcing the ICL32xxE to power on. See the "$\overline{\text{INVALID}}$ DRIVING FORCEON AND $\overline{\text{FORCEOFF}}$" section of Table 2 on page 10 for an operational summary. This operational mode is perfect for handheld devices that communicate with another computer via a detachable cable. Detaching the cable allows the internal receiver pull-down resistors to pull the inputs to GND (an invalid RS-232 level), causing the 30µs timer to time out and drive the IC into powerdown. Reconnecting the cablerestores valid levels, causing the IC to power back up.

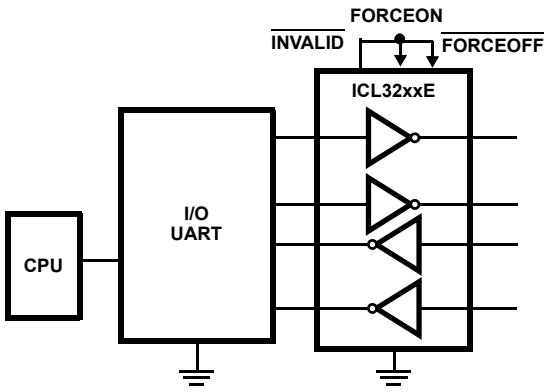


FIGURE 11. CONNECTIONS FOR AUTOMATIC POWERDOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

Hybrid Automatic Powerdown Options

For devices which communicate only through a detachable cable, connecting $\overline{\text{INVALID}}$ to $\overline{\text{FORCEOFF}}$ (with FORCEON = 0) may be a desirable configuration. While the cable is attached $\overline{\text{INVALID}}$ and $\overline{\text{FORCEOFF}}$ remain high, so the enhanced automatic powerdown logic powers down the RS-232 device whenever there is 30 seconds of inactivity on the receiver and transmitter inputs. Detaching the cable allows the receiver inputs to drop to an invalid level (GND), so $\overline{\text{INVALID}}$ switches low and forces the RS-232 device to power down. The ICL32xxE remains powered down until the cable is reconnected ($\overline{\text{INVALID}}$ = $\overline{\text{FORCEOFF}}$ = 1) and a transition occurs on a receiver or transmitter input (see Figure 10 on page 11). For immediate power up when the cable is reattached, connect FORCEON to $\overline{\text{FORCEOFF}}$ through a network similar to that shown in Figure 8 on page 11.

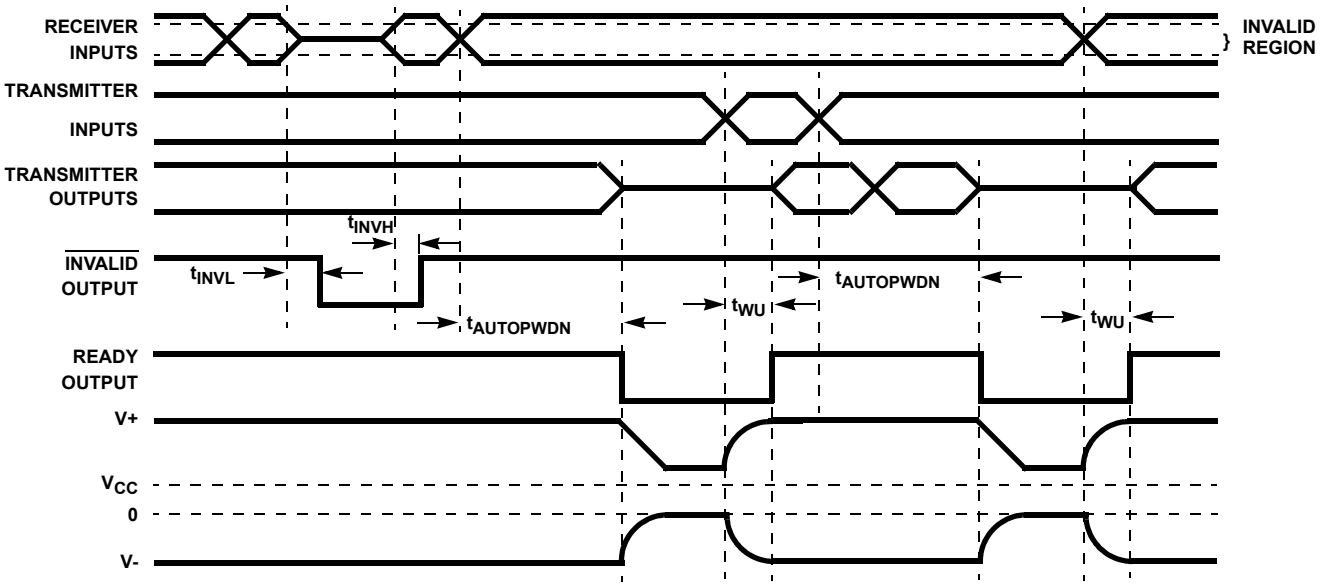


FIGURE 12. ENHANCED AUTOMATIC POWERDOWN, $\overline{\text{INVALID}}$ AND READY TIMING DIAGRAMS

Ready Output (ICL3225E and ICL3227E Only)

The Ready output indicates that the ICL322xE is ready to transmit. Ready switches low whenever the device enters powerdown, and switches back high during power-up when V- reaches -4V or lower.

Capacitor Selection

The charge pumps require 0.1µF capacitors for 3.3V operation. For other supply voltages refer to Table 3 for capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C_2, C_3, and C_4 can be increased without increasing C_1's value, however, do not increase C_1 without also increasing C_2, C_3, and C_4 to maintain the proper ratios (C_1 to the other capacitors).

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's Equivalent Series Resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

TABLE 3. REQUIRED CAPACITOR VALUES

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Operation Down to 2.7V

ICL32xxE transmitter outputs meet RS-562 levels (±3.7V), at full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure inter-operability with RS-232 devices.

Transmitter Outputs when Exiting Powerdown

Figure 13 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

Mouse Driveability

The ICL3245E is specifically designed to power a serial mouse while operating from low voltage supplies. Figure 14 shows the transmitter output voltages under increasing load current. The on-chip switching regulator ensures the transmitters will supply at least ±5V during worst case conditions (15mA for paralleled V+ transmitters, 7.3mA for single V- transmitter).

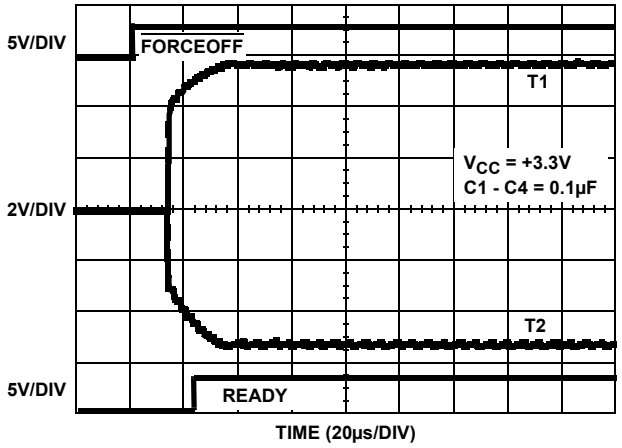


FIGURE 13. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN

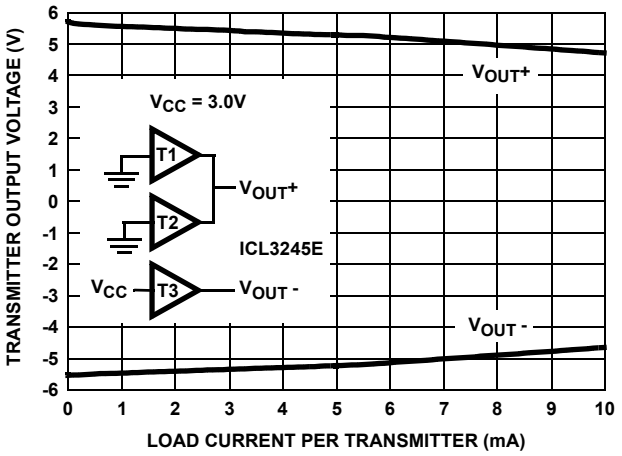


FIGURE 14. TRANSMITTER OUTPUT VOLTAGE vs LOAD CURRENT (PER TRANSMITTER, i.e., DOUBLE CURRENT AXIS FOR TOTAL V_{OUT}+ CURRENT)

High Data Rates

The ICL32xxE maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 15 on page 14 details a transmitter loopback test circuit, and Figure 16 on page 14 illustrates the loopback test result at 250kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 250kbps. Figure 17 on page 14 shows the loopback results for a single transmitter driving 250pF and an RS-232 load at 1Mbps. The static transmitters were also loaded with an RS-232 receiver.

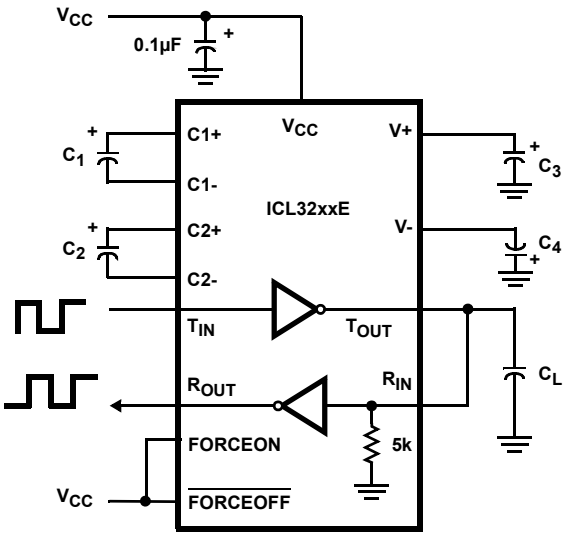


FIGURE 15. TRANSMITTER LOOPBACK TEST CIRCUIT

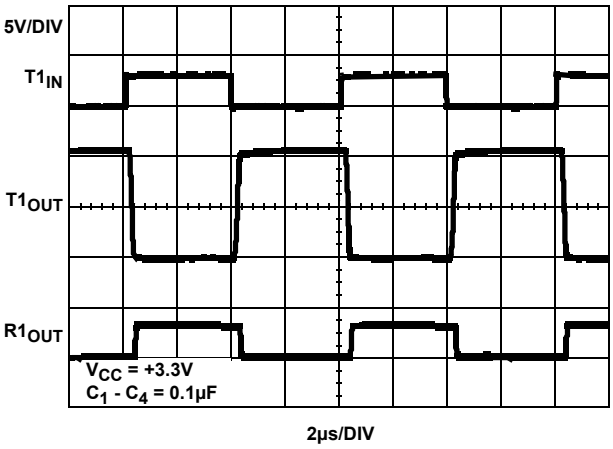


FIGURE 16. LOOPBACK TEST AT 250kbps (C_L = 1000pF)

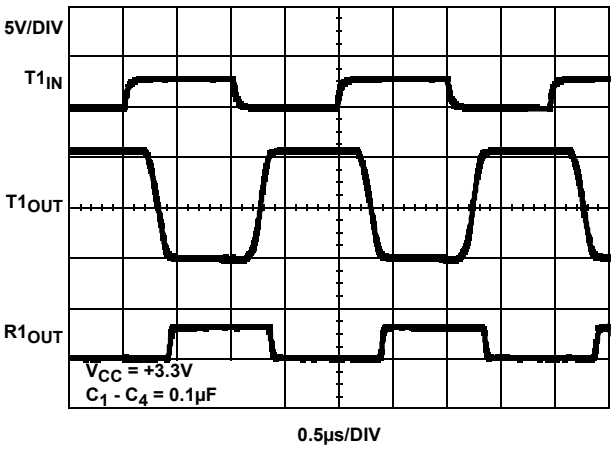


FIGURE 17. LOOPBACK TEST AT 1Mbps (C_L = 250pF)

Interconnection with 3V and 5V Logic

The ICL32xxE directly interfaces with 5V CMOS and TTL logic families. Nevertheless, with the ICL32xx at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ICL32xx inputs, but ICL32xx outputs do not reach the minimum V_{IH} for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ICL32XX outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

±15kV ESD Protection

All pins on ICL32xx devices include ESD protection structures, but the ICL32xxE family incorporates advanced structures, which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an ICs ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM

test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting Level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C

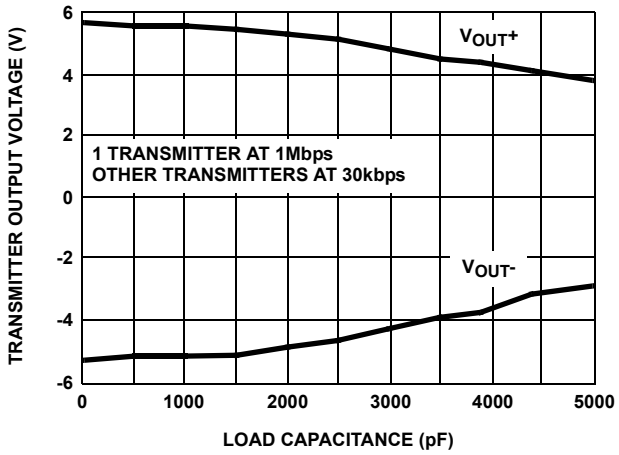


FIGURE 18. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

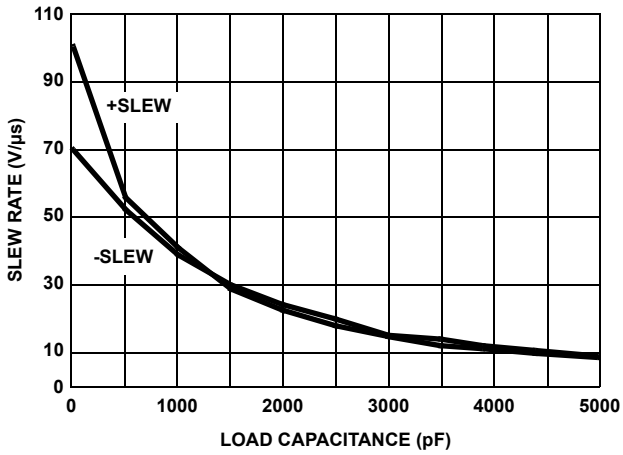


FIGURE 19. SLEW RATE vs LOAD CAPACITANCE

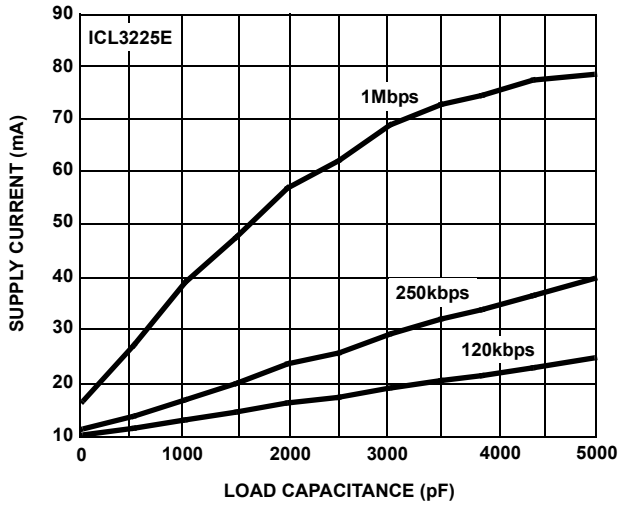


FIGURE 20. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

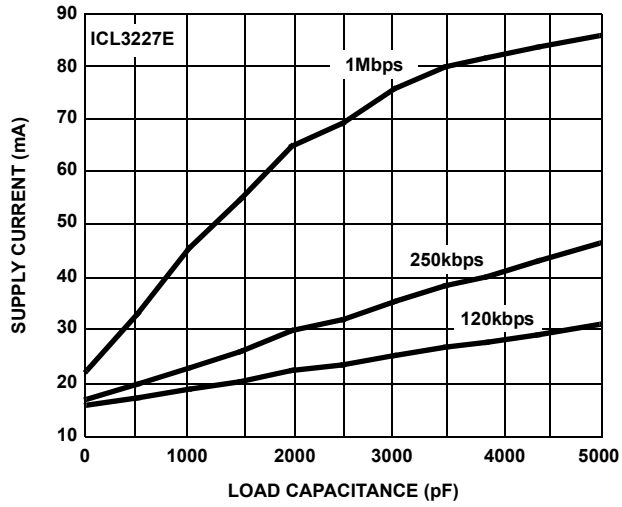


FIGURE 21. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C (Continued)

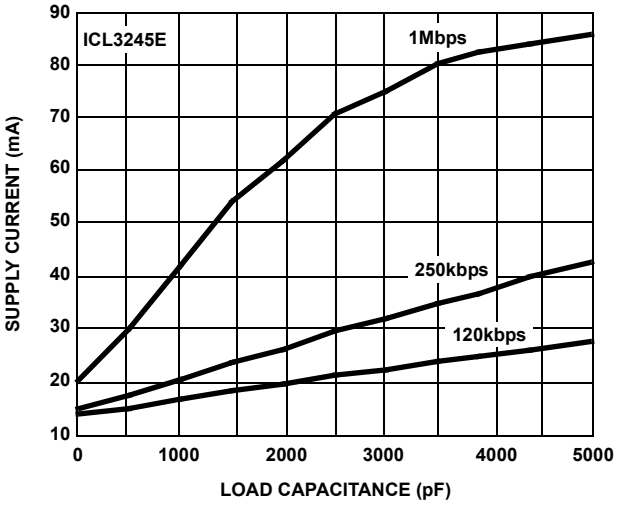


FIGURE 22. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

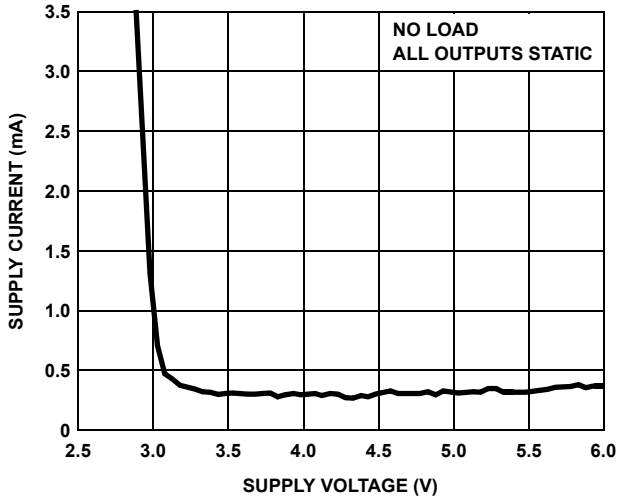


FIGURE 23. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

MSUBSTRATE POTENTIAL (POWERED UP)

GND

TRANSISTOR COUNT

ICL3225E: 937
ICL3227E: 825
ICL3245E: 1109

PROCESS

Si Gate CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 12, 2016	FN4900.12	Updated entire datasheet applying Intersil's new standards. Updated Ordering information table on page 2. -Updated Tape and Reel note. -Updated Note 2. -Added MSL note. -Removed all non-compliant products. In the "Electrical Specifications" table under "ESD PERFORMANCE" on page 8, Updated All Other pins section by changing typical value for the ICL3245E from "±3" to "±2" and adding ICL3225E and ICL3227E information.
December 3, 2015	FN4900.11	Updated Ordering Information Table on page 2: Added replacement part numbers for ICL3245ECBZ and ICL3245ECVZ.
August 31, 2015	FN4900.10	Ordering Information Table on page 2. Added Revision History. Added About Intersil Verbiage. Updated POD M28.3 to latest revision changes: Added land pattern.

About Intersil

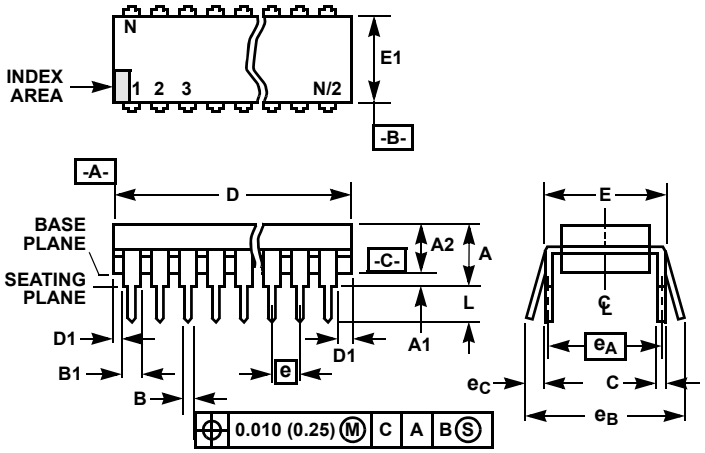
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

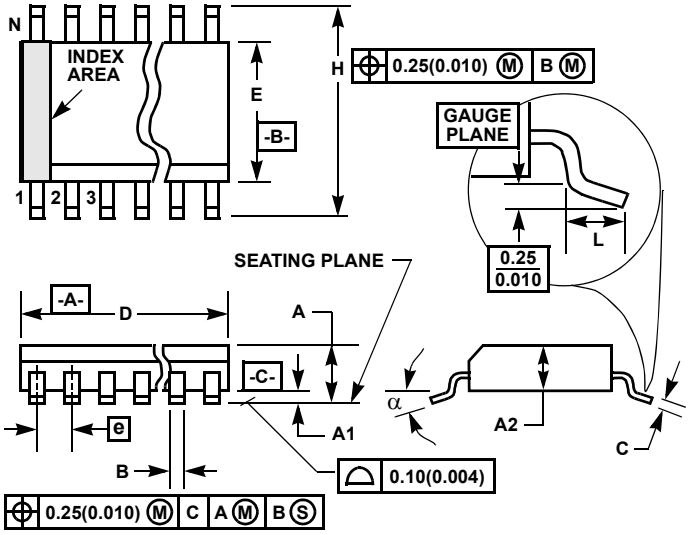
Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

For the most recent package outline drawing, see E20.3.

Small Outline Plastic Packages (SSOP)



M16.209 (JEDEC MO-150-AC ISSUE B)

16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	16		16		7
α	0°	8°	0°	8°	-

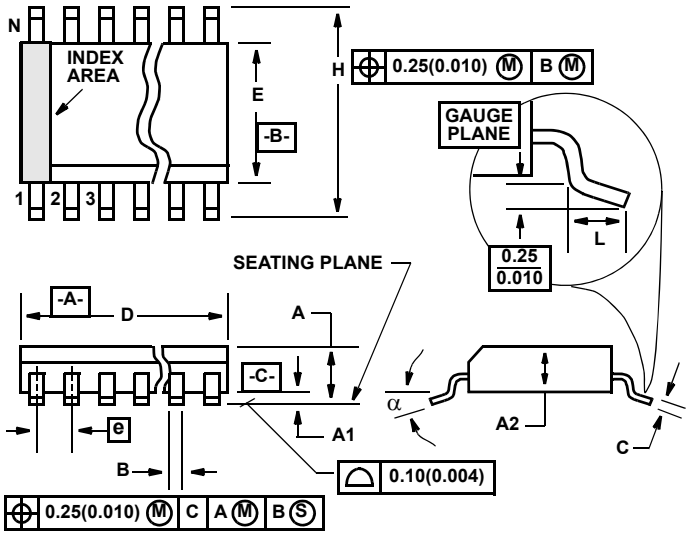
Rev. 3 6/05

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

For the most recent package outline drawing, see M16.209.

Shrink Small Outline Plastic Packages (SSOP)



M20.209 (JEDEC MO-150-AE ISSUE B)
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

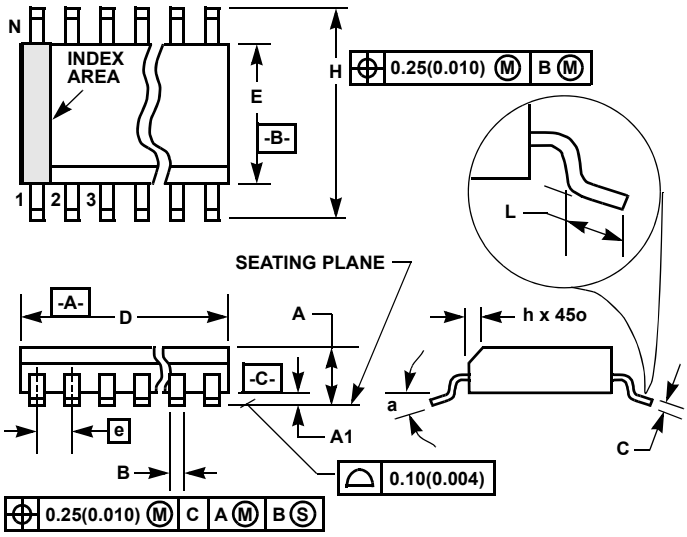
Rev. 3 11/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

For the most recent package outline drawing, see M20.209.

Small Outline Plastic Packages (SOIC)

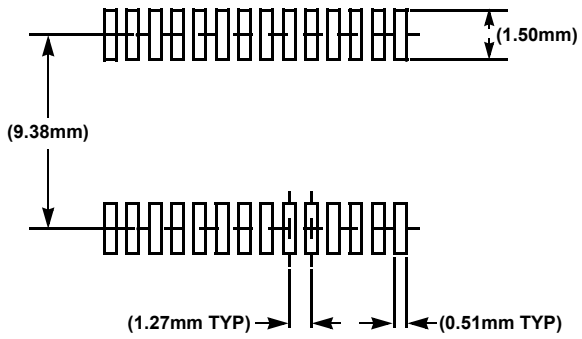


M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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TYPICAL RECOMMENDED LAND PATTERN

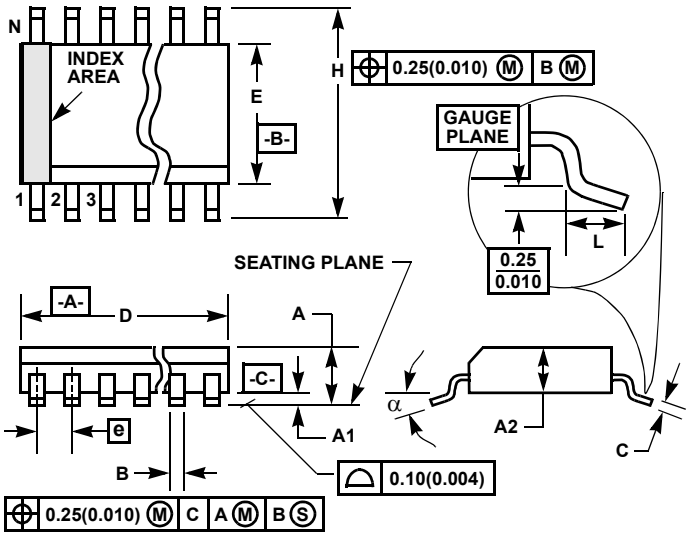


NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

For the most recent package outline drawing, see M28.3.

Shrink Small Outline Plastic Packages (SSOP)



M28.209 (JEDEC MO-150-AH ISSUE B)
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

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NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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For the most recent package outline drawing, see M28.209.