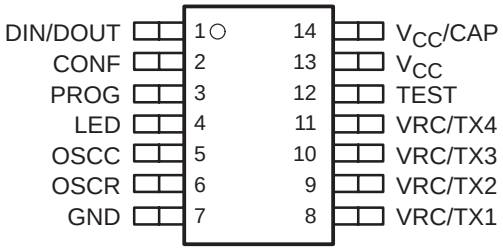
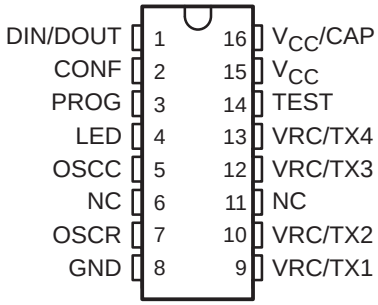
- **Devices can be Configured as an Encoder or a Decoder**
- **Hopping 40-Bit Security Code† (More Than 1 Trillion Combinations) and Transmitter-Lock™ Provide Extremely High Security**
- **Four Independent Inputs/Outputs Allow For Control of Up To 15 Functions**
- **Internal EEPROM and Programming Charge Pump**
- **No Programming Station Required – Self-Programming Encoder**
- **Smart Decoder Learns Up To Four Different Encoders**
- **Adjustable Internal Clock Provides Wide Range of Data-Rate Speeds**
- **Internal Amplifier and Comparator for Amplification and Shaping of Low-Level Input Signals With Autobias Adaptive Threshold Circuitry using Switched-Capacitor Technology**
- **Minimum Number of Required External Components and Surface-Mount Packaging for Extremely Small Circuit Footprint**
- **Advanced CMOS Processing Technology for Minimum Power Consumption and 2.7-V to 15-V Operation**

D PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TRC1300 and TRC1315 are remote control serial-data encoders and decoders, and are members of the MARCSTAR™ (Multichannel Advanced Remote Control Serial Transmitter and Receiver) family of remote control serial-data devices. Each can be configured to perform as either the encoder or the decoder in a remote control system. The TRC1300 and TRC1315 are designed for use in high-volume remote control products such as automobile and home security systems, consumer electronics, electronic keys, and remote keyless entry applications. They are low-power devices and are well suited to battery operation with a supply voltage of 2.7 V to 6 V for the TRC1300 and 2.7 V to 15 V for the TRC1315.

Four independent encoder inputs/decoder outputs allow for control of up to 15 functions. Forty bits of hopping code provide high security, more than one trillion possible combinations, so that the same code will never be used twice by a MARCSTAR device over several lifetimes of a typical system. The MARCSTAR devices are self-programming with internal charge-pump programming circuitry. A smart decoder design learns up to four different encoders, all in a high-security hopping-code format.

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† The coding algorithm and other MARCSTAR functionality are patented or are patent pending.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

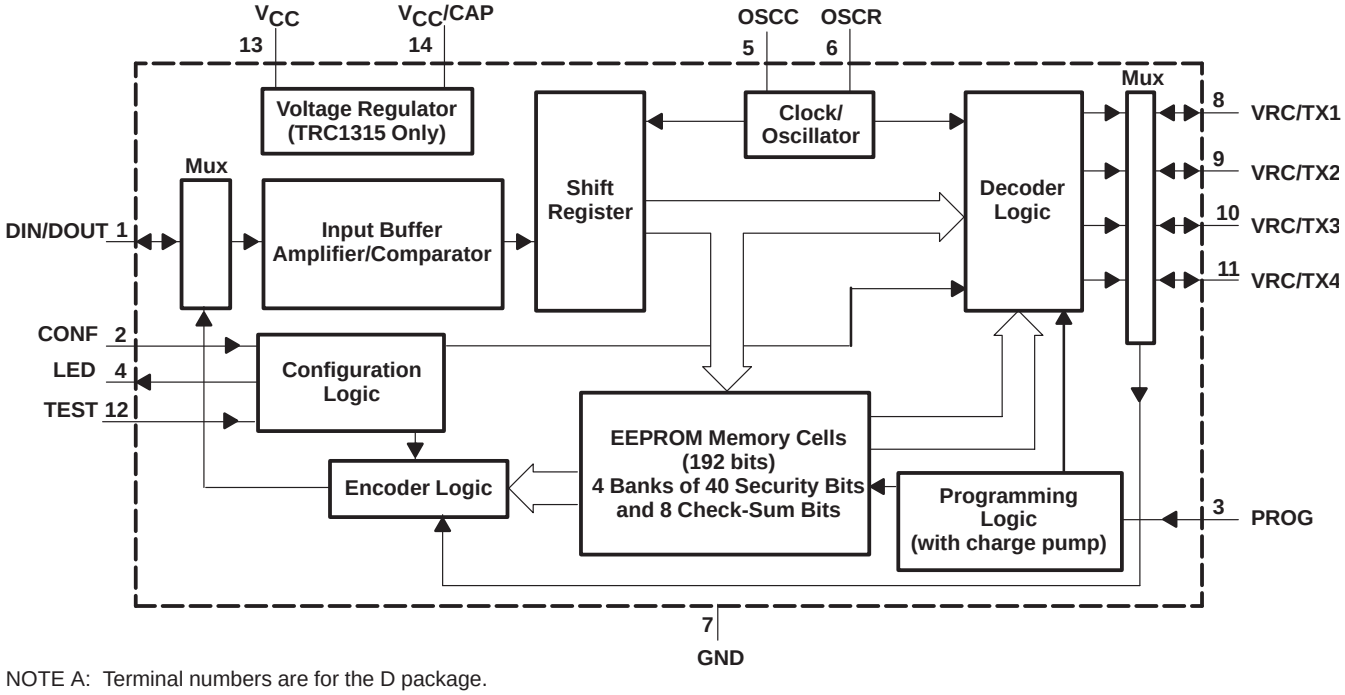
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description (continued)

The TRC1300 and TRC1315 include several on-chip functions that normally require additional circuitry in a system design. These include an amplifier/comparator for detection and shaping of input signals as low as a few millivolts (typically when an RF link is used) and a variable-frequency internal oscillator to clock the transmitted or received security code.

The TRC1300 and TRC1315 MARCSTAR I E/D remote control encoder/decoders are characterized for operation over the temperature range of –40°C to 85°C and are available in 14-pin SOIC small-outline IC surface-mount (D) and 16-pin PDIP plastic dual in-line (N) packages.

functional block diagram



NOTE A: Terminal numbers are for the D package.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	D	N		
CONF	2	2	I	Device configuration select. When CONF is held at a high logic level, the device assumes the encoder mode. CONF is internally pulled up, and no connection to CONF is required for the encoder mode of operation. When CONF is held at a low logic level at power up, the device assumes the decoder mode. Note that this terminal is read only at device power up; CONF must be tied to GND *before* V_{CC} is applied to select the decoder mode.
DIN/DOUT	1	1	I/O	Serial data input/output. In the decoder mode, DIN/DOUT becomes an input to receive serial data from up to four remote encoders. In the learn mode, DIN/DOUT becomes an input to learn code from up to four remote encoders. In the encoder mode, DIN/DOUT becomes an output for the encoded data. DIN/DOUT is clocked by the internal variable oscillator.
GND	7	8		Analog and logic ground
LED	4	4	O	Status indicator. The LED terminal goes low, causing an LED connected from V_{CC} (anode) to the LED terminal (cathode) through a current-limiting resistor to light, indicating the following conditions: • Encoder mode. When the device is configured as an encoder, the LED terminal is active during the transmission of data (including the blank time between frames). • Program mode (encoder). When the device is configured as an encoder and placed in the program mode, the LED terminal is active until the device has generated and stored a new 40-bit security code. • Learn mode (decoder). When the device is configured as a decoder and placed in the program mode, the LED terminal is active until the device has successfully stored 40 bits of security code received from an encoder through terminal DIN/DOUT. • Test mode. When the device is placed in the self-test mode, the results are indicated by flashing the LED connected to the LED terminal.
OSCC	5	5	I/O	Internal oscillator frequency control. A capacitor connected from OSCC to GND and a resistor connected from OSCR to OSCC determine the frequency of the internal oscillator.
OSCR	6	7	I/O	Internal oscillator frequency control. A resistor connected from OSCR to OSCC and a capacitor connected from OSCC to GND determine the frequency of the internal oscillator.
PROG	3	3	I	Programming enable. When PROG is held at a logic-high, device enters the programming mode. In the encoder mode, a new 40-bit security code is generated and stored in EEPROM. In the decoder mode, the device enters a learn cycle that continues until it has successfully received 40 bits of code from an encoder and stored them in EEPROM. PROG is internally pulled down and debounced.
TEST	12	14	I	Test mode select. When TEST is momentarily taken high, the device enters a self-test mode with the results of the self-test mode displayed by flashing the LED connected to the LED terminal. TEST is internally pulled down.
V_{CC} (TRC1300)	13	15		Not used.
V_{CC} (TRC1315)	13	15		Power supply input for the TRC1315 only. The voltage range for V_{CC} is 4.5 V to 15 V. A 0.1-µF bypass capacitor should be connected from V_{CC} to GND.
V_{CC}/CAP (TRC1300)	14	16		Power supply input for the TRC1300 only. The voltage range for V_{CC}/CAP is 2.7 V to 6 V. A 0.1-µF bypass capacitor should be connected from V_{CC}/CAP to GND.
V_{CC}/CAP (TRC1315)	14	16		Regulated voltage output for the TRC1315 only. This terminal provides a regulated 4.5 V to 5.5 V output. A 1-µF and a 0.1-µF bypass capacitor should be connected from V_{CC}/CAP to GND.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO. D	NO. N		
VRC/TX1	8	9	I/O	Function 1 VRC (valid received code) output and function 1 encode enable. In the decode mode, VRC/TX1 is an output that goes to a logic-low state (for one frame — 768 clocks) when the device receives the correct 40 bits of security code and function data (4 bits) matching function 1. In the encoder mode, VRC/TX1 is an input that initiates the encoding of function 1 and output of function 1 data. When VRC/TX1 is pulled to GND, the device continuously outputs the function-1 code sequence stored in EEPROM memory from DIN/DOUT up to 360 times. The device cannot transmit function-1 code again until VRC/TX1 is again pulled to GND. VRC/TX1 has an internal pullup resistor in both the encoder and decoder modes, and switch debouncing in the encoder mode.
VRC/TX2	9	10	I/O	Function 2 VRC (valid received code) output and function 2 encode enable. In the decode mode, VRC/TX2 is an output that goes to a logic-low state (for one frame — 768 clocks) when the device receives the correct 40 bits of security code and function data (4 bits) matching function 2. In the encoder mode, VRC/TX2 is an input that initiates the encoding of function 2 and output of function 2 data. When VRC/TX2 is pulled to GND, the device continuously outputs the function-2 code sequence stored in EEPROM memory from DIN/DOUT up to 360 times. The device cannot transmit function-2 code again until VRC/TX2 is again pulled to GND. VRC/TX2 has an internal pullup resistor in both the encoder and decoder modes, and switch debouncing in the encoder mode.
VRC/TX3	10	12	I/O	Function 3 VRC (valid received code) output and function 3 encode enable. In the decode mode, VRC/TX3 is an output that goes to a logic-low state (for one frame — 768 clocks) when the device receives the correct 40 bits of security code and function data (4 bits) matching function 3. In the encoder mode, VRC/TX3 is an input that initiates the encoding of function 3 and output of function 3 data. When VRC/TX3 is pulled to GND, the device continuously outputs the function-3 code sequence stored in EEPROM memory from DIN/DOUT up to 360 times. The device cannot transmit function-3 code again until VRC/TX3 is again pulled to GND. VRC/TX3 has an internal pullup resistor in both the encoder and decoder modes, and switch debouncing in the encoder mode.
VRC/TX4	11	13	I/O	Function 4 VRC (valid received code) output and function 4 encode enable. In the decode mode, VRC/TX4 is an output that goes to a logic-low state (for one frame — 768 clocks) when the device receives the correct 40 bits of security code and function data (4 bits) matching function 4. In the encoder mode, VRC/TX4 is an input that initiates the encoding of function 4 and output of function 4 data. When VRC/TX4 is pulled to GND, the device continuously outputs the function-4 code sequence stored in EEPROM memory from DIN/DOUT up to 360 times. The device cannot transmit function-4 code again until VRC/TX4 is again pulled to GND. VRC/TX4 has an internal pullup resistor in both the encoder and decoder modes, and switch debouncing in the encoder mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, TRC1300, V_{CC} (see Note 1) . . . . . –0.6 V to 7 V
TRC1315, V_{CC} (see Note 1) . . . . . –0.6 V to 15 V
Input voltage, logic/analog signals, V_I . . . . . –0.6 V to 7 V
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
ESD protection, all terminals, human body . . . . . 2 kV
machine . . . . . 200 V
JEDEC latchup . . . . . 120 mA or 13.2 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to GND.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, device configured as an encoder, V_{CC}	TRC1300	2.7	6	V
	TRC1315	2.7	15	
Supply voltage, device configured as a decoder, V_{CC}	TRC1300	4.5	6	V
	TRC1315	4.5	15	
Low-level input voltage, V_{IL}, at VRC/TX1–VRC/TX4, TEST, CONF, PROG			0.5	V
High-level input voltage, V_{IH}, at VRC/TX1–VRC/TX4, TEST, CONF, PROG		V_{CC}/CAP–0.5		V
Operating free-air temperature, T_A		– 40	85	°C
Input voltage to amplifier/comparator, $V_{I(PP)}$, at DIN/DOUT		10		mV
Common-mode input voltage range, amplifier/comparator		GND + 0.2	V_{CC}/CAP–0.2	V

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

digital interface

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	VRC/TX1–VRC/TX4, DIN/DOUT, LED	I_{OL} = 5 mA			0.5	V
V_{OH}	High-level output voltage	VRC/TX1–VRC/TX4, DIN/DOUT, LED	I_{OH} = –4 mA	V_{CC}/CAP–0.5			V
I_{IL}	Low-level input current	DIN/DOUT	V_I = 0 to V_{IL}			1	µA
		VRC/TX1–VRC/TX4		–20	–12	–5	
		CONF		–20	–11	–5	
		PROG				1	
		TEST				1	
I_{IH}	High-level input current	DIN/DOUT	V_I = V_{IH} to V_{CC}/CAP	5		20	µA
		VRC/TX1–VRC/TX4				1	
		CONF				1	
		PROG		2	5	8	
		TEST		5	12	20	

decoder supply current, V_{CC}/CAP = 6 V, T_A = 25°C

PARAMETER	MIN	TYP	MAX	UNIT
Supply current		1.8	2.2	mA

encoder supply current, TRC1300, V_{CC}/CAP= 6 V, T_A = 25°C

PARAMETER	MIN	TYP	MAX	UNIT
Supply current, standby		35	500	nA
Supply current, code transmission		1.5	1.7	mA

encoder supply current, TRC1315, V_{CC} = 15 V, T_A = 25°C

PARAMETER	MIN	TYP	MAX	UNIT
Supply current, standby			3	µA
Supply current, code transmission		1.4	1.9	mA

regulated output source current, TRC1315, active state, decoder mode, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum current at V_{CC}/CAP for 5 V ± 10% output	V_{CC} = 6.4 V			8	mA
Maximum current at V_{CC}/CAP for 5 V ± 10% output	V_{CC} = 12 V			30	mA

oscillator characteristics

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Sample-clock frequency, $f_{(SCLK)}$		5	50	kHz
Data-clock frequency, $f_{(DCLK)}$		500	5000	Hz
Frequency spread (temperature, V_{CC}) using external capacitor	V_{CC}/CAP 4 V – 6 V (decoder)		±7%	
	V_{CC}/CAP 2.7 V – 6 V (encoder)		±10%	
Required encoder frequency accuracy for synchronization		0.5 f_{RX}†	2 f_{RX}†	

† f_{RX} is decoder frequency.

encoder self programming

PARAMETER	MIN	MAX	UNIT
Minimum time for PROG low to generate a new 40-bit security code		300	µs

EEPROM write/erase endurance

PARAMETER	MIN	TYP	MAX	UNIT
Number of program cycles	100 000	1000000		cycles

EEPROM data retention

PARAMETER	MIN	TYP	MAX	UNIT
Data retention		10		years

function switch input characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Pulldown current at DIN/DOUT, PROG, TEST	V_{CC}/CAP = 5 V		7.7		µA
	V_{CC}/CAP = 4 V		4.8		µA
	V_{CC}/CAP = 3 V		2.3		µA
	V_{CC}/CAP = 2.4 V		1.3		µA
Pulldown resistor value at DIN/DOUT, PROG, TEST	V_{CC}/CAP = 5 V		649		kΩ
	V_{CC}/CAP = 4 V		833		kΩ
	V_{CC}/CAP = 3 V		1304		kΩ
	V_{CC}/CAP = 2.4 V		1846		kΩ
Pullup current at TX1–TX4, CONF, LED	V_{CC}/CAP = 5 V		7.7		µA
	V_{CC}/CAP = 4 V		4.8		µA
	V_{CC}/CAP = 3 V		2.4		µA
	V_{CC}/CAP = 2.4 V		1.3		µA
Pullup resistor value at TX1–TX4, CONF, LED	V_{CC}/CAP = 5 V		649		kΩ
	V_{CC}/CAP = 4 V		833		kΩ
	V_{CC}/CAP = 3 V		1250		kΩ
	V_{CC}/CAP = 2.4 V		1846		kΩ

switching characteristics over recommended ranges of supply voltage and free-air temperature (see Figure 1)

PARAMETER			MIN	TYP	MAX	UNIT
	Cycle time of sample clock (SCLK)	Oscillating period	20		200	µs
t_C	Cycle time of data clock (DCLK)	Oscillating period	200		2000	µs
$t_{C(0)}$	Cycle time of logic-0 symbol			3 t_C		µs
$t_{C(1)}$	Cycle time of logic-1 symbol			3 t_C		µs
$t_{C(sync)}$	Cycle time of sync pulse			2 t_C		µs
t_W	Pulse duration of dummy pulse			t_C		µs

PARAMETER MEASUREMENT INFORMATION

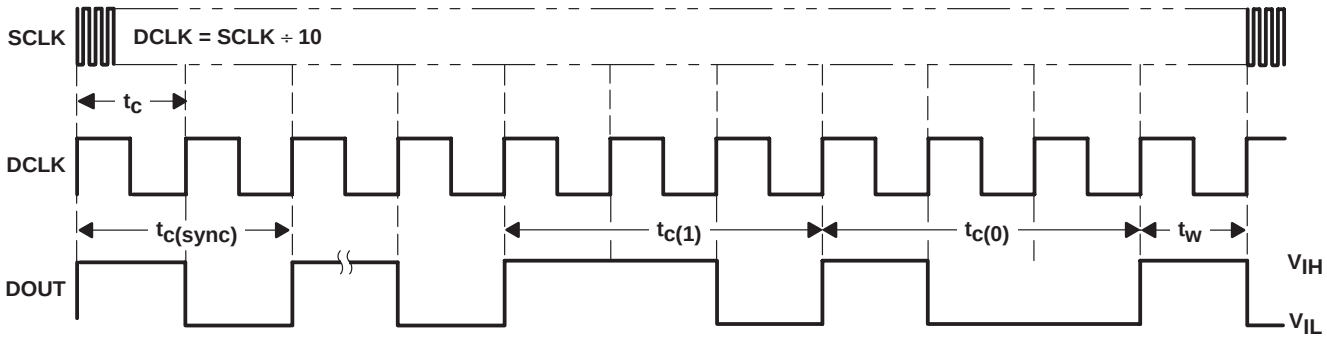


Figure 1. Timing Diagram

PRINCIPLES OF OPERATION

general

Operation of the MARCSTAR I E/D devices is shown in Figure 2. The devices have two primary modes of operation: encoder mode and decoder mode. Additional modes and functions include programming and learning mode, self-testing mode, security code generation, and clock generation.

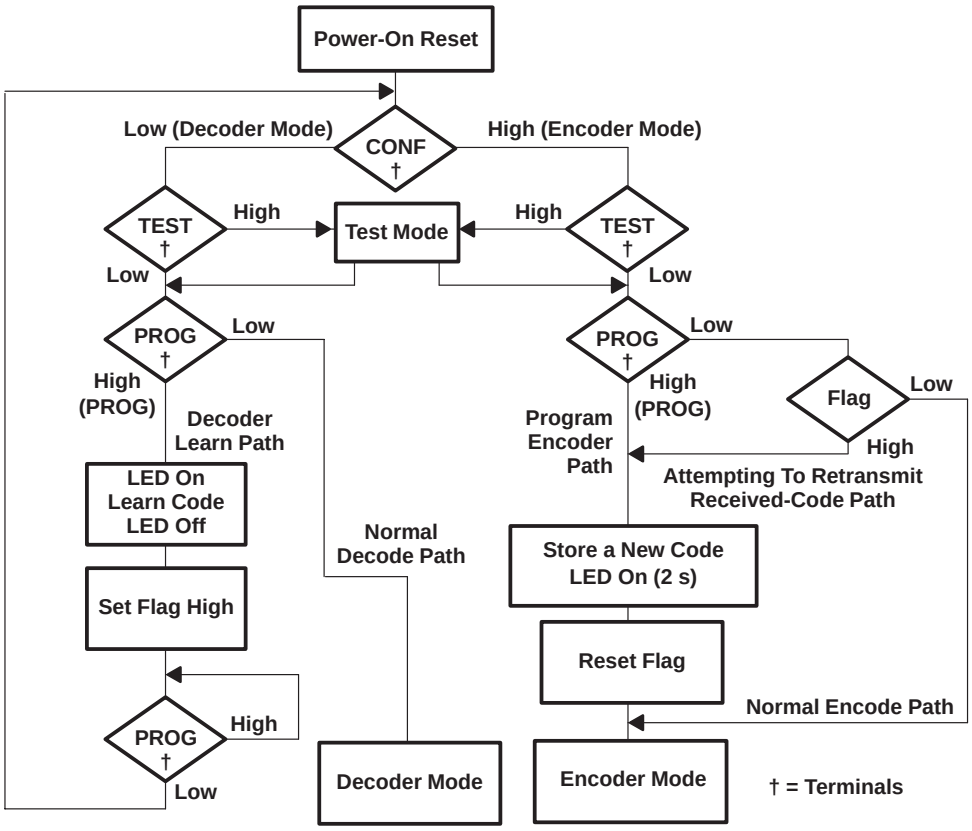


Figure 2. Top Level Operational Flow

PRINCIPLES OF OPERATION

general (continued)

Each of the TRC1300 and TRC1315 MARCSTAR I E/D devices can be pin-selected for operation as either an encoder on the transmitter end of a remote control system, or as a decoder on the receiver end. The intervening medium can be a wired, RF, IR, or any other type of link with sufficient bandwidth to pass the signal. The objective is to transmit a function code to the remote receiver to initiate an event or for some other purpose, with the highest level of certainty that the function code is only accepted from the matching encoder and not from any other.

A MARCSTAR I E/D device operating in the encoder mode can send four different function codes either individually or in any combination to activate up to 15 different functions at the decoder.

Once a decoder learns a security code from an encoder, it then responds only to that particular encoder. A MARCSTAR I E/D device operating in the decoder mode can learn and respond to as many as four different encoders and provides four independent function outputs. These outputs can be further decoded (externally) to provide a 1-of-15 function output.

hopping code

The MARCSTAR I E/D devices use an advanced hopping-code algorithm to significantly increase the security level of the system. The security code sent by the encoder *and* the security code accepted as valid by the decoder change after each transmission. This is done independently for each of the four separate encoder security codes learned by the decoder.

As an encoder, the MARCSTAR I E/D is shipped from the factory with a unique 40-bit security code stored in on-board nonvolatile memory (EEPROM). Since every device shipped has a unique code, it is ready for immediate use and requires no reprogramming. Then, each time a function input is activated, the encoder fetches the 40-bit security code from EEPROM and encrypts it. Next, the encoder assembles the data frame to be output, and then sends it out. The data frame consists of the synchronizing bits, the encrypted security bits, the function data bits, a dummy bit, and the blank-time bits. After the data frames output ends, the encoder immediately increments the 40-bit security code by applying the special hopping-code algorithm to it and then stores the results in EEPROM for the next time a function input is activated. Thus, each time a function input is activated, the 40-bit security code that is sent out is different from the security code in the previous transmission. And with more than a trillion possible combinations, the same code is never sent twice over the lifetime of a system.

As a decoder, the MARCSTAR I E/D initially learns the 40-bit security code stored in a particular encoder by receiving it and storing it in on-board EEPROM. Each time a security code is received from an encoder, the device decrypts the received 40-bit security code and compares it with the *next* security code expected from any of the learned encoders. The next expected security code is calculated by applying the same hopping-code algorithm used in the encoder to the 40-bit code stored in the decoder memory. If the received security code matches the next security code expected from one of the learned encoders, it is declared valid and the attached function code is decoded. If the function code is valid, the appropriate function output or outputs are asserted. The just-received 40-bit security code is then incremented according to the algorithm, becoming the next security code expected from that encoder, and stored in EEPROM for next time. If the received security code does *not* match the next expected code from one of the learned encoders, the received function data and security code are ignored.

Because the decoder activates function outputs only when the next expected code in the hopping-code sequence is received, interception and subsequent retransmission of the same code does not activate the decoder function outputs.

PRINCIPLES OF OPERATION

hopping code (continued)

In some cases, the encoder is activated and sends security and function data code without the decoder receiving and decoding the signal (if the receiver is out of range, for example). This would normally cause the encoder and decoder to fall out of sync with each other. MARCSTAR I E/D devices circumvent this by allowing the decoder to activate the function outputs when any one of the next 256 expected security codes is received from a learned encoder. The 256 expected security codes are based on the currently-stored 40-bit security code. In rare cases, the encoder might be activated more than 256 times without being near the decoder, requiring the encoder and decoder pair to be manually resynchronized. In this case, the decoder can simply learn the current encoder security code, using the procedure detailed in the decoder programming section of this document, resynchronizing the pair.

Hopping code provides extremely high security for the encoder/decoder pair and prevents unauthorized access to the receiver and decoder by means of signal interception and retransmission of the intercepted signal.

Transmitter-Lock

Since the MARCSTAR I E/D devices have a pin-selectable encoder/decoder mode, a safeguard (Transmitter-Lock) has been designed into the devices. Transmitter-Lock prevents unauthorized parties from defeating the MARCSTAR security by using a MARCSTAR I E/D device to intercept a transmitted security code and then transmit the next expected security code to the decoder. The received security code would then be recognized as coming from the original encoder and, therefore, valid causing the decoder function outputs to be activated.

The safeguard works by setting an internal flag, stored in EEPROM, whenever the device, in the decoder mode, learns a code from an encoder. This flag then causes a new 40-bit security code to be generated and stored in the EEPROM if the device is later placed in the encoder mode and a transmission is ever attempted. So, once a decoder learn cycle has occurred in a particular MARCSTAR I E/D device, the learned security code will be overwritten by a new 40-bit security code before output in the encoder mode is permitted. This feature allows the MARCSTAR I E/D devices to be used as either an encoder or a decoder without sacrificing the security provided by separate dedicated encoder and decoder devices.

device/system security

Statistically, the probability that a random code would activate the MARCSTAR I E/D devices operating in the decoder mode is calculated using the formula shown in equation 1.

$$\text{Probability} = \frac{\text{valid}}{\text{possible}} \quad \text{where} \quad \begin{array}{l}\text{valid = the number of security codes that activate the device}\\ \text{possible = the total number of possible security codes}\end{array} \tag{1}$$

A MARCSTAR I E/D device operating in the decoder mode responds to a total of 2^8 (256) security codes (including the 256-code look-ahead feature) for *each* of the four encoders it can learn (256×4 valid security codes).

The total number of possible 40-bit security codes is 2^{40} (1.0995 trillion).

Inserting this into the formula gives equation 2.

$$\text{Probability} = \frac{2^8 \times 4}{2^{40}} = \frac{1}{2^{30}} = \frac{1}{1.074 \times 10^9} \tag{2}$$

Therefore, the security of *the entire system* is one in 1.074 billion — there is one chance in 1.074 billion that a random security code would be recognized as valid by a MARCSTAR I E/D device operating in the decoder mode.

PRINCIPLES OF OPERATION

encoder mode

The MARCSTAR I E/D encoder mode operational flow chart is shown in Figure 3.

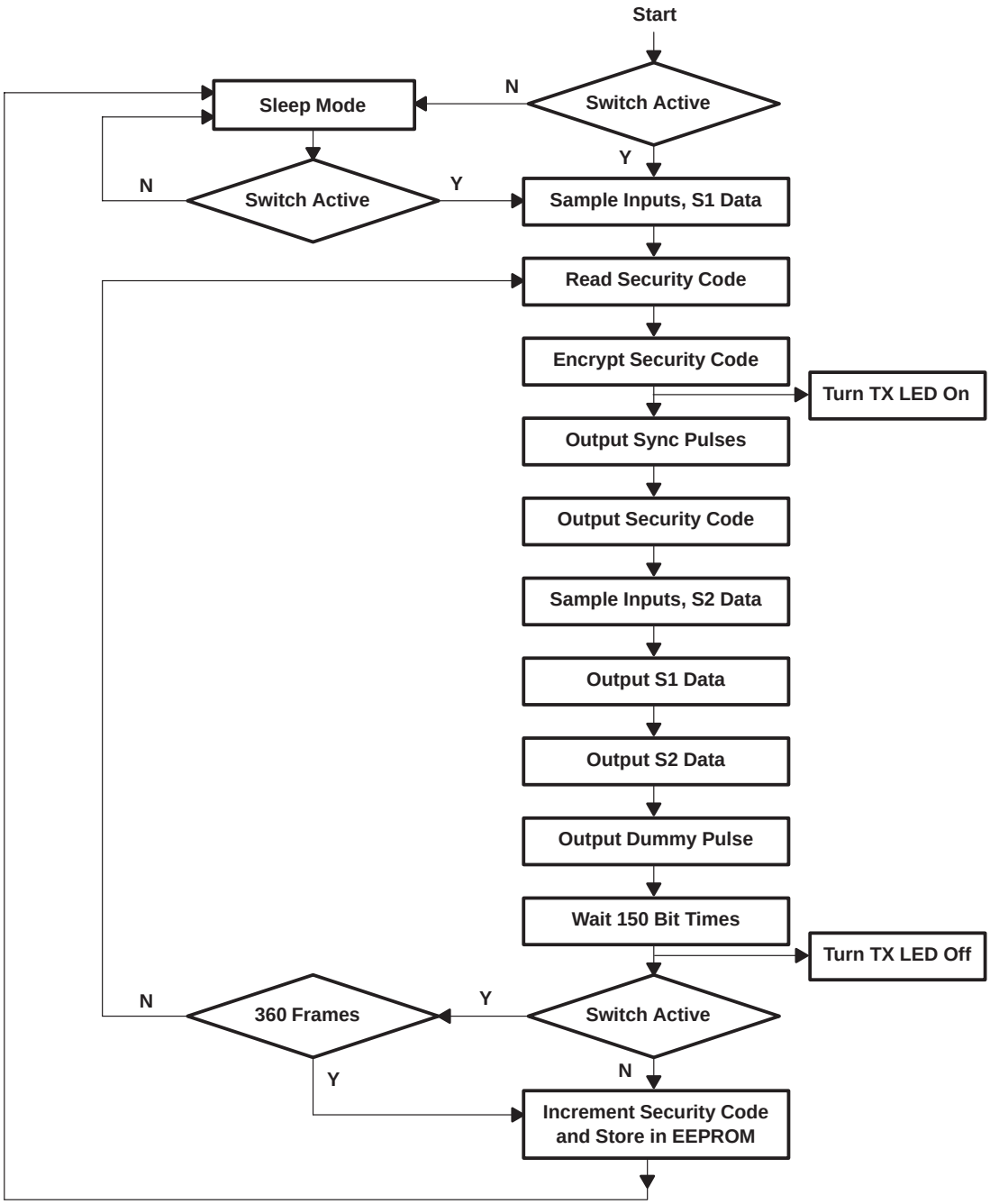


Figure 3. Encoder Mode Operational Flow

PRINCIPLES OF OPERATION

encoder mode (continued)

TRC1300 and TRC1315 MARCSTAR I E/D devices are configured as an encoder by holding the CONF terminal high or by not connecting CONF and allowing the internal pullup to hold it high (a connection to CONF is not required to select the encoder mode).

In the encoder mode, the device sends a maximum of 360 frames of data out through the DIN/DOUT terminal when one or any combination of VRC/TX1 – VRC/TX4 terminals is pulled low — when buttons on a remote transmitter are pressed, for example. The following list and Figure 4 detail the response to various button-press inputs.

- When a button is pressed, a maximum of 360 frames of data are sent.
- Multiple button presses can occur during the output of the 360 frames.
- If all buttons are released before all 360 frames are sent, output of data ceases at that point and the timeout counter resets.
- If any buttons are still pressed after all 360 frames have been sent, no additional data is sent and the timeout counter is not reset.
- The timeout counter resets only when all buttons are released, allowing the device to enter a low-power standby mode while it waits to detect a button press.

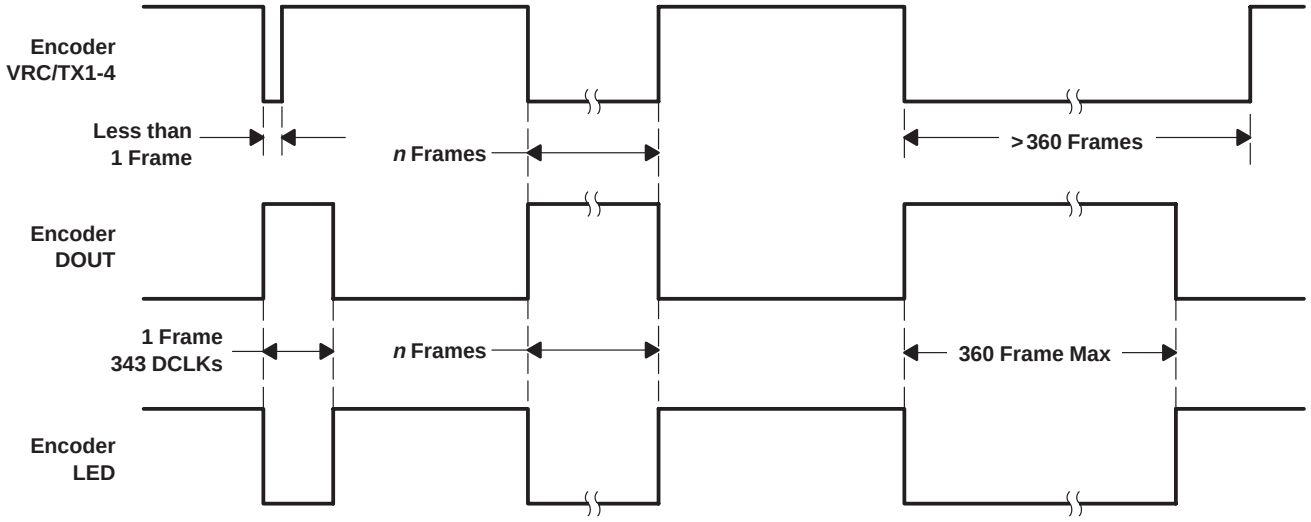


Figure 4. Encoder Timing

PRINCIPLES OF OPERATION

encoder mode (continued)

Two or more buttons can be pressed at the same time to activate additional functions. Since it is not possible to press them at *exactly* the same time, a form of debouncing ensures that only a single function code is received as valid. Function data is sent in two 12-bit packets. The first function-data packet is derived from the first sample of the buttons (S1) at the beginning of the frame, and the second function-data packet is derived from the second sample of the buttons (S2) immediately after the 40-bit security code (see Figure 5). This gives an effective 168 data-clock debounce time because the MARCSTAR I E/D, configured as a decoder, activates function outputs only when the two function data packets in the frame are identical. When valid function data has been received in the first packet but the second packet in a frame contains different function data (caused by a second button being down at sample 2 time), both data packets are discarded and the decoder function outputs remain in their previous state.

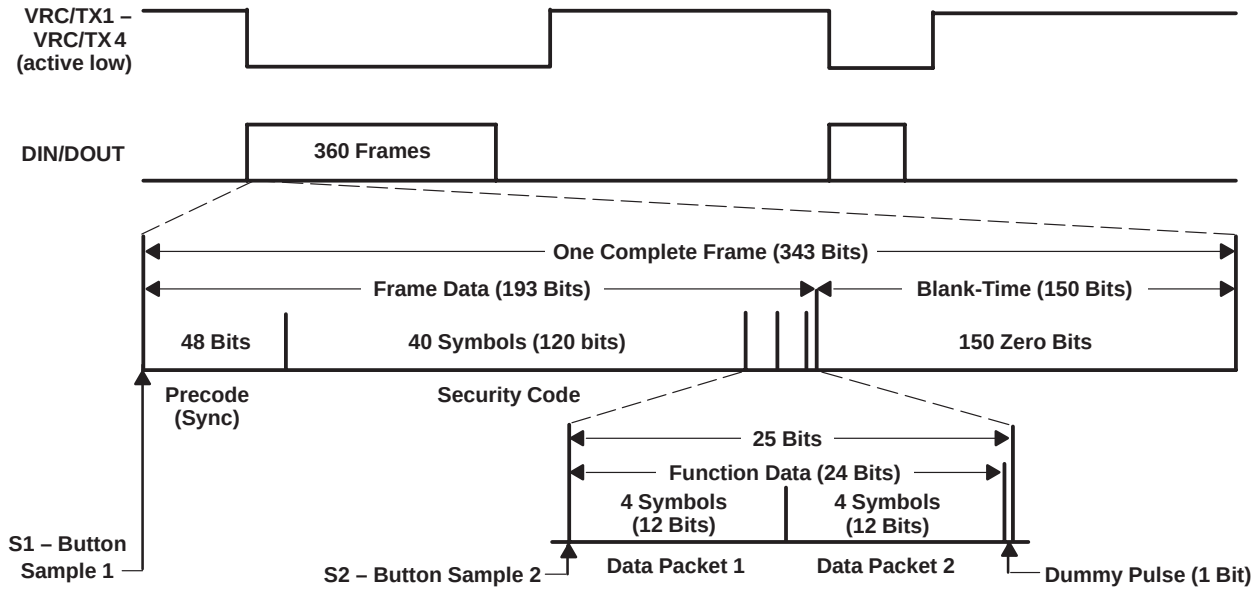


Figure 5. Transmitted Data Format

If the user is holding buttons B1 and B2 on the transmitter down, both the first button sample (S1) and the second button sample (S2) should find both buttons down as the next frame is prepared and sent. So, the *next* frame that is transmitted should contain the same function data in both the first and the second function data packets, and the decoder activates function outputs 1 and 2. So as an example, if transmitter button B1 activates the door locks, button B2 activates the alarm, and both button B1 *and* button B2 pressed at the same time activates the trunk lock, the MARCSTAR sampling/debouncing function prevents the door locks and alarm from being activated when the user intent is to activate only the trunk lock.

PRINCIPLES OF OPERATION

encoder timing

The rate of the transmitted data is variable from 500 Hz to 5 KHz (adjustable using an external resistor and optional capacitor) so that the time to send the data in one frame (193 bits) varies from 386 ms to 38.6 ms. When one or any combination of VRC/TX1 – VRC/TX4 terminals is pulled low, the device outputs up to 360 frames of data and then stops. This is to prevent indefinite code transmission (and battery depletion) when a transmit button is pressed continuously, and increases the opportunity for the decoder to detect the transmitted code. The decoder activates a function output on the first valid received code. The data portions of the transmitted frames are separated by one *dummy pulse* and 150 data clock cycles. This gives a lower effective frame duty cycle, so that the average power output of an interfaced RF oscillator is reduced, and higher peak power can be used for increased range.

The range of frame duty cycle is dependent on the security and function codes, and can vary as calculated:

- Frame duty cycle = total frame high time / total frame time.
- Total frame time = 48 + 120 + 24 + 1 + 150 = 343 data clock cycles.
- The precode (48 bits) always has a duty cycle of 50%.
- The security code (120 bits) duty cycle can vary from 66% (all ones) to 33% (all zeros).
- The function data (24 bits) duty cycle can vary from 58% (one function enabled) to 33% (all functions enabled).
- The dummy pulse (1 bit) always has a duty cycle of 100%.
- The blank time between frames (150 bits) always has a duty cycle of 0%.
- Highest possible duty cycle (48(0.5) + 120(0.66) + 24(0.58) + 1(1) + 150(0)) / 343 = 34%.
- Lowest possible duty cycle (48(0.5) + 120(0.33) + 24(0.33) +1(1) + 150(0)) / 343 = 21%.

Transmitted code format duty cycle is an important consideration when modulating an RF carrier because regulations in many countries concerning maximum RF power output are specified as *average* power. In that respect, higher peak RF power levels can be used, giving increased range, with lower duty-cycle code formats, such as that found in MARCSTAR systems. In the case of the U.S. FCC (Federal Communications Commission) regulations, the average radiated field strength is measured, and the 100 ms sliding window of the highest powered portion of the code frame from the RF transmitter, or the first repeating frame of data, whichever is shorter, is sampled for average power.

The MARCSTAR I E/D device, configured as an encoder, has a 360 frame transmission timeout. When any combination of VRC/TX1 – VRC/TX4 terminals are continuously held low, with a 500-Hz data clock rate, the total transmission time before timeout is $360 \times (2 \times 10^{-3}$ seconds $\times 343) = 4.1$ minutes. Likewise, for a 5-KHz data clock rate, the total transmission time before timeout is $360 \times (2 \times 10^{-4}$ seconds $\times 343) = 25$ seconds. At a 1-KHz clock rate, the total transmission time before timeout is $360 \times (1 \times 10^{-3}$ seconds $\times 343) = 123$ seconds.

PRINCIPLES OF OPERATION

transmitted code bit sequence, symbol format, and function code

The effective bit-length of a complete MARCSTAR I E/D encoder output code sequence is 193 bits, as shown in Figure 5. The output bits, which include the precode, security code, function data, and dummy pulse, change only on the rising edges of an internal data clock (DCLK). The 150 bit-time blank interval completes the data frame, which then has a 343 bit-time duration.

When a MARCSTAR I E/D encoder function input is activated, the stored 40 bits of security code are first translated into 40 symbols, with each symbol consisting of three bits, before being output by the device. A security code zero bit is translated into symbol 0, which is represented by the bit sequence 100. A security code one bit is translated into symbol 1, which is represented by the bit sequence 110. The function data is also translated into symbols of this format before being output.

The result of using these particular bit sequences to represent a 1 or 0 symbol is an increase in decoder function robustness. It also simplifies and improves the accuracy of the comparator adaptive threshold circuitry (see Amplifier/Comparator section).

Function differentiation is provided by four function bits that are translated into symbols by the encoder and sent twice in each data frame to identify the functions that are to be activated at the decoder. Function data is transmitted twice per frame to reduce the probability that accurate security code data and corrupt function data could cause unwanted activation of a function.

After the 40 symbols are decoded into 40 security code bits and found to match a 40-bit security code stored in the decoder EEPROM memory, the next four symbols are decoded into the first set of four function code bits, and the final four symbols are decoded into the second set of four function code bits. The two sets of 4-bit function code are then compared, and if found to match, the function code is used to enable the appropriate function output as shown in Table 1.

Table 1. Function Code

FUNCTION	BIT 1	BIT 2	BIT 3	BIT 4
1	0	1	1	1
2	1	0	1	1
3	1	1	0	1
4	1	1	1	0

More than one encoder function input can be activated at the same time. An external 4-bit binary decoder can be used to control up to 15 devices, one at a time, based on the four MARCSTAR I E/D decoder function outputs.

PRINCIPLES OF OPERATION

decoder mode

The MARCSTAR I E/D decoder mode operational flow is shown in Figure 6.

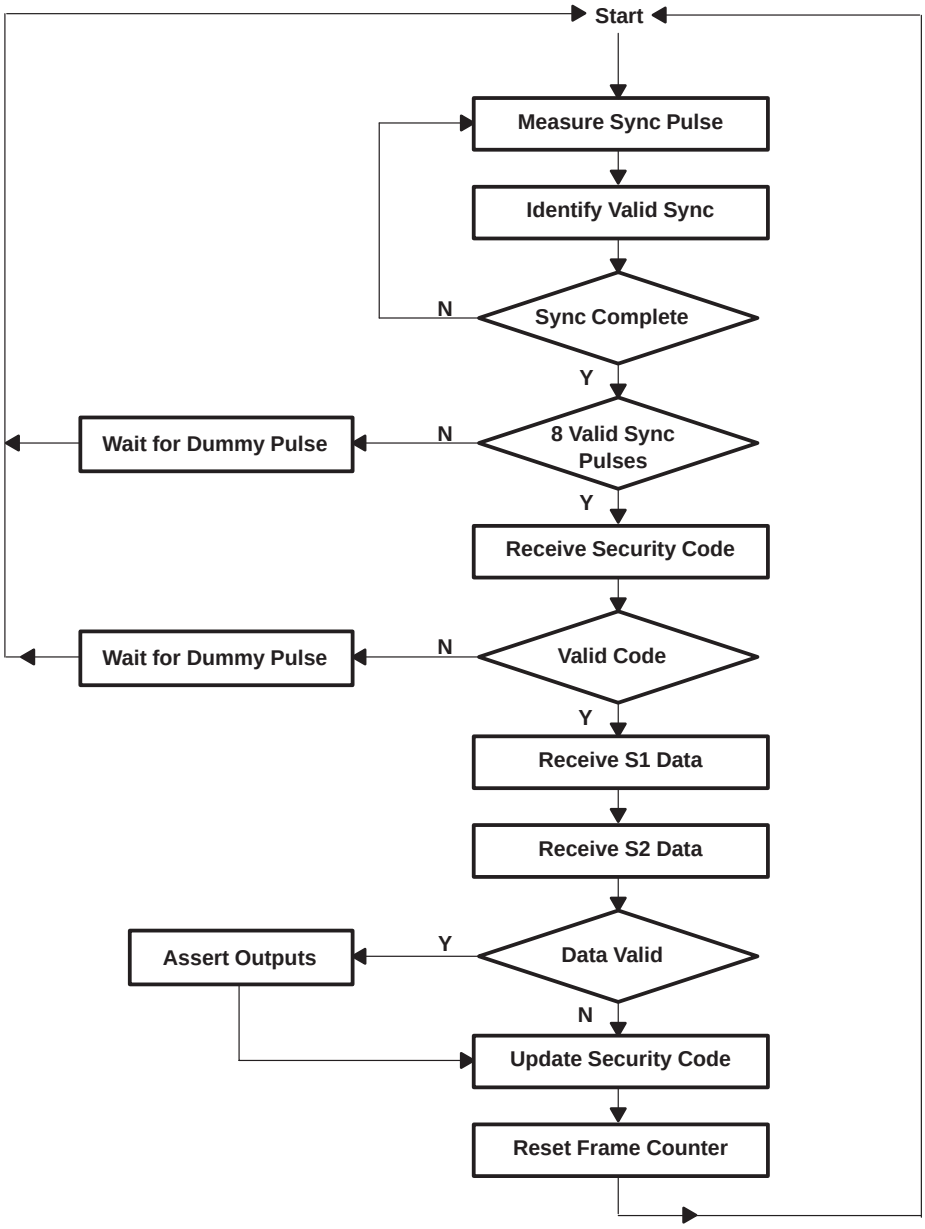


Figure 6. Decoder Mode Operational Flow

PRINCIPLES OF OPERATION

decoder mode (continued)

The TRC1300 and TRC1315 MARCSTAR I E/D devices are configured as a decoder by holding the CONF terminal low *before* the device is powered up (the device reads the CONF terminal during POR, power-on reset).

In the decoder mode, the device receives serial data from input terminal DIN/DOUT. The input data signal is first passed through the internal amplifier/comparator for signal conditioning before being decoded and compared with the four 40-bit security codes stored in EEPROM memory. When a match is found with *one or more* received data frames, the appropriate function output terminals, VRC/TX1 – VRC/TX4, are enabled (active-low). The decoder activates a function output only when two identical function data packets are received in the same frame. The function output remains active for a minimum period of 768 data clock cycles, which can range from 154 ms to 1.54 seconds, depending on the clock frequency used. With a 1-KHz data clock rate, for example, a function output is asserted for a minimum of 768 ms. The decoder keeps the appropriate function output terminals (VRC/TX1 – VRC/TX4) active as long as it receives valid code, and through the blank time between each frame, which is 150 clock cycles. The function outputs go inactive when invalid function data code is received.

Configured as a decoder, the MARCSTAR I E/D samples the incoming serial data at 10 times the expected transmitted data rate. As each symbol is sampled, an integrator determines if it represents a 1 or 0 by the total number of high and low samples. A high symbol (110) has a high level for approximately two-thirds of the symbol period, while a low symbol (100) is high for only one-third of the symbol period. Therefore, if five or more out of eight of the samples are high, the symbol is decoded as a 1, and if three or fewer of the samples are high, the symbol is decoded as a 0. The symbol format also improves synchronization of the decoder with the incoming serial data. A transition from low to high always signifies the beginning of a symbol.

The method of synchronization employed by MARCSTAR I E/D uses a precode sync pattern that precedes the security and function data portions of each frame sent by the encoder. The precode consists of 24 pulses with a 50% duty cycle, each being high or low for one period of the data clock. This equates to a total of 48 bit times.

amplifier/comparator

A representation of the amplifier/comparator section of the MARCSTAR I E/D devices is shown in Figure 7. This circuit is used to amplify and wave-shape low-level input signals to logic levels for input to the shift registers. The internal R1 and C1 components combination form a reference-setting (autobias) network, and the time constant of this network is about three symbols, or 12 bits of code. The internal components R2 and C2 form a low-pass network with a time constant equal to approximately one-tenth of one DCLK period so that high-frequency transients are attenuated before reaching the comparator.

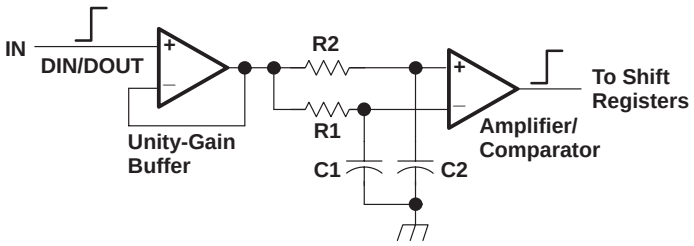


Figure 7. Amplifier/Comparator Equivalent Schematic

PRINCIPLES OF OPERATION

amplifier/comparator (continued)

The amplifier/comparator is implemented with advanced switched-capacitor technology. This is done for two primary reasons. First, since the TRC1300 and TRC1315 devices are variable frequency, the values of R1, C1, R2, and C2 must change depending on the received data rate. Since they are a switched-capacitor design, the filter characteristics scale depending on the oscillator in the decoder device, which must match the encoder oscillator frequency. With this scheme, the amplifier/comparator section functions at all received code data rates. The second reason for using switched-capacitor filters is the increased accuracy and precise filter response that they provide.

programming mode

The MARCSTAR I E/D devices have been designed so that no programming station is required to load the security codes into the EEPROM memory. When the device is configured as an encoder, it generates a 40-bit security code and stores it in EEPROM memory. When configured as a decoder, the device learns the security code from up to four different encoders.

EEPROM stored-code format

The EEPROM memory contains four banks that are used for 40 bits of security code for each of the four channels and an additional 32 bits (eight bits per channel) for error detection. The total EEPROM memory is 192 bits. When configured as a decoder, these EEPROM banks store up to four learned 40-bit security codes; when configured as an encoder, only the first bank of 40 bits is used for the security code.

programming — encoder

When a MARCSTAR I E/D device is configured as an encoder and placed in the programming mode, it generates a 40-bit security code and stores it in the first 40-bit EEPROM memory bank. The remaining three 40-bit memory banks are unused. An LED connected to the LED terminal is required to verify a proper write sequence to EEPROM. The LED anode should be connected to the positive supply and the cathode should be connected to the LED terminal of the MARCSTAR I E/D through a current-limiting resistor.

The procedure for programming a MARCSTAR I E/D device configured as an encoder is described in the following steps:

1. Connect the proper RC combination to the OSCR and OSCC terminals to set the frequency of the internal oscillator.
2. Connect GND and then apply V_{CC}.
3. Apply a logic high to PROG (the PROG terminal is internally pulled down and debounced). The device assumes the program mode. The LED lights, the device generates a new 40-bit security code internally, it loads the first memory bank with that code, and then extinguishes the LED.
4. The MARCSTAR I E/D encoder is now programmed with a new 40-bit security code. Each time step 3 is repeated, a new 40-bit security code is generated and then loaded into the first EEPROM memory location, overwriting the previous security code.

PRINCIPLES OF OPERATION

programming — smart decoder (learn mode)

The MARCSTAR I E/D configured as a smart decoder has the capability of learning up to four 40-bit security codes from four separate encoders. If the decoder attempts to learn a fifth encoder security code, the decoder logic overwrites the first stored security code with the fifth encoder security code. This FIFO (first in, first out) operation always causes the *oldest* code to be overwritten. When an encoder is lost and a new encoder is learned by the decoder, all four of the encoders now being used with the decoder should be relearned to ensure that the decoder contains all the current encoder security codes and no longer stores the security code from the lost encoder. When there are fewer than four encoders being used with a particular decoder, any of them can be learned more than once (for a total of four) to fill the remaining decoder security code storage locations and ensure that the code for the lost encoder has been overwritten.

Each 40-bit security code is loaded into a EEPROM in a single write sequence. An LED connected to the LED terminal is required to verify a proper write sequence to EEPROM memory. The LED anode should be connected to positive supply and the cathode to the LED terminal of the MARCSTAR I E/D through a current-limiting resistor (the LED terminal is active low).

The procedure to write each 40-bit security code into the decoder EEPROM is as follows:

1. Connect the proper RC combination to the OSCR and OSCC terminals to set the frequency of the internal oscillator.
2. Connect the CONF terminal to GND. CONF, which is internally pulled up, must be tied to GND *before* the device is powered up so that when the internal microcontroller reads the CONF terminal during POR (power on reset), CONF will already be at GND.
3. Connect the device to system GND and then V_{CC}.
4. Apply a logic high to PROG (the PROG terminal is internally pulled down and debounced). The device assumes the program mode and the LED lights. The PROG terminal must be held at logic high for the duration of the programming sequence.
5. Apply the MARCSTAR I E/D encoder security code data to be programmed to DIN/DOUT. The first received frame of data is decoded into a 40-bit security code sequence and loaded into the first memory bank of the EEPROM. The LED turns off after the device has decoded and stored the received data. The logic high should now be removed from the PROG terminal. The LED stays on if an attempt is made to exit the programming mode without learning a code.
6. To learn up to four encoder security codes, repeat steps 4 and 5. Each time the device is programmed, the next available memory bank is used, up to four banks.

NOTE: In order to prevent unauthorized programming of the decoder, it is suggested that access to the learn mode be limited to the manufacturer or dealer. In cases where end-user programming is required, a key-switch can limit programming to authorized individuals only.

PRINCIPLES OF OPERATION

oscillator

An internal variable-rate clock runs at the SCLK (sample clock) frequency, and is adjustable from 5 kHz to 50 kHz. DCLK (data clock) is derived from SCLK so that both clocks are synchronous. DCLK runs at one-tenth the speed of SCLK and clocks the transmitted data at a rate variable from 500 bps to 5 kbps. SCLK is used to sample the received data at 10 times the received data rate. The high sampling rate in the decoder combined with the symbol code format and the internal signal-conditioning amplifier circuitry provides accurate correlation of the received signal. The SCLK frequency is set by an external RC at terminals OSCR and OSCC.

The encoder and decoder should be set to the same clock rates; however, the device allows a wide frequency tolerance to increase the robustness of the communications link. The encoder can vary from one-half to two times the decoder clock speed and synchronization still results. This allows for internal oscillator tolerance and frequency change due to external component tolerances and temperature changes. For example, if a serial data speed of 1.5 kbps (DCLK) is desired, then both the encoder and the decoder oscillators (SCLK) must be set to be 10 times the data rate frequency, or 15 kHz. Both the encoder and decoder can vary ±33% in frequency, or from 10 kHz to 20 kHz, and the devices still synchronize successfully. For the worst case example, the encoder SCLK would be running at 10 kHz and the decoder SCLK at 20 kHz, or twice the encoder frequency. The absolute maximum and minimum clock frequency of 5 kHz to 50 kHz must never be violated. Because the device introduces up to ±7% frequency variation, the external RC components can have as much as ±26% tolerance, for a total of ±33% frequency variation.

The encoder and decoder internal SCLK clock rate is set by connecting a resistor between the OSCR and OSCC terminals and an optional capacitor between the OSCC terminal and GND on each device. Equation 3 defines the internal sample clock (SCLK) as a function of the external resistor and capacitor.

$$f_{osc} = \frac{1}{1.386 \times \left(R_{ext} + 2 \times 10^{3}\right) \times \left(C_{ext} + 20 \times 10^{-12}\right)} \quad (3)$$

The 2×10^{3} value (2 kΩ) shown in equation 3 is the internal series resistance with OSCR. The 20×10^{-12} value (20 pF) is the internal capacitance value of the OSCC bond pad (a parasitic shunt capacitance to GND). Figure 8 shows typical R_{ext} values vs. SCLK frequency.

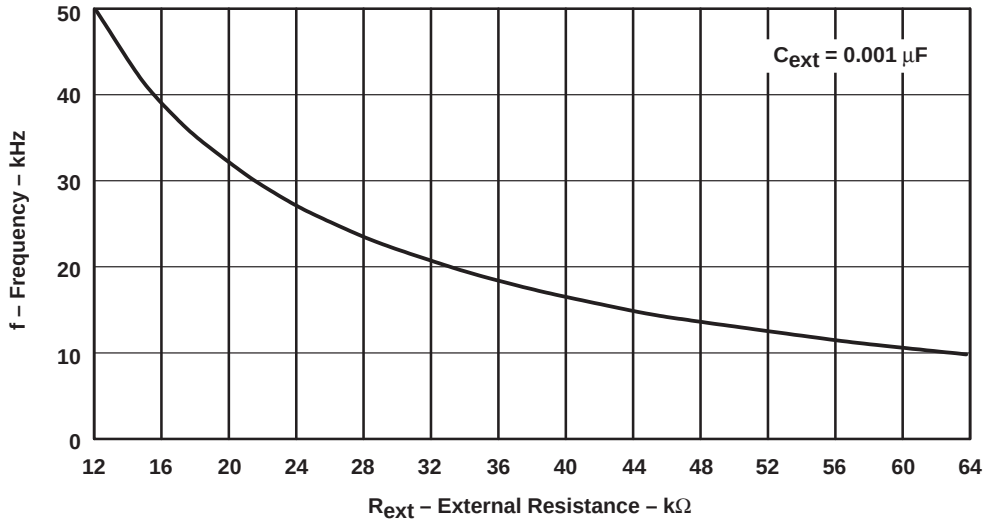


Figure 8. External Resistance vs. Sample Clock Frequency (SCLK)

PRINCIPLES OF OPERATION

test mode

TRC1300 and TRC1315 MARCSTAR I E/D devices are equipped with a self-test function that checks the RAM, ROM, and EEPROM memory areas:

- The RAM is tested by writing checkerboard bit patterns into the RAM and then reading them back. The test is passed if the correct data is read from the RAM.
- The ROM is tested by calculating a new checksum for each location containing data and then comparing it to a predetermined value. The test is passed if the two values match.
- The EEPROM is tested by calculating a new checksum for each of the four 40-bit locations and comparing them with checksum values stored in EEPROM. The test is passed if the two values match.

When TEST is momentarily held at V_{CC}, the device enters the self-test mode. While in this mode, the device runs through the tests and then indicates results with a flashing LED. The result codes are shown in Table 2.

Table 2. LED Flashing Self-Test Error Codes

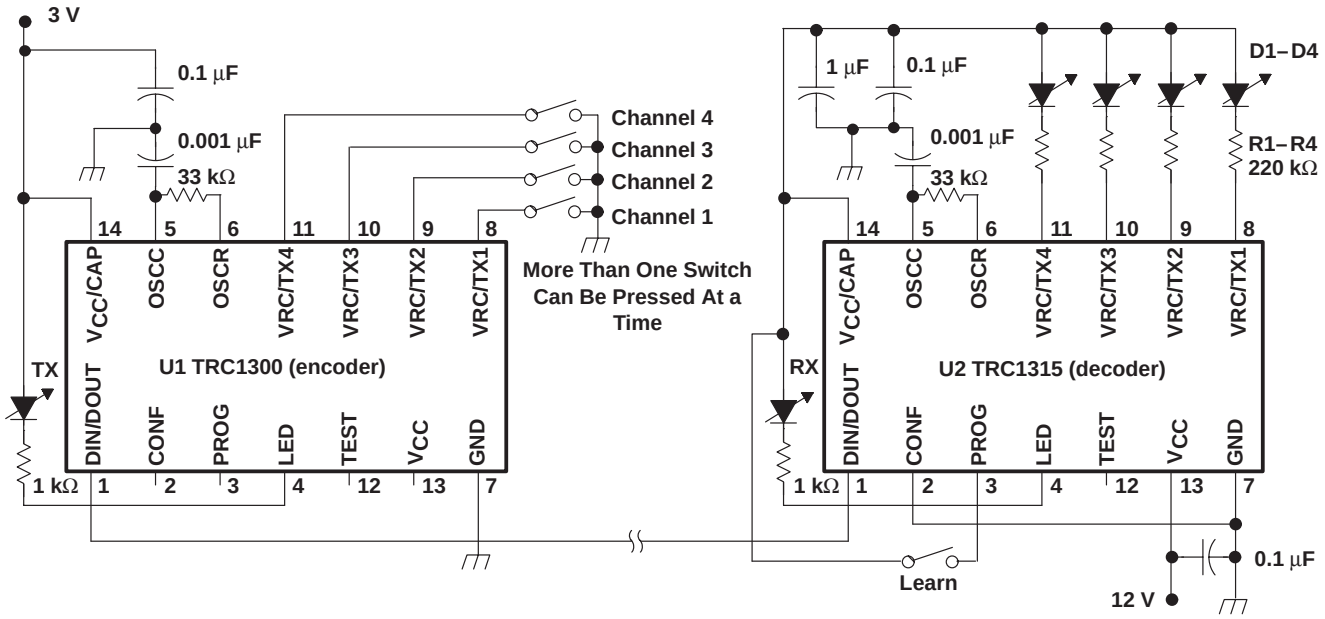
LED FLASHES	CONDITION
0	No tests passed
1	Passed EEPROM test only
2	Passed ROM test only
3	Passed ROM and EEPROM tests
4	Passed RAM test only
5	Passed RAM and EEPROM tests
6	Passed RAM and ROM tests
7	Passed all tests

The switch that initiates the test mode should be momentary — the device continues to run through the tests as long as TEST is held at V_{CC}.

APPLICATION INFORMATION

4-channel, direct-wired

Figure 9 shows an example of MARCSTAR I E/D devices in a single-wire direct connection. This configuration is typically used in cable-box decoders, remote lighting, and wired home-security-system applications. U1 is a TRC1300 configured as an encoder by not connecting the CONF terminal (which is internally pulled up, so no connection is required). U2, a TRC1315, is configured as a decoder by tying CONF low (CONF must be low before V_{CC} is applied). PROG is held low by an internal pulldown to disable the program mode. Closing the Learn switch places U2 in the program mode so that the security code from an encoder can be learned. Both the encoder and decoder are set to a 2-kHz data clock (DCLK) frequency (20 kHz sample clock, SCLK) using an external RC at OSCC and OSCR. An LED is connected through a resistor to the LED terminal of the encoder and indicates transmission of code. When momentary switches S1– S4 are pressed, the corresponding outputs on the U2 decoder go low and LEDs D1–D4 light.



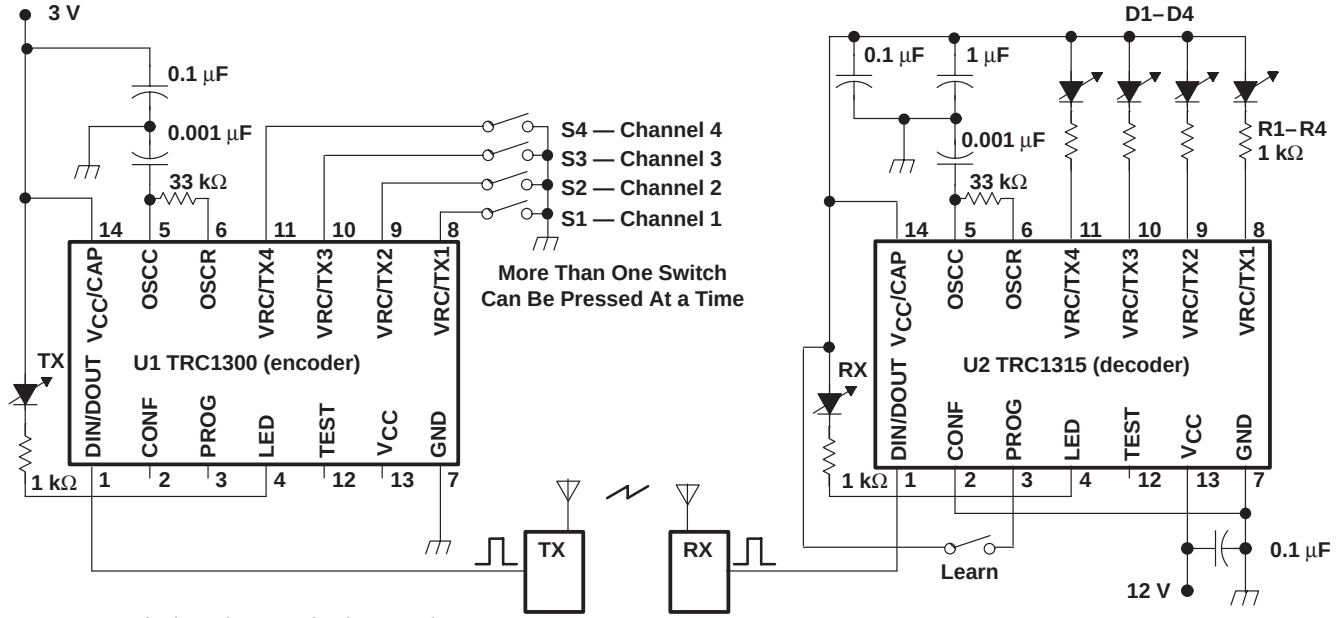
NOTE A: Terminal numbers are for the D package.

Figure 9. A 4-Channel, Single-Wire Connection

APPLICATION INFORMATION

4-channel, infrared or RF connection

Figure 10 shows an example of MARCSTAR I E/D devices in an infrared or RF connection, typically used in automobile RKE or security systems. U1 is a TRC1300 configured as an encoder by not connecting the CONF terminal (which is internally pulled up, so no connection is required). U2, a TRC1315, is configured as a decoder by tying CONF low (CONF must be low before V_{CC} is applied). PROG is held low by an internal pulldown to disable the program mode. Closing the Learn switch places U2 in the program mode so that the security code from an encoder can be learned. Both the encoder and decoder are set to a 2-kHz data clock (DCLK) frequency (20 kHz sample clock, SCLK) using an external RC at OSCC and OSCR. An LED is connected through a resistor to the LED terminal of the encoder and indicates transmission of code. Momentary switches S1–S4 are internally debounced and pulled up at device inputs VRC/TX1–VRC/TX4. When S1–S4 is pressed, the corresponding outputs on the U2 decoder go low and LEDs D1–D4 light.



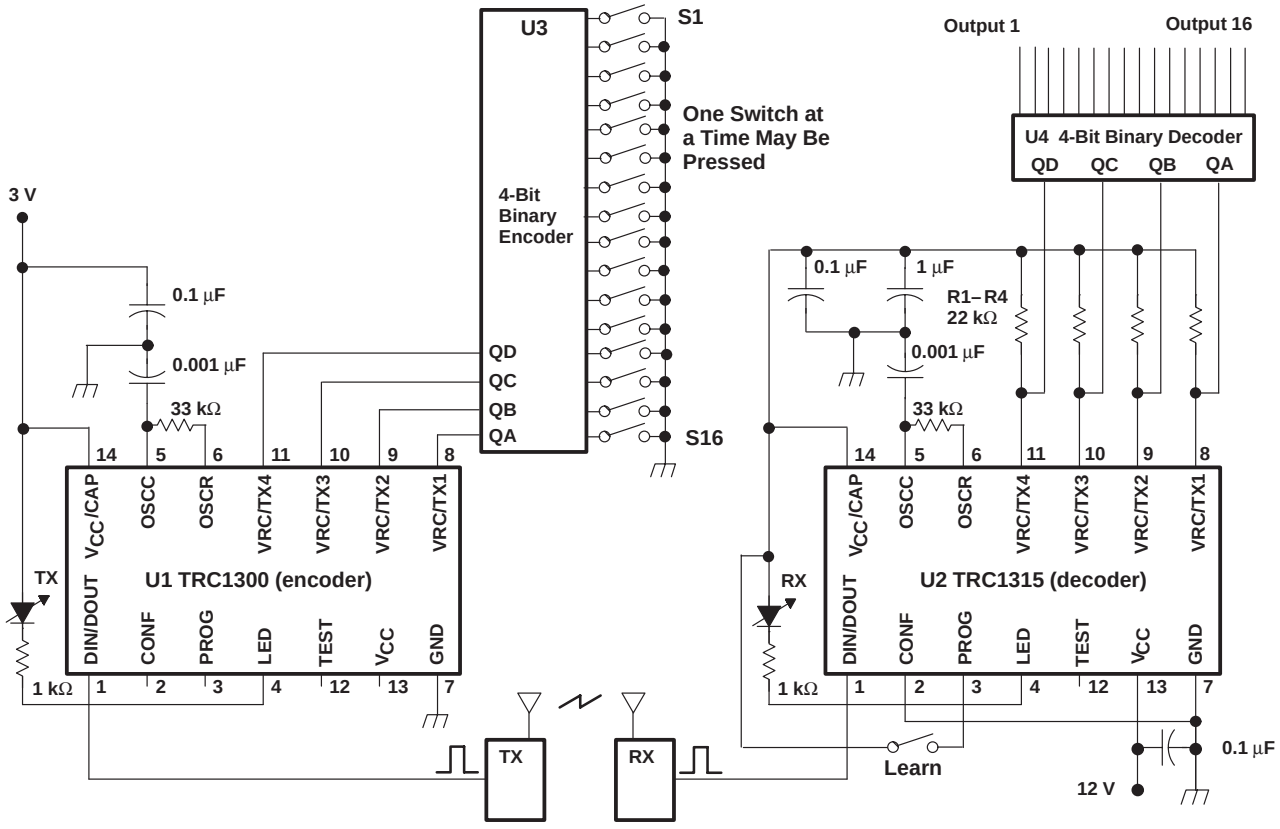
NOTE A: Terminal numbers are for the D package.

Figure 10. A 4-Channel, RF/Infrared Connection

APPLICATION INFORMATION

16-channel, infrared or RF connection

Figure 11 shows an example of MARCSTAR I E/D devices in a 16-channel infrared or RF connection, typically used in consumer electronics (TV, VCR, etc.) or remote-control toy applications. U1 is a TRC1300 configured as an encoder by not connecting the CONF terminal (which is internally pulled up, so no connection is required). U2, a TRC1315, is configured as a decoder by tying CONF low (CONF must be low before V_{CC} is applied). PROG is held low by an internal pulldown to disable the program mode. Closing the Learn switch places U2 in the program mode so that the security code from an encoder can be learned. Both the encoder and decoder are set to a 2-kHz data clock (DCLK) frequency (20 kHz sample clock, SCLK) using an external RC at OSCC and OSCR. An LED is connected to the LED terminal of the encoder and indicates transmission of code. The outputs of a 4-bit binary encoder are connected to inputs VRC/TX1–VRC/TX4 of the MARCSTAR I E/D encoder. When one of the 16 momentary switches (S1–S16) is pressed, the binary equivalent is encoded by U3 and applied to the MARCSTAR I E/D encoder (U1) inputs. The binary equivalent is transmitted to the MARCSTAR I E/D decoder (U2) where the corresponding outputs go low. The inputs of a 4-bit binary decoder are connected to the VRC/TX1–VRC/TX4 outputs of the MARCSTAR I E/D decoder. When these terminals output the received binary function data, they are then decoded by U4, and the appropriate U4 output is activated. The outputs can be used to control one of 15 devices at a time, or for a 15 position semiproportional control.



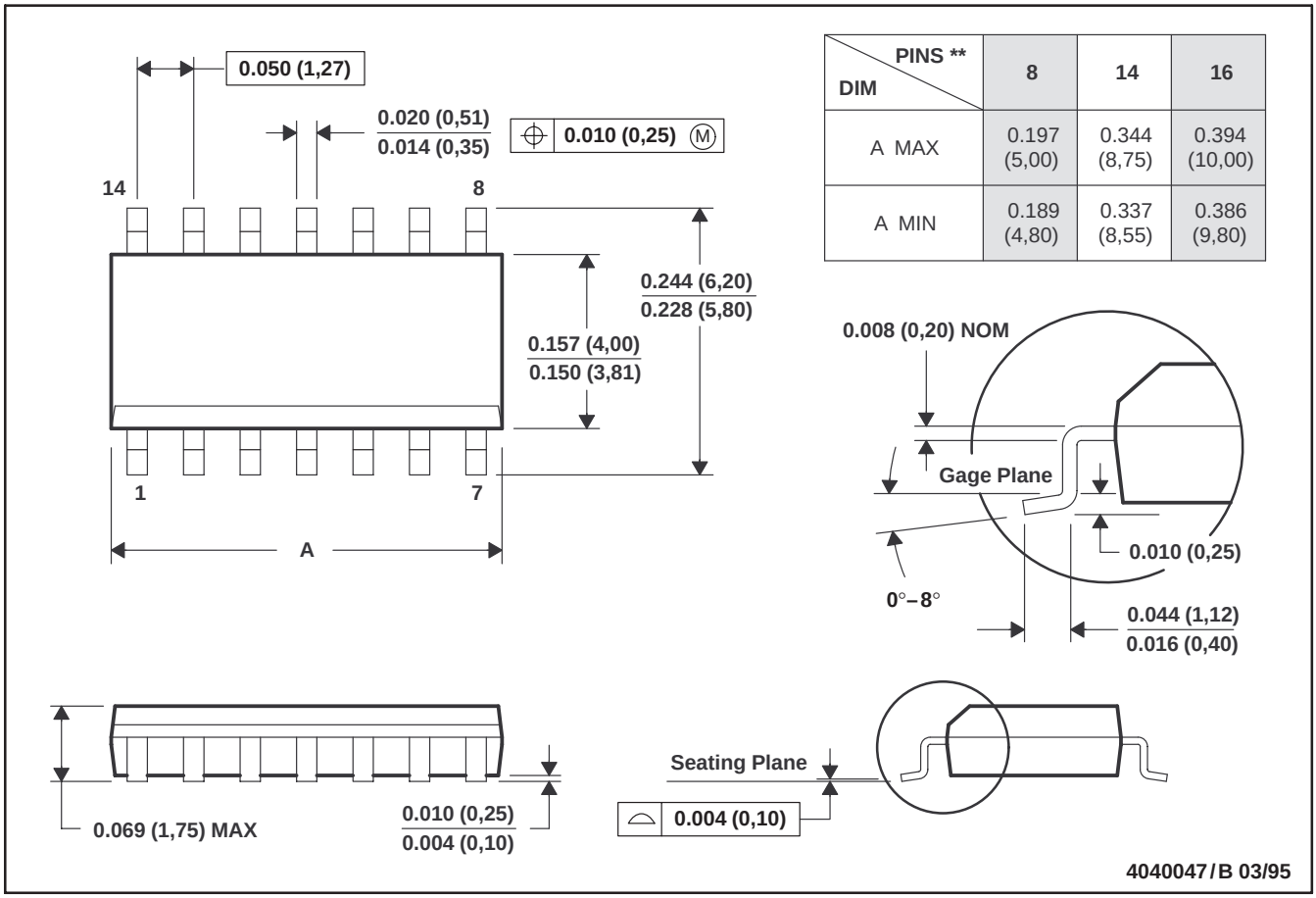
NOTE A: Terminal numbers are for the D package.

Figure 11. A 16-Channel, RF or Infrared Connection

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

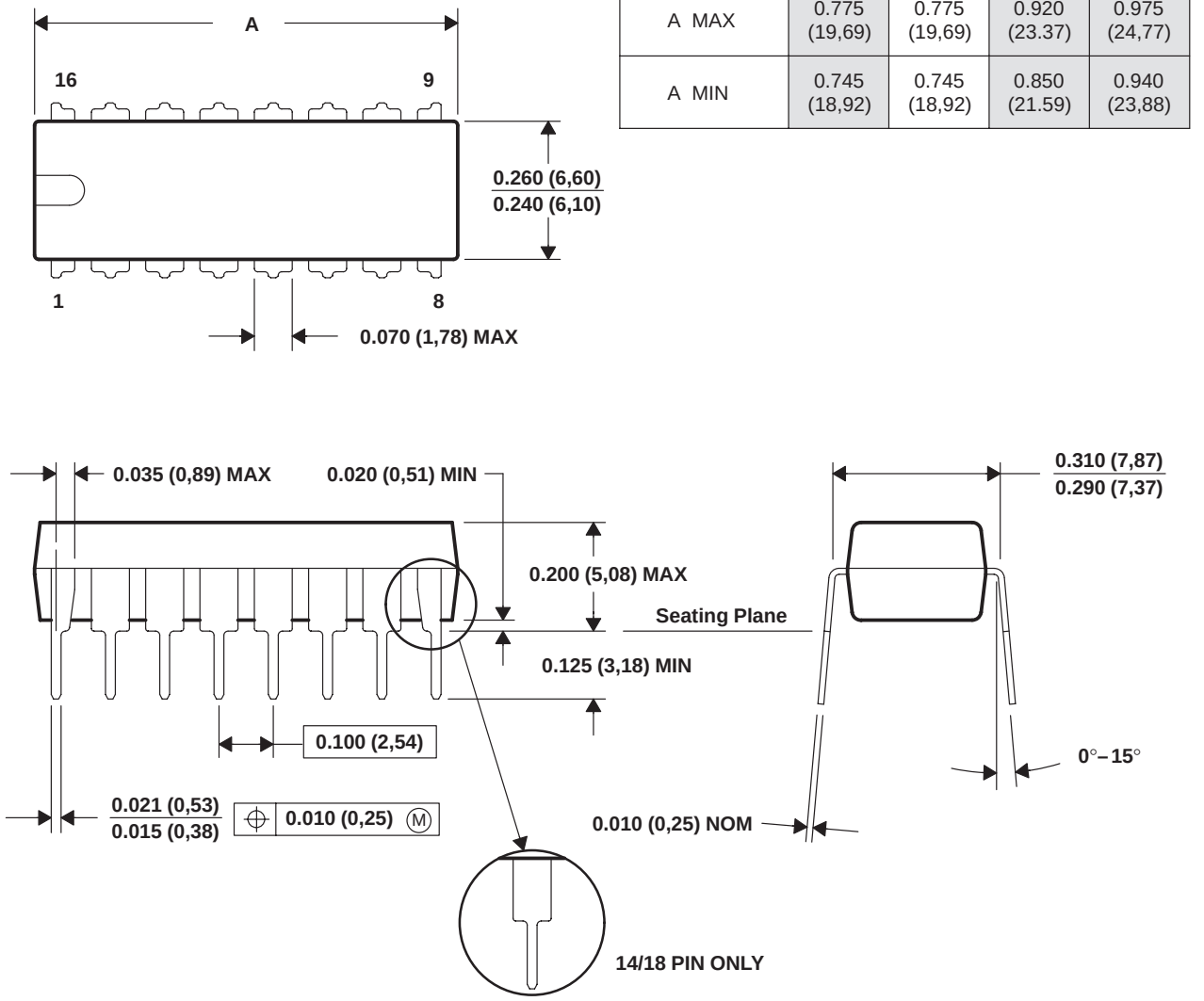
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

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