DATA SHEET

GPC71PXXXA

4-bit Speech with SPU

Dec. 20, 2016

Version 1.2

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4-BIT SPEECH WITH SPU

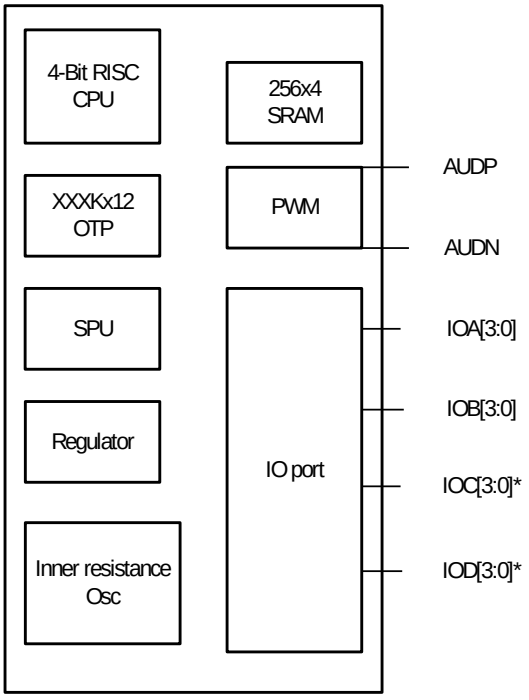
1 GPC71PXXXA SERIES

Product No.	GPC71P340A	GPC71P170A	GPC71P080A	GPC71P064A	GPC71P048A	GPC71P032A	GPC71P016A
OTP density (KWord)	680	340	160	128	96	64	32
Dedicated IOs	16	16	16	16	16	8	8

2 GENERAL DESCRIPTION

GPC71PXXXA, a 4-bit sound controller, is architected with a one-channel SPU for MIDI playback, a 4-bit RISC CPU, a 14-bit PWM, 8/16 IOs, 256-nibble RAM, and OTP with density of 680K/ 340K/ 160K/ 128K/ 96K/ 64K/ 32K x 12-bit of memory space. The operating voltage ranges from 2.0V through 5.5V and operating speed is 1M/2MHz, configurable through inner oscillator. Other features include Low Voltage Reset, IR carry output, watchdog, five interrupt sources with two time-bases, etc.

3 BLOCK DIAGRAM



* Not available in GPC71P032A/GPC71P016A

4 FEATURES

- 4-bit RISC CPU
- CPU Clock: 1M/2M Hz, System clock: 8MHz
- Operating Voltage: 2.0V - 5.5V
- Regulator built-in with input voltage: 2.0~5.5V, output voltage: 2.0~3.0V
- IO IOA~IOD Operating Voltage: 2.0V - 5.5V
- 256 nibbles SRAM
- 14-bit PWM driver for driving speaker directly
- 680K/340K/160K/128K/96K/64K/32Kx12-bit OTP
- Standby mode for power savings
- Five interrupt sources with two time-bases
- 1-channel Sound Processing Unit (SPU) supports MIDI playback
- 16 or 8 general I/Os (bit programmable)
- Key wakeup function (IOA~IOD for 16 IO, IOA~IOB for 8 IO)
- Low voltage reset
- Watchdog

5 APPLICATION FIELD

- Talking instrument controller
- General Music Synthesizer
- Toy controller
- Intelligent toy controller
- And more

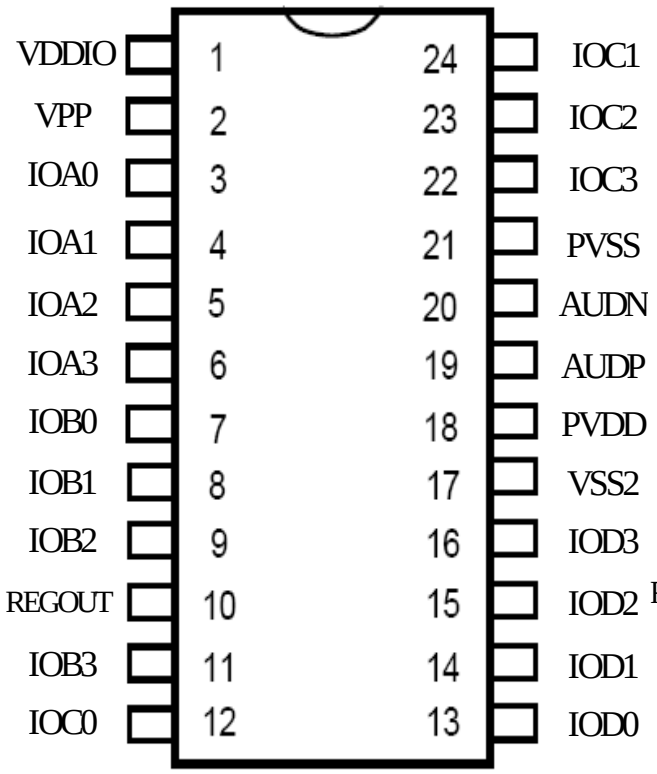
6 SIGNAL DESCRIPTIONS

PIN Name	Type	Description
IOA[3：0]	I/O	IOA[3：0] is a bi-directional I/O port which wakeup capability (via body option). 1Mohm || 200K feedback Pull Low resistor IOA3 shares pad with OTP writer's signal SDA IOA2 shares pad with External Interrupt Input (via body option), or with OTP writer's signal SCK. IOA1 shares pad with IR Output, (Body Option) IOA0 shares pad with Key Reset Input, (Body Option)
IOB[3：0]	I/O	IOB[3：0] is a bi-directional I/O port with wakeup capability (via body option). 1Mohm || 200K feedback Pull Low resistor IOB2 shares pad with External Interrupt Input (via body option). IOB1 shares pad with IR Output (via body option). IOB0 shares pad with Key Reset Input (via body option)
IOC[3：0]	I/O	GPC71P032A/GPC71P016A do not have these ports. IOC[3：0] is a bi-directional I/O port with wakeup capability (body option). 1Mohm || 200K feedback Pull Low resistor IOC2 shares pad with External Interrupt Input (body option) IOC1 shares pad with IR Output (body option) IOC0 shares pad with Key Reset Input (body option)
IOD[3：0]	I/O	GPC71P032A/GPC71P016A do not have these ports. IOD[3：0] is a bi-directional I/O port with wakeup capability (body option). 1Mohm || 200K feedback Pull Low resistor IOD2 shares pad with External Interrupt Input (via body option) IOD1 shares pad with IR Output (via body option) IOD0 shares pad with Key Reset Input (via body option)
TEST	I	GPC71P032A and GPC71P016A do not have this port. Non-used pin for user; it's default in pull low and can be optioned as floating state.
AUDP AUDN	O	PWM audio output
VDDIO	P	Power supply voltage input
VSS1,VSS2	G	Ground reference(only 1 VSS pad in GPC71P032A/GPC71P016A)
VPP	P	OTP program power input
REGOUT	P	3.3V regulator output for core power
VDDTRM	P	Power for e-fuse, user should keep this pin in floating state.
VSS_FUSE	G	Ground for e-fuse for testing only, user should keep this pin in floating state. (Pad available only in GPC71P032A/GPC71P016A)
PVDD	P	PWM driver power
PVSS	G	PWM driver ground reference

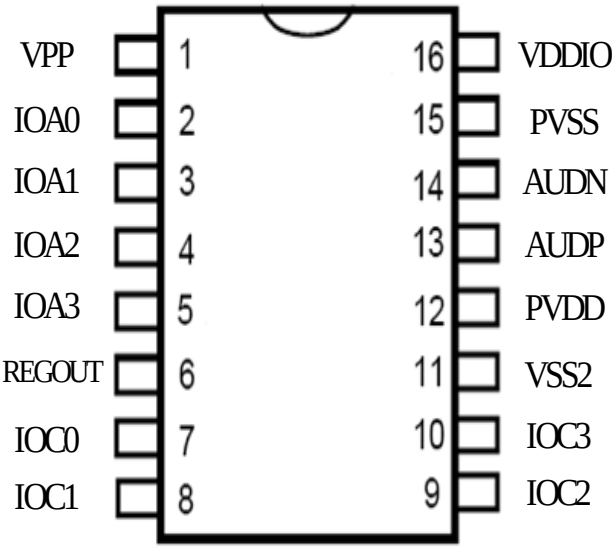
6.1 Package Pad Assignment

6.1.1 Package for GPC71P340A / GPC71P170A /GPC71P080A/GPC71P064A/GPC71P048A

24 PIN SOP（300 mil）



16 PIN SOP（150 mil）

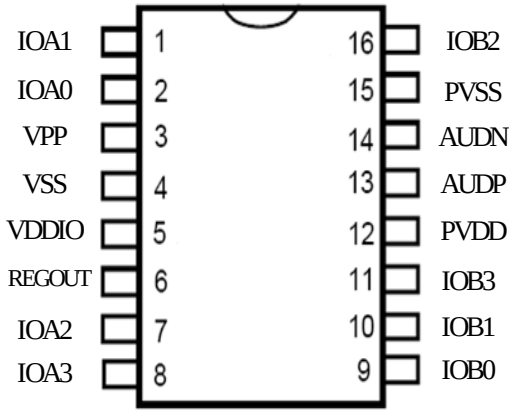


8 PIN SOP（150 mil）

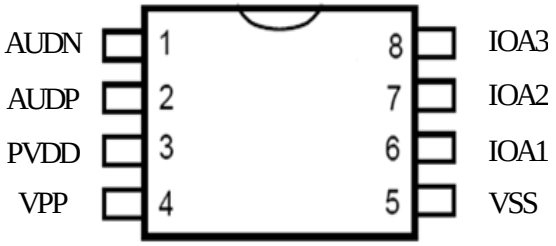


6.1.2 Package for GPC71P032A/GPC71P016A

16 PIN SOP（150 mil）



8 PIN SOP（150 mil）



7 FUNCTION DESCRIPTIONS

7.1 CPU

GPC71PXXXA features a 4-bit RISC CPU, executing the 12-bit instruction set with total of 72 instructions available, 7 stacks managed by a 3-bit stack pointer, three DPRs(Data Pointer to read ROM) sharing stack 4 ~ 6, and two VPRs(Voice Data Pointer) for SPU.

7.2 Memory

7.2.1 SRAM

There are 256 nibbles of SRAM, grouped into 4 banks. Each bank has 64 nibbles and supports index mode to read/write its content addressed by TXR.

7.2.2 OTP

The One Time Programming (OTP) memory is featured in GPC71PXXXA with density of 680K/ 340K/ 160K/ 128K/ 96K/ 64K/ 32K x 12-bit of memory.

7.3 Clock Source

Clock source is an inner resistance oscillator with CPU clock options of 1MHz or 2MHz

7.4 Low Voltage Reset

With the LVR function, a reset signal is generated to reset system when the operating voltage drops below LVR level.

7.5 Interrupt

An interrupt is a special event request to microcontroller. When it occurs, the corresponding interrupt will activate and direct the program code to execute the respective functions. The GPC71PXXXA has 5 interrupt sources. Please refer to programming guide for more details.

7.5.1 Timebase

There are two Timebases, TB1 and TB2, generated by the system clock. The interval of TB1 is allowed up to 1ms and TB2 allows up to 2ms.

7.6 SPU

One channel SPU supports MIDI playback with A3400Pro-like decode or PCM format, and each channel has an 8-bit envelope control.

7.7 PWM

The PWM module consists of a 14-bit PWM driver to drive speaker directly.

7.8 Sleep Mode, Wakeup and Watchdog

7.8.1 Sleep mode and wakeup

Sleep mode or known as power down mode is an operating state that requires an extremely low power consumption to maintain the system in active. The sleep mode is particularly useful for the application areas where the system is required to constantly maintain its basic functionality and where the power capacity is limited. GPC71PXXXA enters sleep mode when SLEEP instruction is executed and can be woken up by interrupt or key state change. CPU will continue to execute the rest of program code from where it entered sleep mode.

7.8.2 Watchdog Reset

A watchdog reset is a reset signal that is generated to reset the entire system when watchdog counter is overflow. In case when the program code has been running into an unknown state and without the watchdog signal being cleared for a certain period of time, watchdog function automatically generates a reset signal pulling the system back from unknown state.

7.9 . I/O

The GPC71PXXXA features 16-bit or 8-bit programmable Input/output pins and many of them feature wakeup capability. These IOs normally support input function with floating or pull-low and output options. In addition to the ordinary I/O function, some IO ports have special functions. The following table summarizes the special functions for these IOs.

Special Function in Port

Port	Special Function	Function Description	Note
IOA0/IOB0~IOD0	Key Reset	Key reset pin, configurable through code option	High active; IOC0/IOD0 isn't supported in GPC71P032A/GPC71P016A
IOA1/IOB1~IOD1	IROUT	IR carry output, configurable through code option	IOC1/IOD1 isn't supported in GPC71P032A/GPC71P016A
IOA2/IOB2~IOD2	EXT INT	External interrupt input, configurable through code option	IOC2/IOD2 isn't supported in GPC71P032A/GPC71P016A

8 ELECTRICAL SPECIFICATIONS

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	(VSS-0.3V) to (V_+ + 0.3V)
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-65℃ to +150℃

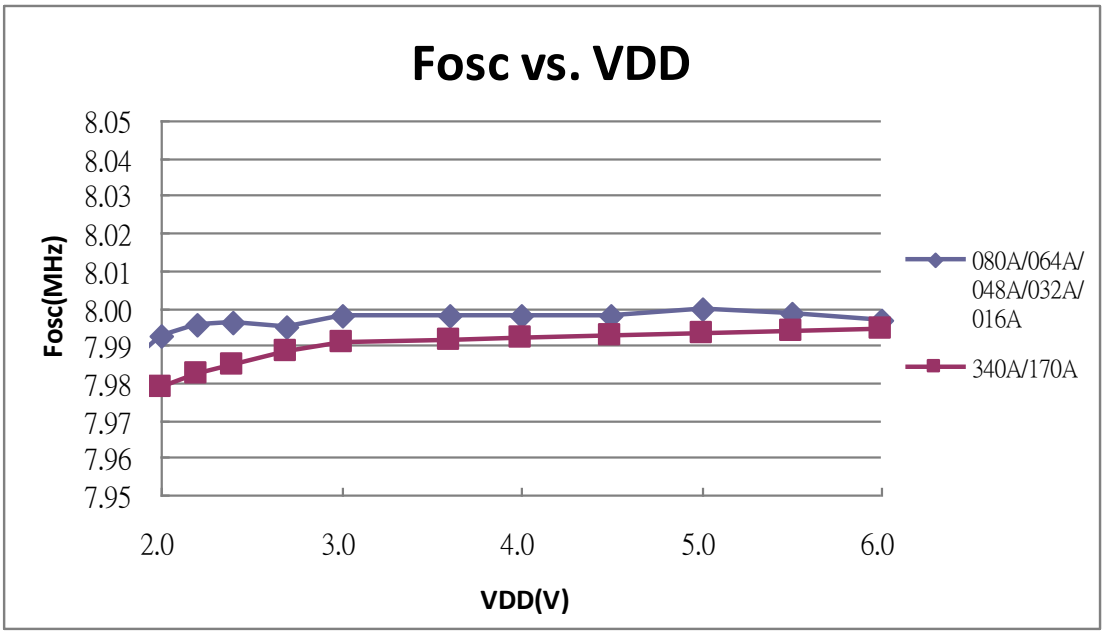
Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, see DC Electrical Characteristics.

8.1 DC Characteristics (VDD = 3/4.5V (IOA ~ IOD), TA = 25℃)

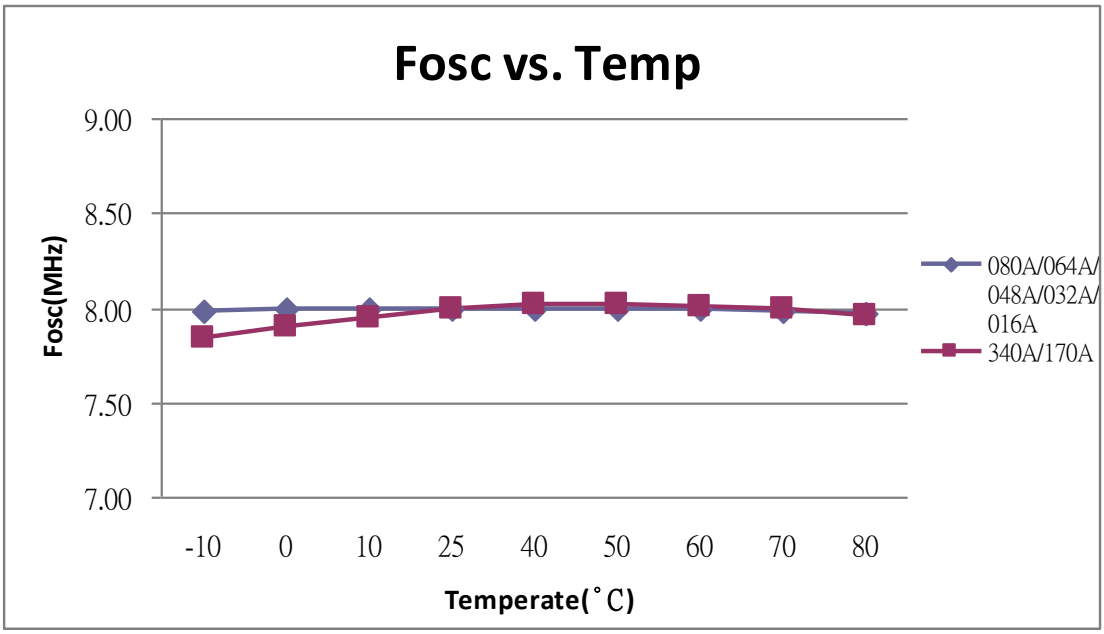
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	5.5	V	
Operating Current	I_{OP}	-	1.5	-	mA	F_{CPU} = 2MHz @ 3.0V, PWM output off **For GPC71P080A/064A/048A/ 032A/016A**
		-	2	-	mA	F_{CPU} = 2MHz @ 4.5V, PWM output off **For GPC71P080A/064A/048A/ 032A/016A**
		-	5	-	mA	F_{CPU} = 2MHz @ 3.0V, PWM output off **For GPC71P340A/170A**
		-	6	-	mA	F_{CPU} = 2MHz @ 4.5V, PWM output off **For GPC71P340A/170A**
Standby Current	I_{STBY}	-	-	5	uA	VDD = 3.0V
		-	-	5	uA	VDD = 4.5V
GPIO Input High Level (IOA, IOB, IOC, IOD)	V_{IH}	0.5VDD	-	-	V	VDD = 4.5V
GPIO Input Low Level (IOA, IOB, IOC, IOD)	V_{IL}	-	-	0.5VDD	V	VDD = 4.5V
Output High Current (IOA, IOB, IOC, IOD)	I_{OH}	-	10	-	mA	VDD = 3.0V, V_{OH} = 0.7*VDD
		-	20	-	mA	VDD = 4.5V, V_{OH} = 0.7*VDD
Output Low Current (Normal)	I_{OL1}	-	10	-	mA	VDD = 3.0V, V_{OL} = 0.3*VDD
		-	20	-	mA	VDD = 4.5V, V_{OL} = 0.3*VDD
Output Low Current (High sink , by Body Option)	I_{OL2}	-	20	-	mA	VDD = 3.0V, V_{OL} = 0.3*VDD
		-	40	-	mA	VDD =4.5V, V_{OL} = 0.3*VDD
Input Pull Low Resistor (IOA, IOB, IOC, IOD)I	R_{L1}	-	200	-	Kohm	VDD = 3.0V, IO = 0V **For GPC71P080A/064A/048A/ 032A/016A**
		-	100	-	Kohm	VDD = 4.5V, IO = 0V **For GPC71P080A/064A/048A/ 032A/016A**
		-	150	-	Kohm	VDD = 3.0V, IO = 0V **For GPC71P340A/170A**
		-	150	-	Kohm	VDD = 4.5V, IO = 0V **For GPC71P340A/170A**

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Pull Low Resistor (IOA, IOB, IOC, IOD)	R_{L2}	-	1000	-	Kohm	VDD = 3.0V, IO = 3.0V **For GPC71P080A/064A/048A/ 032A/016A**
		-	500	-	Kohm	VDD = 4.5V, IO = 4.5V **For GPC71P080A/064A/048A/ 032A/016A**
		-	850	-	Kohm	VDD = 3.0V, IO = 3.0V **For GPC71P340A/170A**
		-	850	-	Kohm	VDD = 4.5V, IO = 4.5V **For GPC71P340A/170A**
PWM Driver Current	I_{PWM}	-	180	-	mA	VDD = 3.0V, 8 Ohms load
		-	280	-	mA	VDD = 4.5V, 8 Ohms load
Frequency deviation by voltage drop	△F/F	-1	-	+1	%	$\frac{Fosc(5.5v) - Fosc(2.4v)}{Fosc(3.0v)}$ F_{CPU} = 2MHz
Frequency lot deviation	△F/F	-1	-	1	%	$\frac{Fmax(3.0v) - Fmin(3.0v)}{Fmax(3.0v)}$ F_{CPU} = 2MHz @ 3.0V (tentative)
		-1	-	1	%	$\frac{Fmax(4.5v) - Fmin(4.5v)}{Fmax(4.5v)}$ F_{CPU} = 2MHz @ 4.5V (tentative)

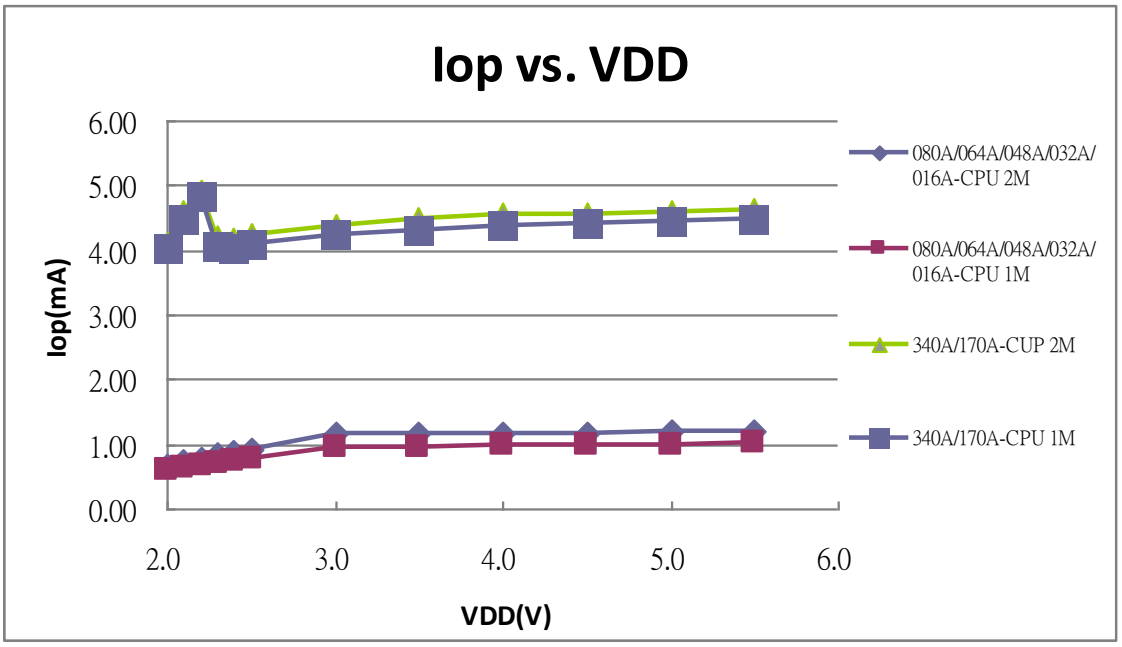
8.2 Internal Frequency (Fosc) and VDD



8.3 Internal Frequency (Fosc) and Temperature

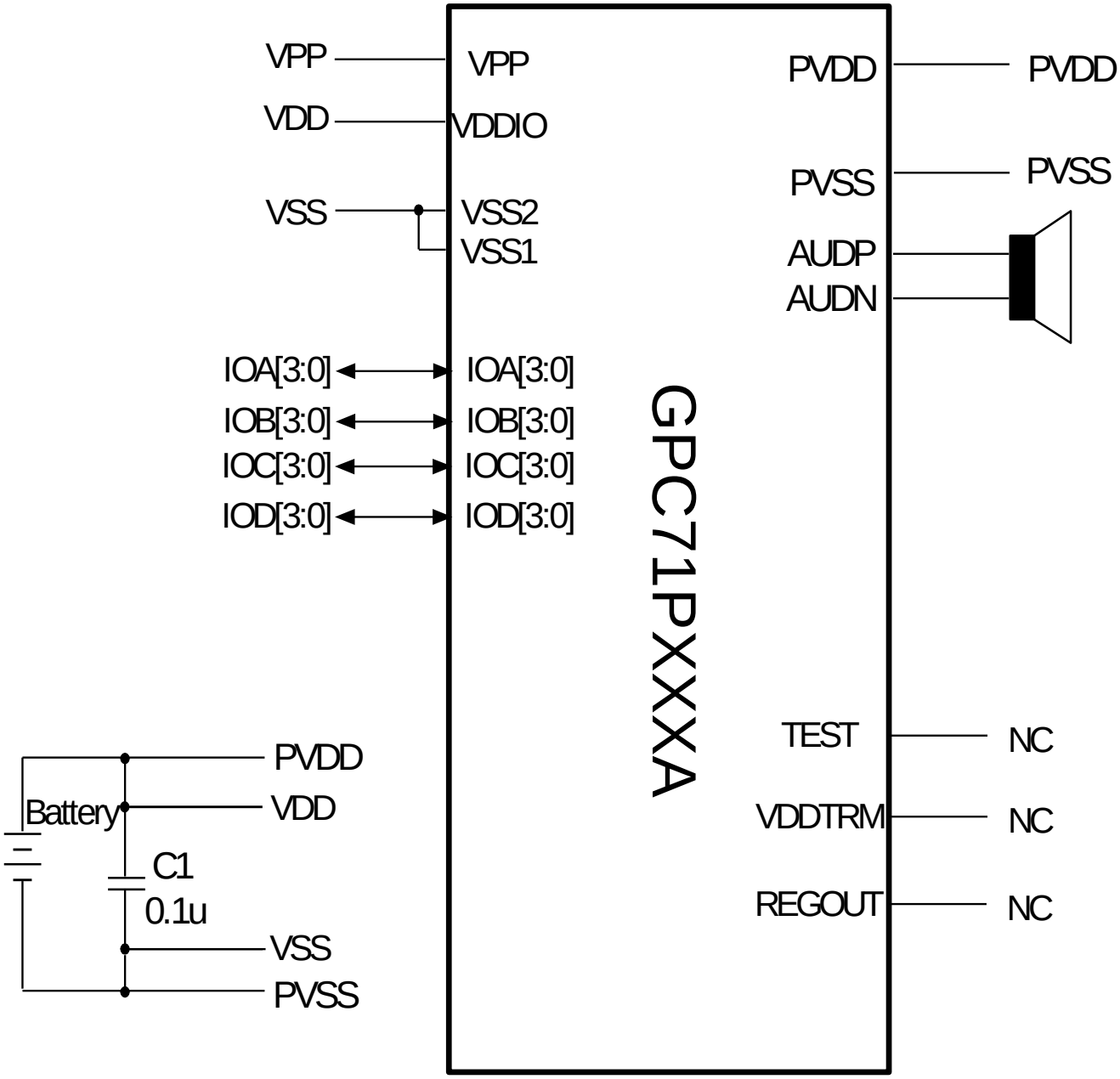


8.4 Operating Current (Iop) and VDD



9 APPLICATION CIRCUITS

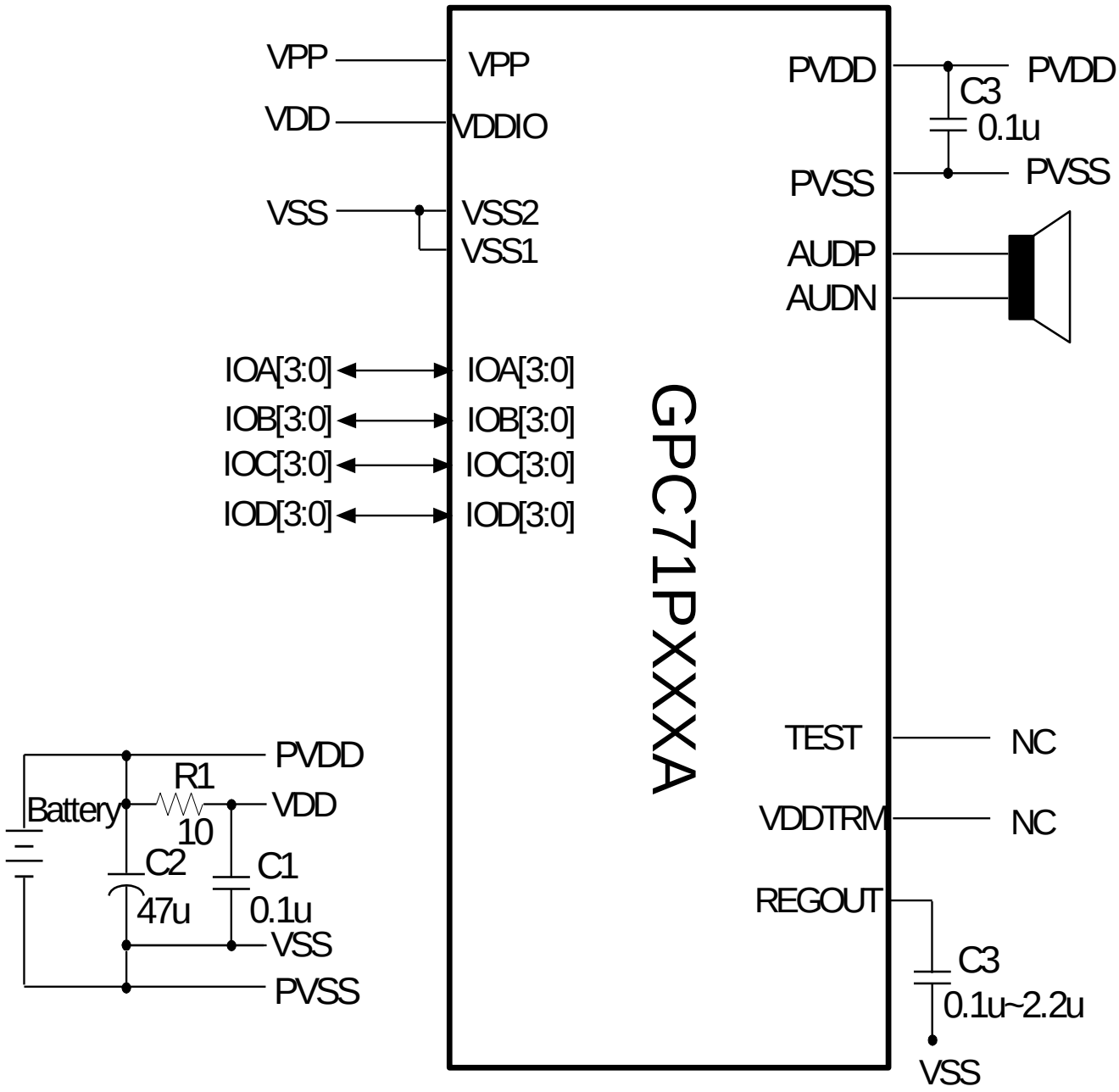
9.1 Light Loading and Circuit without Noise



PCB Layout Guidelines:

1. PVDD may be greater than or equal to VDD.
2. VSS, PVSS must be connected to ground input directly, not the branch of each other.
3. When using two batteries, 0.1uF ~ 4.7uF is suggested for C1, and it should be increased in a high volume application.
4. IOC/IOD isn't supported in GPC71P032A/GPC71P016A.
5. There is no "TEST" pin in GPC71P032A/GPC71P016A.

9.2 Heavy Loading or Circuit with Noise



PCB Layout Guidelines:

1. PVDD may be greater than or equal to VDD.
2. VSS, PVSS must be connected to ground input directly, not the branch of each other.
3. A typical value of C1 is 47uf, and it should vary in different loadings.
4. If there is application with motor, REGOUT should be connected with C3.
5. IOC/IOD isn't supported in GPC71P032A/GPC71P016A.
6. There is no "TEST" pin in GPC71P032A/GPC71P016A.

10 PACKAGE/PAD LOCATIONS

10.1 Ordering Information

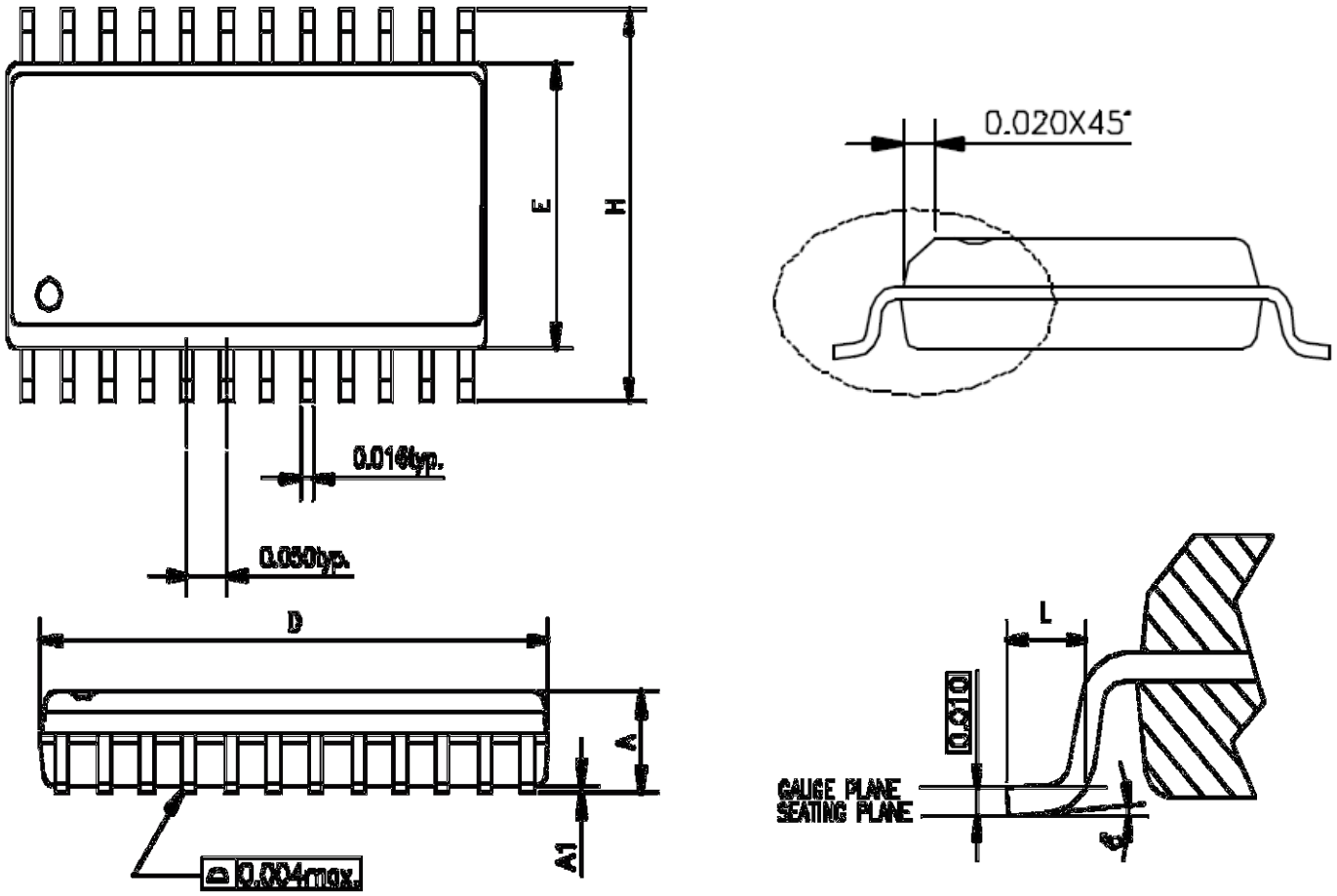
Product Number	Package Type
GPC71PXXXA-NnnV-C	Chip form
GPC71P340A-PS011	Green Package –SOP8
GPC71P170A-PS011	Green Package –SOP8
GPC71P080A-HS011	Green Package –SOP8
GPC71P064A-HS011	Green Package –SOP8
GPC71P048A-HS012	Green Package –SOP8
GPC71P032A-HS011	Green Package –SOP8
GPC71P016A-HS011	Green Package –SOP8
GPC71P340A-PS031	Green Package –SOP16
GPC71P170A-PS031	Green Package –SOP16
GPC71P080A-HS031	Green Package –SOP16
GPC71P064A-HS031	Green Package –SOP16
GPC71P048A-HS032	Green Package –SOP16
GPC71P032A-HS031	Green Package –SOP16
GPC71P016A-HS031	Green Package –SOP16

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10.2 Package Information

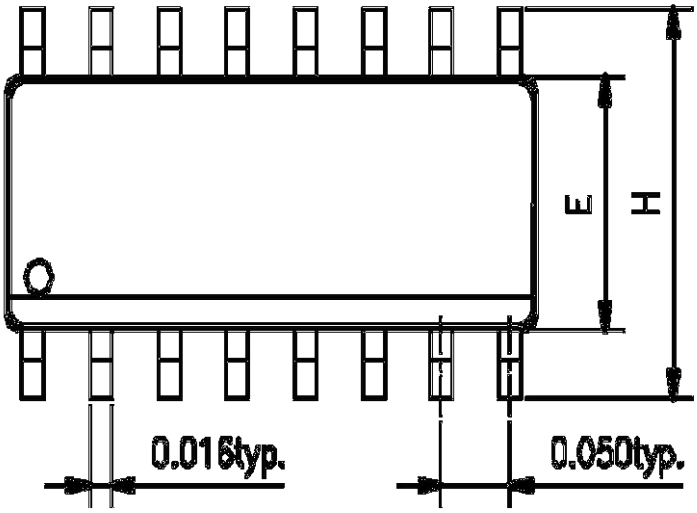
24 PIN SOP(300 mil)

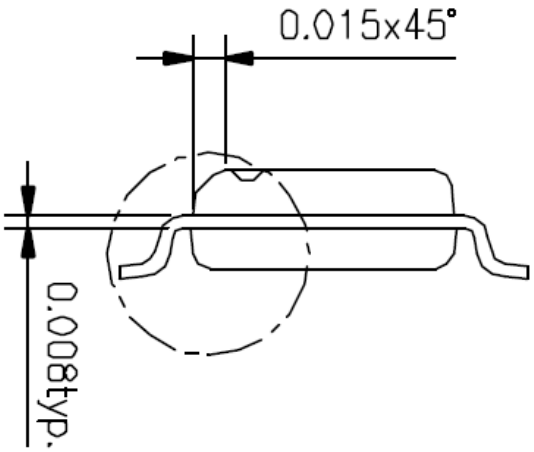


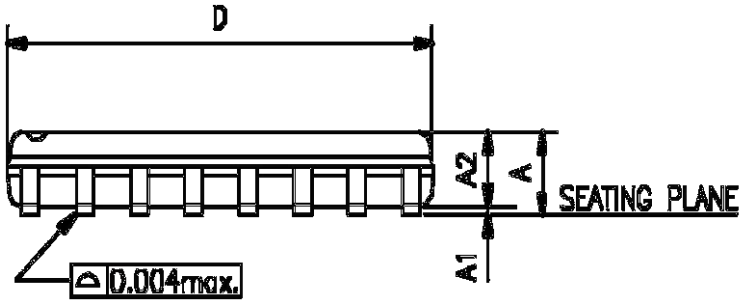
SYMBOLS	MIN.	NOM	MAX.
A	0.093	0.099	0.104
A1	0.004	–	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	–	8

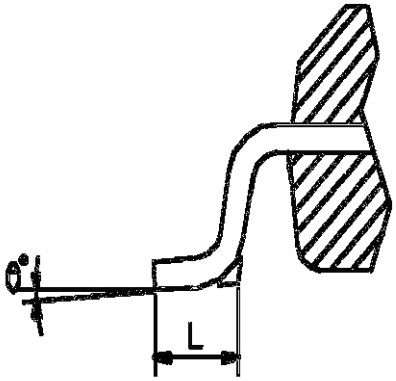
UNIT : INCH

16 PIN SOP(150 mil)





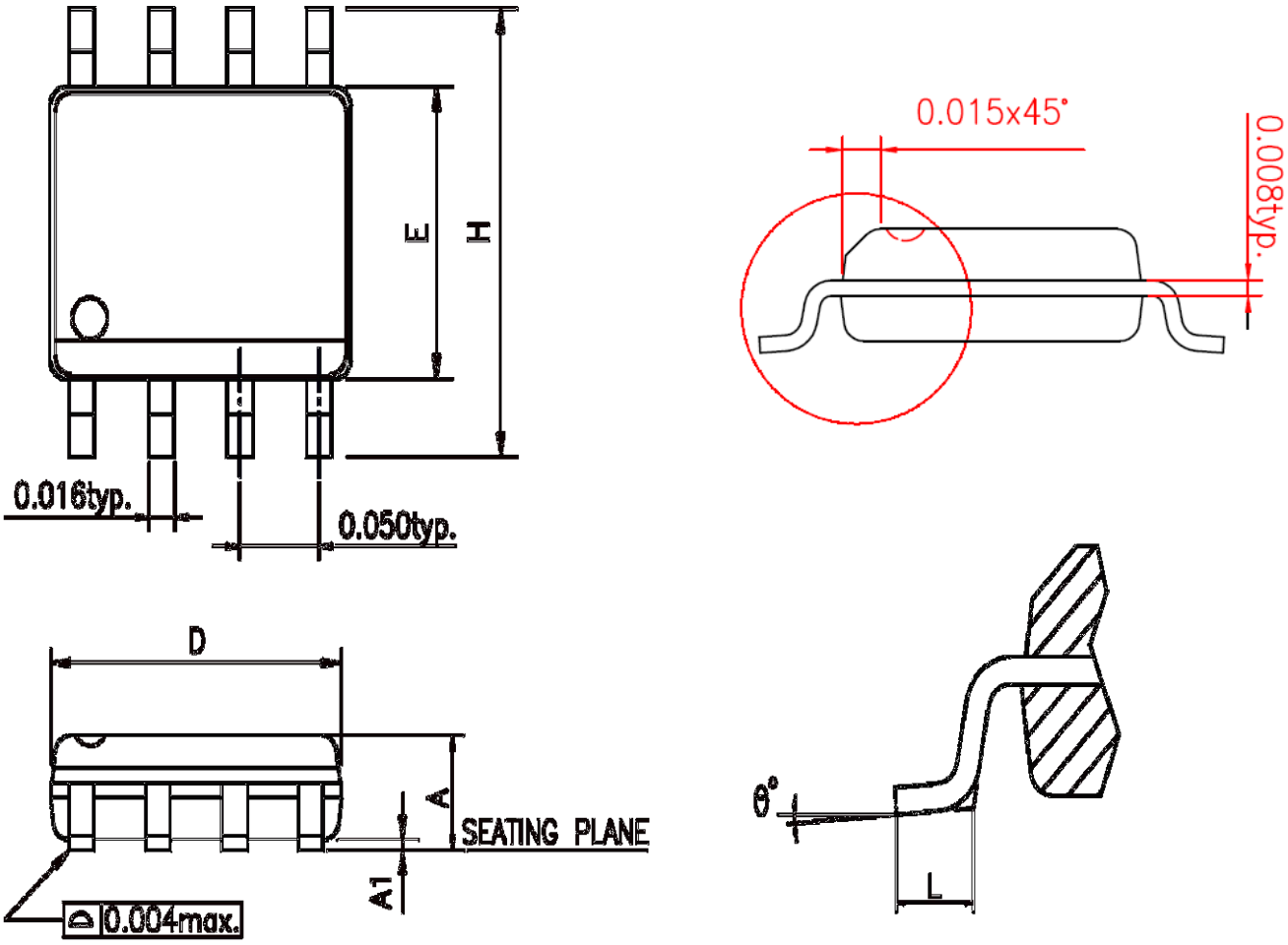




SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ	0	8

UNIT : INCH

8 PIN SOP(150 mil)



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

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12 REVISION HISTORY

Date	Revision #	Description	Page
Dec. 20, 2016	1.2	Add GPC71P340A/GPC71P170A and related information.	3,4,5,6,7, 8-10,11, 14
Apr. 18, 2016	1.1	1. Remove Note of section 1. 2. Add VSS_FUSE pad description.	3 4
Dec. 02, 2015	1.0	Original	17