2.5 V Low Profile 184-pin Registered DDR-I SDRAM Modules

256MB, 512MB & 1GByte
PC1600 & PC2100
Preliminary Datasheet Revision 0.91

- 184-pin Registered 8-Byte Dual-In-Line DDR-I SDRAM Module for “1U” PC, Workstation and Server main memory applications
- One bank 32M × 72, 64M x 72 and two bank 128M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR-I SDRAM) with a single + 2.5 V (± 0.2 V) power supply
- Built with DDR-I SDRAMs in 66-Lead TSOPII package
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Performance:
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 133.35 mm x 30,40 mm (1.2”) x 4.00 mm (6,80 mm with stacked components)
- Based on Jedec standard reference card layouts RawCard “L”, “M”, “N”
- Gold plated contacts

		-7F	-7	-8	Unit
	Component Speed Grade	DDR266F	DDR266A	DDR200	
	Module Speed Grade	PC2100	PC2100	PC1600	
f_{CK}	Clock Frequency (max.) @ CL = 2.5	143	143	125	MHz
f_{CK}	Clock Frequency (max.) @ CL = 2	133	133	100	MHz

The HYS72Dxx5x0GR are low profile versions of the standard Registered DIMM modules with 1.2” inch (30,40 mm) height for 1U Server Applications. The Low Profile DIMM versions are available as 32M x 72 (256MB), 64M x 72 (512MB) and 128M x 72 (1 GB).

The memory array is designed with Double Data Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology	Module height
PC2100 (CL=2):				
HYS 72D32500GR-7F-B	PC2100R-20220-L	one bank 256 MB Reg. DIMM	256 MBit (x8)	1.2”
HYS 72D32500GR-7-B	PC2100R-20330-L	one bank 256 MB Reg. DIMM	256 MBit (x8)	1.2”
HYS 72D64500GR-7F-B	PC2100R-20220-M	one bank 512 MB Reg. DIMM	256 Mbit (x4)	1.2”
HYS 72D64500GR-7-B	PC2100R-20330-M	one bank 512 MB Reg. DIMM	256 Mbit (x4)	1.2”
HYS 72D128520GR-7F-B	PC2100R-20220-N	two banks 1 GByte Reg. DIMM	256 MBit (x4) (stacked with soldering process)	1.2”
HYS 72D128520GR-7-B	PC2100R-20330-N	two banks 1 GByte Reg. DIMM	256 MBit (x4) (stacked with soldering process)	1.2”
HYS 72D128521GR-7F-B	PC2100R-20220-N	two banks 1 GByte Reg. DIMM	256 MBit (x4) (stacked with laser welding process)	1.2”
HYS 72D128521GR-7-B	PC2100R-20330-N	two banks 1 GByte Reg. DIMM	256 MBit (x4) (stacked with laser welding process)	1.2”
PC1600 (CL=2):				
HYS 72D32500GR-8-B	PC1600R-20220-L	one bank 256 MB Reg. DIMM	256 MBit (x8)	1.2”
HYS 72D64500GR-8-B	PC1600R-20220-M	one bank 512 MB Reg. DIMM	256 Mbit (x4)	1.2”
HYS 72D128520GR-8-B	PC1600R-20220-N	two banks 1 GByte Reg. DIMM	256 MBit (x4) (stacked with soldering process)	1.2”
HYS 72D128521GR-8-B	PC1600R-20220-N	two banks 1 GByte Reg. DIMM	256 MBit (x4) (stacked with laser welding process)	1.2”

Notes:

1. All part numbers end with a place code (not shown), designating the silicon-die revision. Reference information available on request. Example: HYS 72D32500GR-8-A, indicating Rev.A die are used for SDRAM components.
2. The Compliance Code is printed on the module labels and describes the speed sort fe. “PC2100R”, the latencies (f.e. “20330” means CAS latency = 2.5, trcd latency = 3 and trp latency =3) and the Raw Card used for this module

Pin Definitions and Functions

A0 - A11,A12	Address Inputs (A12 for 256Mb & 512Mb based modules)	V_{DD}	Power (+ 2.5 V)
BA0, BA1	Bank Selects	V_{SS}	Ground
DQ0 - DQ63	Data Input/Output	V_{DDQ}	I/O Driver power supply
CB0 - CB7	Check Bits (x72 organization only)	V_{DDID}	VDD Indentification flag
$\overline{RAS}$	Row Address Strobe	V_{DDSPD}	EEPROM power supply
$\overline{CAS}$	Column Address Strobe	V_{REF}	I/O reference supply
$\overline{WE}$	Read/Write Input	SCL	Serial bus clock
CKE0, CKE1	Clock Enable	SDA	Serial bus data line
DQS0 - DQS8	SDRAM low data strobes	SA0 - SA2	slave address select
CK0, $\overline{CK0}$	Differential Clock Input	NC	no connect
DM0 - DM8 DQS9 - DQS17	SDRAM low data mask/ high data strobes	DU	don't use
$\overline{CS0}$ - $\overline{CS1}$	Chip Selects	$\overline{RESET}$	Reset pin (forces register inputs low) *)

*) for detailed description of the Power Up and Power Management on DDR Registered DIMMs see the Application Note at the end of this datasheet

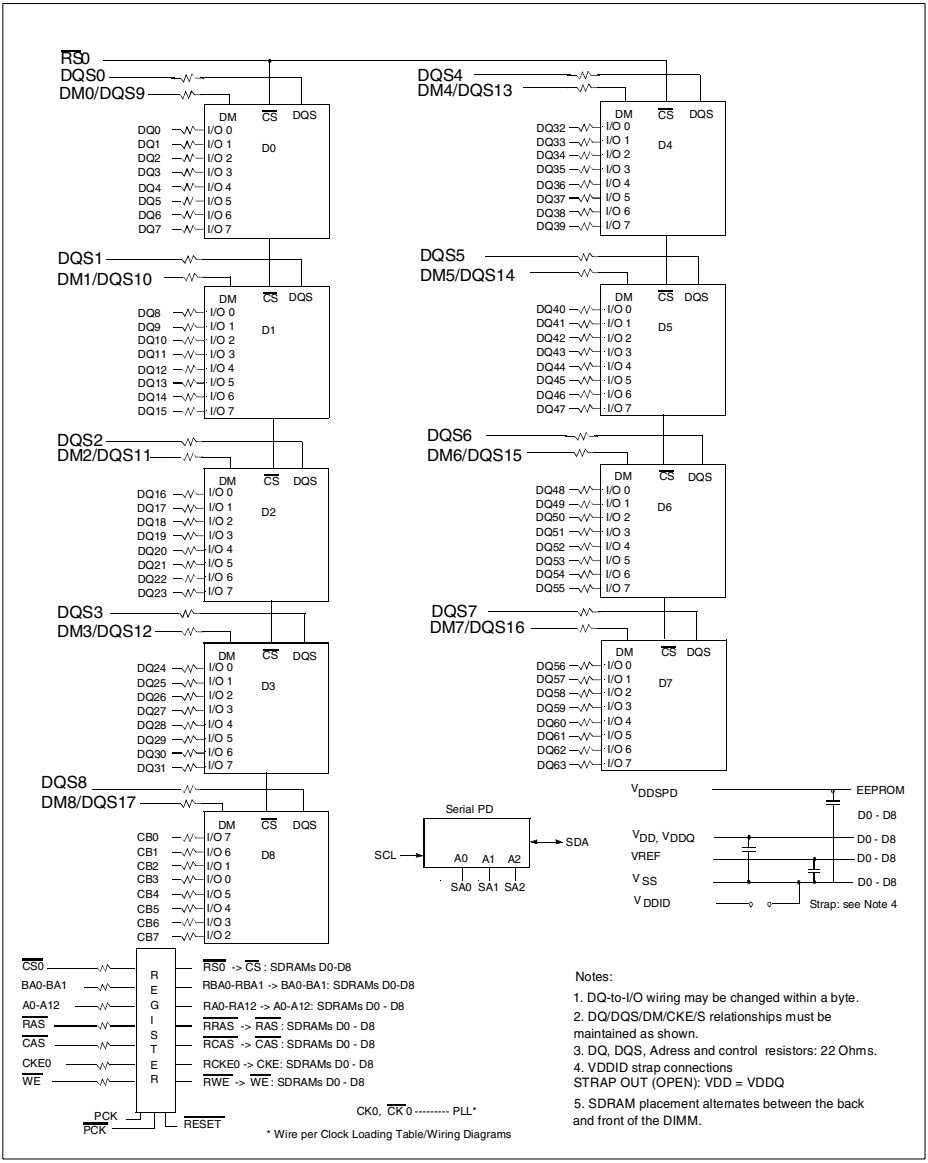
Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M x 72	1	(256Mb) 32M x 8	9	13/2/10	8k	64 ms	7.8 µs
512 MB	64M × 72	1	(256Mb) 64M × 4	18	13/2/11	8k	64 ms	7.8 µs
1 GB	128M × 72	2	(256Mb) 64M × 4	36 (stacked)	13/2/11	8k	64 ms	7.8 µs

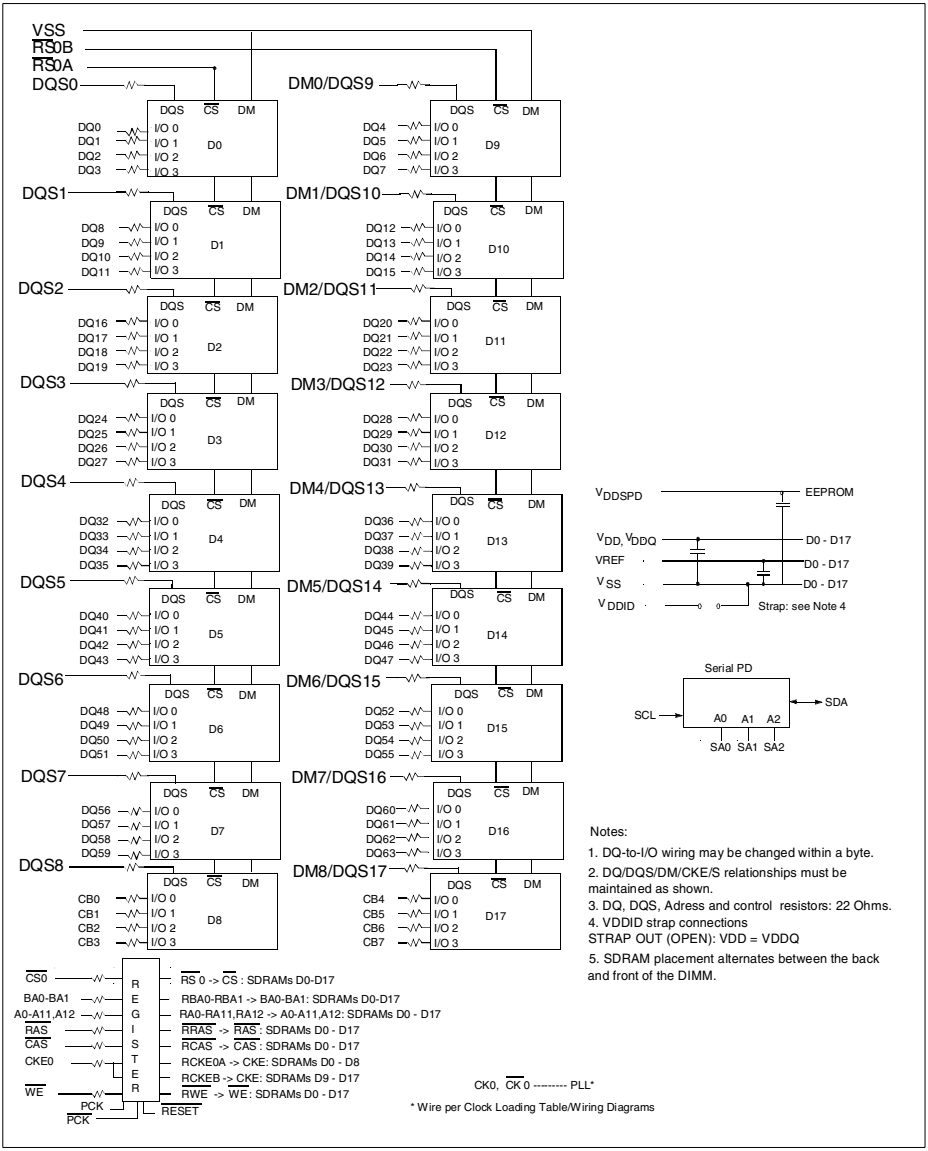
Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol		Symbol
1	VREF	48	A0	93	VSS	140	DM8/DQS17
2	DQ0	49	CB2	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	CB6
4	DQ1	51	CB3	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DM0/DQS9	144	CB7
6	DQ2		KEY	98	DQ6		KEY
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	$\overline{\text{RESET}}$	56	DQS4	102	NC	148	VDD
11	VSS	57	DQ34	103	NC	149	DM4/DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	DU	62	VDDQ	108	VDD	154	$\overline{\text{RAS}}$
17	DU	63	$\overline{\text{WE}}$	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	$\overline{\text{CAS}}$	111	CKE1	157	$\overline{\text{CS0}}$
20	DQ11	66	VSS	112	VDDQ	158	$\overline{\text{CS1}}$
21	CKE0	67	DQS5	113	NC	159	DM5/DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	NC / A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	DU	121	DQ22	167	NC
30	VDDQ	76	DU	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	CB4	180	VDDQ
43	A1	89	VSS	135	CB5	181	SA0
44	CB0	90	NC	136	VDDQ	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	$\overline{\text{CK0}}$	184	VDDSPD
47	DQS8			139	VSS		

Note: A12 is used for 256Mbit and 512Mbit based modules only



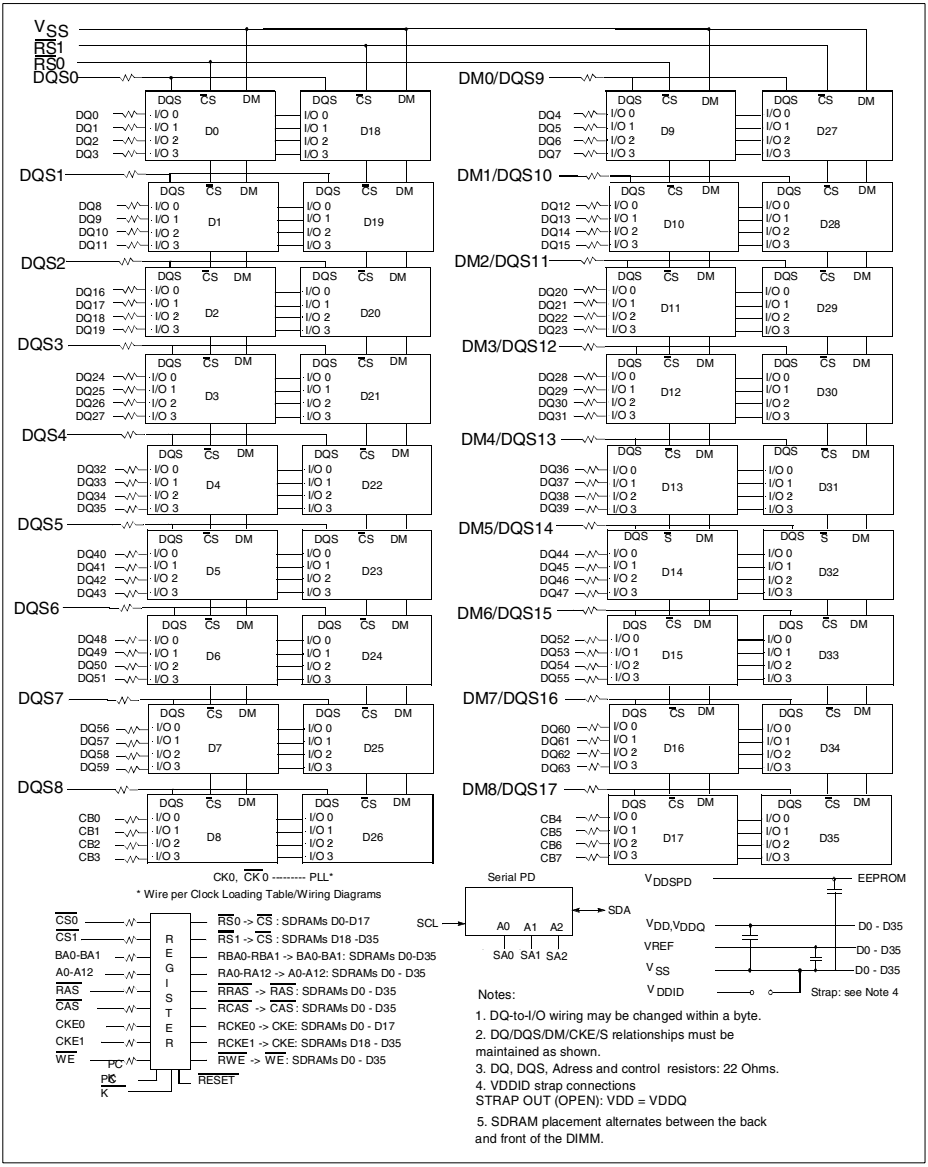
Block Diagram: One Bank 32M x 72 DDR-I SDRAM DIMM Module (x8 components) HYS72D32500GR on Raw Card L



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, Adress and control resistors: 22 Ohms.
4. VDDID strap connections
STRAP OUT (OPEN): VDD = VDDQ
5. SDRAM placement alternates between the back and front of the DIMM.

Block Diagram: One Bank 64M x 72 DDR-I SDRAM DIMM Modules (x4 comp.)
HYS72D64500GR on Raw Card M



Block Diagram: Two Bank 128M x 72 and DDR-I SDRAM DIMM Modules (x4 comp.)
HYS72D128520GR on Raw Card N

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	3.6	V
Power supply voltage on V_{DD}/V_{DDQ} to V_{SS}	V_{DD}, V_{DDQ}	– 0.5	3.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

Supply Voltage Levels

Parameter	Symbol	Limit Values			Unit	Notes
		min.	nom.	max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	-
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
Termination Voltage	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V	3)
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	

1 Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2 Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$.
V_{REF} is also expected to track noise variations in V_{DDQ}.
3 V_{TT} of the transmitting device must track V_{REF} of the receiving device.

DC Operating Conditions (SSTL_2 Inputs)

(VDDQ = 2.5 V, TA = 70 °C, Voltage Referenced to VSS)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DC Input Logic High	$V_{IH\ (DC)}$	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1)
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	V_{REF} – 0.15	V	–
Input Leakage Current	I_{IL}	– 5	5	µA	1)
Output Leakage Current	I_{OL}	– 5	5	µA	2)

1) The relationship between the V_{DDQ} of the driving device and the V_{REF} of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max)}$ (input overdrive), it is the V_{DDQ} of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).
2) For any pin under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V. Values are shown per DDR-SDRAM component.

Operating, Standby and Refresh Currents (-8: PC1600)

Symbol	Parameter/Condition	256MB x72 1bank -8	512MB x72 1bank -8	1GB x72 2bank -8	Unit	Notes
		MAX	MAX	MAX		5
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	810	1620	2430	mA	1, 4
IDD1	**Operating Current**: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	900	1800	2610	mA	1, 3, 4
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	63	126	252	mA	2, 4
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	315	630	1260	mA	2, 4
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	198	396	792	mA	2, 4
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	144	288	576	mA	2, 4
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	405	810	1620	mA	2, 4
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	855	1710	2520	mA	1, 3, 4
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	945	1890	2700	mA	1, 4
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	1530	3060	3870	mA	1, 4
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	22,5	45	90	mA	2, 4
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	1890	3780	4590	mA	1, 3, 4

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. DRAM component currents only: module IDD will be measured differently depending upon register and PLL operation currents
5. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Operating, Standby and Refresh Currents (-7: PC2100)

Symbol	Parameter/Condition	256MB x72 1bank -7	512MB x72 1bank -7	1GB x72 2bank -7	Unit	Notes
		MAX	MAX	MAX		5
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	900	1800	2790	mA	1, 4
IDD1	**Operating Current**: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	990	1980	2970	mA	1, 3, 4
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	72	144	288	mA	2, 4
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	360	720	1440	mA	2, 4
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	225	450	900	mA	2, 4
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	162	324	648	mA	2, 4
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	495	990	1980	mA	2, 4
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	1035	2070	3060	mA	1, 3, 4
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	1125	2250	3240	mA	1, 4
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	1620	3240	4230	mA	1, 4
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	23	45	90	mA	2, 4
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	2025	4050	5040	mA	1, 3, 4

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. DRAM component currents only: module IDD will be measured differently depending upon register and PLL operation currents
5. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Operating, Standby and Refresh Currents (-7F: PC2100)

Symbol	Parameter/Condition	256MB x72 1bank -7F	512MB x72 1bank -7F	1GB x72 2bank -7F	Unit	Notes
		MAX	MAX	MAX		5
IDD0	**Operating Current**: one bank; active / precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles	990	1980	2970	mA	1, 4
IDD1	**Operating Current**: one bank; active/read/precharge; Burst = 4; Refer to the following page for detailed test conditions.	1080	2160	3150	mA	1, 3, 4
IDD2P	**Precharge Power-Down Standby Current**: all banks idle; power-down mode; CKE <= VIL MAX; tCK = tCK MIN	72	144	288	mA	2, 4
IDD2F	**Precharge Floating Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs changing once per clock cycle, VIN = VREF for DQ, DQS and DM.	360	720	1440	mA	2, 4
IDD2Q	**Precharge Quiet Standby Current**: /CS >= VIH MIN, all banks idle; CKE >= VIH MIN; tCK = tCK MIN ,address and other control inputs stable at >= VIH MIN or <= VIL MAX; VIN = VREF for DQ, DQS and DM.	225	450	900	mA	2, 4
IDD3P	**Active Power-Down Standby Current**: one bank active; power-down mode; CKE <= VIL MAX; tCK = tCK MIN;VIN = VREF for DQ, DQS and DM.	162	324	648	mA	2, 4
IDD3N	**Active Standby Current**: one bank active; active / precharge;CS >= VIH MIN; CKE >= VIH MIN; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	495	990	1980	mA	2, 4
IDD4R	**Operating Current**: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN; IOUT = 0mA	1035	2070	3060	mA	1, 3, 4
IDD4W	**Operating Current**: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200, and DDR266A, CL=3 for DDR333; tCK = tCK MIN	1125	2250	3240	mA	1, 4
IDD5	**Auto-Refresh Current**: tRC = tRFC MIN, distributed refresh	1620	3240	4230	mA	1, 4
IDD6	**Self-Refresh Current**: CKE <= 0.2V; external clock on; tCK = tCK MIN	23	45	90	mA	2, 4
IDD7	**Operating Current**: four bank; four bank interleaving with BL=4; Refer to the following page for detailed test conditions.	2025	4050	5040	mA	1, 3, 4

1. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   n * IDDx[component] + n * IDD3N[component] for two bank modules (n: number of components per module bank)
2. The module IDD values are calculated from the component IDD datasheet values as:
   n * IDDx[component] for single bank modules (n: number of components per module bank)
   2 * n * IDDx[component] for two bank modules (n: number of components per module bank)
3. DQ I/O (IDDQ) currents are not included into calculations: module IDD values will be measured differently depending on load conditions
4. DRAM component currents only: module IDD will be measured differently depending upon register and PLL operation currents
5. Test condition for maximum values: VDD = 2.7V ,Ta = 10°C

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR266F -7F		DDR266A -7		DDR200 -8		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{AC}	DQ output access time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4
t_{CH}	CK high-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{CL}	CK low-level width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	1-4
t_{HP}	Clock Half Period		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		min (t_{CL}, t_{CH})		ns	1-4
t_{CK}	Clock cycle time	CL = 2.5	7	12	7	12	8	12	ns	1-4
t_{CK}		CL = 2.0	7.5	12	7.5	12	10	12	ns	1-4
t_{DH}	DQ and DM input hold time		0.5		0.5		0.6		ns	1-4
t_{DS}	DQ and DM input setup time		0.5		0.5		0.6		ns	1-4
t_{IPW}	Control and Addr. input pulse width (each input)		2.2		2.2		2.5		ns	1, 10
t_{DIPW}	DQ and DM input pulse width (each input)		1.75		1.75		2		ns	1-4,11
t_{HZ}	Data-out high-impedence time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4, 5
t_{LZ}	Data-out low-impedence time from CK/$\overline{CK}$		– 0.75	+ 0.75	– 0.75	+ 0.75	– 0.8	+ 0.8	ns	1-4, 5
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	1-4
t_{DQSQ}	DQS-DQ skew (for DQS & associated DQ signals)			+ 0.5		+ 0.5		+ 0.6	ns	1-4
t_{QHS}	Data hold skew factor			+ 0.75		+ 0.75		+ 1.0	ns	1-4
t_{QH}	Data Output hold time from DQS		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	1-4
$t_{DQSL,H}$	DQS input low (high) pulse width (write cycle)		0.35		0.35		0.35		t_{CK}	1-4
t_{DSS}	DQS falling edge to CK setup time (write cycle)		0.2		0.2		0.2		t_{CK}	1-4
t_{DSH}	DQS falling edge hold time from CK (write cycle)		0.2		0.2		0.2		t_{CK}	1-4
t_{MRD}	Mode register set command cycle time		14		14		16		ns	1-4
t_{WPRES}	Write preamble setup time		0		0		0		ns	1-4, 7
t_{WPST}	Write postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4, 6
t_{WPRE}	Write preamble		0.25		0.25		0.25		t_{CK}	1-4
t_{IS}	Address and control input setup time	fast slew rate	0.9		0.9		1.1		ns	2-4, 10,11
		slow slew rate	1.0		1.0		1.1		ns	
t_{IH}	Address and control input hold time	fast slew rate	0.9		0.9		1.1		ns	
		slow slew rate	1.0		1.0		1.1		ns	
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	1-4
t_{RPST}	Read postamble		0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	1-4
t_{RAS}	Active to Precharge command		45	120,000	45	120,000	50	120,000	ns	1-4
t_{RC}	Active to Active/Auto-refresh command period		60		65		70		ns	1-4
t_{RFC}	Auto-refresh to Active/Auto-refresh command period		75		75		80		ns	1-4
t_{RCD}	Active to Read or Write delay		15		20		20		ns	1-4
t_{RP}	Precharge command period		15		20		20		ns	1-4
t_{RRD}	Active bank A to Active bank B command		15		15		15		ns	1-4

Electrical Characteristics & AC Timing for DDR-I components

(for reference only)

(0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V)

Symbol	Parameter		DDR266F -7F		DDR266A -7		DDR200 -8		Unit	Notes
			Min	Max	Min	Max	Min	Max		
t_{WR}	Write recovery time		15		15		15		ns	1-4
t_{DAL}	Auto precharge write recovery + precharge time		(twr/tck) + (trp/tck)		(twr/tck) + (trp/tck)				t_{CK}	1-4,9
t_{WTR}	Internal write to read command delay		1		1		1		t_{CK}	1-4
t_{XSNR}	Exit self-refresh to non-read command		75		75		80		ns	1-4
t_{XSRD}	Exit self-refresh to read command		200		200		200		t_{CK}	1-4
t_{REFI}	Average Periodic Refresh Interval	256Mb based		7.8		7.8		7.8	µs	1-4, 8

1. Input slew rate >=1V/ns for DDR266 and = 1V/ns for DDR200.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are >= 1.0 V/ns.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
8. A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.
9. For each of the terms, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
10. These parameters guarantee device timing, but they are not necessarily tested on each device
11. Fast slew rate >= 1.0 V/ns , slow slew rate >= 0.5 V/ns and < 1V/ns for command/address and CK & $\overline{CK}$ slew rate >1.0 V/ns, measured between VOH(ac) and VOL(ac)

SPD Codes

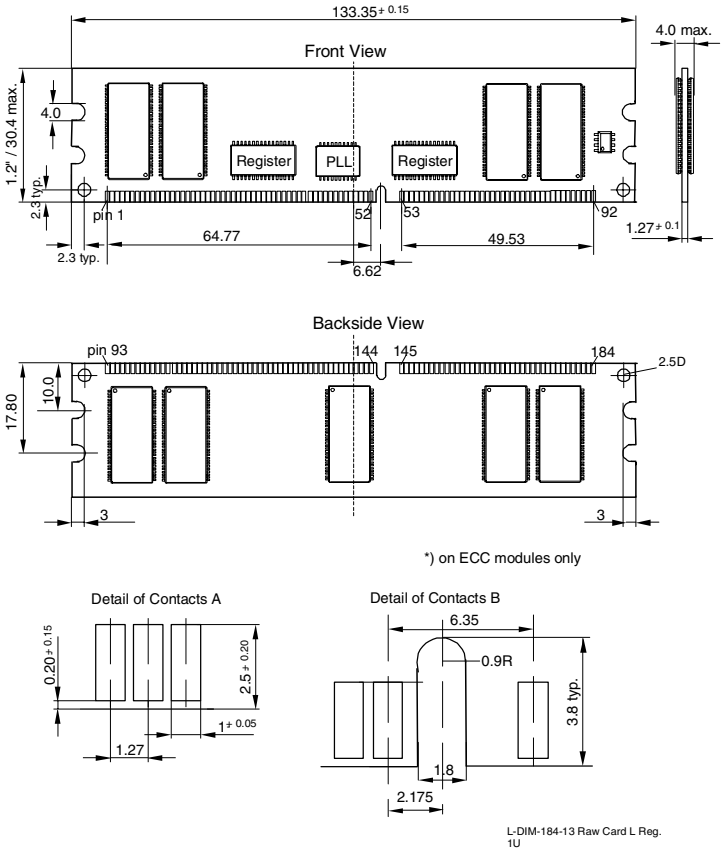
Byte#	Description		256MB x72 1bank -7F	256MB x72 1bank -7	256MB x72 1bank -8	512MB x72 1bank -7F	512MB x72 1bank -7	512MB x72 1bank -8	1GB x72 2bank -7F	1GB x72 2bank -7	1GB x72 2bank -8
			HEX	HEX	HEX	HEX	HEX	HEX	HEX	HEX	HEX
0	Number of SPD Bytes	128	80	80	80	80	80	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08	08	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07	07	07	07	07	07
3	Number of Row Addresses	13	0D	0D	0D	0D	0D	0D	0D	0D	0D
4	Number of Column Addresses	10 / 11	0A	0A	0A	0B	0B	0B	0B	0B	0B
5	Number of DIMM Banks	1 / 2	01	01	01	01	01	01	02	02	02
6	Module Data Width	x72	48	48	48	48	48	48	48	48	48
7	Module Data Width (cont'd)	0	00	00	00	00	00	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04	04	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	7ns / 8ns	70	70	80	70	70	80	70	70	80
10	Access Time from Clock at CL = 2.5	0.75ns / 0.8ns	75	75	80	75	75	80	75	75	80
11	DIMM Config	ECC	02	02	02	02	02	02	02	02	02
12	Refresh Rate/Type	Self-Refresh, 7.8ms	82	82	82	82	82	82	82	82	82
13	SDRAM Width, Primary	x8 / x4	08	08	08	04	04	04	04	04	04
14	Error Checking SDRAM Data Width	na	08	08	08	04	04	04	04	04	04
15	Minimum Clock Delay for Back-to-Back Random Column Address	tccd = 1 CLK	01	01	01	01	01	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E	0E	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04	04	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C	0C	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01	01	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02	02	02	02	02	02
21	SDRAM DIMM Module Attributes	registered	26	26	26	26	26	26	26	26	26
22	SDRAM Device Attributes: General	Concurrent Auto Precharge	C0	C0	C0	C0	C0	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	7.5ns / 10ns	75	75	A0	75	75	A0	75	75	A0
24	Access Time from Clock for CL = 2	0.75ns / 0.8ns	75	75	80	75	75	80	75	75	80
25	Minimum Clock Cycle Time at CL = 1.5	not supported	00	00	00	00	00	00	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00	00	00	00	00	00
27	Minimum Row Precharge Time	20ns	3C	50	50	3C	50	50	3C	50	50
28	Minimum Row Act. to Row Act. Delay tRRD	15ns	3C	3C	3C	3C	3C	3C	3C	3C	3C
29	Minimum RAS to CAS Delay tRCD	20ns	3C	50	50	3C	50	50	3C	50	50
30	Minimum RAS Pulse Width tRAS	45ns / 50ns	2D	2D	32	2D	2D	32	2D	2D	32
31	Module Bank Density (per bank)	256MByte / 512MByte	40	40	40	80	80	80	80	80	80
32	Addr. and Command Setup Time	0.9ns / 1.1ns	90	90	B0	90	90	B0	90	90	B0
33	Addr. and Command Hold Time	0.9ns / 1.1ns	90	90	B0	90	90	B0	90	90	B0
34	Data Input Setup Time	0.5ns / 0.6ns	50	50	60	50	50	60	50	50	60
35	Data Input Hold Time	0.5ns / 0.6ns	50	50	60	50	50	60	50	50	60
36-40	Superset Information	–	00	00	00	00	00	00	00	00	00
41	Minimum Core Cycle Time tRC	65ns / 70ns	3C	41	46	3C	41	46	3C	41	46
42	Min. Auto Refresh Cmd Cycle Time tRFC	75ns / 80ns	4B	4B	50	4B	4B	50	4B	4B	50
43	Maximum Clock Cycle Time tck	12ns	30	30	30	30	30	30	30	30	30
44	Max. DQS-DQ Skew tDQSQ	0.5ns / 0.6ns	32	32	3C	32	32	3C	32	32	3C
45	X-Factor tQHS	0.75ns / 1.0ns	75	75	A0	75	75	A0	75	75	A0
46-61	Superset Information	–	00	00	00	00	00	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00	00	00	00	00	00
63	Checksum for Bytes 0 - 62	–	9D	CA	BF	D6	03	F8	D7	04	F9
64	Manufacturers JEDEC ID Code	–	C1	C1	C1	C1	C1	C1	C1	C1	C1
65-71	Manufacturer	–	INFI-NEON	INFI-NEON	INFI-NEON	INFI-NEON	INFI-NEON	INFI-NEON	INFI-NEON	INFI-NEON	INFI-NEON
72	Module Assembly Location	–									
73-90	Module Part Number	–									
91-92	Module Revision Code	–									
93-94	Module Manufacturing Date	–									
95-98	Module Serial Number	–									
99-127	–	–									
128-255	open for Customer use	–									

Package Outlines Raw Card L

Module Package

DDR-I Registered DIMM Modules 1.2” Low Profile Raw Card L

256MB (one physical bank, 9 components)



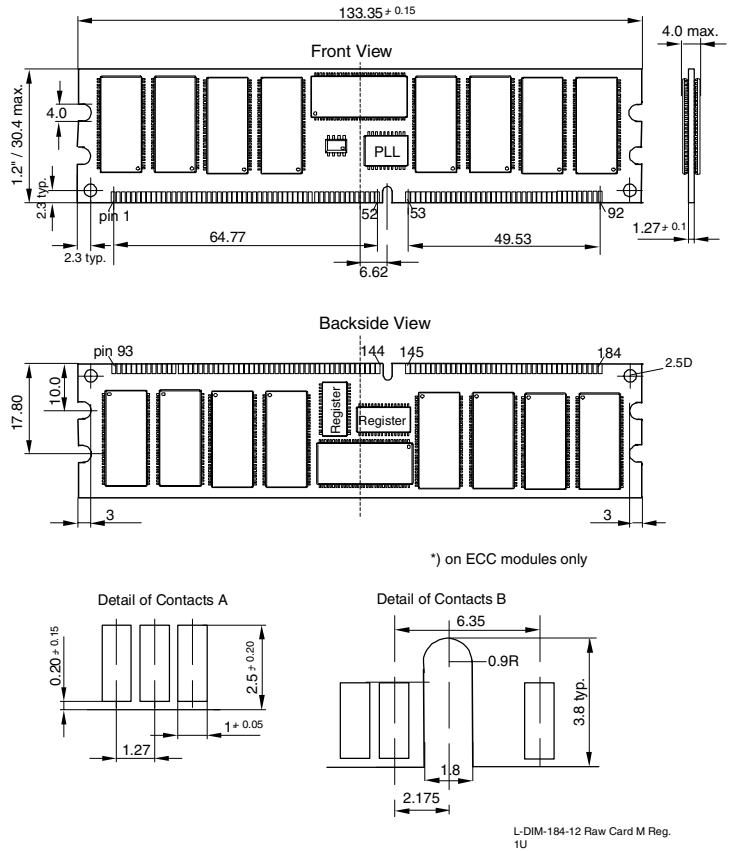
note: all outline dimensions and tolerances are in accordance with the JEDEC standard

Package Outlines Raw Card M

Module Package

DDR-I Registered DIMM Modules 1.2” Low Profile Raw Card M

512 MB (one physical bank, 18 components)



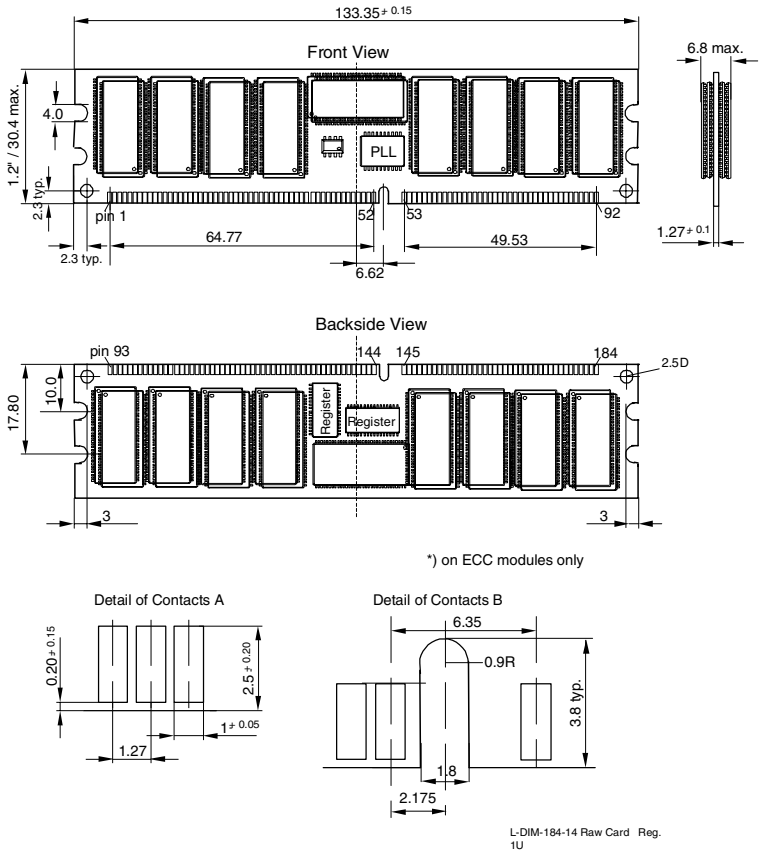
note: all outline dimensions and tolerances are in accordance with the JEDEC standard

Package Outlines Raw Card with stacked components

Module Package

DDR-I Registered DIMM Modules 1.2" Low Profile Raw Card N

1GB (two physical banks, 36 components)



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

APPLICATION NOTE:

Power Up and Power Management on DDR Registered DIMMs

(according to JEDEC ballot JC-42.5 Item 1173)

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated RESET signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new RESET pin controls power dissipation on the module's registers and ensures that CKE and other SDRAM inputs are maintained at a valid 'low' level during power-up and self refresh. When RESET is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

The function for RESET is as follows:

Register Inputs				Register Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	Data in (D)	Data out (Q)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal input conditions
L	X or Hi-Z	X or Hi-Z	X or Hi-Z	L

X : Don't care, Hi-Z : High Impedance, Qo: Data latched at the previous of CK risning and $\overline{\text{CK}}$ falling

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs — where they will remain until activated by a valid 'read' cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20MHz. When an input clock frequency of 20MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95MHz). If the clock input frequency drops below 20MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are

made High-Z, and the differential inputs are powered down — resulting in a total PLL current consumption of less than 1mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or $\overline{\text{G}}$ pin) unnecessary, and it is tied inactive on the DIMM.
This application note describes the required and optional system sequences associated with the DDR Registered DIMM '$\overline{\text{RESET}}$' function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with $\overline{\text{RESET}}$ — Required

1. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.
2. The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.
3. Stabilization of Clocks to the SDRAM
   The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 µsec prior to SDRAM operation.
4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
5. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).
6. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-pproved initialization sequence).

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the $\overline{\text{RESET}}$ pin, as this can reduce register power consumption ($\overline{\text{RESET}}$ low deactivates register CK and CK, data input receivers, and data output drivers).

1. The system applies Self Refresh entry command.

(CKE→Low, $\overline{CS}$→Low, $\overline{RAS}$ → Low, $\overline{CAS}$→ Low, $\overline{WE}$→ High)

Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Cares— with the exception of CKE.

2. The system sets $\overline{RESET}$ at a valid low level.

This input condition forces all register outputs to a low state, independent of the condition on the registerm inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the $\overline{RESET}$ signal is asynchronous, setting the $\overline{RESET}$ timing in relation to a specific clock edge is not required.

3. The system turns off clock inputs to the DIMM. (Optional)

a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock inputs to both the SDRAMs and the registers. This must be done after the $\overline{RESET}$ deactivate time of the register (t (INACT)). The deactivate time defines the time in which the clocks and the control and address signals must maintain valid levels after $\overline{RESET}$ low has been applied and is specified in the register and DIMM documentation.

b. The system may release DIMM address and control inputs to High-Z.

This can be done after the $\overline{RESET}$ deactivate time of the register. The deactivate time defines the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{RESET}$ low has been applied. It is highly recommended that CKE continue to remain low during this operation.

4. The DIMM is in lowest power Self Refresh mode.

Self Refresh Exit ($\overline{RESET}$ low, clocks powered off) — Optional

1. Stabilization of Clocks to the SDRAM.

The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches ~20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds.

2. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).

CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC Self Refresh Exit sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs, to be consistent with the state of the register outputs.

3. The system switches $\overline{RESET}$ to a logic 'high' level.

The SDRAM is now functional and prepared to receive commands. Since the $\overline{RESET}$ signal is asynchronous, $\overline{RESET}$ timing relationship to a specific clock edge is not required (during this period, register inputs must remain stable).

4. The system must maintain stable register inputs until normal register operation is attained.

The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 2. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{RESET}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.

5. System can begin the JEDEC-defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry ($\overline{RESET}$ low, clocks running) — Optional

Although keeping the clocks running increases power consumption from the on-DIMM PLL during self refresh, this is an alternate operating mode for these DIMMs.

1. System enters Self Refresh entry command.
   (CKE→ Low, $\overline{CS}$→ Low, $\overline{RAS}$→ Low, $\overline{CAS}$→ Low, $\overline{WE}$→ High)

   Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Cares — with the exception of CKE.
2. The system sets $\overline{RESET}$ at a valid low level.
   This input condition forces all register outputs to a low state, independent of the condition on the data and clock register inputs, and ensures that CKE is a stable low-level at the DDR SDRAMs.
3. The system may release DIMM address and control inputs to High-Z.
   This can be done after the $\overline{RESET}$ deactivate time of the register (t (INACT)). The deactivate time describes the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{RESET}$ low has been applied. It is highly recommended that CKE continue to remain low during the operation.
4. The DIMM is in a low power, Self Refresh mode.

Self Refresh Exit ($\overline{RESET}$ low, clocks running) — Optional

1. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the Self Refresh Exit sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
2. The system switches $\overline{RESET}$ to a logic 'high' level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{RESET}$ signal is asynchronous, it does not need to be tied to a particular clock edge (during this period, register inputs must continue to remain stable).
3. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 1. It is also a functional requirement that the registers maintain a low state at the CKE outputs in order to guarantee that the DDR SDRAMs continue to receive a low level on CKE. This activation time, from asynchronous switching of $\overline{RESET}$ from low to high, until the registers are stable and ready to accept an input signal, is t (ACT) as specified in the register and DIMM documentation.
4. The system can begin JEDEC defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry/Exit ($\overline{RESET}$ high, clocks running) — Optional

As this sequence does not involve the use of the $\overline{RESET}$ function, the JEDEC standard SDRAM specification explains in detail the method for entering and exiting Self Refresh for this case.

Self Refresh Entry ($\overline{RESET}$ high, clocks powered off) — Not Permissible

In order to maintain a valid low level on the register output, it is required that either the clocks be running and the system drive a low level on CKE, or the clocks are powered off and $\overline{RESET}$ is asserted low according to the

sequence defined in this application note. In the case where $\overline{\text{RESET}}$ remains high and the clocks are powered off, the PLL drives a High-Z clock input into the register clock input. Without the low level on $\overline{\text{RESET}}$ an unknown DIMM state will result.