DATA SHEET

GPCD2T020A

Two-channel Sound Controller

Nov. 16, 2018

Version 1.1

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2-CHANNEL SOUND CONTROLLER

1.GENERAL DESCRIPTION

GPCD2T020A series features a 64K-bytes factory programmed OTP memory, maximum of 512-byte SRAM, three 12-bit timers, 20 general I/Os, and one 14-bit audio push-pull driver. GPCD2T020A operates in a broad range of working voltage from 2.2V through 5.5V along with low voltage reset function. In addition, a sleep mode is designed to save powers for those applications with limited power resources available. In audio processing, speech can be mixed into one output. A Serial Peripheral Interface (SPI) controller is also included to facilitate communication with other devices and components.

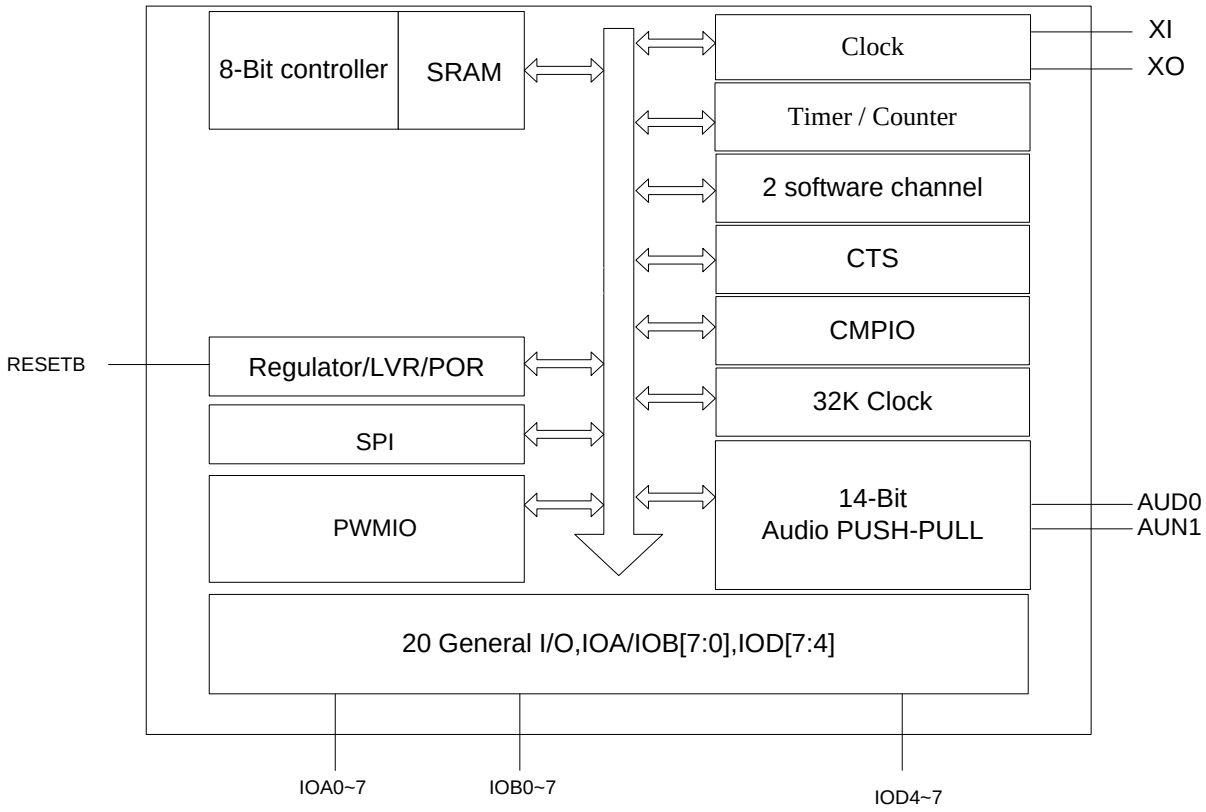
2.FEATURES

- 8-bit micro-processor
- 512-byte SRAM
- 64K-bytes factory programmed OTP memory
- Operating voltage: 2.2V – 5.5V
- Max. of CPU operating speed: 8.0MHz (Fosc=16MHz)
- Five wakeup sources
- 17 IRQs & 6 NMI Interrupts
- Internal built-in regulator to supply core power
- Two software channels with noise filter for high quality sound playback
- Low Voltage Detection
  8-level (2.2V/ 2.4V/ 2.6V/ 2.8V/ 3.0V/ 3.2V/ 3.4/ 3.6V) voltage detector
- Low Voltage Reset
- Peripherals
  - 20 I/O pins (IOA[7:0], IOB[7:0], IOD[7:4])
  - 12 I/Os with high sink current
  - Key wakeup/interrupt function
  - 32.768KHz oscillator circuit for real time clock function (X'tal or R-osc)
  - Built-in R-oscillator (external resistor needed), X'tal or internal R-oscillator (only 16MHz available for IOSC) for system operating clock
  - Internal time base generator
  - Three 12-bit timers/counters, TMA with capture and comparison function, TMB/TMC with comparison function (Programmable and auto reload)
  - Watchdog function
  - 14-bit PUSH-PULL driver for driving speaker directly
  - IR output
  - 12 hardware PWMIOs
  - One SPI serial interface I/Os
  - Hardware Touch function
  - One set built-in comparator with PGA.
- Sleep mode to reduce power consumption

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High-end toy controller
- Intelligent education toy
- And more

4.BLOCK DIAGRAM



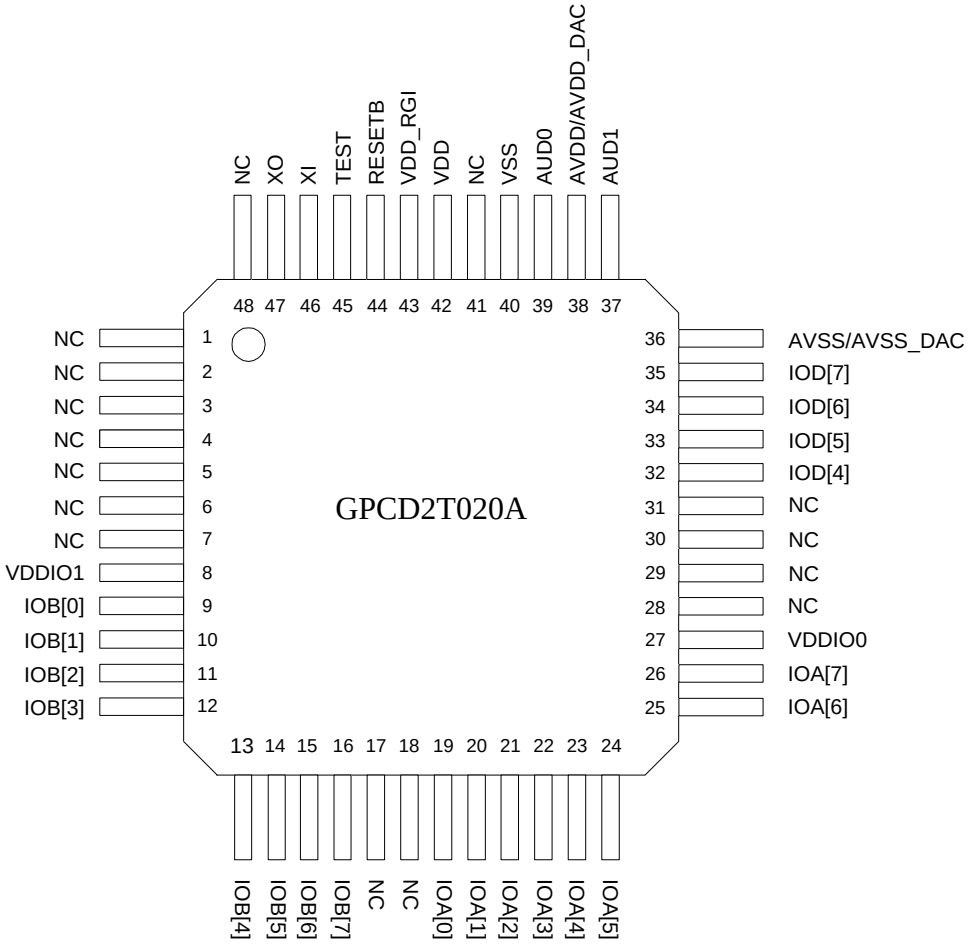
5. SIGNAL DESCRIPTION

5.1. Main Function Pin

Mnemonic	Type	Description
Dedicate IO		
VDDIO0	P	Power for IOA/IOD
VSSIO0	G	GND for all IOA/IOD
VDDIO1	P	Power for IOB
VSSIO1	G	GND for all IOB
IOA0~IOA7	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOB0~IOB7	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD4~IOD7	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power		
VDD_RGI	P	Positive supply for regulator
VSS	G	Ground for Regulator
VDD	P	Power output from regulator out
Clock (max. frequency: 16Mhz)		
XI	O	Crystal input or connected to VDD through a resistor for ROSC
XO	O	Crystal output
Audio		
AVDD	P	Power for amplifier
AVSS	G	GND for amplifier
AVDD_DAC	P	Power for DAC
AVSS_DAC	G	GND for DAC
AUD0	O	Audio output
AUD1	O	Audio output
ACIN	I	Microphone input
Other Signal		
TEST	I	TEST Mode selection pin, NC for normal application
RESETB	I	System reset pin (active low)

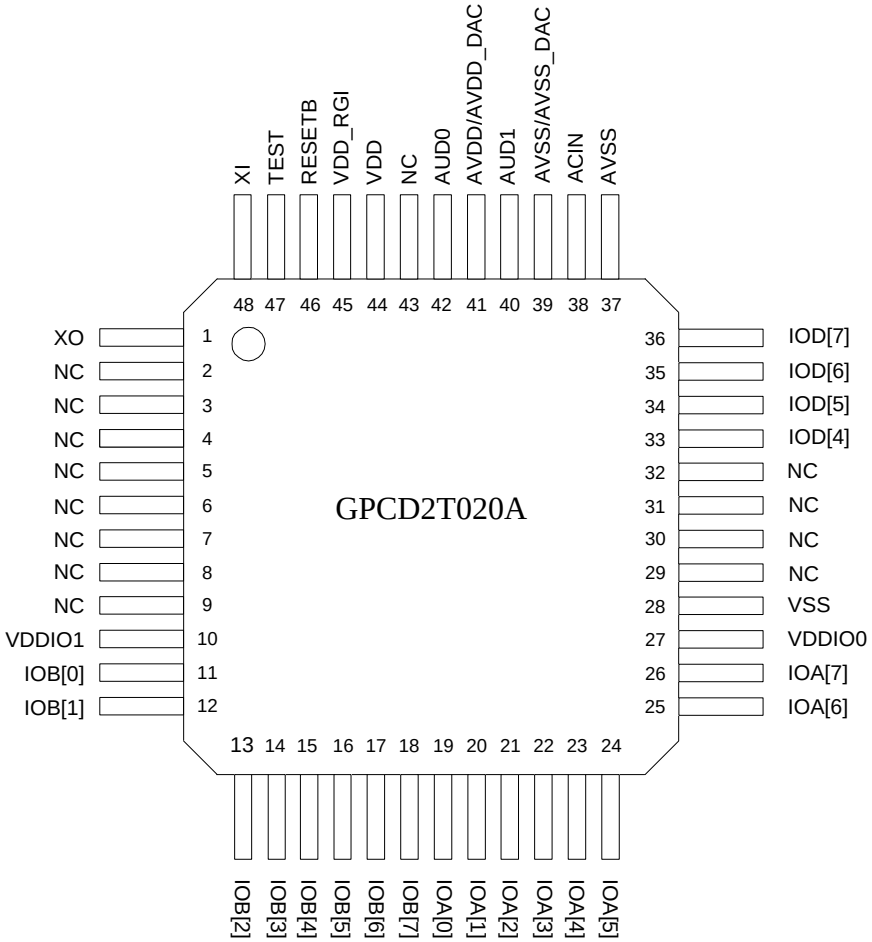
5.2. LQFP48 Package Pin Assignment

5.2.1. GPCD2T020A (LQFP48-type1)



Mnemonic	Pin No. (LQFP48)	Type	Description
Dedicate IO			
VDDIO0	27	P	Power for IOA/IOD
VSSIO0	40	G	GND for all IOA/IOD
VDDIO1	8	P	Power for IOB
VSSIO1	40	G	GND for all IOB
IOA0~IOA7	19~26	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOB0~IOB7	9~16	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD4~IOD7	32~35	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	43	P	Positive supply for regulator
VSS	40	G	Ground for regulator
VDD	42	P	Power output from regulator out
Clock (Max. Freq. 16Mhz)			
XI	46	O	Crystal input or connected to VDD through a resistor as ROSC
XO	47	O	Crystal output
Audio			
AVDD	38	P	Power for amplifier
AVSS	36	G	GND for amplifier
AVDD_DAC	38	P	Power for DAC
AVSS_DAC	36	G	GND for DAC
AUD0	39	O	Audio output
AUD1	40	O	Audio output
ACIN	-	I	Microphone input
Other Signal			
TEST	45	I	TEST Mode selection pin, NC for normal application
RESETB	44	I	System reset pin (active low)

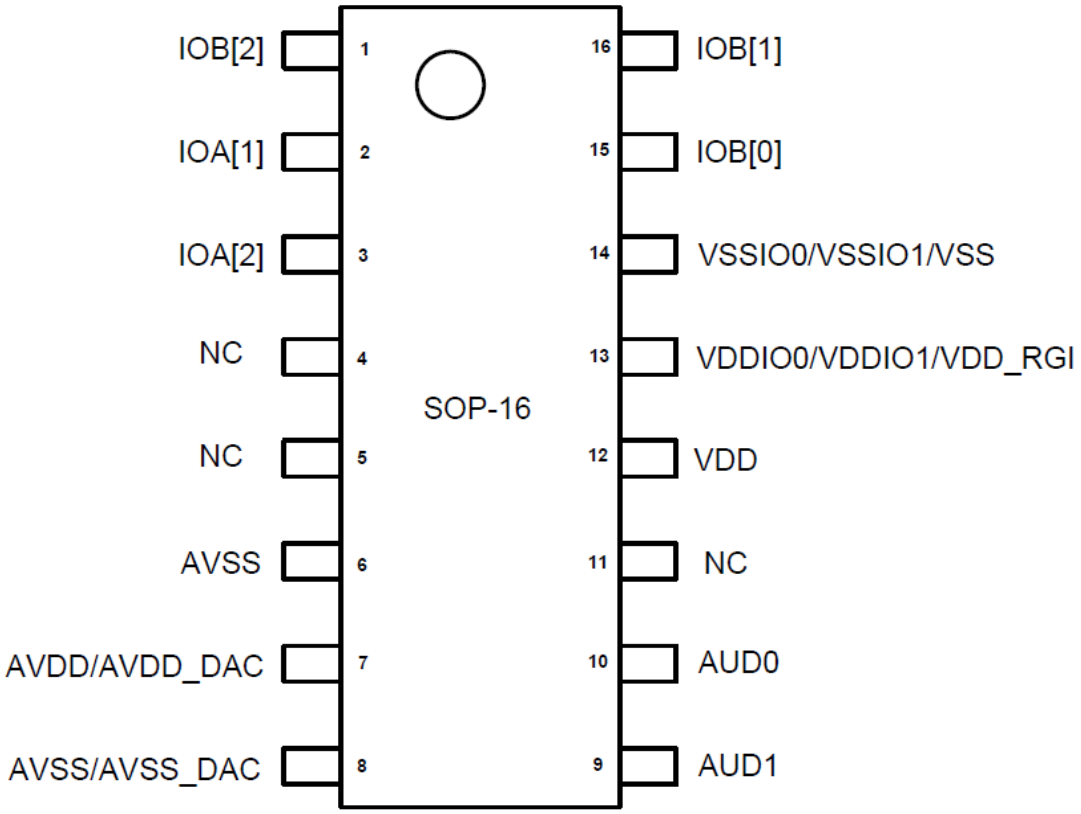
5.2.2. GPCD2T020A (LQFP48-type2)



Mnemonic	Pin No. (LQFP48)	Type	Description
Dedicate IO			
VDDIO0	27	P	Power for IOA/IOD
VSSIO0	28	G	GND for all IOA/IOD
VDDIO1	10	P	Power for IOB
VSSIO1	28	G	GND for all IOB
IOA0~IOA7	19~26	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOB0~IOB7	11~18	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD4~IOD7	33~36	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	45	P	Positive supply for regulator
VSS	28	G	Ground for regulator
VDD	44	P	Power output from regulator out
Clock (Max. Freq. 16Mhz)			
XI	48	O	Crystal input or connected to VDD through a resistor as ROSC
XO	1	O	Crystal output
Audio			
AVDD	41	P	Power for amplifier
AVSS	37,39	G	GND for amplifier
AVDD_DAC	41	P	Power for DAC
AVSS_DAC	39	G	GND for DAC
AUD0	42	O	Audio output
AUD1	40	O	Audio output
ACIN	38	I	Microphone input
Other Signal			
TEST	47	I	TEST Mode selection pin, NC for normal application
RESETB	46	I	System reset pin (active low)

5.3. SOP16 Package Pin Assignment

5.3.1. GPCD2T020A (HS032)

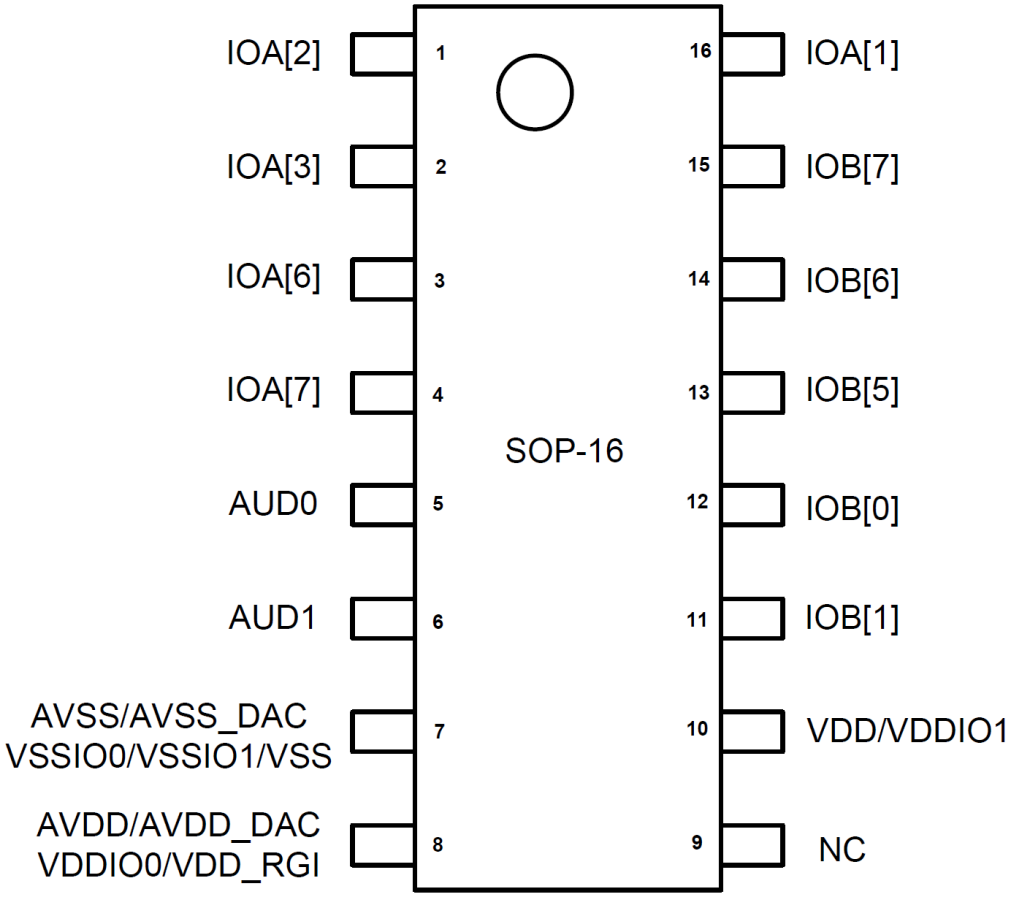


Mnemonic	Pin No. (SOP16)	Type	Description
Dedicate IO			
VDDIO0/VDDIO1	13	P	Power for IOA/IOB/IOD
VSSIO0/VSSIO1	14	G	GND for all IOA/IOB/IOD
IOA1~2	2~3	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOB0~IOB2	15~16,1	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
NC	4~5	NC	NC
Regulator - related power			
VDD_RGI	13	P	Positive supply for regulator
VSS	14	G	Ground for regulator
VDD	12	P	Power output from regulator out
Audio			
AVDD	7	P	Power for amplifier
AVSS	6,8	G	GND for amplifier
AVDD_DAC	7	P	Power for DAC
AVSS_DAC	8	G	GND for DAC
AUD0	10	O	Audio output
AUD1	9	O	Audio output

Note1: only internal R-oscillator (only 16MHz available for IOSC) for system operating clock

Note2: without SPI application

5.3.2. GPCD2T020A (HS031)



Mnemonic	Pin No. (SOP16)	Type	Description
Dedicate IO			
VDDIO0	8	P	Power for IOA/IOD
VDDIO1	10	P	Power for IOB
VSSIO0/VSSIO1	7	G	GND for all IOA/IOB/IOD
IOA1~3, IOA6~7	16,1~4	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOB0~1, IOB5~7	12,11,13~15	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	8	P	Positive supply for regulator
VSS	7	G	Ground for regulator
VDD	10	P	Power output from regulator out
Audio			
AVDD	8	P	Power for amplifier
AVSS	7	G	GND for amplifier
AVDD_DAC	8	P	Power for DAC
AVSS_DAC	7	G	GND for DAC
AUD0	5	O	Audio output
AUD1	6	O	Audio output

Note1: Only internal R-oscillator (only 16MHz available for IOSC) for system operating clock

Note2: with SPI application

6. FUNCTION DESCRIPTION

6.1. SRAM

The 512-byte SRAM (including Stack) area is located in $000000h~$0003FFh.

6.2. ROM

GPCD2T020A is equipped with 64K-bytes factory programmed OTP memory.

6.3. Low Voltage Reset

GPCD2T020A features an important feature, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops under LVR. Without LVR, CPU becomes unstable and abnormal when working voltage is too low.

6.4. Interrupt

GPCD2T020A has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls 17 IRQs and 6 NMIs. A NMI cannot be interrupted by any other IRQ.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
CPU_CLOCK/4096	NMI_D4096	NMI
EXT	NMI_EXT	NMI
Timer A	IRQ_TIMER_A	IRQ1
Timer B	IRQ_TIMER_B	IRQ2
Timer C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
16 Hz	IRQ_16Hz	IRQ6
TBL	IRQ_TBL	IRQ7
KEY	IRQ_KEY	IRQ8
EXT	IRQ_EXT	IRQ9
SPI	IRQ_SPI	IRQ10
QD1_F	IRQ_QD1_F	IRQ11
QD1_B	IRQ_QD1_B	IRQ12
QD2_F	IRQ_QD2_F	IRQ13
QD2_B	IRQ_QD2_B	IRQ14
CTS_TMA	IRQ_CTS_TMA	IRQ15
CTS_TMB	IRQ_CTS_TMB	IRQ16
CMPIO	IRQ_CMPIO	IRQ17

6.5. Hardware PWMIO

Hardware PWMIO supports 12 LED outputs (IOA[3:0],IOB[3:0], IOD[7:4]) with 256-level brightness control. The clock source of PWMIO can be selected by user's request.

6.6. I/O

The purpose of input and output ports is to communicate with other devices. Four programmable I/O ports are built-in, including Port A, B, and D. All Ports are general I/O with programmable wake-up capability and pull low function. In addition to general I/O function, I/O also provides some special functions in certain pins.

6.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are embedded in GPCD2T020A: Timer A, Timer B, and Timer C. These three timers all have 12-bit up counter, a preloaded register, and programmable clock source. Timer A/B can also be the clock source of the software channel 1/2 respectively. The clock source of each timer can be set individually. Two clock sources, including CPU clock and external clock, can be selected individually or their combination to be timer's clock source. Besides, capture and comparison function are supported by TMA. Comparison is supported by TMB and TMC.

6.8. Sleep, Wakeup and Watchdog

6.8.1. Sleep and Wakeup

Sleep mode is designed to save power by stopping clock while device is not in use. When sleep acts, the device runs from operating mode to standby mode. Waking up from sleep mode turns system back to operating mode.

(1) Sleep: After power on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

(2) Wake-up: While a wakeup signal is generated, GPCD2T020A is waking up from sleep mode. While wake-up is completed, program counter will continue to execute the next command of where entering sleep.

6.8.2. Watchdog

The purpose of watchdog is to monitor system's operation normally. Within a certain period, watchdog must be cleared. It protects the system from incorrect code execution by generating a system reset when software fails to clear watchdog flag within around 0.67 seconds.

6.9. Speech and Push-Pull

GPCD2T020A uses two 14-bit software channels with noise filter is also supported. There is one 14-bit PUSH-PULL driver for direct audio output.

6.10. Comparator

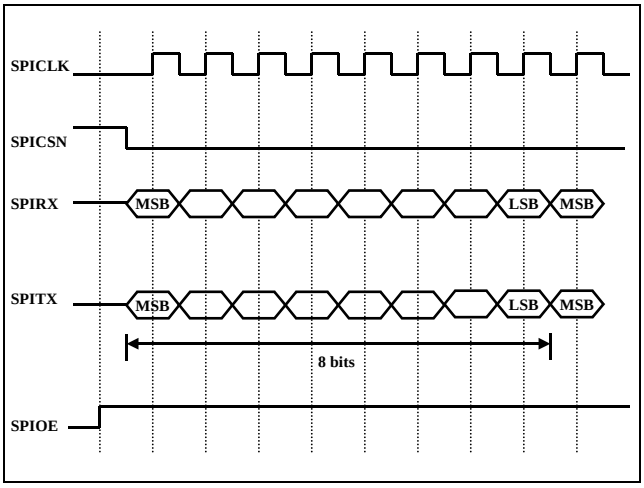
A set of comparator is embedded in GPCD2T020A. Users can using the comparator to sample specific signal.

6.11. Capacitive Touch Sensor (CTS) and CTS Timers

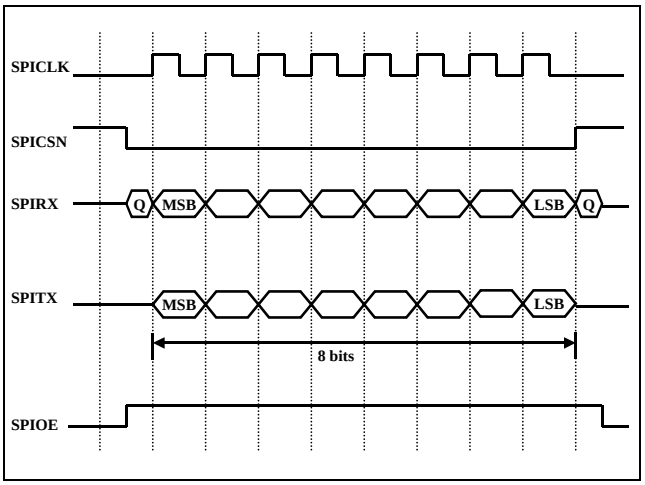
GPCD2T020A provides hardware Capacitive Touch Sensor. It is provided that the ability to perform capacitive sensing, decision making, responsive actions and other duties pertinent to the system as well.

6.12. SPI Controller

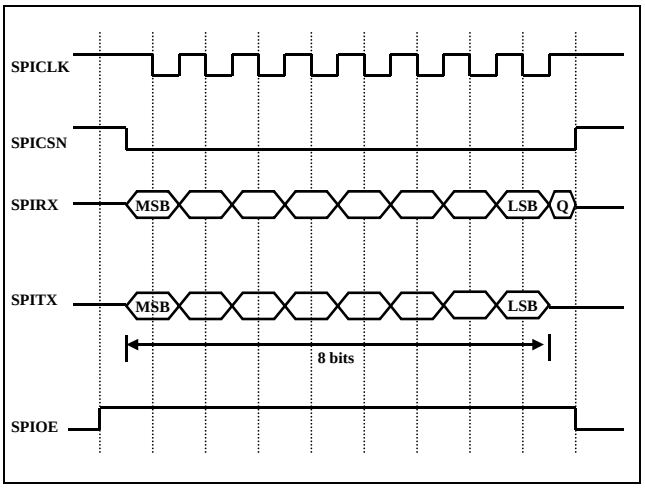
A Serial Peripheral Interface (SPI) controller is built-in GPCD2T020A to facilitate communicating with other devices and components. There are four control signals on SPI including SPITX(SDO), and SPIRX(SDI), SPICLK(SCK) and SPICSN; the four signals are shared with PortA3, PorA2, PortA1 and PortA0 or PortB7, PortB6, PortB5 and PortB4. While SPI module is enabled by corresponding control bit. These four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are supported as follows:



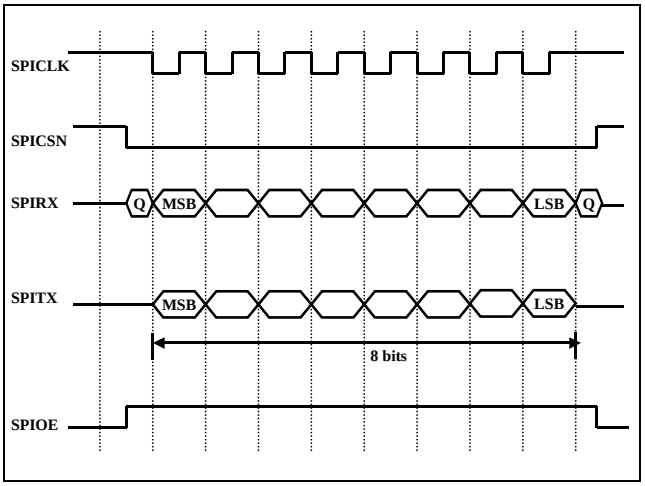
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0



Master Mode, SPO = 1, SPH=1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

7.2. DC Characteristics (VDDIO/VDD_RGI=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	3.0	3.6	V	For 2-battery
Operating Current-1	I_{OP1}	-	8	11	mA	VDDIO/AVDD /VDD_RGI=3.0V F_{CPU} = 8MHz , PWM on, no load
Operating Current-2	I_{OP2}	-	6	8	mA	VDDIO/AVDD /VDD_RGI=3.0V F_{CPU} = 8MHz , PWM off, no load
Standby Current	I_{STBY}	-	-	7	μA	VDDIO/AVDD/VDD_RGI=3.0V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDDIO/AVDD/VDD_RGI=3.0V
Input High Level-1	V_{IH}	0.7*VDDIO	-	-	V	With Schmitt trigger
Input Low Level-1	V_{IL}	-	-	0.3*VDDIO	V	With Schmitt trigger
Input High Level-2	V_{IH}	0.6*VDDIO	-	-	V	Without Schmitt trigger
Input Low Level-2	V_{IL}	-	-	0.4*VDDIO	V	Without Schmitt trigger
Output High Current (IOA/B, IOD[7:4])	I_{OH}	3.5	5	6.5	mA	VDDIO/AVDD/VDD_RGI=3.0V, V_{OH} =2.1V
Output Low Sink Current (IOA/B[7:4])	I_{OL1}	7	10	13	mA	VDDIO/AVDD/VDD_RGI=3.0V, V_{OL} =0.9V
Output Low Sink Current (IOA/B[3:0], IOD[7:4])	I_{OL2}	10	20	30	mA	VDDIO/AVDD/VDD_RGI=3.0V, V_{OL} =0.9V
Input Pull-Low Resistor-1 (IOA/B, IOD[7:4])	R_{PL}	550	800	1100	Kohm	VDDIO/AVDD/VDD_RGI=3.0V, Vin=3.0V
Input Pull-Low Resistor-2 (IOA/B, IOD[7:4])	R_{PL}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=3.0V, Vin=3.0V
Input Pull-High Resistor (IOA/B, IOD[7:4])	R_{PH}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=3.0V, Vin=VSS
IROSC16M Frequency deviation for chip (lot deviation) *	F_{I16M}	-1	-	+1	%	VDDIO/AVDD/VDD_RGI=3.0V
IROSC16M Frequency deviation for LQFP48	$F_{I16M\text{-}LQFP48}$	-3	-	+3	%	VDDIO/AVDD/VDD_RGI=3.0V
EROSC16M Frequency deviation(lot deviation)	F_{E16M}	-7	-	+7	%	VDDIO/AVDD/VDD_RGI=3.0V

***Note:** IROSC16M Frequency deviation is without epoxy on chip.

7.3. DC Characteristics (VDDIO/VDD_RGI=4.5V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	4.5	5.5	V	For 3-battery
Operating Current-1	I_{OP1}	-	11	15	mA	VDDIO/AVDD/VDD_RGI=4.5V F_{CPU} = 8MHz , PWM on, no load
Operating Current-2	I_{OP2}	-	7	10	mA	VDDIO/AVDD/VDD_RGI=4.5V F_{CPU} = 8MHz , PWM off, no load
Standby Current	I_{STBY}	-	-	7	μA	VDDIO/AVDD/VDD_RGI=4.5V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDDIO/AVDD/VDD_RGI=4.5V
Input High Level-1	V_{IH}	0.7*VDD	-	-	V	With Schmitt trigger
Input Low Level-1	V_{IL}	-	-	0.3*VDD	V	With Schmitt trigger
Input High Level-2	V_{IH}	0.6*VDD	-	-	V	Without Schmitt trigger
Input Low Level-2	V_{IL}	-	-	0.4*VDD	V	Without Schmitt trigger
Output High Current (IOA/B, IOD[7:4])	I_{OH}	7	10	13	mA	VDDIO/AVDD/VDD_RGI=4.5V, V_{OH} =3.15V
Output Low Sink Current (IOA/B[7:4])	I_{OL1}	14	20	26	mA	VDDIO/AVDD/VDD_RGI=4.5V, V_{OL} =1.35V
Output Low Sink Current (IOA/B[3:0], IOD[7:4])	I_{OL2}	20	40	60	mA	VDDIO/AVDD/VDD_RGI=4.5V, V_{OL} =1.35V
Input Pull-Low Resistor-1 (IOA/B, IOD[7:4])	R_{PL}	550	800	1100	Kohm	VDDIO/AVDD/VDD_RGI=4.5V, Vin=4.5V
Input Pull-Low Resistor-2 (IOA/B, IOD[7:4])	R_{PL}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=4.5V, Vin=4.5V
Input Pull-High Resistor (IOA/B, IOD[7:4])	R_{PH}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=4.5V, Vin=VSS
IROSC16M Frequency deviation for chip (lot deviation)*	F_{I16M}	-1	-	+1	%	VDDIO/AVDD/VDD_RGI=4.5V
IROSC16M Frequency deviation for LQFP48	$F_{I16M-LQFP48}$	-3	-	+3	%	VDDIO/AVDD/VDD_RGI=4.5V
EROSC16M Frequency deviation(lot deviation)	F_{E16M}	-7	-	+7	%	VDDIO/AVDD/VDD_RGI=4.5V

***Note:** IROSC16M Frequency deviation is without epoxy on chip.

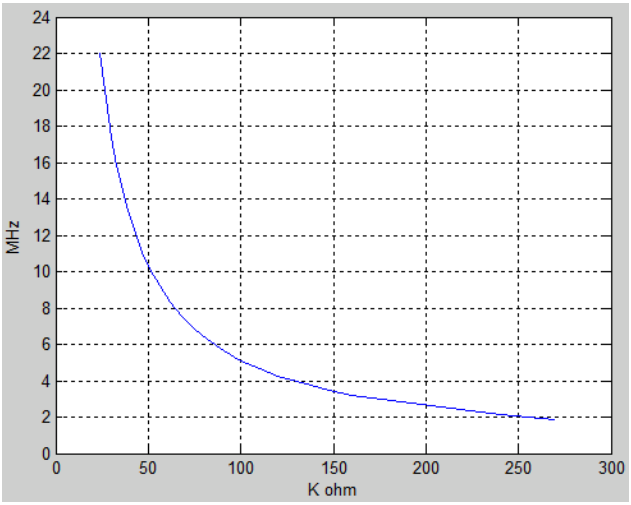
7.4. DAC Characteristics (VDDIO/VDD_RGI/AVDD =4.5V, R_L=8Ω, f=1KHz, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n(5V@0.7W)	--	-	1	-	%
Noise at No Signal	-	-	-100	-	dBr A
Dynamic Range (-60dB)	-	-	-80	-	dBr A

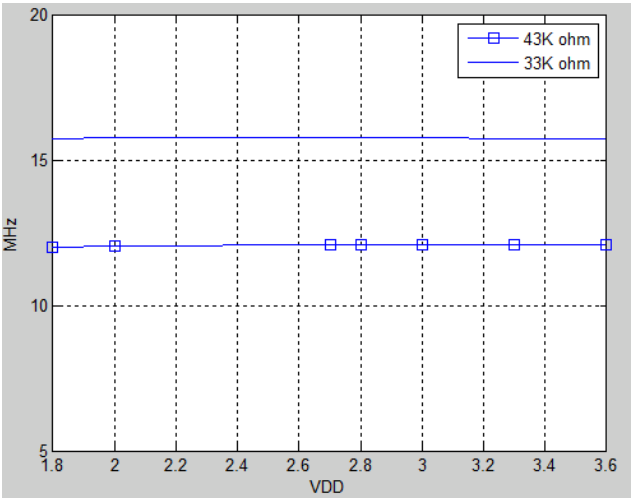
7.5. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VREGI	2.1	-	5.5	V	
Maximum Current Output	IREGO	-	-	40	mA	VDD_RGI (Regulator in)= 4.5V,△VDD (Regulator out) <100mV
Output Voltage	V3_REGO	3.14	3.3	3.47	V	VDD_RGI > 3.5V and V3_REGO is 3.3V
Standby Current	IREGS	-	2.5	-	uA	

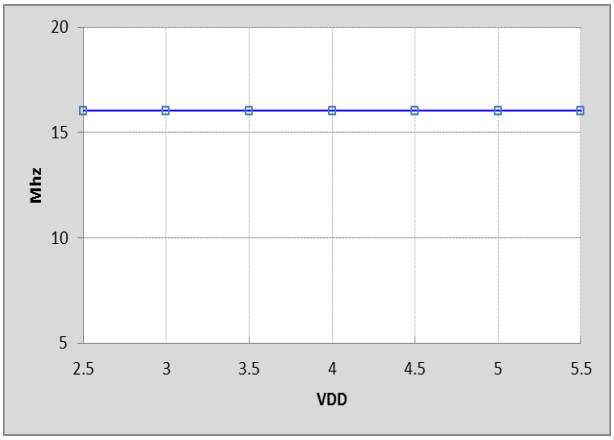
7.6. The EROSC Relationship between R_{OSC} and F_{OSC} (TA=25℃)



7.7. The EROSC Relationship between VDD and F_{OSC} (TA=25℃)

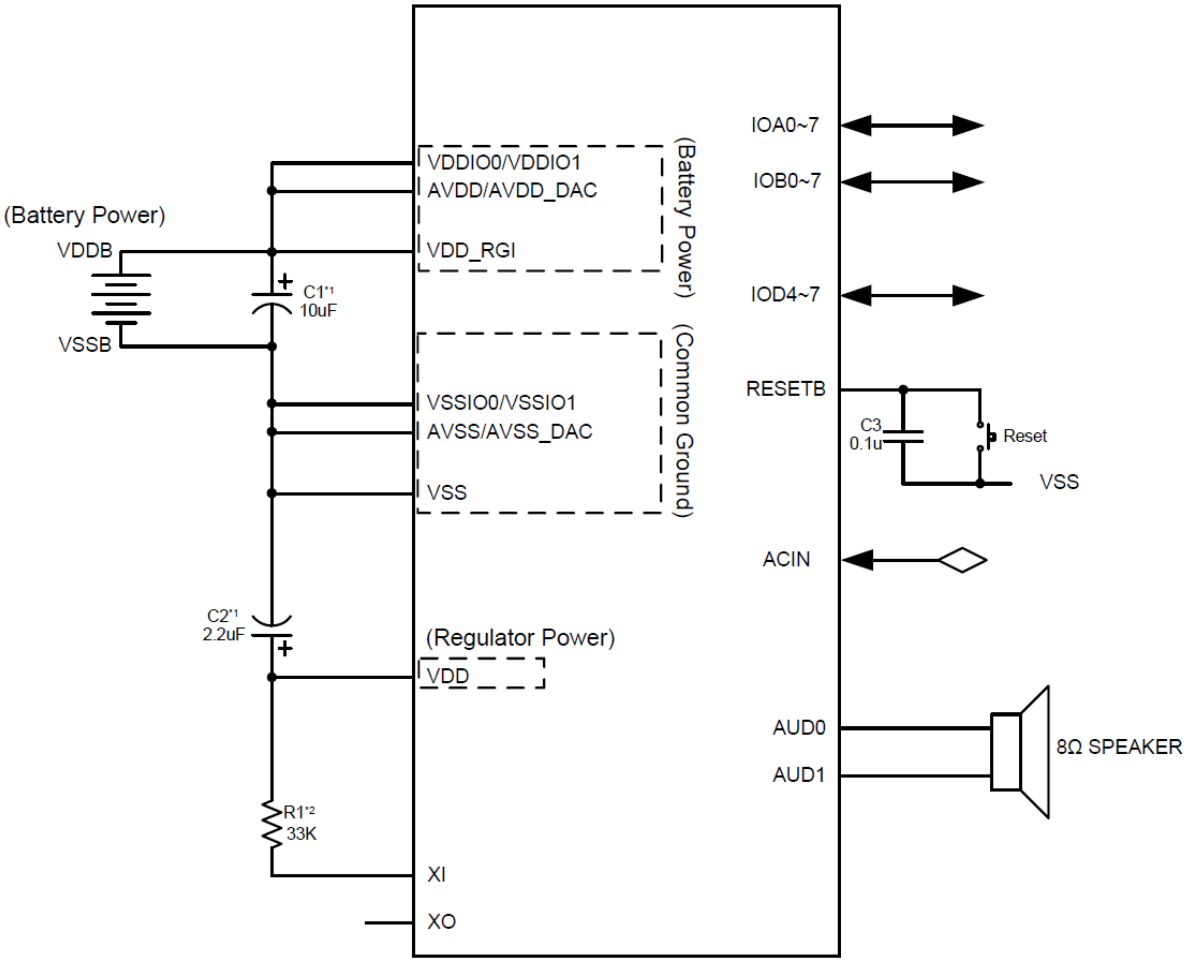


7.8. The IROSC Relationship between VDD and F_{OSC} (TA=25℃)



8. APPLICATION CIRCUITS

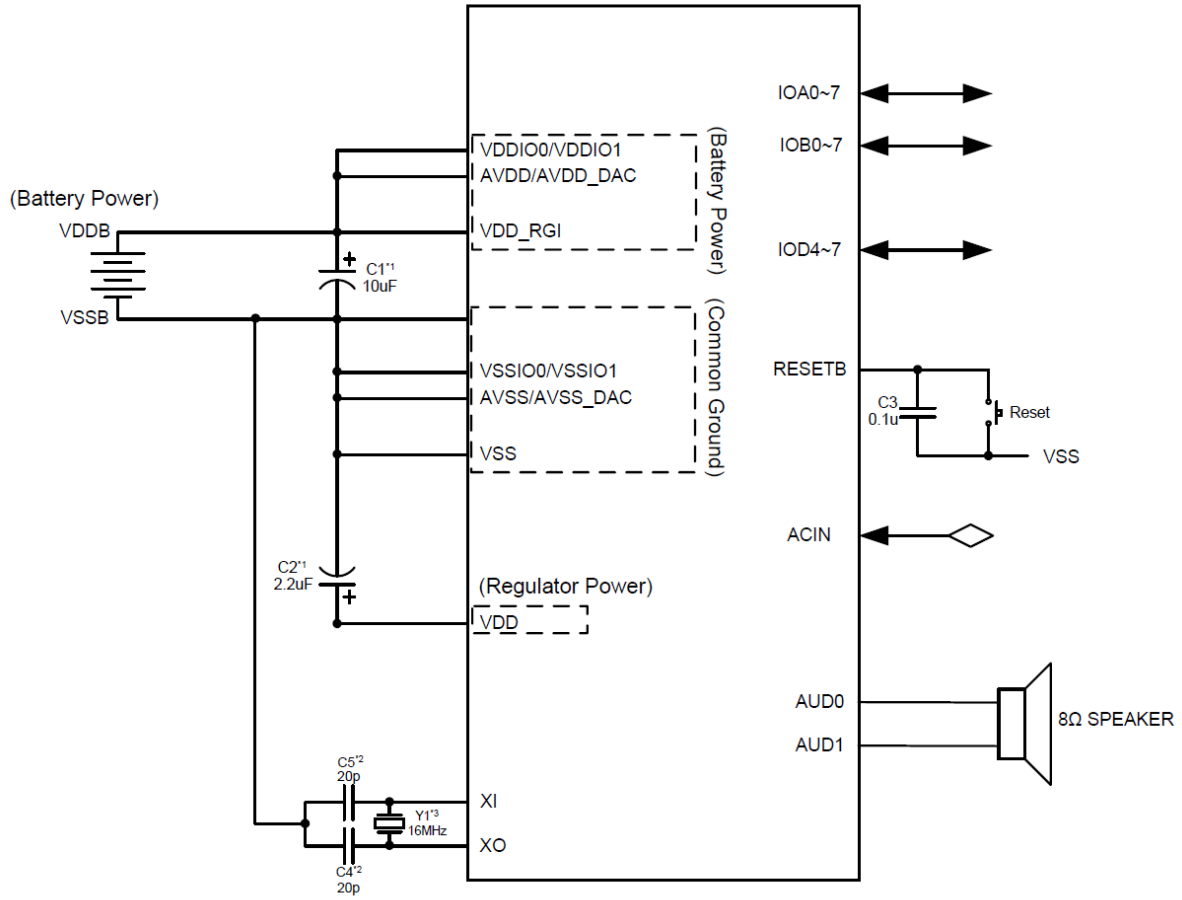
8.1. GPCD2T020A Application Circuit with External ROSC Mode (R_{OSC}-mode)



Note*1: These capacitor values are for design guidance only. Adding 10uF and 0.1uF capacitors in parallel to each power group are recommended for noise sensitive application. The recommended features are ESR=0.05~1Ω

Note*2: R1=33K ohm for 16MHz clock and R1=43K ohm for 12MHz clock.

8.2. GPCD2T020A Application Circuit with 16MHz X'tal (XTAL-mode)

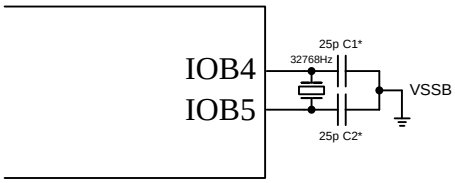


Note*1: These capacitor values are for design guidance only. Adding 10uF and 0.1uF capacitors in parallel to each power group are recommended for noise sensitive application. The recommended features are ESR=0.05~1Ω

Note*2: These capacitor values are for design guidance only. The recommended features are ESR=11.2~60K and C4=C5=18~28pF (including PCB parasitic loading, for example, user should apply additional 12~22pF on XI and XO if PCB parasitic loading is 6pF)

Note*3: 16MHz X'tal or 12Mhz X'tal can be used for different speed applications.

8.3. GPCD2T020A 32K X'tal Application Circuit



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and C1=C2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPCD2T020A-NnnV-C	Chip form
GPCD2T020A-NnnV-QL23x	Green Package – LQFP48
GPCD2T020A-NnnV-HS03x	Green Package – SOP16

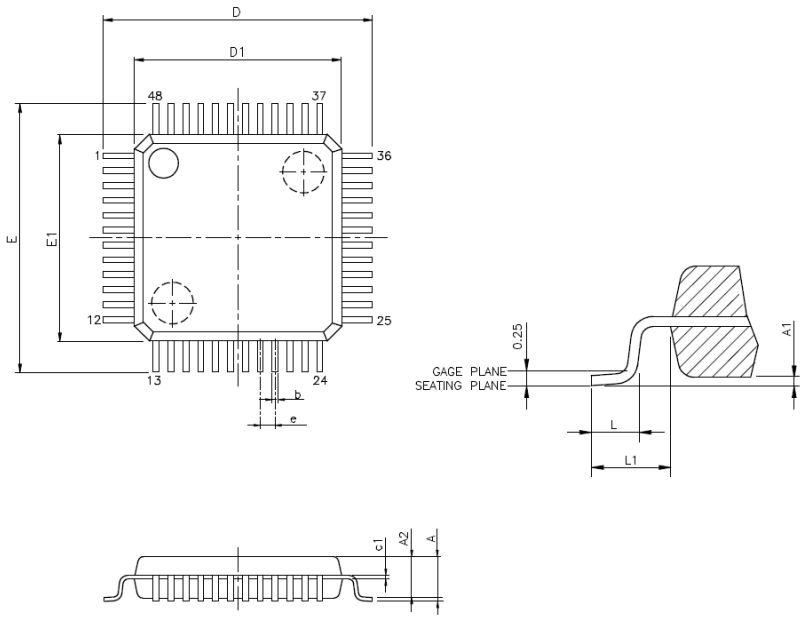
Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

9.2. Package Information

9.2.1. LQFP 48



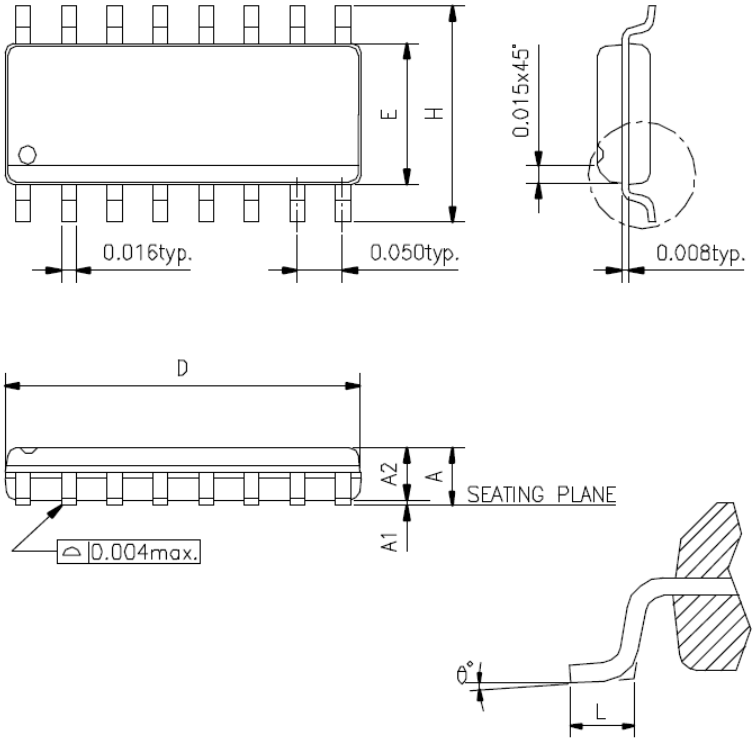
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

9.2.2. SOP 16



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-012 AC
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
Nov. 16, 2018	1.1	Modify Package SOP-16 information.	11,13
May 17, 2018	1.0	Original	26