TOSHIBA Bi-CMOS
Constant Current Interface Driver

TB62708N

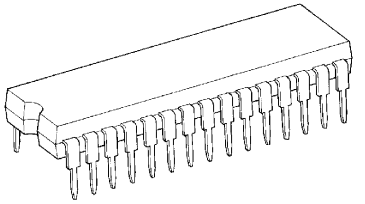
16 Bit Constant Current LED Source Driver with Shift Register and Latch Functions

Product Description:

The TB62708N is specifically designed for LED display applications. The Bi-CMOS device has 16 Bi-polar constant current output source channels and includes CMOS shift register and latch functions.

The LED drive current is programmed by the installation of a single resistor per device. Current is programmable from 5-90mA and is held constant across all 16 source outputs effectively compensating for the inherent circuit and component variables which affect the brightness of the LEDs.

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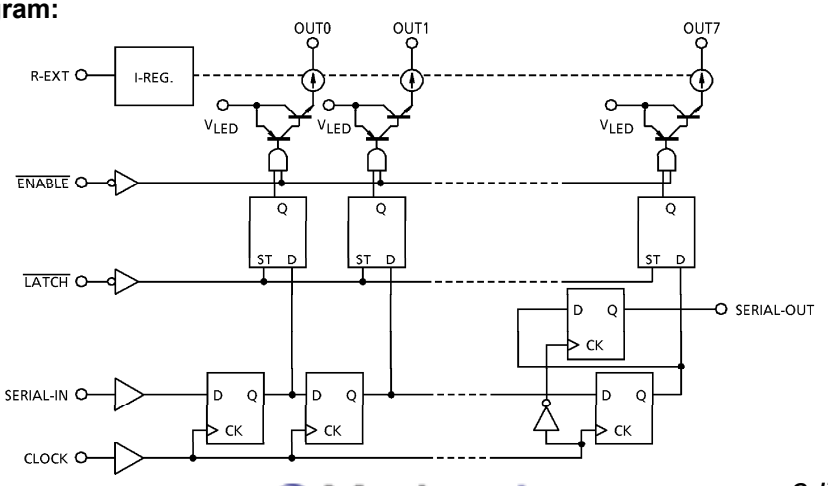


SDIP30-P-400

Features:

- Current Source Device
- 16 Constant Current Output Channels
- Current Programmable from 5-90mA
- 5V CMOS Compatible Inputs
- 15MHz Max Clock Frequency (Cascade)

Block Diagram:



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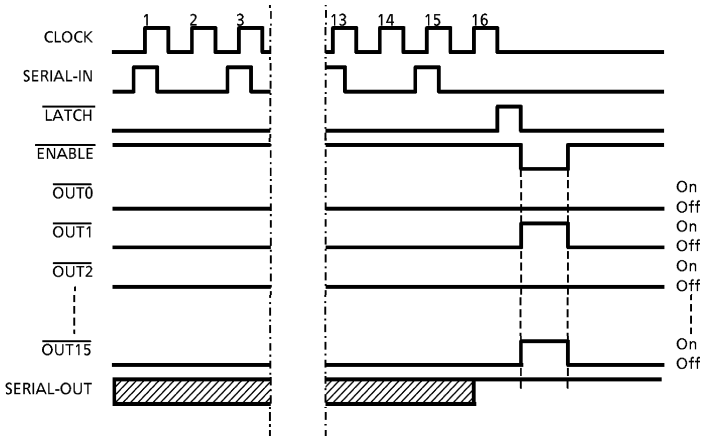
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Timing Diagram:



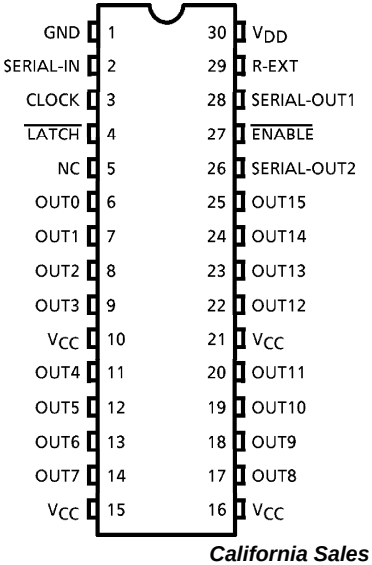
Latches are:

1. Level Sesitive
2. Not edge sensitive
3. Not clock synchronous
4. Passing Data when $\overline{\text{LATCH}}$ is H
5. Hold Data when $\overline{\text{LATCH}}$ is L

All Outputs are OFF when $\overline{\text{ENABLE}}$ is H and ON when $\overline{\text{ENABLE}}$ is L.

Terminal Description & Pin Out:

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal
2	SERIAL-IN	Serial Data Input terminal
3	CLOCK	Clock Input terminal
4	$\overline{\text{LATCH}}$	Latch Input Terminal
6~9,11~14, 17~20,22~25	OUT0~15	Output terminals
27	$\overline{\text{ENABLE}}$	Output Enable Input Terminal
28	SERIAL-OUT	Serial Data Out Terminal
29	R-EXT	Constant Current Programming
30	VDD	5V Supply voltage terminal
10,15,16,21	VLED	0~17V Supply voltage terminal for LED



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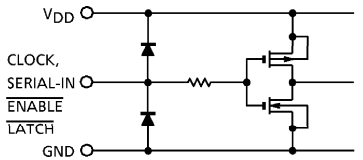
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Truth Table:

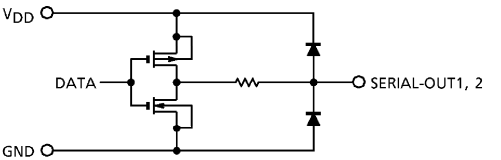
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	OUT0	OUT7	OUT15	SERIAL-OUT2
UP	H	L	Dn	Dn	Dn-7	Dn-15	Dn-16
DOWN	H	L	Dn	Dn	Dn-7	Dn-15	Dn-15
UP	L	L	Dn+1	No Change (data hold)			No Change
DOWN	L	L	Dn+1	No Change (data hold)			Dn-14
No Edge	H	L	Dn+1	Dn +1	Dn-6	Dn-14	No Change
No Edge	X	H	Dn+1	Off			No Change

Equivalent Circuit of Inputs and Outputs:

1. $\overline{\text{ENABLE}}$, $\overline{\text{LATCH}}$, CLOCK & SERIAL-IN terminal



2. SERIAL-OUT terminal



Maximum Ratings:

CHARACTER	SYMBOL	RATING	UNIT
Supply Voltage	VDD	+7.0	V
Supply Voltage for LED	VCC	+17.0	V
Output Voltage	VCE	-0.4~+17.0	V
Output Current	IOUT	-90	mA
Input Voltage	VIN	-0.4~VDD + 0.4	V
GND Terminal Current	IGND	1440	mA
Clock Frequency	FCLK	15	MHz
Power Dissipation	PD	2.08 (ON PCB,Ta=25°C) 1.56 (FREE AIR, Ta=25°C)	W
Operating Temperature	Topr	-40~+85	°C
Storage Temperature	Tstg	-55~+150	°C

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Recommended Operating Condition:

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD		4.5	5.0	5.5	V
Supply Voltage for LED	VCC		—	—	17	V
Outout Voltage	VOUT		—	—	-17	V
Output Current	IOUT	DC 1 Circuit	-5	—	-78	mA
	IOH	SERIAL-OUT	—	—	1.0	mA
	IOL	SERIAL-OUT	—	—	-1.0	mA
Input Voltage	VIH		0.7VDD	—	VDD+0.3	V
	VIL		-0.3	—	0.3VDD	V
$\overline{\text{LATCH}}$ Pulse Width	tw LAT	VDD=4.5 ~ 5.5V	100	—	—	ns
CLOCK Pulse Width	tw CLK		50	—	—	ns
$\overline{\text{ENABLE}}$ Pulse Width	tw EN		1000	—	—	ns
Set-up Time	tsetup(D)		50	—	—	ns
Hold Time	thold(D)		30	—	—	ns
Clock Frequency	FCLK	Cascade Operation	—	—	10.0	MHz
Power Dissipation	PD	ON PCB, Ta=85°C	—	—	1.08	W

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Electrical Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	VIH	—	—	0.7VDD	—	VDD	V
	"L" level	VIL	—	—	GND	—	0.3VDD	
Output Leakage Current		I LEAK	—	VLED=17.0V	—	—	-10	μA
Output Voltage	SERIAL-OUT	VOL	—	IOL=+1.0mA	—	—	0.4	V
		VOH		IOH=-1.0mA	4.6	—	—	V
Output Current 1		IOL1	—	V_{OUT}=VCC-2 REXT=360Ω	-66.3	-78	-89.7	mA
	Current Skew	ΔIOL1	—	V_{OUT}=VCC-2 REXT=360Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / VDD	—	REXT=360Ω Ta=-40~+85°C	—	1.5	5.0	% /V
Supply Current		IDD (off) 1	—	REXT=OPEN OUT0~15=off	—	0.6	1.2	mA
		IDD (on)	—	REXT=360Ω, DATA="H"OUT0~15=on	—	10.0	15.0	
		ICC(off)	—	REXT=360Ω, ALL DATA="L" OUT0~15=off	—	1	2	
		ICC(on)	—	REXT=360Ω, ALL DATA="H" OUT0~15=on	—	1260	—	

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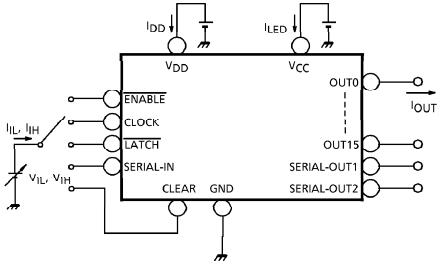
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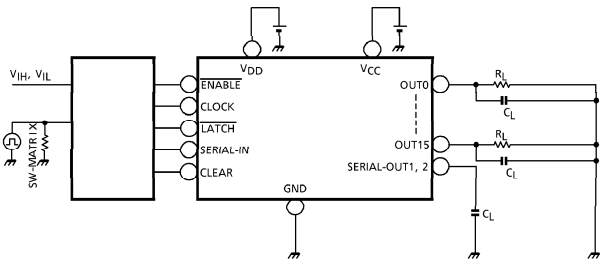
Switching Characteristics:

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK-SOUT	tpLH	{CLK,LATCH & ENABLE to tpLH & tpHL : 50% to 50%} VDD = 5.0V,VCC=17.0V VOUT=VCC-2.0V VIH = VDD VIL = GND REXT = 360Ω RL = 300Ω	—	30	70	ns
	CLK-OUTn			—	200	500	
	$\overline{\text{LATCH}}$-OUTn			—	200	500	
	$\overline{\text{ENABLE}}$-OUTn			—	200	500	
Propagation Delay Time ("H" to "L")	CLK-OUTn	tpHL		—	200	500	ns
	$\overline{\text{LATCH}}$-OUTn			—	200	500	
	$\overline{\text{ENABLE}}$-OUTn			—	200	500	
	CLK-SOUT			—	30	70	
Pulse Width	CLK	tw CLK,CLK		—	20	30	ns
	LATCH	tw LAT,LAT		—	10	25	
$\overline{\text{Latch}}$ Set Up Time		tsetup LAT		—	25	50	ns
$\overline{\text{Latch}}$ Hold Time		thold LAT		—	0	15	ns
Maximum Clock Rise Time		tr		—	—	10	μs
Maximum Clock Fall Time		tf		—	—	10	
Maximum Output Rise Time		tor		150	300	600	ns
Maximum Output Fall Time		tof		150	300	600	ns

DC Characteristic Test Circuit:



AC Characteristic Test Circuit:



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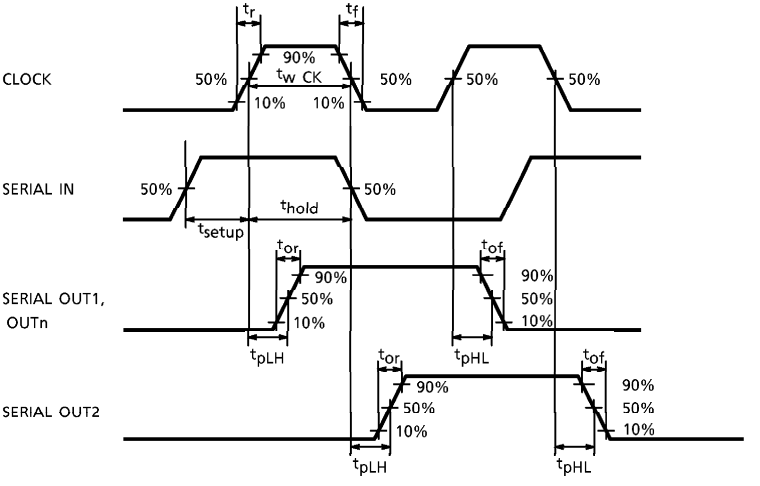
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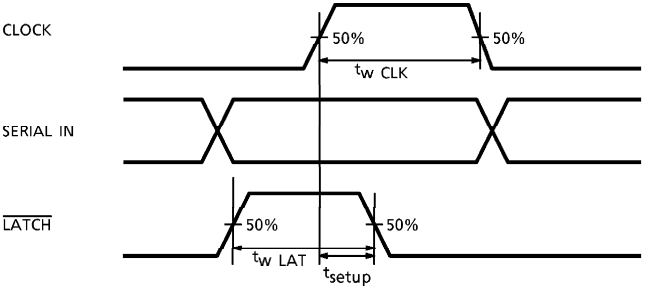
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Timing Wave Form:

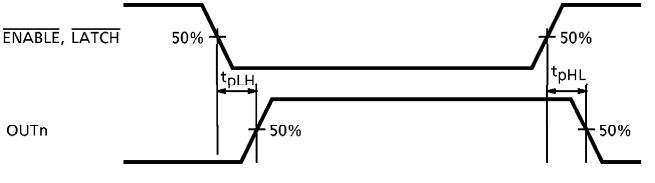
1. CLOCK-SERIAL OUT, OUTn



2. CLOCK-$\overline{\text{LATCH}}$



3. $\overline{\text{ENABLE}}$, $\overline{\text{LATCH}}$-OUTn



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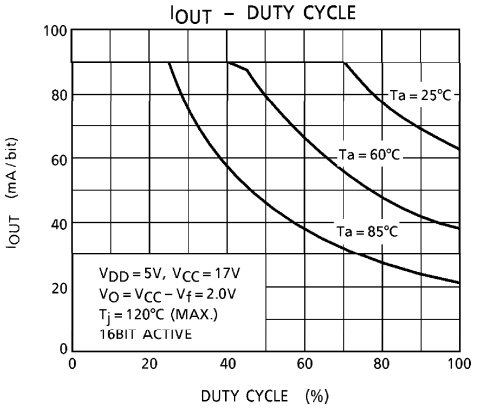
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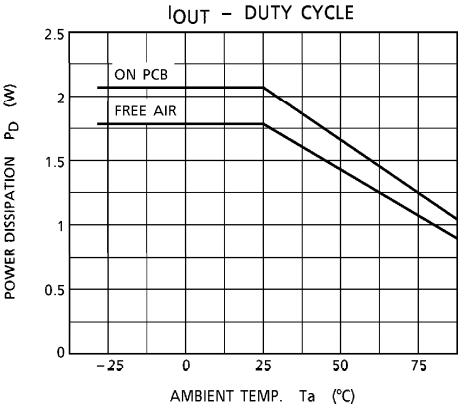
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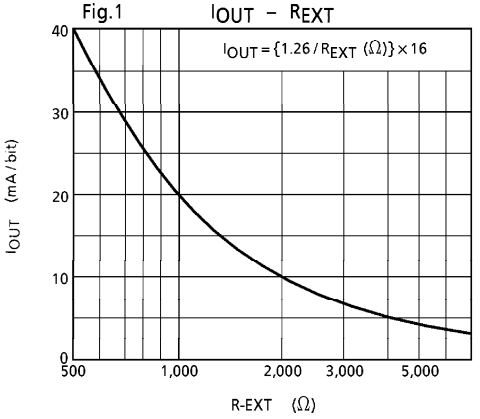
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Graphs:





Current Programming Resistor Selection::



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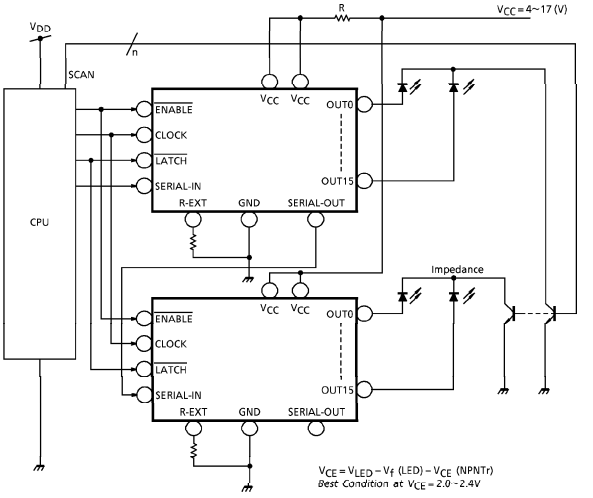
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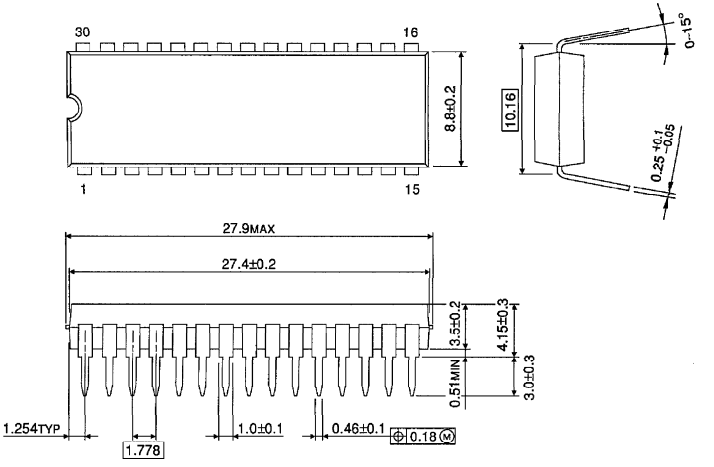
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Application Circuit:



Outline Drawing:

SDIP30-P-400-1.78 Unit : mm



Weight : 1.99g (Typ.)

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