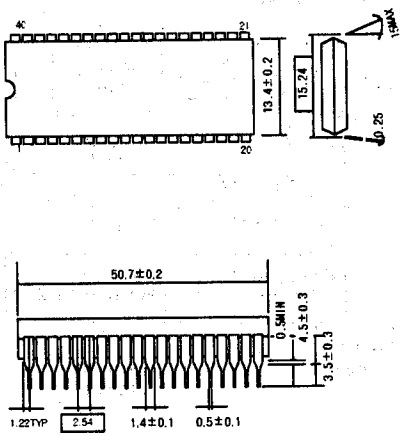
CMOS SINGLE-COMPONENT
8-BIT KEYBOARD CONTROLLER

40 DIP UNIT : mm



☐ FEATURES

- O 8 bit CPU optimized for control applications
- O 4K bytes of ROM / 128 bytes of SRAM
- O Two 16bit Timer/Counters
- O 34 Programmable Bi-directional I/O pins
- O 3 LED direct sink pins with internal serial resister
- O Mask optional for built-in either RC Oscillator with External resistor applied or ceramic resonator applied
- O Watch-dog Timer
- O Built-in power on reset
- O Built-in low voltage reset
- O 5 interrupt sources
- O 2 Level Programmable serial port
- O Power control modes
- O CMOS technology for low power consumption
- O 0.5 to 12MHz@ 5V±10%

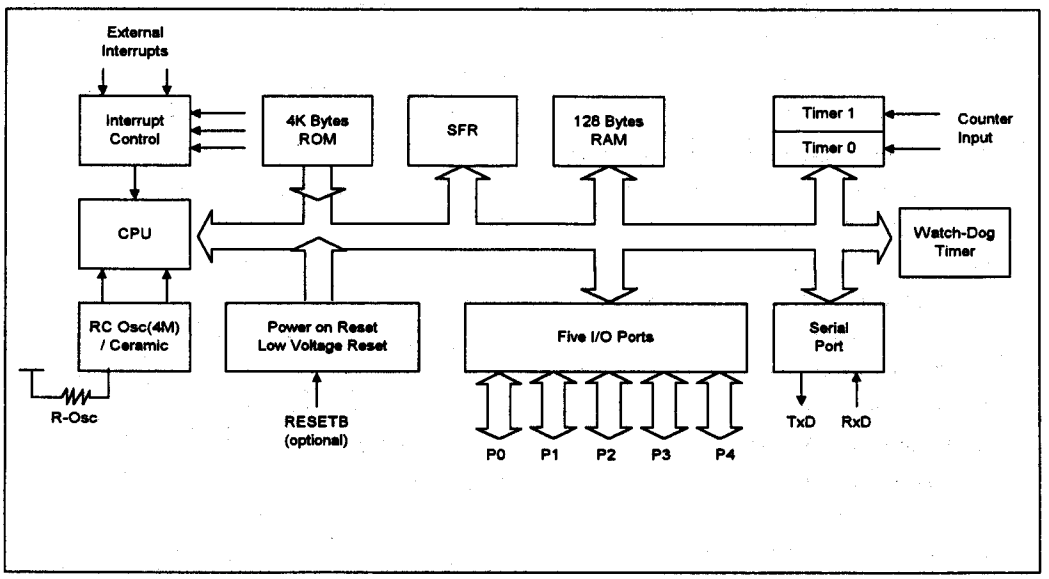
☐ Absolute Maximum Ratings*

- O DC Supply Voltage : -0.3V to +7.0V
- O Input / Output Voltage : GND - 0.2V to V_{DD} + 0.2V
- O Operating Ambient Temperature : 0℃ to +70℃
- O Storage temperature : -55℃ to +125℃
- O Operating Voltage (V_{DD}) : +4.5V to +5.5V

* Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☐ BLOCK DIAGRAM



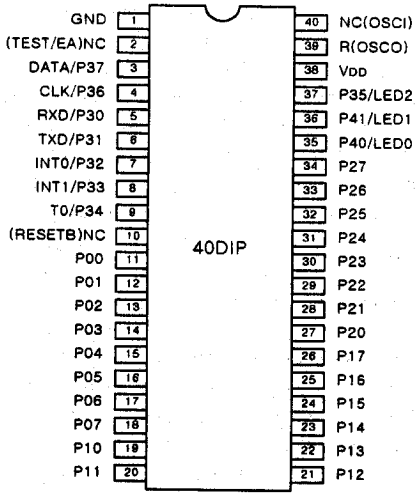
☐ DESCRIPTION

The DMC60C68A is a high-performance micro controller fabricated with DAEWOO high-density CMOS technology. The DAEWOO CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS.

It contains basic function of Intel's 80C51 , which consists of a 4K×8ROM, a 128×8RAM, 32 I/O lines, two 16bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communication, I/O expansion or full duplex UART, and extended function of a on-chip RC oscillator, a 16bit Watch-dog counter, a Power-on reset with Low voltage reset, and a two more I/O lines.

In addition, the device has two software selectable modes of power reduction idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, and interrupt system to continue functioning.

☐ PIN CONFIGURATION :



☐ DC Electrical Characteristics (Vdd=5V, GND=0V, T_A=25℃, Fosc=4MHz,unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply Current	I_{CC}			20	mA	No load
Input High Voltage	V_{IH}	2			V	
Input Low Voltage	V_{IL}			0.8	V	
Output High Voltage (Port0,1,2,P30~P34)	V_{OH1}	2.4			V	I_{OH} = -100 μA
Output High Voltage(P36,P37)	V_{OH2}	2.4			V	I_{OH} = -400 μA
Output Low Voltage(Port0,1,2)	V_{OL1}			0.4	V	I_{OL} = 4 mA
Output Low Voltage(P30~P34)	V_{OL2}			0.4	V	I_{OL} = 5 mA
Output Low Voltage(P36,P37)	V_{OL3}			0.4	V	I_{OL} = 10 mA
Initial Frequency Variation 1	△F/F			+/-10	%	For RC OSC only
Frequency Variation 2	△F/F			+/-1	%	For ceramic resonator only
Sink Current(P35,P40,P41)	I_{LED}	10	14	17	mA	V_{OL} = 3.2V
Low Voltage Reset Threshold	V_{LVR}		3.5		V	
Power On Reset Time	T_{POR}		50		μs	RC OSC only
RESETB Pull High Resister	R_{PH}		220		Kohm	

☐ PIN Descriptions

Pin No	Designation	I/O	Description
1	GND	P	Ground pin
2	NC(TEST/EA)	-	No connection, recommended to connect V_{DD} or floating
3	P37/DATA	I/O	Bi-directional I/O pin, 10K ohm pull-up resistor for communication
4	P36/CLK	I/O	Bi-directional I/O pin, 10K ohm pull-up resistor for communication
5	P30/RxD	I/O	Bi-directional I/O pin with serial input function , 40K ohm pull-up
6	P31/TxD	I/O	Bi-directional I/O pin with serial output function , 40K ohm pull-up
7	P32/INT0	I/O	Bi-directional I/O pin with external interrupt 0 function , 40K ohm pull-up
8	P33/INT1	I/O	Bi-directional I/O pin with external interrupt 1 function , 40K ohm pull-up
9	P34/T0	I/O	Bi-directional I/O pin with timer0 external input function , 40K ohm pull-up
10	NC(RESETB)	I	RESETB signal input pin with pull up resistor internally, Active low
11	P00	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
12	P01	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
13	P02	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
14	P03	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
15	P04	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
16	P05	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
17	P06	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
18	P07	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
19	P10	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
20	P11	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
21	P12	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
22	P13	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
23	P14	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
24	P15	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
25	P16	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
26	P17	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
27	P20	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
28	P21	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
29	P22	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
30	P23	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
31	P24	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
32	P25	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
33	P26	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
34	P27	I/O	Bi-directional I/O pin with 40K ohm internal pull-up resistor
35	P40/LED0	I/O	I/O pin, LED direct sink possible when use to do output port
36	P41/LED1	I/O	I/O pin, LED direct sink possible when use to do output port
37	P35/LED2 /T1	I/O	I/O pin, LED direct sink possible when use to do output port Bi-directional I/O pin with timer1 external input function , 40K ohm pull-up
38	VDD	P	Power supply pin
39	R(OSCO)	I	47kohm resistor connected for RC OSC or ceramic resonator connected
40	NC(OSCI)	I	No connection for RC OSC or ceramic resonator connected

☐ SFR(Special Function Register) Memory Map

8 Bytes

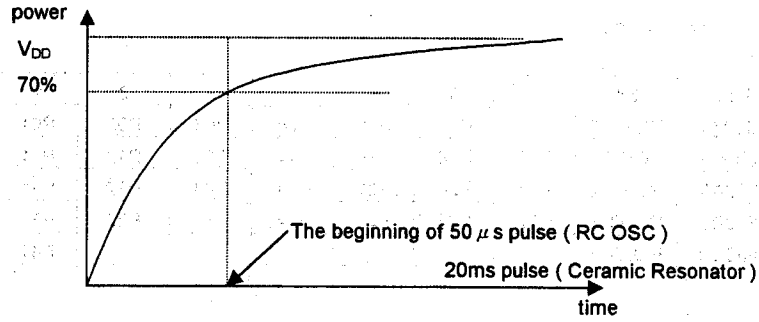
F8								FF
F0	B							F7
E8								EF
E0	ACC							E7
D8								DF
D0	PSW							D7
C8								CF
C0	P4*							CLRWDT* C7
B8	IP							BF
B0	P3							B7
A8	IE							AF
A0	P2							A7
98	SCON	SBUF						9F
90	P1							97
88	TCON	TMOD	TL0	TL1	TH0	TH1		8F
80	P0	SP	DPL	DPH				PCON 87

Bit Addressable

* Additional SFRs map to Intel's 80C51

☐ Power On Reset

In RC OSC option case, built-in power on reset circuit can generate an about 50 μs pulse to reset the entire chip. The beginning of the 50 μs pulse is on the reaching of 70% of VCC if powered on. In Ceramic Resonator case, power on reset can generate an about 20ms pulse with external capacitor (at least 0.1uF)



☐ I/O Ports

The DMC60C68A has 34pins dedicated to input & output. These pins are grouped into 5 ports, as follows:

PORT 0 (P00 ~ P07)

Port 0 is an 8-bit bi-directional CMOS I/O port that is internally pulled high by PMOS. Each pin of port 0 can be bit programmed as an input or output port under software control. When programmed as output, data is latched to the port data register and output to the pin. Port 0 pins with '1' written to them are pulled high by the internal PMOS pull-ups with 40K ohms, and can be used as inputs in that state. Then these input signals can be read. The port output high after reset.

PORT 1 (P10 ~ P17)

Functions the same as PORT 0.

PORT 2 (P20 ~ P27)

Functions the same as PORT 0.

PORT 3 (P30 ~ P37)

Functions the same as PORT 0. Especially P35 can be used for driving of LED without any external components in keyboard systems. And P36, P37 got the 10K ohm internal pull ups for using DATA and CLK communication in keyboard systems.

PORT 4 (P40 ~ P41)

Functions the same as PORT 0. It can be used for driving of LEDs without any external components in keyboard systems.

PORT Registers ;

Addr.	Bit	7	6	5	4	3	2	1	0	
$0080	PORT 0	P07	P06	P05	P04	P03	P02	P01	P00	(RW)
$0090	PORT 1	P17	P16	P15	P14	P13	P12	P11	P10	(RW)
$00A0	PORT 2	P27	P26	P25	P24	P23	P22	P21	P20	(RW)
$00B0	PORT 3	P37	P36	P35	P34	P33	P32	P31	P30	(RW)
$00C0	PORT 4							P41	P40	(RW)

☐ WATCH-DOG TIMER

The DMC60C68A implements a watch-dog timer, which process programs against system standstill. The clock of the watch-dog timer is derived from the on-chip RC oscillator. The watch-dog timer interval is about 0.195 of a second. The timer must be cleared within every 0.195 second during normal operation. Otherwise, it will overflow and cause a system reset. The watch-dog timer is cleared and enabled after a system reset. It cannot be disabled by software. The user can clear the watch-dog timer by writing #80H to CLRWDT ($00C7H) register.

For example :

MOV C7H, #80H

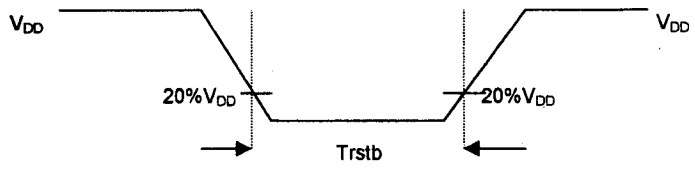
Addr.	Bit	7	6	5	4	3	2	1	0	
$00C7	CLRWDT	1	-	-	-	-	-	-	-	(W)

☐ Low Voltage Reset (LVR) Circuit

The DW-KBD IC will check on voltage level of power supply. When the voltage level of power supply is below a threshold of 3.5V(Typical), the LVRC will issue a reset output to the chip until the power voltage level above threshold voltage 3.5V(Typical) again. As soon as the power voltage arises to 3.5V(Typical), the entire chip will be reset for about 50 μs.

☐ RESETB

The DW-KBD IC can also be reset via RESETB pin externally. A reset is initiated when the signal at the RESETB pin is held Low for at least 24 system clock. When the DMC60C68A is in initial power on reset with ceramic resonator option, RESETB must keep the active state minimum 20msec. The following shows the definition of RESETB input low pulse width.



☐ IDLE MODE

In the Idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operating mode before Idle mode is activated.

The content of the on-chip RAM and all the Special Function Registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

☐ POWER DOWN MODE

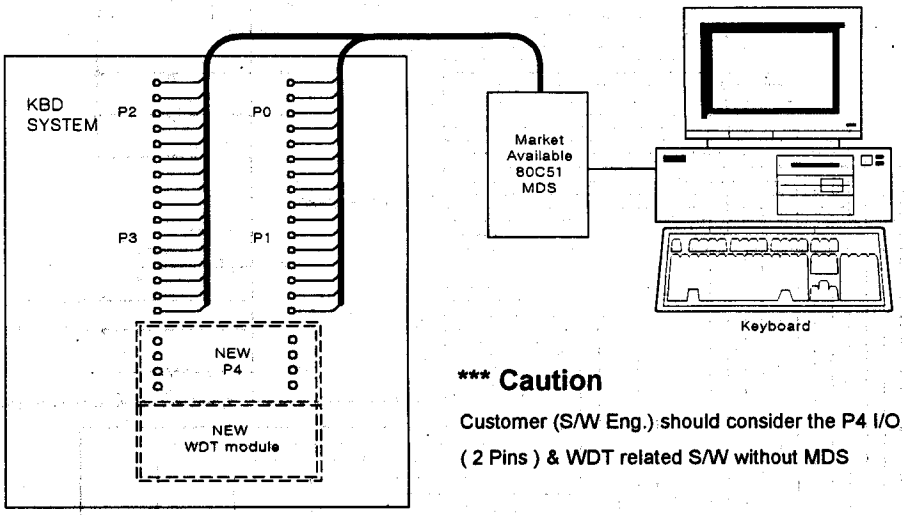
In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Register retain their values until the Power Down mode is terminated. The control bits for the reduced power modes are in the Special Function Register PCON.

CAUTION

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{DD} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

☐ System Development Method

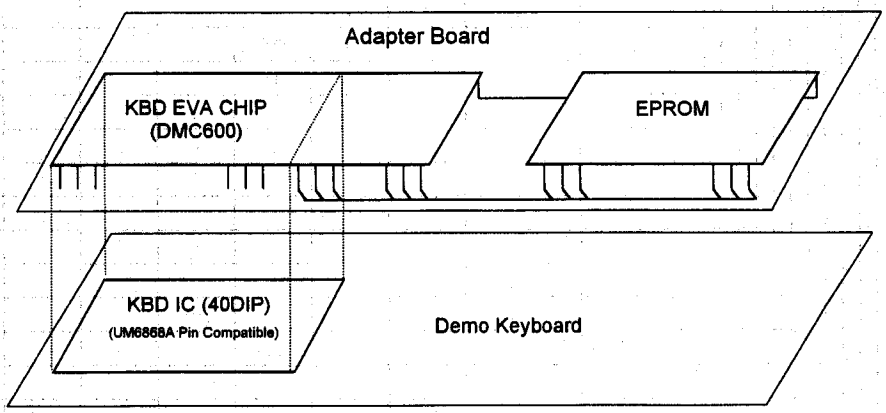
1. **First Stage** : S/W Development with traditional Intel 80C51 MDS



***** Caution**

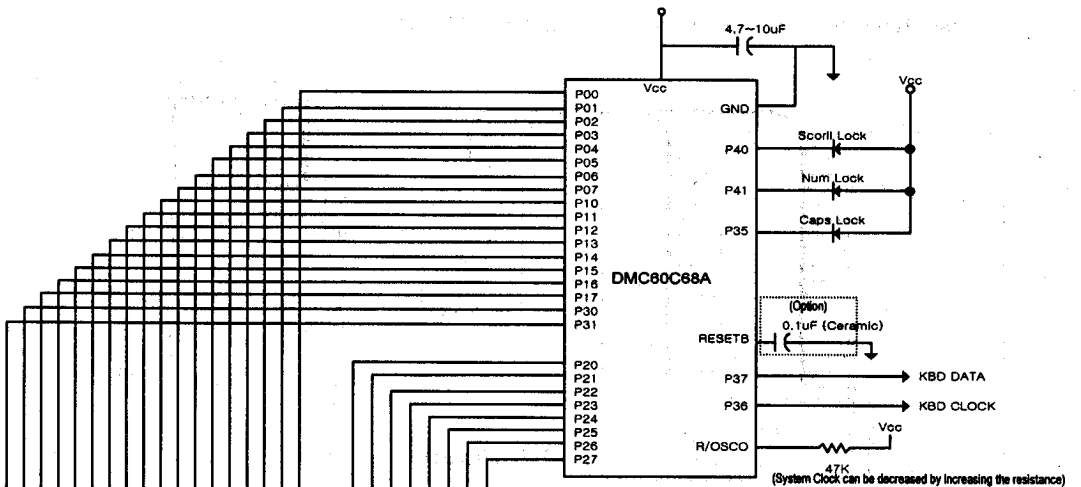
Customer (S/W Eng.) should consider the P4 I/O pin (2 Pins) & WDT related S/W without MDS

2. **Second Stage** : Target System Emulation with Adapter B/D which including EVA Chip and EPROM



3. **Third Stage** : Order DW KBD MICOM (DMC60C68A) with EPROM S/W

Application Circuit (for reference only)



	R0	R1	R2	R3	R4	R5	R6	R7
S0	Pause				(R) Ctrl		(L) Ctrl	F5
S1	Q	Tab	A	Esc	Z	K131	-	1
S2	W	Caps Lock	S	(K45) Macro	X	K132	F1	2
S3	E	F3	D	F4	C	K133	F2	3
S4	R	T	F	G	V	B	5	4
S5	U	Y	J	H	M	N	6	7
S6	I	]	K	F6	,	K56	=	8
S7	O	F7	L		.	APP	F8	9
S8	P	[	;	'	↑ (K42)	? /	-	0
S9	Scroll Lock			(L) Alt		(R) Alt		Print Screen
S10	K14	Back Space	↓ (K29)	F11	↵ Enter	F12	F9	F10
S11	7 Home	4 ←	1 End	Space	Num Lock	↓	Delete	
S12	8 ↑	5	2 ↓	0 Ins	/	→	Insert	
S13	9 PgUp	6 →	3 PgDn	Del	*	-	Page Up	Page Down
S14	*	K107	(R) Enter	↑		←	Home	End
S15		(L) Shift	(R) Shift					
S16		WINL						
S17			WINR					