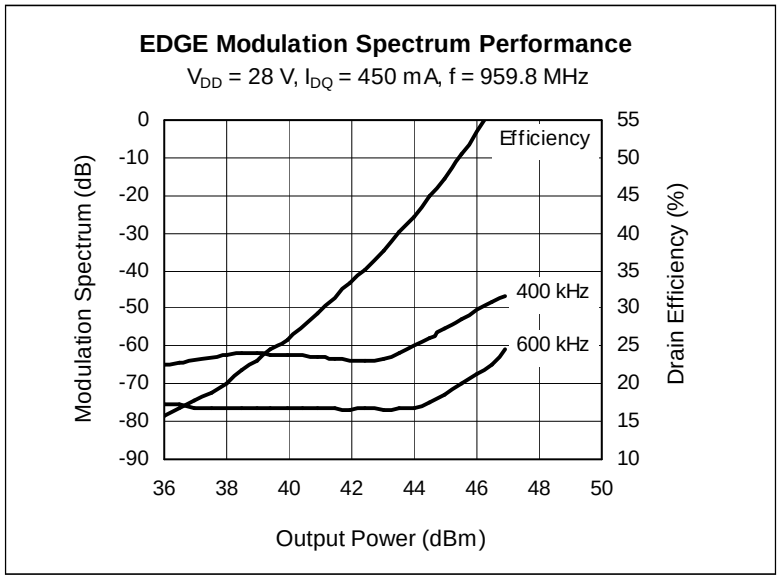
LDMOS RF Power Field Effect Transistor
45 W, 869–960 MHz

Description

The PTF080451 is a 45 W, internally matched *GOLDMOS* FET intended for EDGE and CDMA applications in the 860 to 960 MHz band. Full gold metallization ensures excellent device lifetime and reliability.



Features

- Broadband internal matching
- Typical EDGE performance
  - Average output power = 22.5 W
  - Gain = 18 dB
  - Efficiency = 40%
- Typical CW performance
  - Output power at P–1dB = 60 W
  - Gain = 17 dB
  - Efficiency = 60%
- Integrated ESD protection: Human Body Model, Class 1 (minimum)
- Excellent thermal stability
- Low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 45 W (CW) output power

PTF080451E
Package 30265

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics at T_{CASE} = 25°C unless otherwise indicated

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 450 mA, P_{OUT} = 22.5 W, f = 959.8 MHz

Characteristic	Symbol	Min	Typ	Max	Units
Error Vector Magnitude	EVM (RMS)	—	2.0	—	%
Modulation Spectrum @ 400 kHz	ACPR	—	–62	—	dBc
Modulation Spectrum @ 600 kHz	ACPR	—	–76	—	dBc
Gain	G_{ps}	—	18	—	dB
Drain Efficiency	η_D	—	40	—	%

Two–Tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 450 mA, P_{OUT} = 45 W PEP, f = 960 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Units
Gain	G_{ps}	17	18	—	dB
Drain Efficiency	η_D	40	42	—	%
Intermodulation Distortion	IMD	—	–32	–30	dBc

DC Characteristics at T_{CASE} = 25°C unless otherwise indicated

Characteristic	Conditions	Symbol	Min	Typ	Max	Units
Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On–State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.1	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 450 mA	V_{GS}	2.5	3.2	4	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

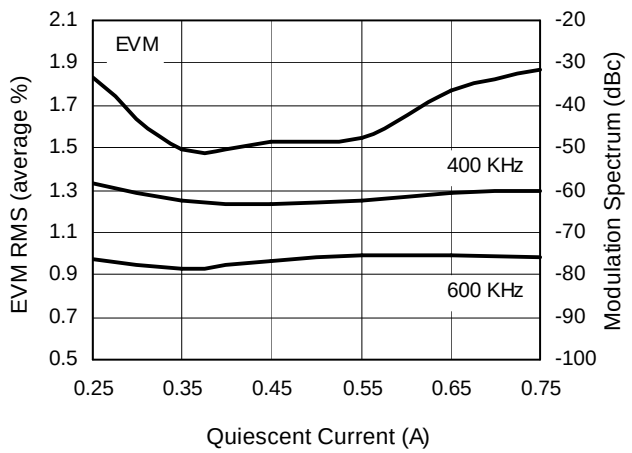
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	V
Gate–Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	184	W
Above 25°C derate by		1.05	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	0.95	°C/W

Typical Performance (measurements taken in production test fixture)

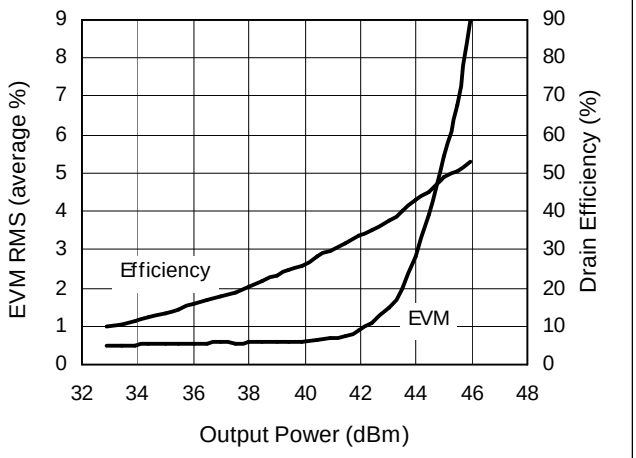
Modulation Spectrum

P_{OUT} = 20 W, f = 959.8 MHz



EDGE EVM Performance

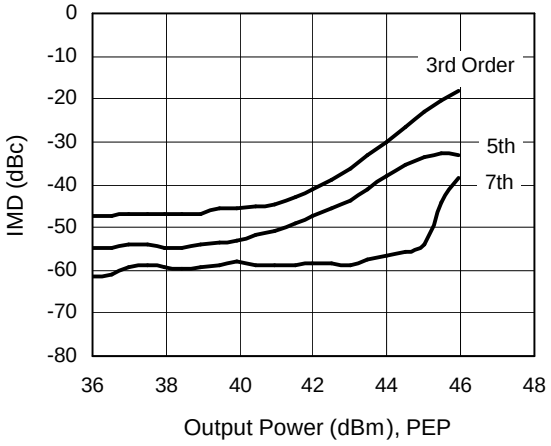
V_{DD} = 28 V, I_{DQ} = 450 mA, f = 959.8 MHz



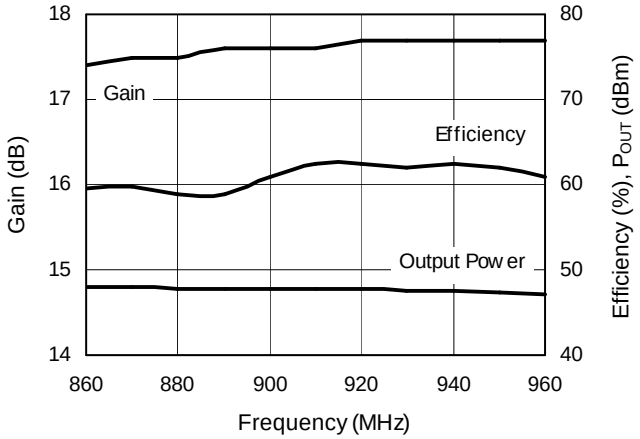
All published data at T_{CASE} = 25°C unless otherwise indicated.

Typical Performance (cont.)

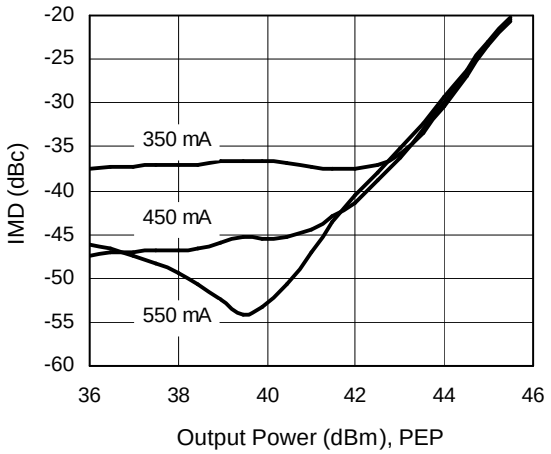
Intermodulation Distortion vs. Output Power
(as measured in a broadband circuit)
V_{DD} = 28 V, I_{DQ} = 450 mA, f_1 = 959 MHz, f_2 = 960 MHz



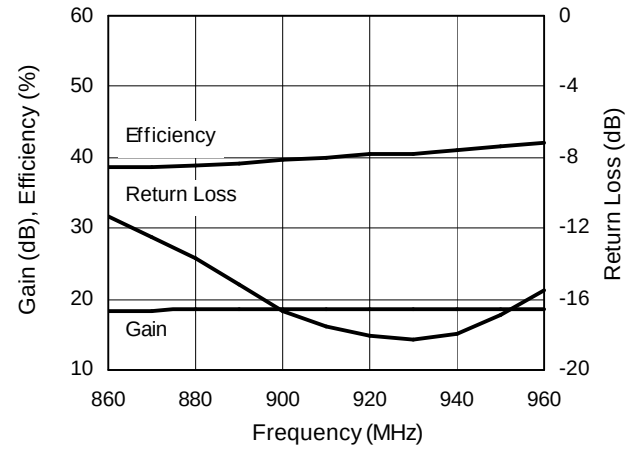
Typical P_{OUT}, Gain & Efficiency (at P-1dB)
vs. Frequency
V_{DD} = 28 V, I_{DQ} = 450 mA



IM3 vs. Output Power at Selected Biases
V_{DD} = 28 V, f_1 = 959, f_2 = 960 MHz



Broadband Performance
V_{DD} = 28 V, I_{DQ} = 450 mA, P_{OUT} = 22.5 W

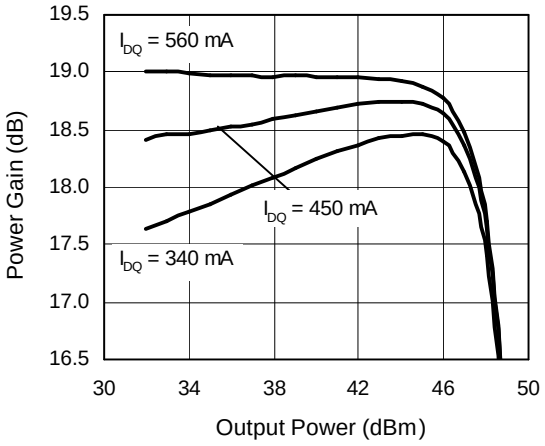


All published data at T_{CASE} = 25°C unless otherwise indicated.

Typical Performance (cont.)

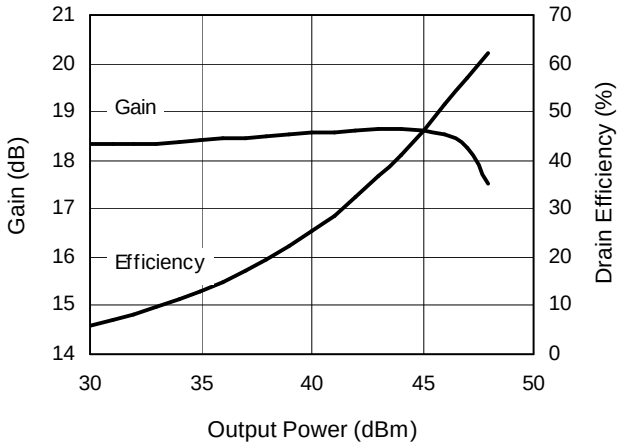
Power Sweep

V_{DD} = 28 V, f = 960 MHz



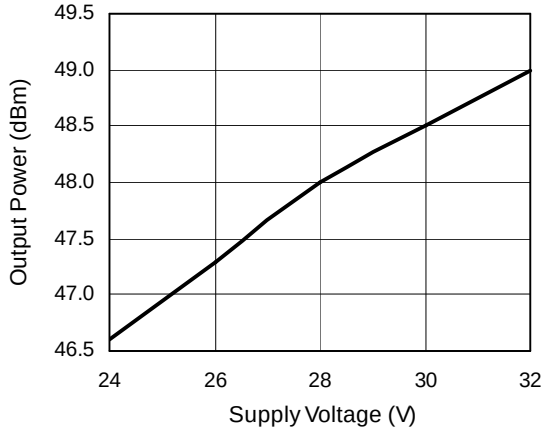
Gain & Efficiency vs. Output Power

V_{DD} = 28 V, I_{DQ} = 450 mA, f = 960 MHz



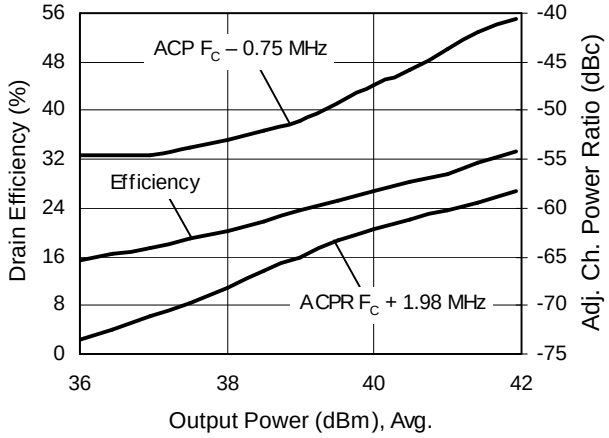
Output Power (at 1 dB Compression) vs. Supply Voltage

I_{DQ} = 450 mA, f = 960 MHz



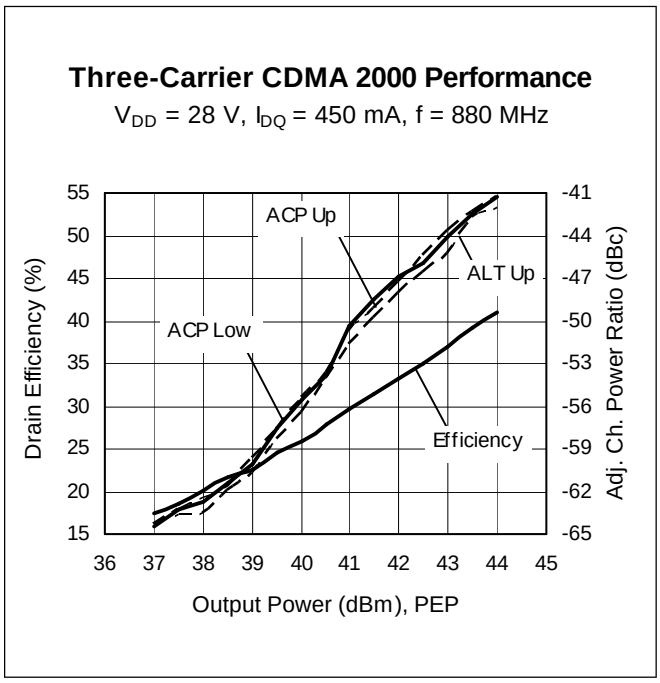
IS-95 CDMA Performance

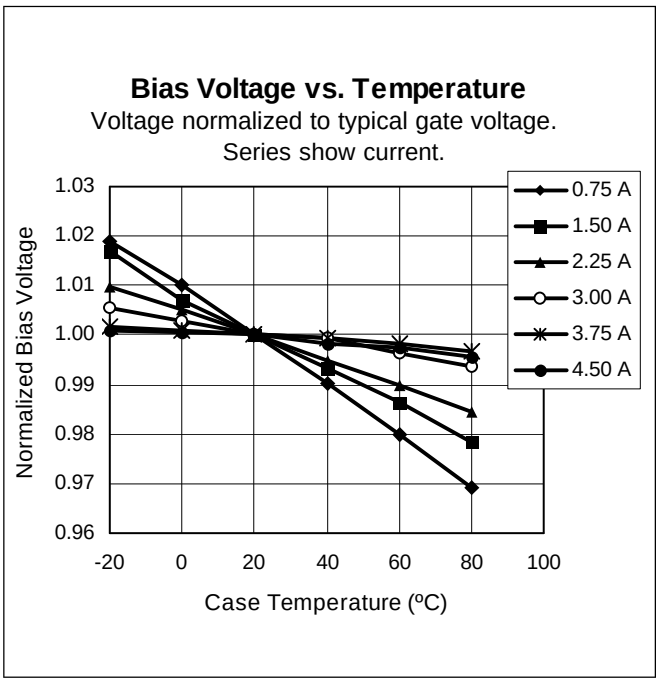
V_{DD} = 28 V, I_{DQ} = 450 mA, f = 880 MHz



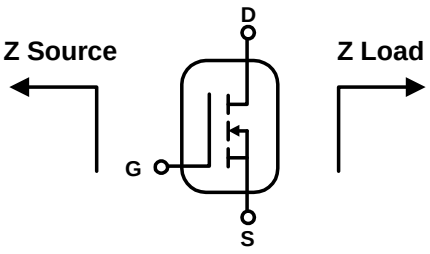
All published data at T_{CASE} = 25°C unless otherwise indicated.

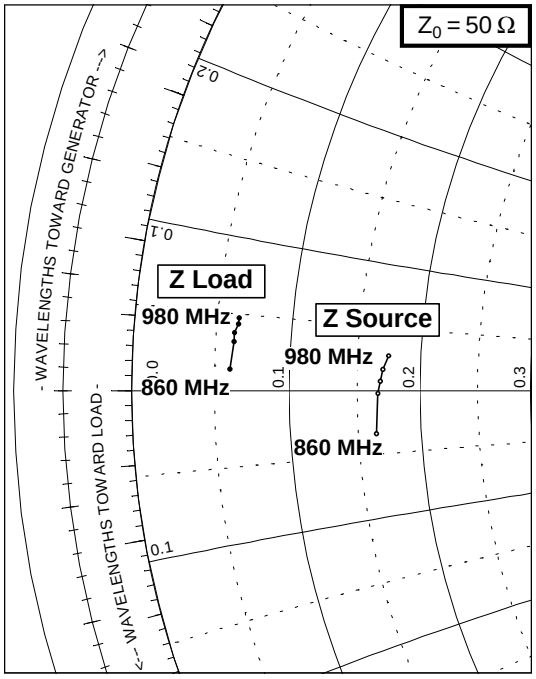
Typical Performance (cont.)





Broadband Circuit Impedance

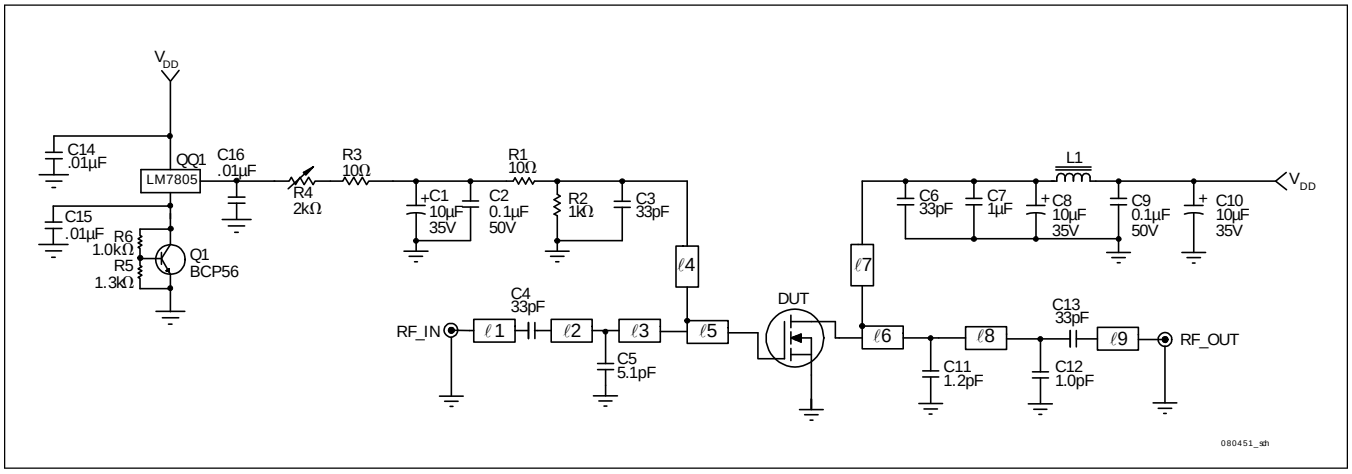




Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
860	8.20	-1.70	3.00	0.70
920	8.30	-0.12	3.10	1.60
940	8.40	0.38	3.10	1.90
960	8.50	0.85	3.20	2.20
980	8.70	1.40	3.20	2.40

All published data at T_{CASE} = 25°C unless otherwise indicated.

Test Circuit



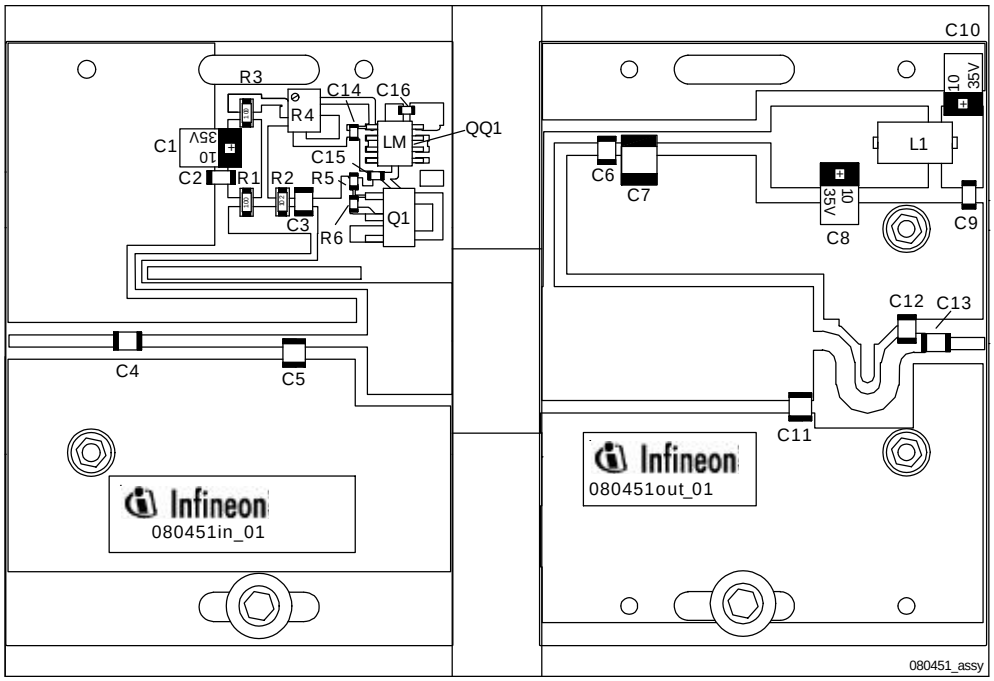
Test Circuit Schematic for 960 MHz

Circuit Assembly Information

DUT	PTF080451	LDMOS Transistor	
PCB	0.76 mm. [.030"] thick, ε_r = 4.5	2 oz. copper	Rogers TMM4

Microstrip	Electrical Characteristics at 960 MHz	Dimensions: L x W (mm.)	Dimensions: L x W (in.)
ℓ1	0.075 λ, 50.770 Ω	0.505 x 0.053	12.83 x 1.35
ℓ2	0.114 λ, 50.770 Ω	0.765 x 0.053	19.43 x 1.35
ℓ3	0.050 λ, 50.770 Ω	0.335 x 0.053	8.51 x 1.35
ℓ4	0.289 λ, 73.660 Ω	2.000 x 0.025	50.80 x 0.64
ℓ5	0.060 λ, 9.350 Ω	0.360 x 0.506	9.14 x 12.85
ℓ6	0.199 λ, 9.190 Ω	1.200 x 0.510	30.48 x 12.95
ℓ7	0.132 λ, 52.470 Ω	0.890 x 0.050	22.61 x 1.27
ℓ8	0.134 λ, 38.020 Ω	0.880 x 0.085	22.35 x 2.16
ℓ9	0.029 λ, 50.200 Ω	0.195 x 0.054	4.95 x 1.37

Test Circuit (cont.)



Reference Circuit[1] (not to scale)

Component	Description	Manufacturer	P/N or Comment
C1, C8, C10	Capacitor, 10 µF, 35 V, Tant TE Series SMD	Digi-Key	PCS6106TR-ND
C2, C9	Capacitor, 0.1 µF, 50 V	Digi-Key	P4525-ND
C3, C4, C6, C13	Capacitor, 33 pF	ATC	100B 330
C5	Capacitor, 5.1 pF	ATC	100B 5R1
C7	Capacitor, 1 µF, 50 V	Digi-Key	19528-ND
C11	Capacitor, 1.2 pF	ATC	100B 1R2
C12	Capacitor, 1.0 pF	ATC	100B 1R0
C14, C15, C16	Capacitor, .01 µF	Digi-Key	PCC1772CT-ND
L1	Ferrite, 6 mm	Philips	53/3/4.6-452
Q1	Transistor	Infineon	BCP56
QQ1	Voltage Regulator	Digi-Key	LM7805
R1, R3	Resistor, 10 ohm	Digi-Key	100ECT-ND
R2	Resistor, 1.0 k-ohm	Digi-Key	1KQBK
R4	Resistor, Variable 2 k-ohm, 4 W	Digi-Key	3224 W-202ETR-ND
R5	Resistor, 1.3 k-ohm 1/10 W, 0603	Digi-Key	P1.3KGCT-ND
R6	Resistor, 1.0 k-ohm 1/10 W, 0603	Digi-Key	P1.0KGCT-ND

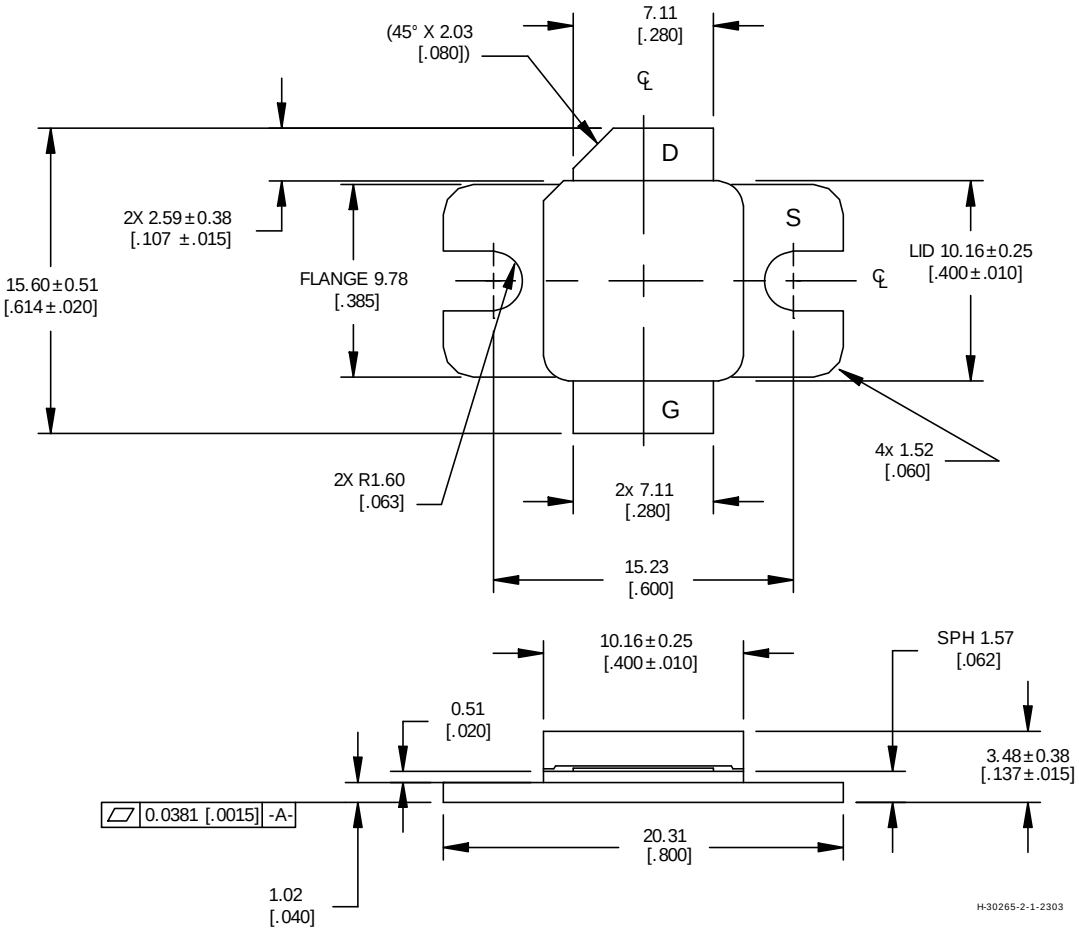
[1]Gerber files for this circuit are available on request.

Ordering Information

Type	Package Outline	Package Description	Marking
PTF080451E	30265	Thermally enhanced, flange mount	PTF080451E

Package Outline Specifications

Package 30265



Notes: Unless otherwise specified

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. Pins: D = drain, S = source, G = gate
4. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001]

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PTF080451

Revision History:	**2004-06-24**	Data Sheet
Previous Version:	2003-11-04, Developmental Data Sheet	
Page	Subjects (major changes since last revision)	
all	Include further data	

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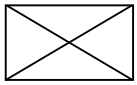

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