PCA9306

Dual bidirectional I^2C-bus and SMBus voltage-level translator

Rev. 9.1 — 31 August 2021 Product data sheet

1 General description

The PCA9306 is a dual bidirectional I^2C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.6 V ($V_{ref(1)}$) and 1.8 V to 5.5 V ($V_{bias(ref)(2)}$).

The PCA9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (R_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PCA9306 is not a bus buffer like the PCA9509 or PCA9517A that provide both level translation and physically isolate the capacitance to either side of the bus when both sides are connected. The PCA9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The PCA9306 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the controller is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PCA9306 has a standard open-collector configuration of the I^2C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast-mode Plus I^2C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2 MHz.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage ($V_{pu(D)}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

2 Features and benefits

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I^2C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I^2C-bus and SMBus compatible
- Less than 1.5 ns maximum propagation delay to accommodate Standard-mode and Fast-mode I^2C-bus devices and multiple controllers
- Allows voltage level translation between:
  - 1.0 V $V_{ref(1)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 1.2 V $V_{ref(1)}$ and 1.8 V, 2.5 V, 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 1.8 V $V_{ref(1)}$ and 3.3 V or 5 V $V_{bias(ref)(2)}$
  - 2.5 V $V_{ref(1)}$ and 5 V $V_{bias(ref)(2)}$
  - 3.3 V $V_{ref(1)}$ and 5 V $V_{bias(ref)(2)}$
- Provides bidirectional voltage translation with no direction pin
- Low 3.5 Ω ON-state connection between input and output ports provides less signal distortion
- Open-drain I^2C-bus I/O ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V tolerant I^2C-bus I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Lock-up free operation
- Flow through pinout for ease of printed-circuit board trace routing
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Packages offered: SO8, TSSOP8, VSSOP8, XQFN8, XSON8

3 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9306D	PCA9306	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9306DC1[1]	P06	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
PCA9306DC1/DG[2]	P06	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
PCA9306DP	306P	TSSOP8[3]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9306DP1[4]	306T	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
PCA9306GF[5]	06	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089
PCA9306GM	P6X[6]	XQFN8	plastic extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2

[1] Same footprint and pinout as the Texas Instruments PA9306DCU. VSSOP8 transfers to ASEN in dark green - refer to PCN202103046A.

[2] PCA9306DC1/DG is functionally the same (electrically and mechanically) as the PCA9306DC1 and the Texas Instruments PCA9306DCU. It is produced in dark green (lead-free and halogen/antimony-free) package material, with a unique orderable part number for customers who desire to order and only receive dark green package material.
[3] Also known as MSOP8.
[4] Same footprint and pinout as the Texas Instruments PCA9306DCT.
[5] Device migrates to new drop-in replacement package in the future, because SOT1089 will be phased out.
[6] 'X' will change based on date code.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9306D	PCA9306D,118	SO8	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = -40 °C to +105 °C
PCA9306DC1	PCA9306DC1,125[1]	VSSOP8	Reel 7” Q3/T4 *standard mark	3000	T_{amb} = -40 °C to +105 °C
	PCA9306DC1Z	VSSOP8	Reel 7” Q3/T4 *standard mark SSB [2]	3000	T_{amb} = -40 °C to +105 °C
PCA9306DC1/DG	PCA9306DC1/DG,125[1]	VSSOP8	Reel 7” Q3/T4 *standard mark	3000	T_{amb} = -40 °C to +105 °C
PCA9306DP	PCA9306DP,118	TSSOP8	Reel 13” Q1/T1 *standard mark SMD	2500	T_{amb} = -40 °C to +105 °C
PCA9306DP1	PCA9306DP1,125	TSSOP8	Reel 7” Q3/T4 *standard mark	3000	T_{amb} = -40 °C to +105 °C
PCA9306GF	PCA9306GF,115	XSON8	Reel 7” Q1/T1 *standard mark SMD	5000	T_{amb} = -40 °C to +105 °C
PCA9306GM	PCA9306GM,125	XQFN8	Reel 7” Q3/T4 *standard mark	4000	T_{amb} = -40 °C to +105 °C

[1] Discontinuation notice 202108009DN - move to PCA9306DC1Z.
[2] This packing method uses a Static Shielding Bag (SSB) solution. Material should be kept in the sealed bag between uses.

4 Functional diagram

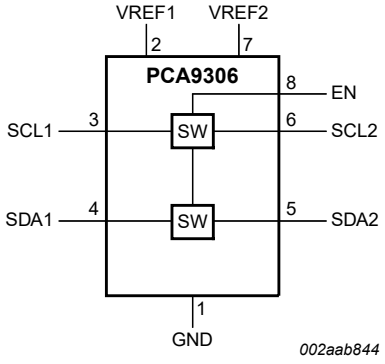


Figure 1. Logic diagram of PCA9306 (positive logic)

5 Pinning information

5.1 Pinning

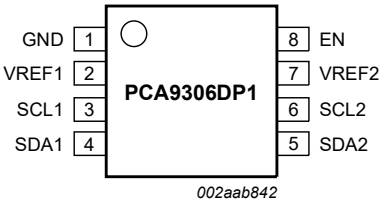


Figure 2. Pin configuration for TSSOP8 (DP1)

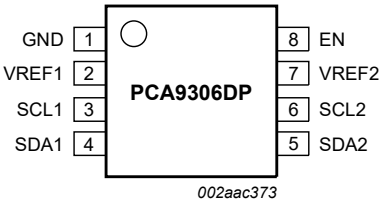


Figure 3. Pin configuration for TSSOP8 (DP) (MSOP8)

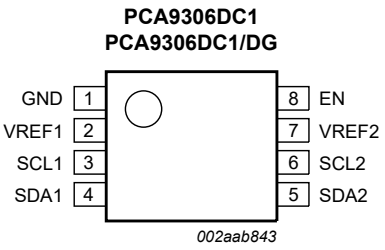


Figure 4. Pin configuration for VSSOP8 (DC1; DC1/DG)

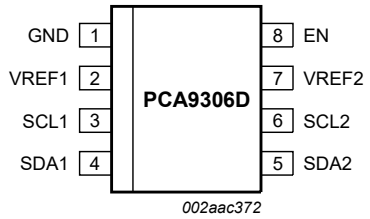
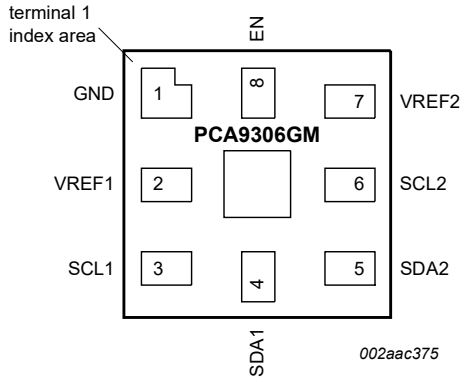
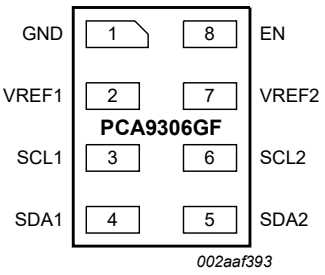


Figure 5. Pin configuration for SO8



Transparent top view

Figure 6. Pin configuration for XQFN8



Transparent top view

Figure 7. Pin configuration for XSON8

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
	SO8, TSSOP8 (MSOP8), TSSOP8, VSSOP8 (DC1), XQFN8, XSON8	
GND	1	ground (0 V)
VREF1	2	low-voltage side reference supply voltage for SCL1 and SDA1

Table 3. Pin description...*continued*

Symbol	Pin	Description
	SO8, TSSOP8 (MSOP8), TSSOP8, VSSOP8 (DC1), XQFN8, XSON8	
SCL1	3	serial clock, low-voltage side; connect to VREF1 through a pull-up resistor
SDA1	4	serial data, low-voltage side; connect to VREF1 through a pull-up resistor
SDA2	5	serial data, high-voltage side; connect to VREF2 through a pull-up resistor
SCL2	6	serial clock, high-voltage side; connect to VREF2 through a pull-up resistor
VREF2	7	high-voltage side reference supply voltage for SCL2 and SDA2
EN	8	switch enable input; connect to VREF2 and pull-up through a high resistor

6 Functional description

Refer to Figure 1.

6.1 Function table

Table 4. Function selection (example)

H = HIGH level; L = LOW level.

Input EN[1]	Function
H	SCL1 = SCL2; SDA1 = SDA2
L	disconnect

[1] EN is controlled by the $V_{bias(ref)(2)}$ logic levels and should be at least 1 V higher than $V_{ref(1)}$ for best translator operation.

7 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Over operating free-air temperature range.

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{ref(1)}$	reference voltage (1)			-0.5	+6	V
$V_{bias(ref)(2)}$	reference bias voltage (2)			-0.5	+6	V
V_I	input voltage			-0.5[1]	+6	V
$V_{I/O}$	voltage on an input/output pin			-0.5[1]	+6	V
I_{ch}	channel current (DC)			-	128	mA
I_{IK}	input clamping current	V_I < 0 V		-	-50	mA
T_{stg}	storage temperature			-65	+150	°C

[1] The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

8 Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{I/O}$	voltage on an input/output pin	SCL1, SDA1, SCL2, SDA2		0	5	V
$V_{ref(1)}$[1]	reference voltage (1)	VREF1		0	5	V
$V_{bias(ref)(2)}$[1]	reference bias voltage (2)	VREF2		0	5	V
$V_{I(EN)}$	input voltage on pin EN			0	5	V
$I_{sw(pass)}$	pass switch current			-	64	mA
T_{amb}	ambient temperature	operating in free-air		-40	+105	°C

[1] $V_{ref(1)} \leq V_{bias(ref)(2)}$ - 1 V for best results in level shifting applications.

9 Static characteristics

Table 7. Static characteristics

T_{amb} = -40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = -18 mA; $V_{I(EN)}$ = 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; $V_{I(EN)}$ = 0 V		-	-	5	µA
$C_{i(EN)}$	input capacitance on pin EN	V_I = 3 V or 0 V		-	7.1	-	pF
$C_{io(off)}$	off-state input/output capacitance	SCLn, SDAn; V_O = 3 V or 0 V; $V_{I(EN)}$ = 0 V		-	4	6	pF
$C_{io(on)}$	on-state input/output capacitance	SCLn, SDAn; V_O = 3 V or 0 V; $V_{I(EN)}$ = 3 V		-	9.3	12.5	pF
R_{on}	ON-state resistance[2]	SCLn, SDAn; V_I = 0 V; I_O = 64 mA	[3]				
		$V_{I(EN)}$ = 4.5 V		-	2.4	5.0	Ω
		$V_{I(EN)}$ = 3 V		-	3.0	6.0	Ω
		$V_{I(EN)}$ = 2.3 V		-	3.8	8.0	Ω
		$V_{I(EN)}$ = 1.5 V		-	15	32	Ω
		$V_{I(EN)}$ = 1.5 V	[4]	-	32	80	Ω
		V_I = 2.4 V; I_O = 15 mA					
		$V_{I(EN)}$ = 4.5 V		-	4.8	7.5	Ω
		$V_{I(EN)}$ = 3 V		-	46	80	Ω
		V_I = 1.7 V; I_O = 15 mA					
		$V_{I(EN)}$ = 2.3 V		-	40	80	Ω

[1] All typical values are at T_{amb} = 25 °C.
[2] Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

[3] Guaranteed by design.
[4] For DC, DC1 (VSSOP8) and GD1 (XSON8U) packages only.

10 Dynamic characteristics

Table 8. Dynamic characteristics (translating down)

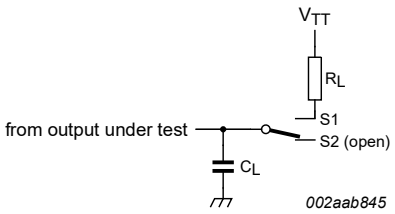
T_{amb} = -40 °C to +105 °C, unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$ = 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.0	0	1.2	0	0.6	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.0	0	1.5	0	0.75	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.0	0	1.2	0	0.6	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	2.5	0	1.5	0	0.75	ns

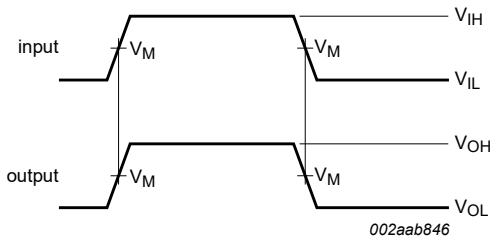
Table 9. Dynamic characteristics (translating up)

T_{amb} = -40 °C to +105 °C, unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)}$ = 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_{TT} = 3.3 V; V_M = 1.15 V; R_L = 300 Ω (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.75	0	1.0	0	0.5	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	2.75	0	1.65	0	0.8	ns
$V_{I(EN)}$ = 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_{TT} = 2.5 V; V_M = 0.75 V; R_L = 300 Ω (see Figure 8)									
t_{PLH}	LOW to HIGH propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.75	0	1.0	0	0.5	ns
t_{PHL}	HIGH to LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	3.3	0	2.0	0	1.0	ns



a. Load circuit



b. Timing diagram

S1 = translating up; S2 = translating down.

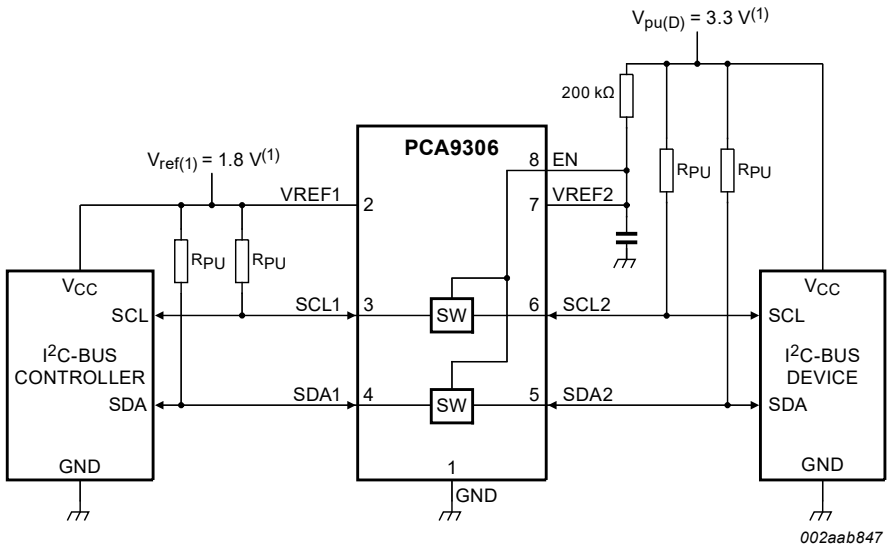
C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2 ns; t_f ≤ 2 ns.

The outputs are measured one at a time, with one transition per measurement.

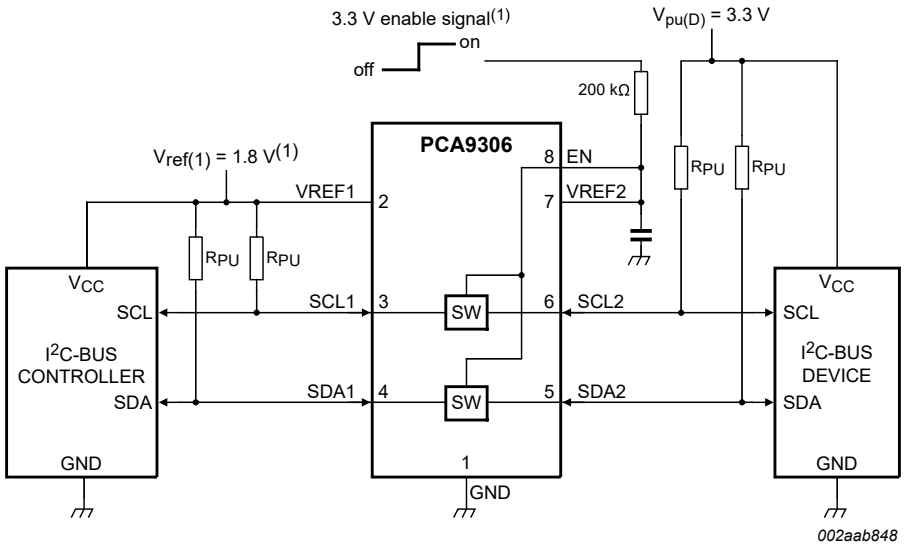
Figure 8. Load circuit for outputs

11 Application information



1. The applied voltages at $V_{ref(1)}$ and $V_{pu(D)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Figure 9. Typical application circuit (switch always enabled)



1. In the Enabled mode, the applied enable voltage and the applied voltage at $V_{ref(1)}$ should be such that $V_{bias(ref)(2)}$ is at least 1 V higher than $V_{ref(1)}$ for best translator operation.

Figure 10. Typical application circuit (switch enable control)

11.1 Bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to HIGH side $V_{pu(D)}$ through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended. The I²C-bus controller output can be totem pole or open-drain (pull-up resistors may be required) and the I²C-bus device output can be totem pole or open-drain (pull-up resistors are required to pull the SCL2 and SDA2 outputs to $V_{pu(D)}$). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage ($V_{ref(1)}$) is connected to the processor core power supply voltage. When VREF2 is connected through a 200 kΩ resistor to a 3.3 V to 5.5 V $V_{pu(D)}$ power supply, and $V_{ref(1)}$ is set between 1.0 V and ($V_{pu(D)}$ - 1 V), the output of each SCL1 and SDA1 has a maximum output voltage equal to VREF1, and the output of each SCL2 and SDA2 has a maximum output voltage equal to $V_{pu(D)}$.

Table 10. Application operating conditions

Refer to Figure 9.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{bias(ref)(2)}$	reference bias voltage (2)			$V_{ref(1)}$ + 0.6	2.1	5	V
$V_{I(EN)}$	input voltage on pin EN			$V_{ref(1)}$ + 0.6	2.1	5	V
$V_{ref(1)}$	reference voltage (1)			0	1.5	4.4	V
$I_{sw(pass)}$	pass switch current			-	14	-	mA
I_{ref}	reference current	transistor		-	5	-	µA
T_{amb}	ambient temperature	operating in free-air		-40	-	+105	°C

[1] All typical values are at T_{amb} = 25 °C.

11.2 How to size pull-up resistor value

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Table 11, Table 12 and Table 13 contain suggested minimum values of pull-up resistors for the PCA9306 and NVT20xx devices with typical voltage translation levels and drive currents. The calculated values assume that both drive currents are the same. V_{OL} = V_{IL} = 0.1 × V_{CC} and accounts for a ±5 % V_{CC} tolerance of the supplies, ±1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in Table 11, Table 12 and Table 13 to ensure that the pass voltage is less than 10 % of the V_{CC} voltage, and the external driver should be able to sink the total current from both pull-up resistors. When selecting the minimum resistor value in Table 11, Table 12 or Table 13, the drive current strength that should be chosen should be the lowest drive current seen in the application and account for any drive strength current scaling with output voltage. For the GTL devices, the resistance table should be recalculated to account for the difference in ON resistance and bias voltage limitations between $V_{CC(B)}$ and $V_{CC(A)}$.

Table 11. Pull-up resistor minimum values, 3 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 750 Ω $R_{pu(B)}$ = 750 Ω	$R_{pu(A)}$ = 845 Ω $R_{pu(B)}$ = 845 Ω	$R_{pu(A)}$ = 976 Ω $R_{pu(B)}$ = 976 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 887 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.82 kΩ
1.2 V		$R_{pu(A)}$ = 931 Ω $R_{pu(B)}$ = 931 Ω	$R_{pu(A)}$ = 1.02 kΩ $R_{pu(B)}$ = 1.02 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 887 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.82 kΩ
1.5 V			$R_{pu(A)}$ = 1.1 kΩ $R_{pu(B)}$ = 1.1 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 866 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.18 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
1.8 V				$R_{pu(A)}$ = 1.47 kΩ $R_{pu(B)}$ = 1.47 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.15 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
2.5 V					$R_{pu(A)}$ = 1.96 kΩ $R_{pu(B)}$ = 1.96 kΩ	$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.78 kΩ
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 1.74 kΩ

Table 12. Pull-up resistor minimum values, 10 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 221 Ω $R_{pu(B)}$ = 221 Ω	$R_{pu(A)}$ = 255 Ω $R_{pu(B)}$ = 255 Ω	$R_{pu(A)}$ = 287 Ω $R_{pu(B)}$ = 287 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 267 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 549 Ω
1.2 V		$R_{pu(A)}$ = 274 Ω $R_{pu(B)}$ = 274 Ω	$R_{pu(A)}$ = 309 Ω $R_{pu(B)}$ = 309 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 267 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 549 Ω
1.5 V			$R_{pu(A)}$ = 332 Ω $R_{pu(B)}$ = 332 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 261 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 536 Ω
1.8 V				$R_{pu(A)}$ = 442 Ω $R_{pu(B)}$ = 442 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 536 Ω
2.5 V					$R_{pu(A)}$ = 590 Ω $R_{pu(B)}$ = 590 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 523 Ω
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 523 Ω

Table 13. Pull-up resistor minimum values, 15 mA driver sink current for PCA9306 and NVT20xx

A-side	B-side					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.0 V	$R_{pu(A)}$ = 147 Ω $R_{pu(B)}$ = 147 Ω	$R_{pu(A)}$ = 169 Ω $R_{pu(B)}$ = 169 Ω	$R_{pu(A)}$ = 191 Ω $R_{pu(B)}$ = 191 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 178 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 237 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 365 Ω
1.2 V		$R_{pu(A)}$ = 182 Ω $R_{pu(B)}$ = 182 Ω	$R_{pu(A)}$ = 205 Ω $R_{pu(B)}$ = 205 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 178 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 237 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 365 Ω
1.5 V			$R_{pu(A)}$ = 221 Ω $R_{pu(B)}$ = 221 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 174 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 232 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
1.8 V				$R_{pu(A)}$ = 294 Ω $R_{pu(B)}$ = 294 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 232 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
2.5 V					$R_{pu(A)}$ = 392 Ω $R_{pu(B)}$ = 392 Ω	$R_{pu(A)}$ = none $R_{pu(B)}$ = 357 Ω
3.3 V						$R_{pu(A)}$ = none $R_{pu(B)}$ = 348 Ω

11.3 How to design for maximum frequency operation

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time. See Equation 1 as an example of the maximum frequency. The rise and fall times are shown in Figure 11.

$$f_{max} = \frac{1}{t_{LOW(min)} + t_{HIGH(min)} + t_{r(actual)} + t_{f(actual)}} \quad (1)$$

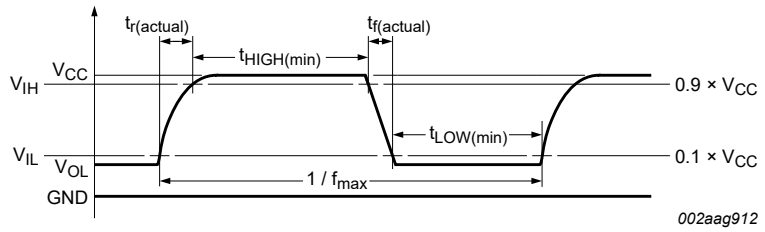


Figure 11. An example waveform for maximum frequency

The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance ($C_{L(tot)}$) and the pull-up resistors (R_{PU}) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus. Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

A description of the fall time applied to either An or Bn output going from HIGH to LOW is as follows. Whichever side is asserted first, the B-side down must discharge to the $V_{CC(A)}$ voltage. The time is determined by the pull-up resistor, pull-down driver strength and the capacitance. As the level moves below the $V_{CC(A)}$ voltage, the channel resistance drops so that both A and B sides equal. The capacitance on both sides is connected to form the total capacitance and the pull-up resistors on both sides combine to the parallel equivalent resistance. The R_{on} of the device is small compared to the pull-up resistor values, so its effect on the pull-up resistance can be neglected and the fall is determined by the driver pulling the combined capacitance and pull-up resistor currents. An estimation of the actual fall time seen by the device is equal to the time it takes for the B-side to fall to the $V_{CC(A)}$ voltage and the time it takes for both sides to fall from the $V_{CC(A)}$ voltage to the V_{IL} level.

A description of the rise time applied to either An or Bn output going from LOW to HIGH is as follows. When the signal level is LOW, the R_{on} is at its minimum, so the A and B sides are essentially one node. They will rise together with an RC time constant that is the sum of all the capacitance from both sides and the parallel of the resistance from both sides. As the signal approaches the $V_{CC(A)}$ voltage, the channel resistance goes up and the waveforms separate, with the B side finishing its rise with the RC time constant of the B side. The rise to $V_{CC(A)}$ is essentially the same for both sides.

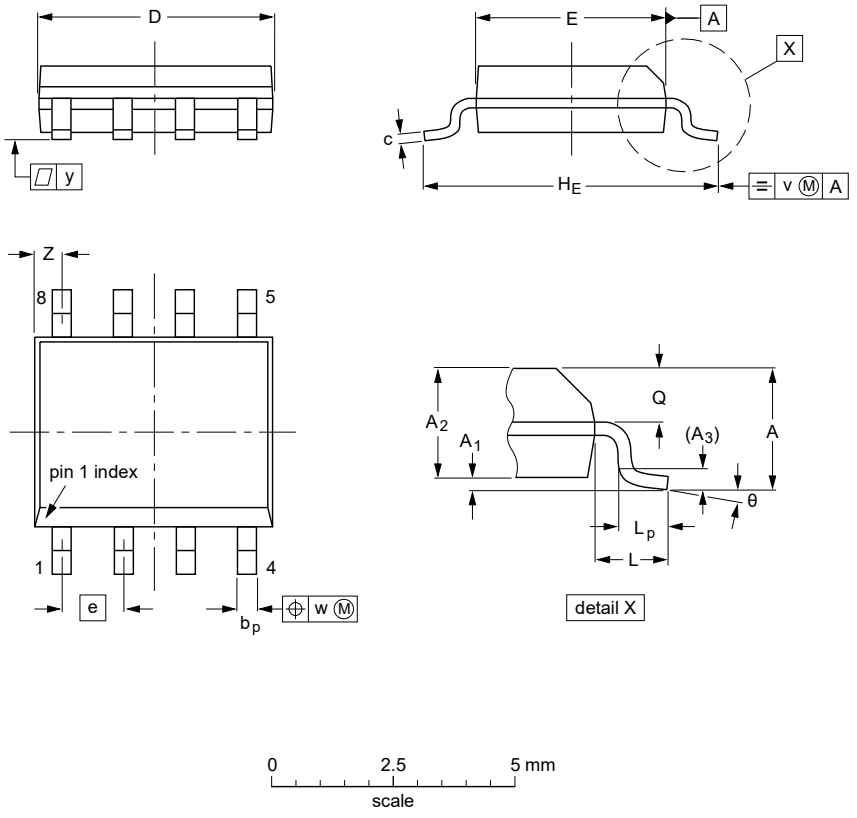
There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the NVT device close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

12 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

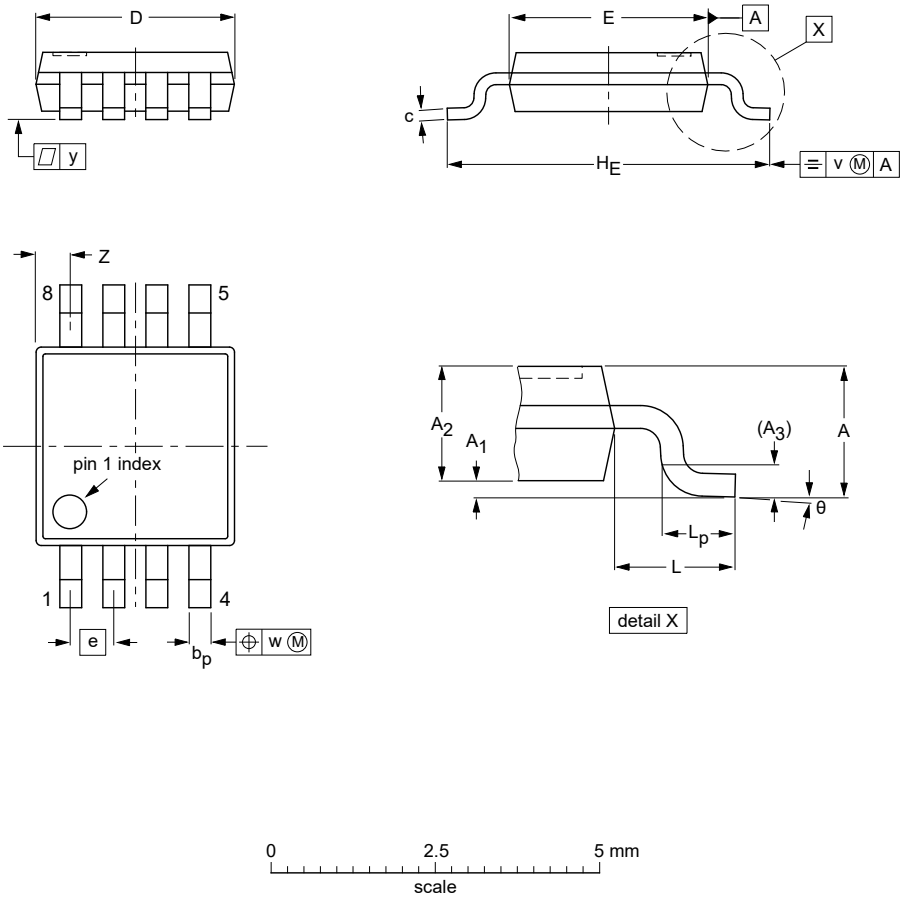
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 12. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

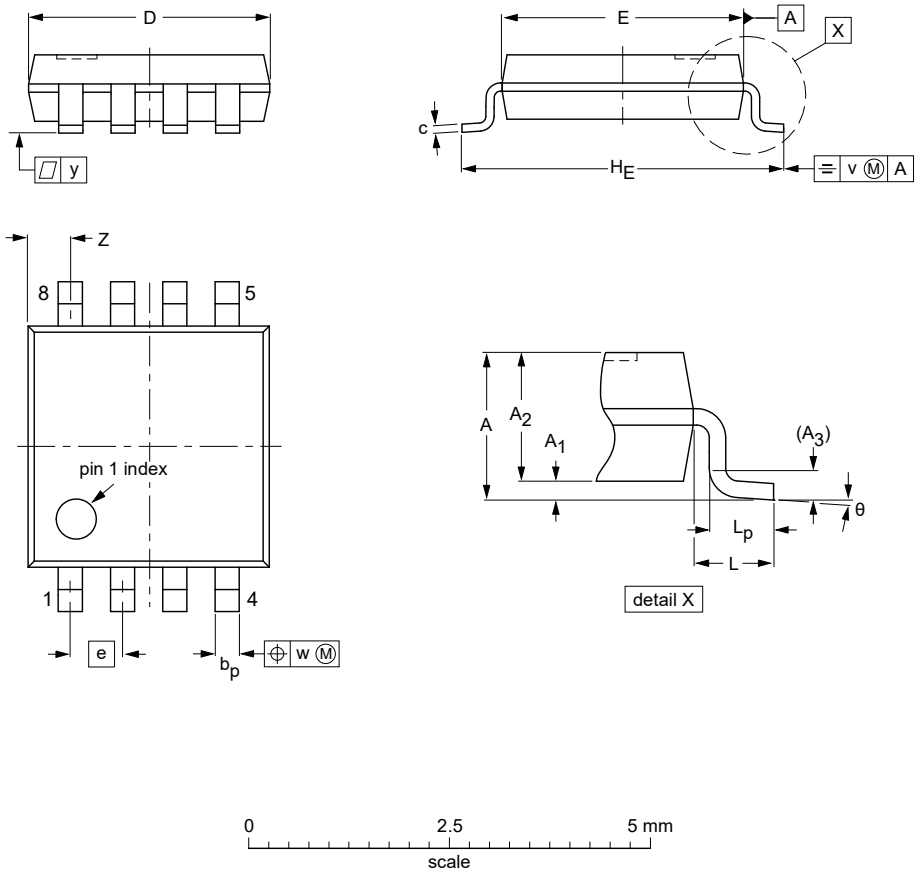
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Figure 13. Package outline SOT505-1 (TSSOP8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

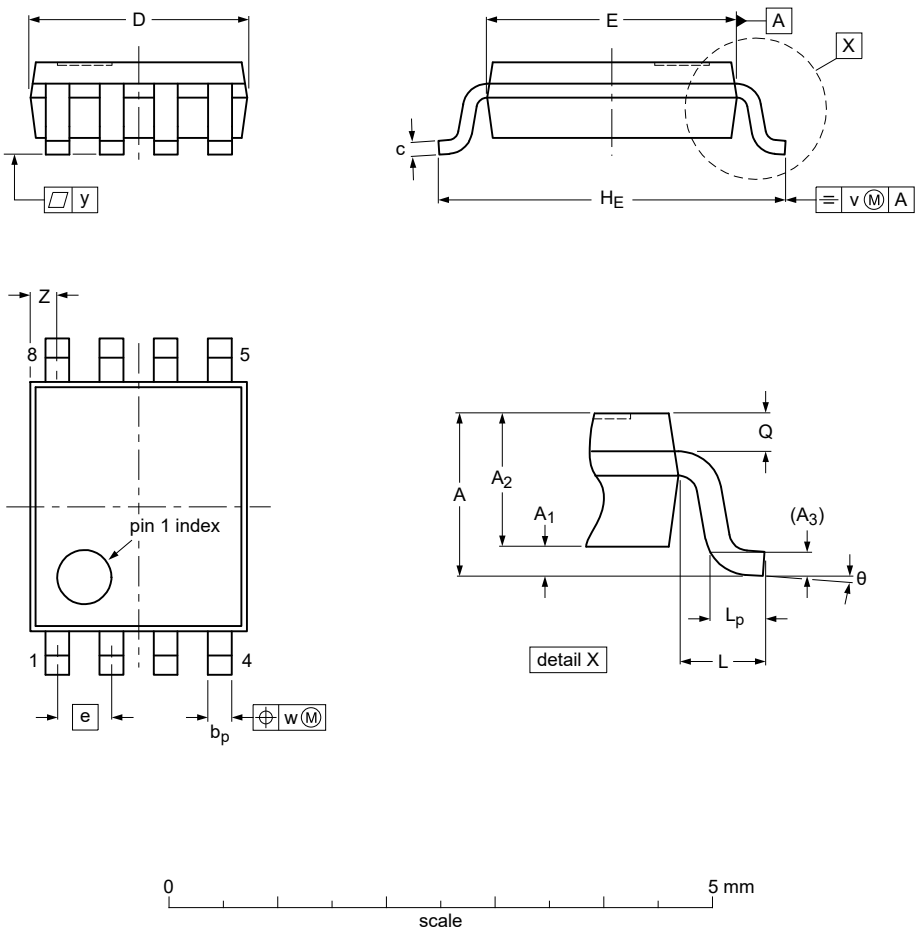
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Figure 14. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
max		0.15	0.85		0.27	0.23	2.1	2.4		3.2		0.40	0.21				0.4	8°
mm nom	1			0.12					0.5		0.4			0.2	0.08	0.1		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

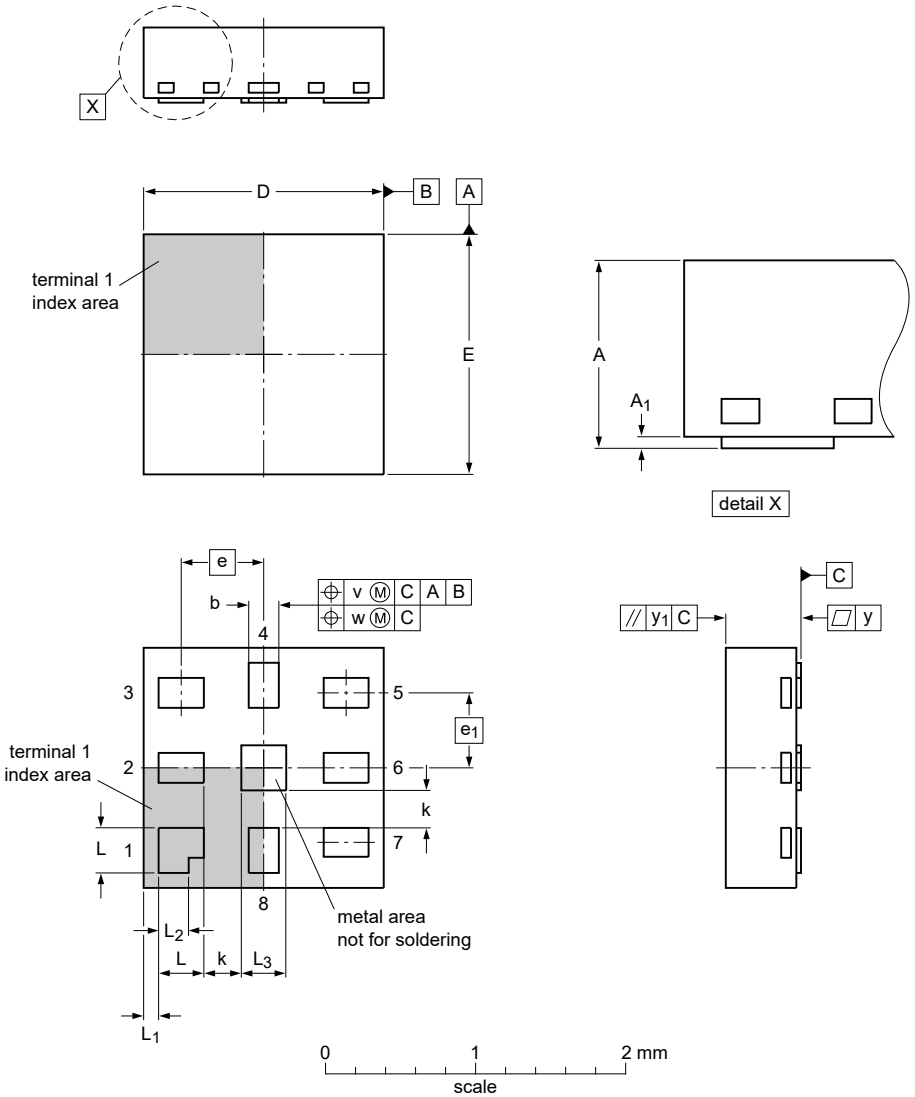
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Figure 15. Package outline SOT765-1 (VSSOP8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit(1)		A	A_1	b	D	E	e	e_1	k	L	L_1	L_2	L_3	v	w	y	y_1
	max	0.5	0.05	0.25	1.65	1.65				0.35	0.15	0.25	0.35				
mm	nom			0.20	1.60	1.60	0.55	0.5		0.30	0.10	0.20	0.30	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.2	0.25	0.05	0.15	0.25				

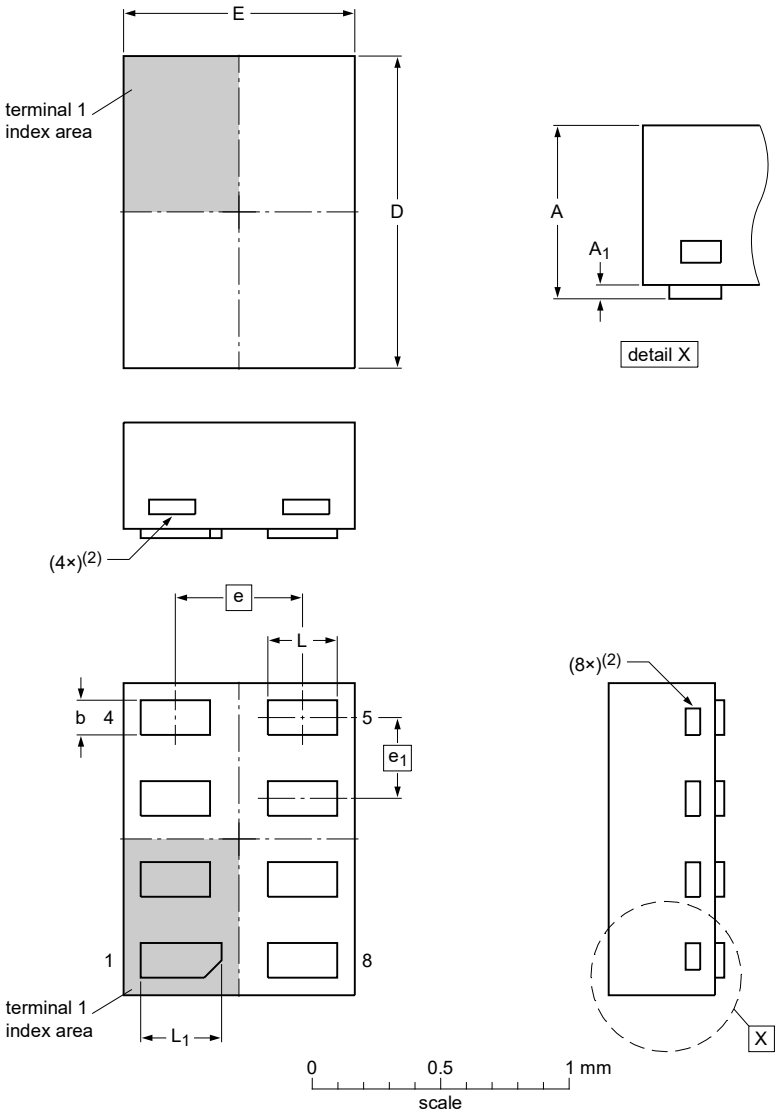
Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~16-07-14~~ 16-11-08

Figure 16. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

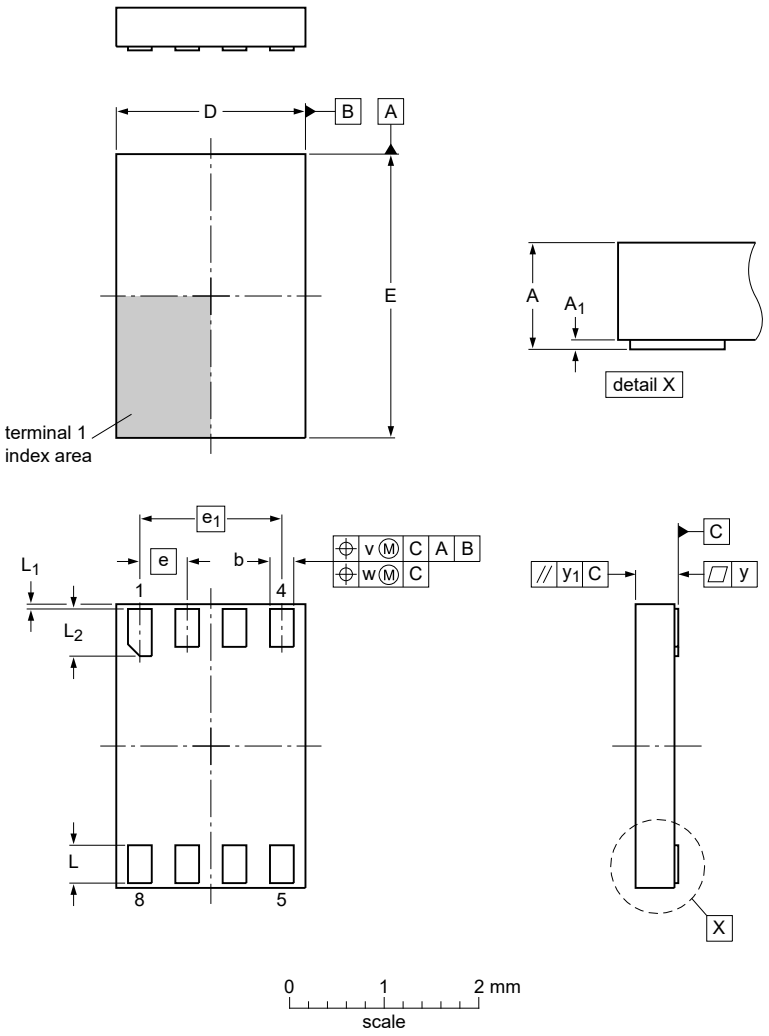
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Figure 17. Package outline SOT1089 (XSON8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm **SOT996-2**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	max		0.05	0.35	2.1	3.1			0.5	0.15	0.6				
	nom	0.5					0.5	1.5				0.1	0.05	0.05	0.1
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT996-2						~~07-12-21~~ 12-11-20

Figure 18. Package outline SOT996-2 (XSON8U)

13 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and Table 15

Table 14. SnPb eutectic process (from J-STD-020D)

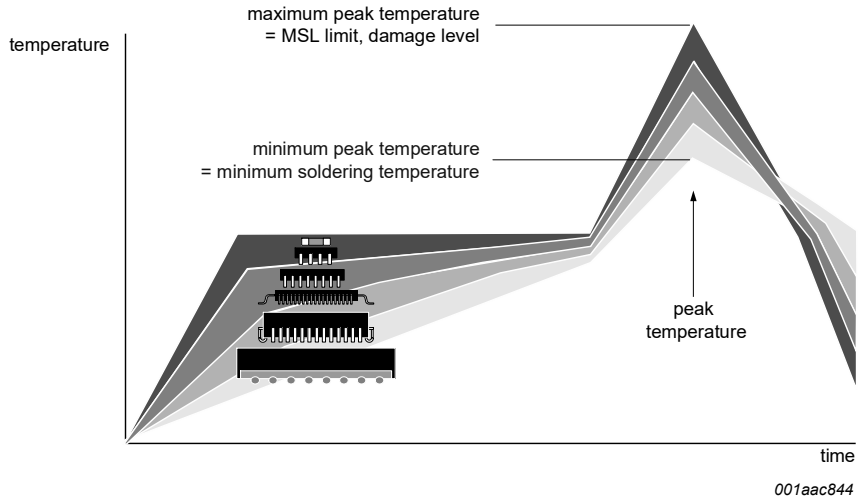
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Figure 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14 Soldering: PCB footprints

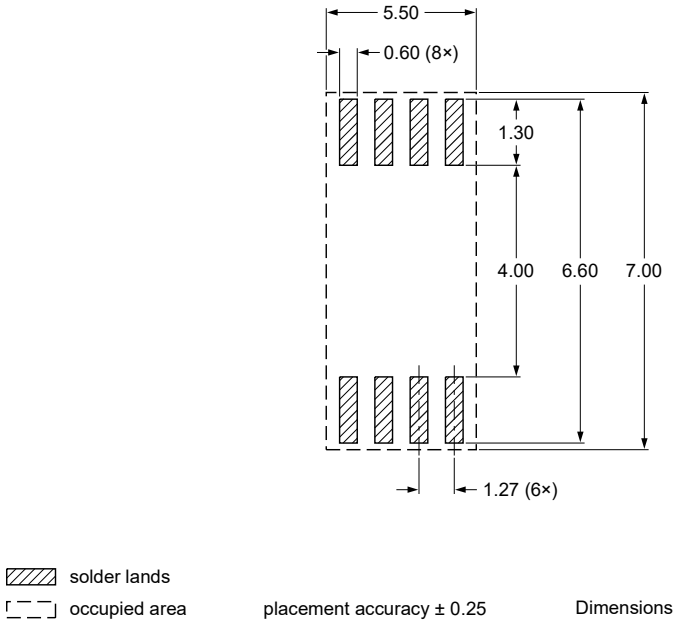


Figure 20. PCB footprint for SOT96-1 (SO8); reflow soldering

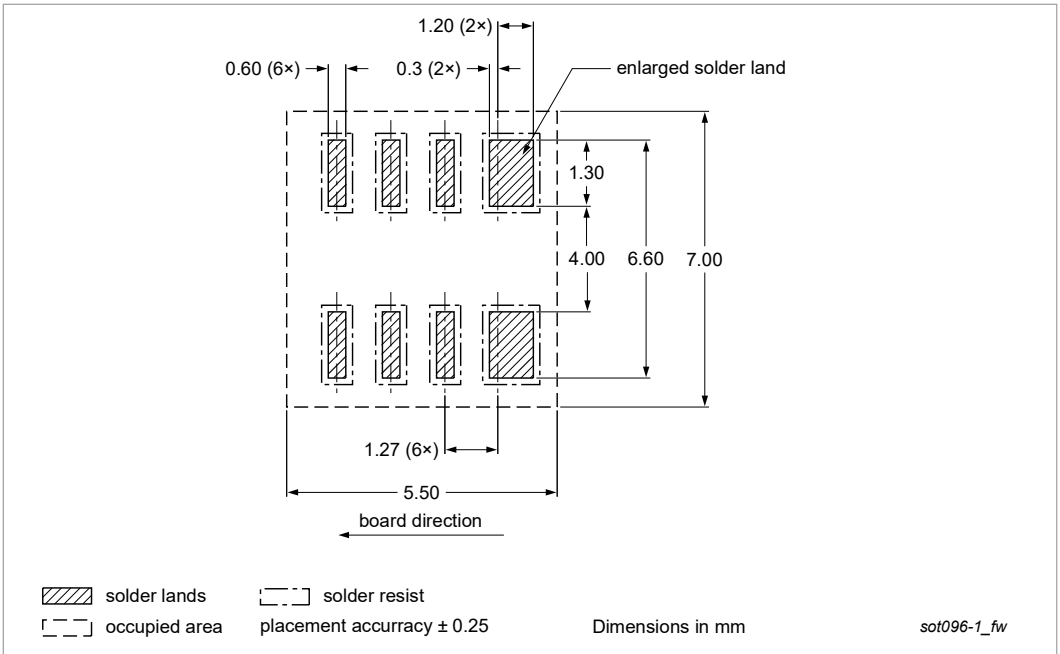


Figure 21. PCB footprint for SOT96-1 (SO8); wave soldering

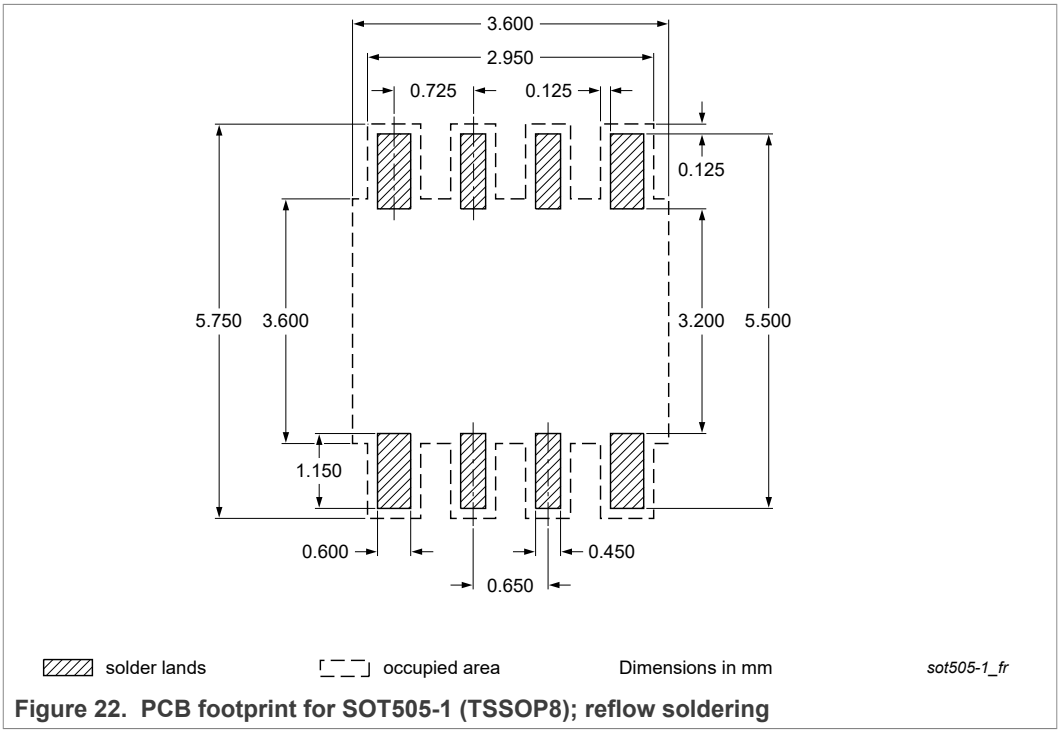
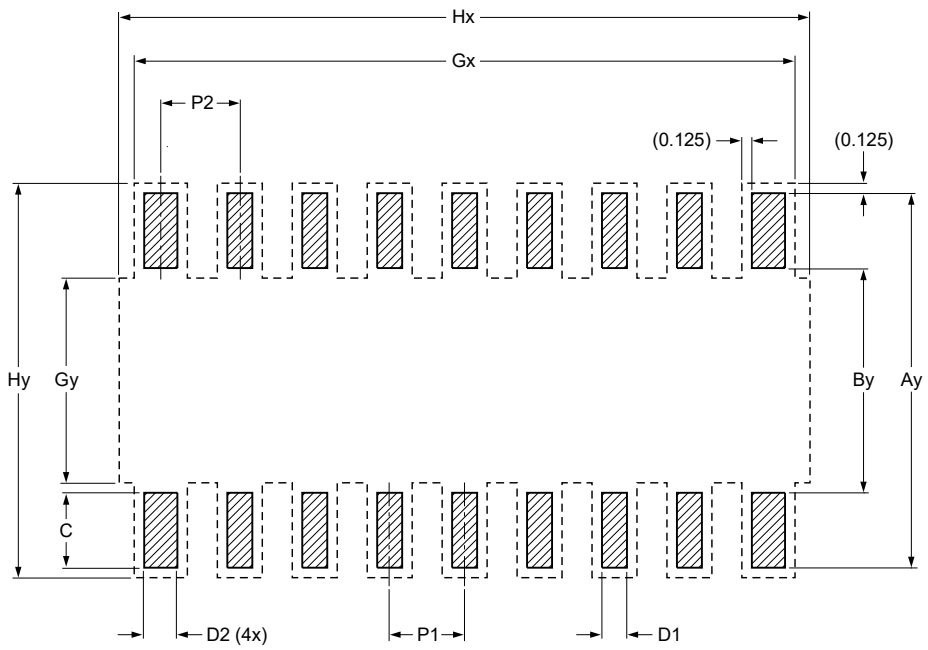


Figure 22. PCB footprint for SOT505-1 (TSSOP8); reflow soldering

Footprint information for reflow soldering of TSSOP8 package **SOT505-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

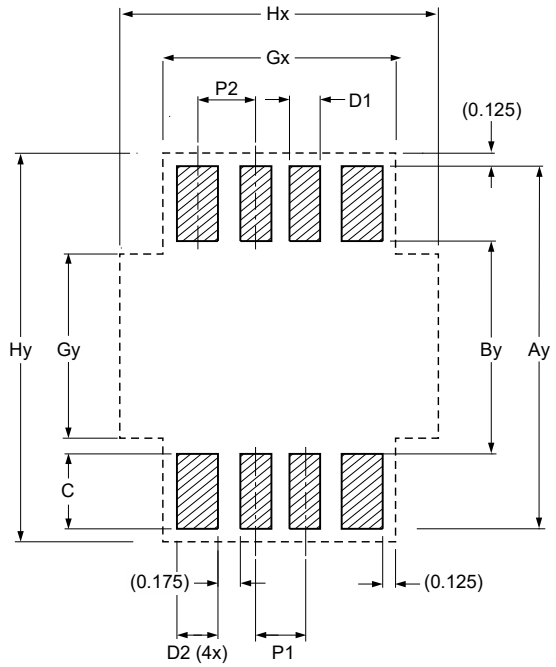
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.700	4.400	2.700	0.850	0.400	0.500	2.800	3.600	3.600	4.650

sot505-2_fr

Figure 23. PCB footprint for SOT505-2 (TSSOP8); reflow soldering

Footprint information for reflow soldering of VSSOP8 package **SOT765-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.550	3.500	2.000	0.750	0.300	0.400	2.250	1.750	3.075	3.750

sot765-1_fr

Figure 24. PCB footprint for SOT765-1 (VSSOP8); reflow soldering

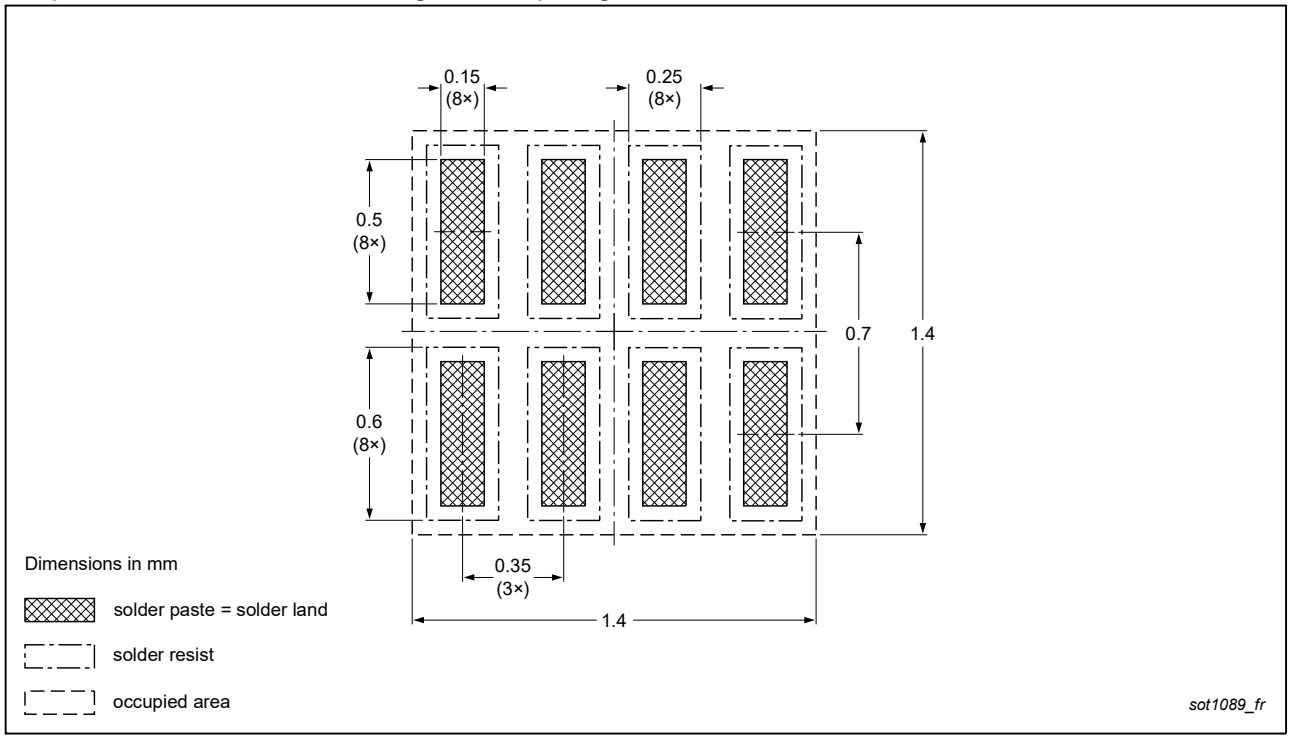


Figure 25. PCB footprint for SOT1089 (XSON8); reflow soldering

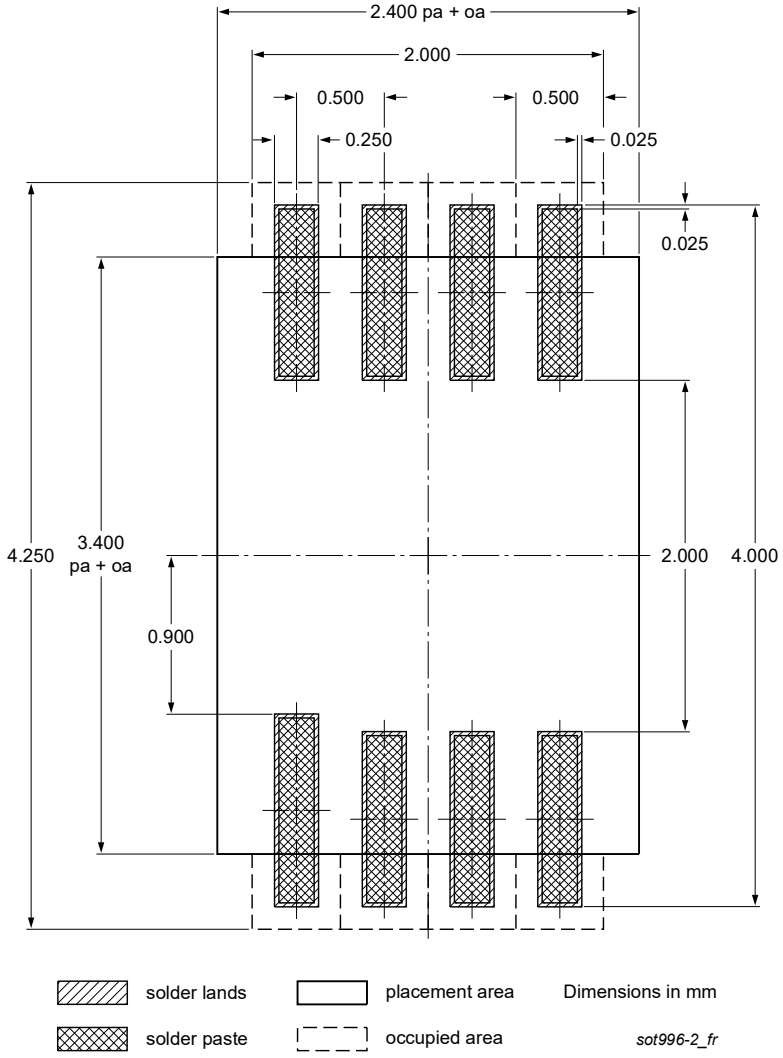


Figure 26. PCB footprint for SOT996-2 (XSON8U); reflow soldering

Footprint information for reflow soldering of XQFN8 package **SOT902-2**

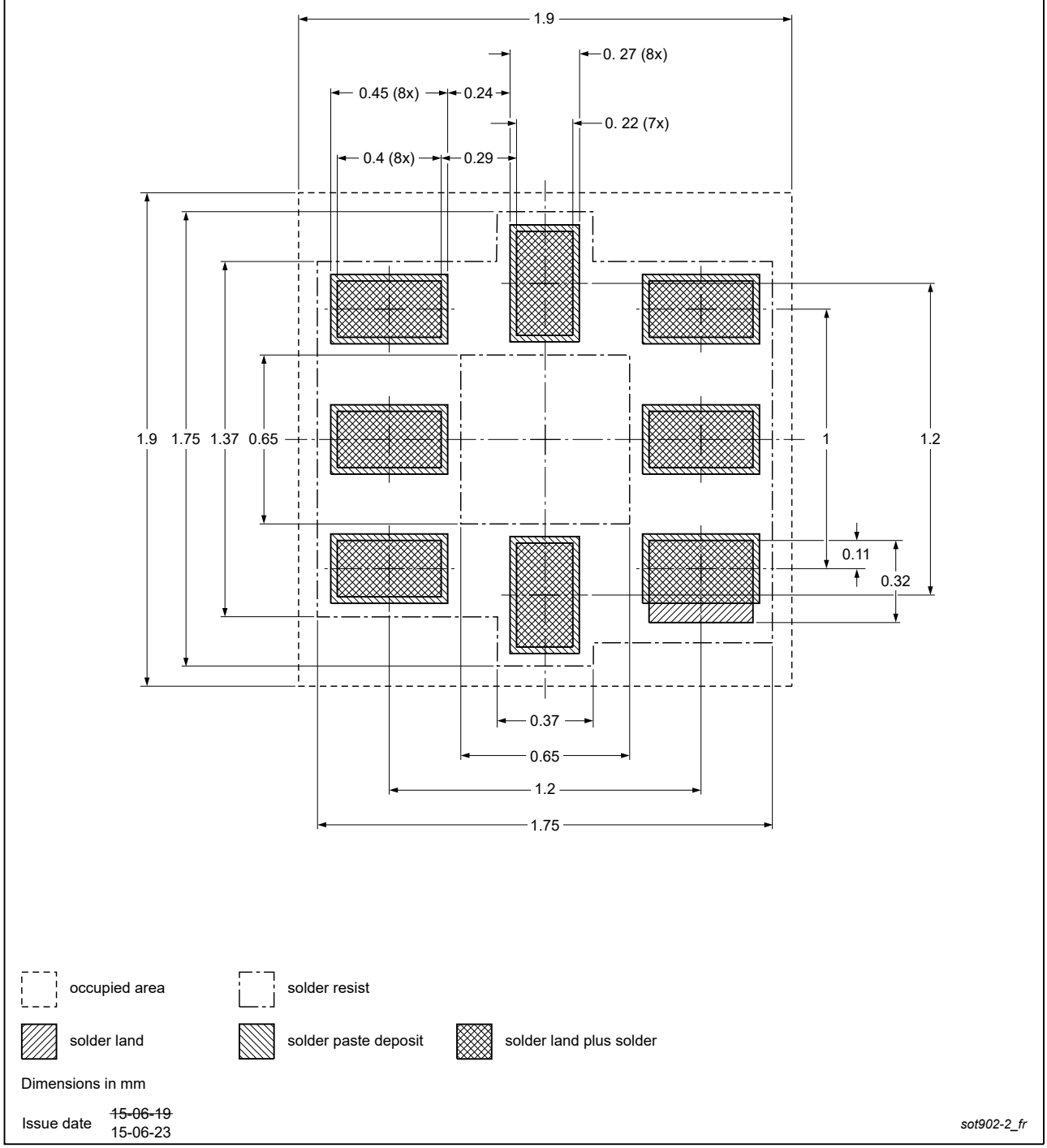


Figure 27. PCB footprint for SOT902-2 (XQFN8); reflow soldering

15 Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	(Obsolete) Mobile Industry Processor Interface
PLL	Phase-Locked Loop
PRR	Pulse Repetition Rate
RC	Resistor-Capacitor network
SMBus	System Management Bus

16 Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9306 v9.1	20210831	Product data sheet	PCN202103046A	PCA9306 v.9
Modifications	• Updated ordering information for PCA9306DC1 assembly site transfer from Hana to ASEN. – Removed these types, since they are withdrawn: PCA9306DC and PCA9306GD1. • The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy.			
PCA9306 v.9	20191206	Product data sheet	201912004I	PCA9306 v.8
Modifications:	• Updated ordering information • Removed PCA9306D,112 • Improved temperature range from "-40 °C to +85 °C" to "-40 °C to +105 °C"			
PCA9306 v.8	20140122	Product data sheet	-	PCA9306 v.7
Modifications:	• deleted (old) Section 11.2, "Sizing pull-up resistor" • added (new) Section 11.2 • added (new) Section 11.3			
PCA9306 v.7	20130517	Product data sheet	-	PCA9306 v.6
PCA9306 v.6	20101125	Product data sheet	-	PCA9306 v.5
PCA9306 v.5	20100319	Product data sheet	-	PCA9306 v.4
PCA9306 v.4	20091026	Product data sheet	-	PCA9306 v.3
PCA9306 v.3	20080804	Product data sheet	-	PCA9306 v.2
PCA9306 v.2	20070221	Product data sheet	-	PCA9306 v.1
PCA9306 v.1	20061020	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

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17.3 Disclaimers

17.4 Trademarks

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Date of release: 31 August 2021
Document identifier: PCA9306