QUAD 5V RAIL-TO-RAIL PRECISION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD4702A/ALD4702B/ALD4702 is a quad monolithic precision CMOS rail-to-rail operational amplifier intended for a broad range of analog applications using ±2.5V to ±5V dual power supply systems, as well as +4V to +10V battery operated systems. All device characteristics are specified for +5V single supply or ±2.5V dual supply systems. Total supply current for four operational amplifiers is 6mA maximum at 5V supply voltage. It is manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process.

The ALD4702A/ALD4702B/ALD4702 is designed to offer a trade-off of performance parameters providing a wide range of desired specifications. It has been developed specifically with the +5V single supply or ±2.5V dual supply user andoffers the popular industry pin configuration of LM324 and ICL7641 types.

Several important characteristics of the device make many applications easy to implement for these supply voltages. First, the operational amplifier can operate with rail to rail input and output voltages. This feature allows numerous analog serial stages to be implemented without losing operating voltage margin. Second, the device was designed to accommodate mixed applications where digital and analog circuits may work off the same 5V power supply. Third, the output stage can drive up to 400pF capacitive and 5KΩ resistive loads in non-inverting unity gain connection and double the capacitance in the inverting unity gain mode.

These features, coupled with extremely low input currents, high voltage gain, useful bandwidth of 1.5MHz, a slew rate of 2.1V/μs, low power dissipation, low offset voltage and temperature drift, make the ALD4702A/ALD4702B/ALD4702 a truly versatile, user friendly, operational amplifier.

The ALD4702A/ALD4702B/ALD4702 is designed and fabricated with silicon gate CMOS technology, and offers 1pA typical input bias current. On-chip offset voltage trimming allows the device to be used without nulling in most applications. The device offers typical offset drift of less than 7μV/°C which eliminates many trim or temperature compensation circuits. For precision applications, the ALD4702A/ALD4702B/ALD4702 is designed to settle to 0.01% in 8μs. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to 125°C
14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD4702ASBL ALD4702BSBL ALD4702SBL	ALD4702APBL ALD4702BPBL ALD4702PBL	ALD4702ADB ALD4702BDB ALD4702DB

* Contact factory for leaded (non-RoHS) or high temperature versions.

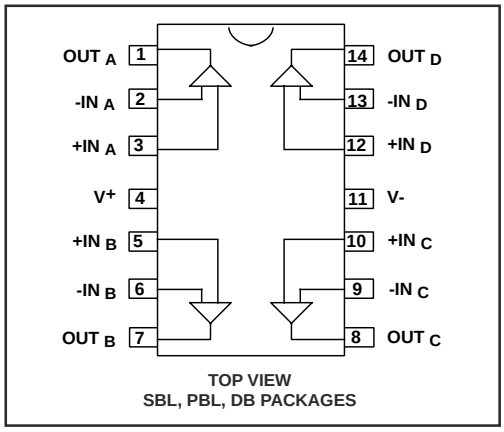
FEATURES

- Rail-to-rail input and output voltage ranges
- Symmetrical push-pull class AB output drivers
- All parameters specified for +5V single supply or ±2.5V dual supply systems
- Inputs can extend beyond supply rails by 300mV
- Outputs settle to 2mV of supply rails
- High load capacitance capability up to 4000pF
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- 1.0pA typical
- Ideal for high source impedance applications
- Dual power supply ±2.5V to ±5.0V operation
- Single power supply +5V to +10V operation
- High voltage gain-typically 85V/mV @ ±2.5V and 250V/mV @ ±5.0V
- Drive as low as 2KΩ load with 5mA drive current
- Output short circuit protected
- Unity gain bandwidth of 1.5MHz
- Slew rate of 1.9V/μs
- Low power dissipation
- Suitable for rugged, temperature-extreme environments

APPLICATIONS

- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage convert
- Coaxial cable driver

PIN CONFIGURATION



TOP VIEW
SBL, PBL, DB PACKAGES

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+ referenced to V^- ——— -0.3V to V^++10.6V
Supply voltage, V_S referenced to V^- ——— ±5.3V
Differential input voltage range ——— -0.3V to V^+ +0.3V
Power dissipation ——— 600 mW
Operating tempurature range SBL, PBL packages ——— 0°C to +70°C
DB package ——— -55°C to +125°C
Storage tempurature range ——— -65°C to +150°C
Lead tempurature, 10 seconds ——— +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±2.5V unless otherwise specified

		4702A			4702B			4702				Test
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Supply Voltage	V_S V^+	±2.0 4.0		±5.0 10.0	±2.0 4.0		±5.0 10.0	±2.0 4.0		±5.0 10.0	V V	Dual Supply Single Supply
Input Offset Voltage	V_{OS}			2.0 2.8			5.0 5.8			10.0 11.0	mV mV	$R_S \le 100K\Omega$ $0°C \le T_A \le +70°C$
Input Offset Current	I_{OS}		1.0	25 240		1.0	25 240		1.0	25 240	pA pA	T_A = 25°C $0°C \le T_A \le +70°C$
Input Bias Current	I_B		1.0	30 300		1.0	30 300		1.0	30 300	pA pA	T_A = 25°C $0°C \le T_A \le +70°C$
Input Voltage Range	V_{IR}	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	V V	V^+ = +5V V_S = ±2.5V
Input Resistance	R_{IN}		10^{12}			10^{12}			10^{12}		Ω	
Input Offset Voltage Drift	TCV_{OS}		7			7			7		µV/°C	$R_S \le 100K\Omega$
Power Supply Rejection Ratio	PSRR	65 65	83 83		65 65	83 83		60 60	83 83		dB	$R_S \le 100K\Omega$ $0°C \le T_A \le +70°C$
Common Mode Rejection Ratio	CMRR	65 65	83 83		65 65	83 83		60 60	83 83		dB	$R_S \le 100K\Omega$ $0°C \le T_A \le +70°C$
Large Signal Voltage Gain	A_V	15	28 100		15	28 100		12	28 100		V/mV V/mV	R_L = 10KΩ $R_L \ge 1M\Omega$
Output Voltage Range	V_O low V_O high	4.99	0.002 4.998	0.01	4.99	0.002 4.998	0.01	4.99	0.002 4.998	0.01	V	R_L = 1MΩ Single supply $0°C \le T_A \le +70°C$
	V_O low V_O high	2.40	-2.44 2.44	-2.40	2.40	-2.44 2.44	-2.40	2.40	-2.44 2.44	-2.40	V V	R_L = 10KΩ Dual supply $0°C \le T_A \le +70°C$
Output Short Circuit Current	I_{SC}		8			8			8		mA	
Supply Current	I_S		4.0	6.0		4.0	6.0		4.0	6.0	mA	V_{IN} = 0V No Load
Power Dissipation	P_D		20	30		20	30		20	30	mW	Both amplifiers V_S = ±2.5V
Input Capacitance	C_{IN}		1			1			1		pF	
Bandwidth	B_W	0.7	1.5		0.7	1.5		0.7	1.5		MHz	
Slew Rate	S_R	1.1	1.9		1.1	1.9		1.1	1.9		V/µs	A_V = +1 R_L = 10KΩ
Rise time	t_r		0.2			0.2			0.2		µs	R_L = 10KΩ
Overshoot Factor			10			10			10		%	R_L = 10KΩ C_L = 100pF

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	4702A			4702B			4702			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Load Capacitance	C_L		400 4000			400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Input Noise Voltage	e_n		26			26			26		nV/√HZ	f = 1KHz
Input Current Noise	i_n		0.6			0.6			0.6		fA/√HZ	f = 10Hz
Settling Time	t_S		8.0 3.0			8.0 3.0			8.0 3.0		µs µs	0.01% 0.1% A_V = -1 R_L = 5KΩ C_L = 50pF

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	4702A			4702B			4702			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		83			83			83		dB	R_S ≤ 100KΩ
Common Mode Rejection Ratio	CMRR		83			83			83		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V		250			250			250		V/mV	R_L = 10KΩ
Output Voltage Range	V_O low V_O high	4.8	-4.90 4.93	-4.8	4.8	-4.90 4.93	-4.8	4.8	-4.90 4.93	-4.8	V	R_L = 10KΩ
Bandwidth	B_W		1.7			1.7			1.7		MH_Z	
Slew Rate	S_R		2.8			2.8			2.8		V/µs	A_V =+1 C_L =50pF

V_S = +5.0V -55°C ≤ T_A ≤ +125°C unless otherwise specified

Parameter	Symbol	4702ADA			4702BDA			4702DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{OS}			3.0			6.0			10.0	mV	R_S ≤ 100KΩ
Input Offset Current	I_{OS}			8.0			8.0			8.0	nA	
Input Bias Current	I_B			10.0			10.0			10.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		60	75		dB	R_S ≤ 100KΩ
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V	10	25		10	25		7	25		V/mV	R_L ≤ 10KΩ
Output Voltage Range	V_O low V_O high	4.8	0.1 4.9	0.2	4.8	0.1 4.9	0.2	4.8	0.1 4.9	0.2	V	R_L ≤ 10KΩ

Design & Operating Notes:

1. The ALD4702A/ALD4702B/ALD4702 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. The ALD4702A/ALD4702B/ALD4702 is internally compensated for unity gain stability using a novel scheme. This design produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD4702A/ALD4702B/ALD4702 will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD4702A/ALD4702B/ALD4702 is much more resistant to parasitic oscillations.

2. The ALD4702A/ALD4702B/ALD4702 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. With the common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. As offset voltage trimming on the ALD4702A/ALD4702B/ALD4702 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain greater than 2.5 (5V operation), where the common mode voltage does not make excursions below this switching point.

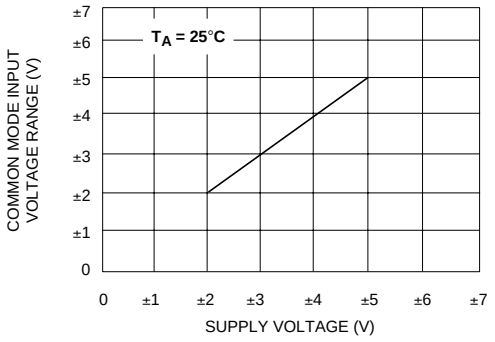
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor when connected. In the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes the ALD4702A/ALD4702B/ALD4702 an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

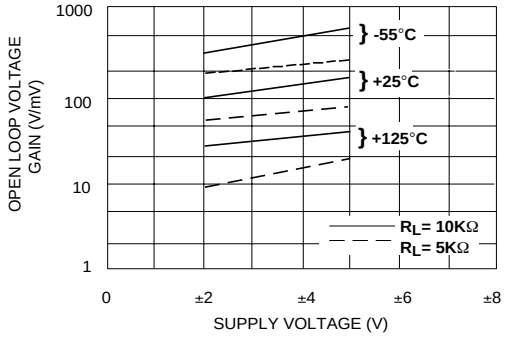
5. The ALD4702A/ALD4702B/ALD4702 operational amplifier has been designed with static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels. Alternatively, a 100KΩ or higher value resistor at the input terminals will limit input currents to acceptable levels while causing very small or negligible accuracy effects.

TYPICAL PERFORMANCE CHARACTERISTICS

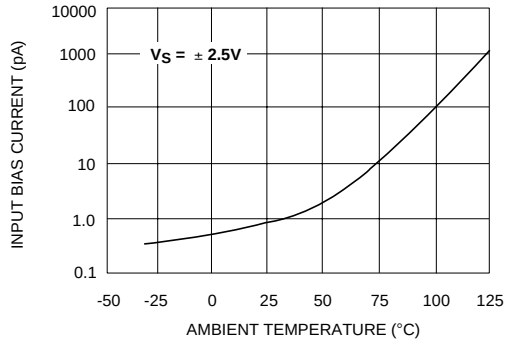
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



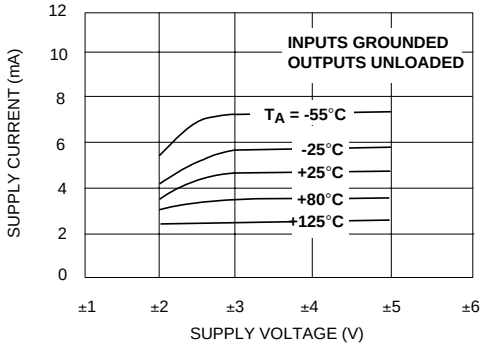
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

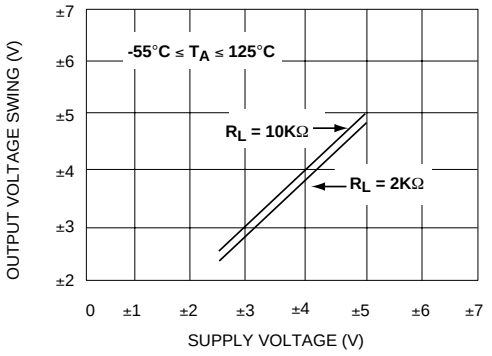


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

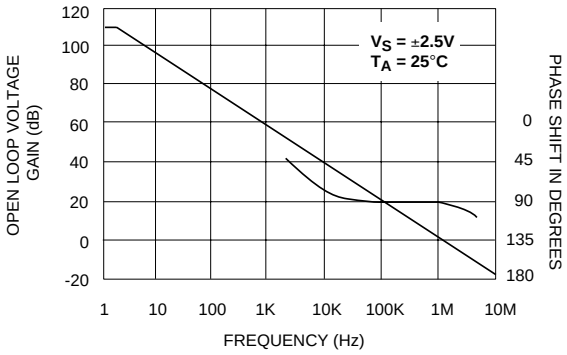


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

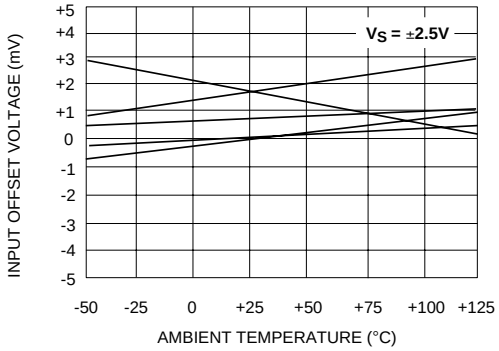
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



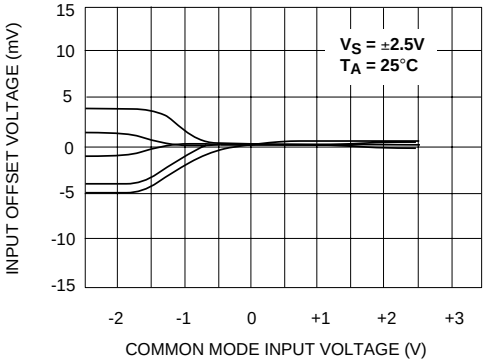
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



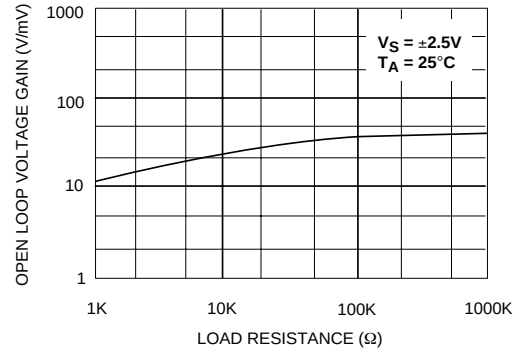
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS



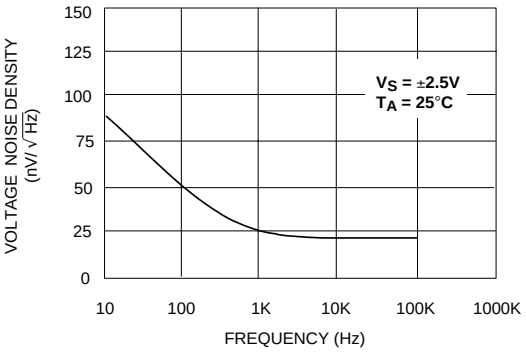
INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



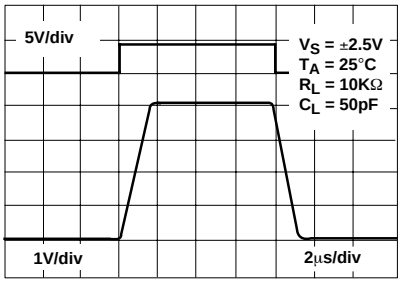
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



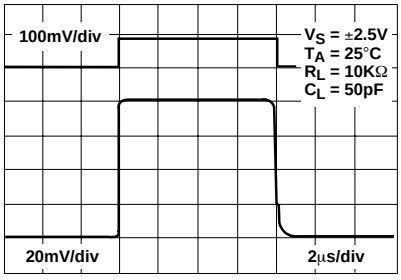
VOLTAGE NOISE DENSITY AS A FUNCTION OF FREQUENCY



LARGE - SIGNAL TRANSIENT RESPONSE

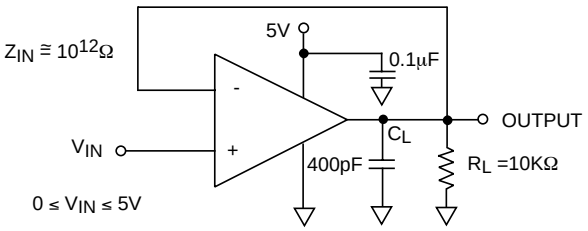


SMALL - SIGNAL TRANSIENT RESPONSE



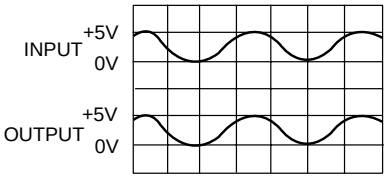
TYPICAL APPLICATIONS

RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER



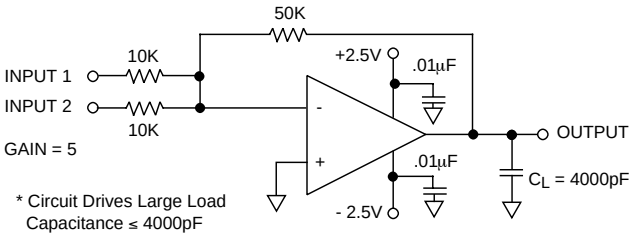
* See rail to rail waveform

RAIL-TO-RAIL WAVEFORM



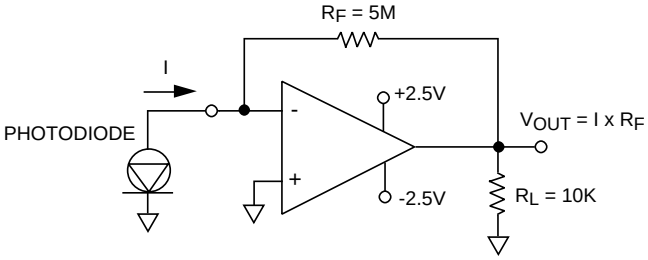
Performance waveforms.
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-Rail voltage follower.

LOW OFFSET SUMMING AMPLIFIER

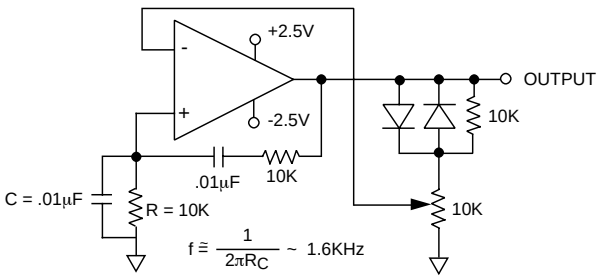


* Circuit Drives Large Load Capacitance ≤ 4000pF

PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER

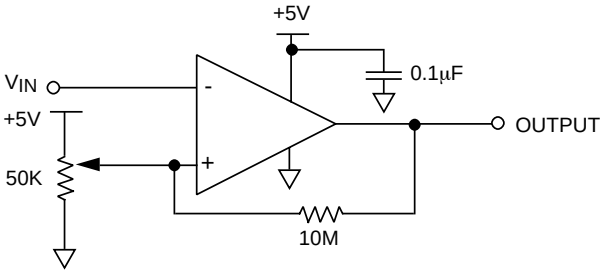


WIEN BRIDGE OSCILLATOR (RAIL-TO -RAIL) SINE WAVE GENERATOR



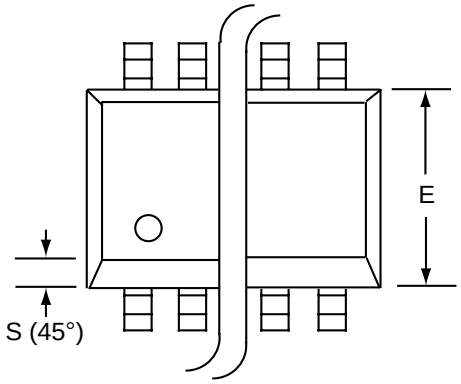
* See rail to rail waveform

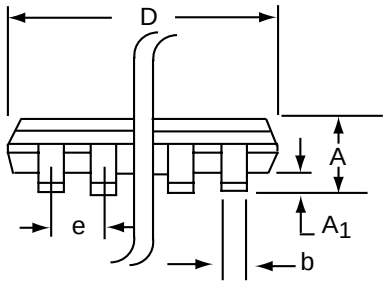
RAIL-TO-RAIL VOLTAGE COMPARATOR

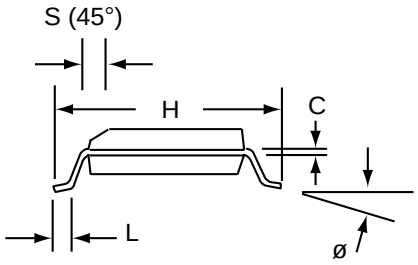


SOIC-14 PACKAGE DRAWING

14 Pin Plastic SOIC Package



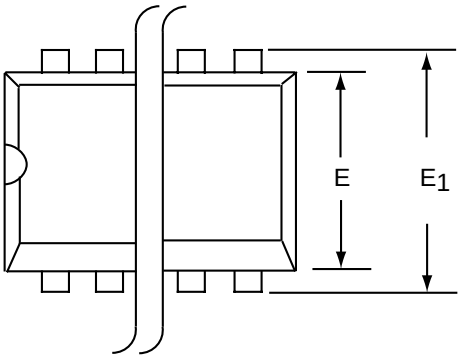


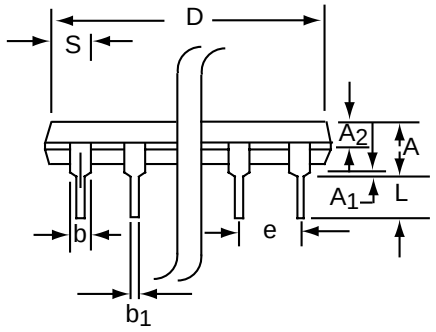


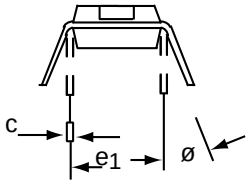
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

14 Pin Plastic DIP Package



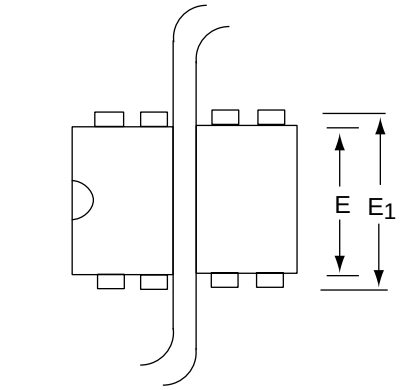


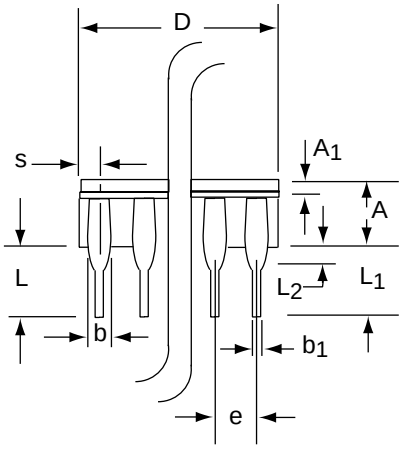


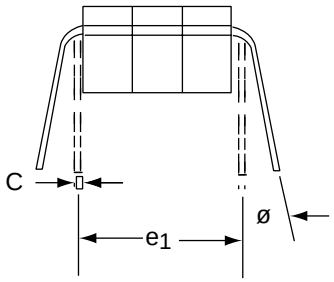
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-14	--	19.94	--	0.785
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°