HI-8685, HI-8686

ARINC INTERFACE DEVICE

February 2001

ARINC 429 & 561 Serial Data to 16-Bit Parallel Data

DESCRIPTION

The HI-8685 and HI-8686 are system components for interfacing incoming ARINC 429 signals to 16-bit parallel data using proven +5V analog/digital CMOS technology. Both products incorporate the digital logic and analog line receiver circuitry in a single device.

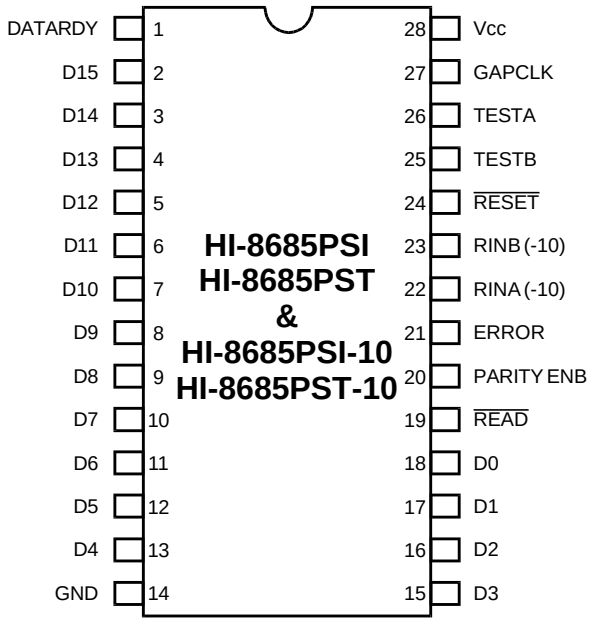
The receivers on the HI-8685 and the HI-8686 connect directly to the ARINC 429 Bus and translate the incoming signals to normal CMOS levels. Internal comparator levels are set just below the standard 6.5 volt minimum data threshold and just above the standard 2.5 volt maximum null threshold. The -10 version of the HI-8685 allows the incorporation of an external 10KΩ resistance in series with each ARINC input for lightning protection without affecting ARINC level detection.

Both products offer high speed 16-bit parallel bus interface, a 32-bit buffer, and error detection for word length and parity. A reset pin is also provided for power-on initialization.

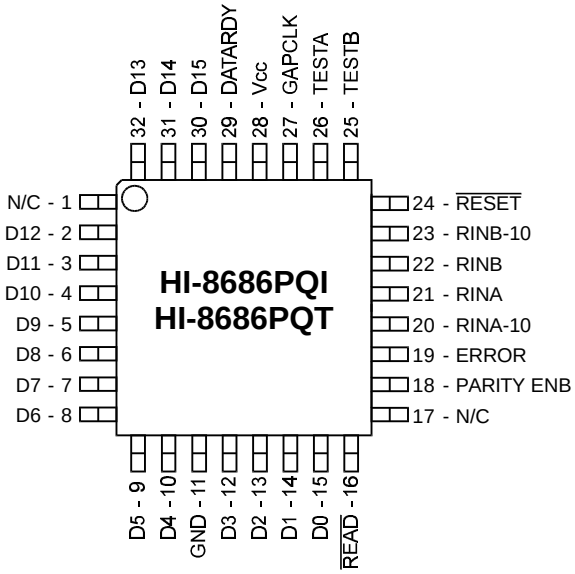
FEATURES

- Automatic conversion of serial ARINC 429, 575 & 561 data to 16-bit parallel data
- High speed parallel 16-bit data bus
- Error detection - word length and parity
- Reset input for power-on initialization
- On-chip line receiver
- Input hysteresis of at least 2 volts
- Test Inputs bypass analog inputs
- Simplified lightning protection with the ability to add 10 Kohm external series resistors
- Small, surface mount, plastic package options: SOIC, TQFP and PLCC
- Military processing available

PIN CONFIGURATIONS (Top View)



HI-8685
28-Pin Plastic SOIC - WB Package



HI-8686
32-Pin PlasticTQFP Package

(See page 8 for additional pin configurations)

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
DATA RDY	OUTPUT	Receiver data ready flag. A high level indicates data is available in the receive buffer. Flag goes low when the first 16-bit byte is read.
D0 to D15	OUTPUT	16-bit parallel data bus (tri-state)
GND	POWER	0V
$\overline{\text{READ}}$	INPUT	Read strobe. A low level transfers receive buffer data to the data bus
PARITY ENB	INPUT	Parity Enable - A high level activates odd parity checking which replaces the 32nd ARINC bit with an error bit. Otherwise, the 32nd ARINC bit is unchanged
ERROR	OUTPUT	Error Flag. A high level indicates a bit count error (number of ARINC bits was less than or greater than 32) and/or a parity error if parity detection was enabled (PARITY ENB high)
RINA/RINA-10	INPUT	Positive direct ARINC serial data input (both RINA and RINA-10 on HI-8686)
RINB/RINB-10	INPUT	Negative direct ARINC serial data input (both RINB and RINB-10 on HI-8686)
$\overline{\text{RESET}}$	INPUT	Internal logic states are initialized with a low level
TESTA	INPUT	Used in conjunction with the TESTB input to bypass the built-in analog line receiver circuitry
TESTB	INPUT	Used in conjunction with the TESTA input to bypass the built-in analog line receiver circuitry
GAPCLK	INPUT	Gap Clock. Determines the minimum time required between ARINC words for detection. The minimum word gap time is between 16 and 17 clock cycles of this signal.
Vcc	POWER	+5V ±10% supply

FUNCTIONAL DESCRIPTION

The HI-8685 and HI-8686 are serial to 16-bit parallel converters. The incoming data stream is serially shifted into an input register, checked for errors, and then transferred in parallel to a 32-bit receive buffer. The receive data can be accessed using two 16-bit parallel read operations while the next serial data steam is being received.

RECEIVER INPUTS

The block diagram for both the HI-8685 and HI-8685-10 products is found in Figure 1. Both have built-in receivers eliminating the need for additional external ARINC level detection circuitry. The only difference between the two products is the amount of internal resistance in series with each ARINC input.

HI-8685 ARINC INPUTS (RINA & RINB)

Typically 35KΩ resistors are in series with both the RINA and RINB ARINC 429 inputs. They connect to level translators whose resistance to GND is typically 10KΩ. After level translation, the buffered inputs drive a differential amplifier. The differential signal is compared to levels derived from a divider between VCC and GND. The nominal settings correspond to a One/Zero amplitude of 6.0V and a Null amplitude of 3.3V. A valid ARINC One/Zero input sets a latch and a Null input resets the latch.

HI-8685-10 ARINC INPUTS (RINA-10 & RINB-10)

Since any added external series resistance will affect the voltage translation, the HI-8685-10 product has only 25KΩ of the 35KΩ series resistance required for proper ARINC 429 level detection. The remaining 10KΩ required is available to the user for incorporation in external circuitry such as for lightning protection.

HI-8686 ARINC INPUTS

The HI-8686 has both sets of ARINC inputs, RINA/RINA-10 and RINB/RINB-10 available to the user.

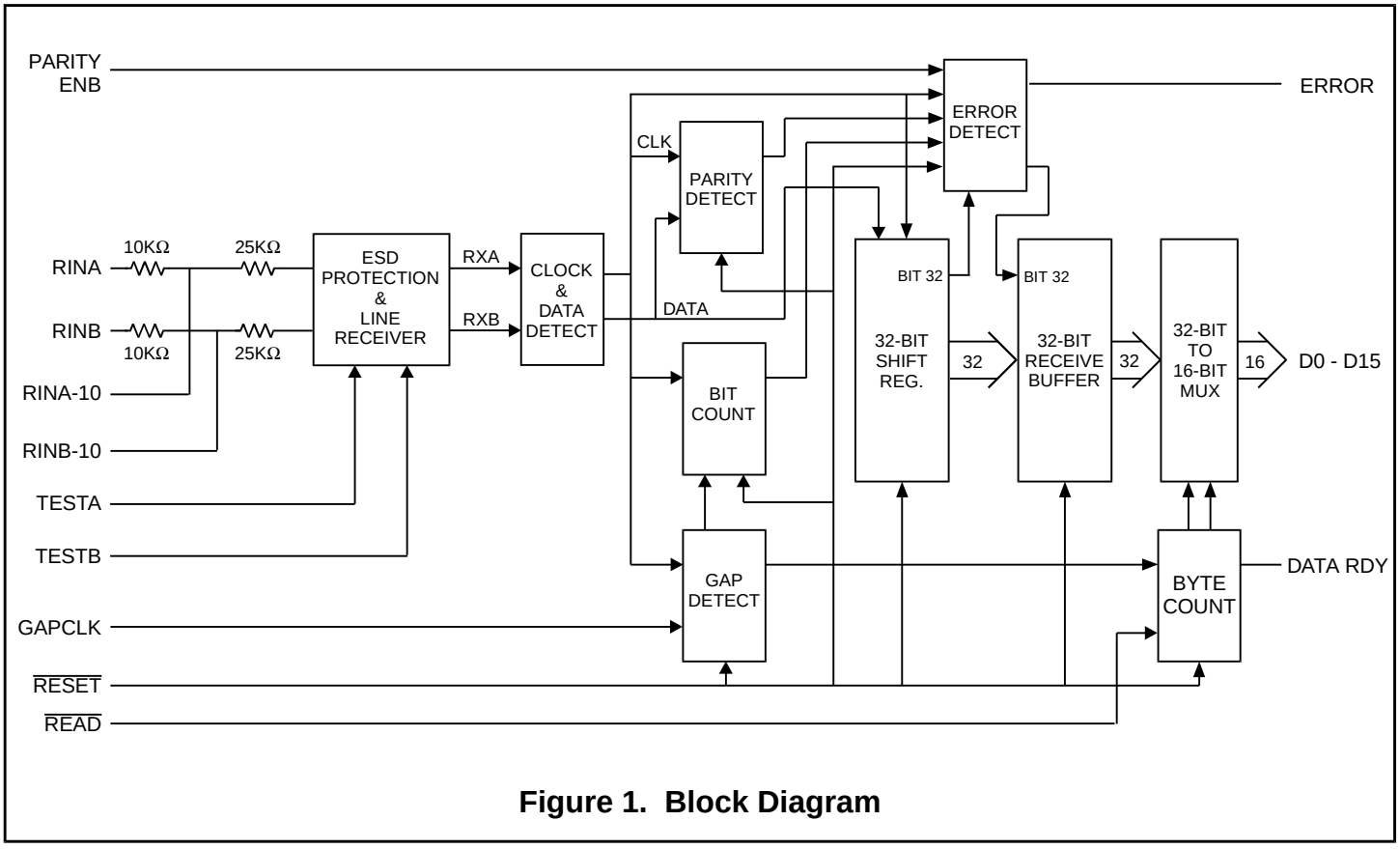


Figure 1. Block Diagram

FUNCTIONAL DESCRIPTION (cont.)

PROTOCOL DETECTION

The ARINC clock and One/Zero data that are derived from the digital outputs of the built-in line receiver is illustrated in Figure 3. The resulting steam of digital data is shifted into a 32-bit input register.

The ARINC clock and One/Zero data can also be created from the TESTA and TESTB inputs as shown in Figure 4. When either test input is high, the built-in analog line driver is disabled.

For ARINC 561 operation, the TESTA and TESTB digital input data streams must be derived from the ARINC 561 data, clock and sync with external logic.

GAP DETECTION

The end of a data word is detected by an internal counter that times out when a data One or Zero is not received for a period equal to 16 cycles of the GAPCLK signal. The gap detection time may vary between 16 and 17 cycles of the GAPCLK signal since the incoming data and GAPCLK are not usually synchronous inputs. The required frequency of GAPCLK is a function of the mininum gap time specified for the type of ARINC data being received. Table 1 indicates typical frequencies that may be used for the various data rates normally encountered.

DATABUS TYPE	BIT PERIOD (μs)	MINIMUM GAP (μs)	GAP CLOCK MHz	GAP DETECTION TIME (μs)
429	10	45	0.75 1.0 1.5	21.3 - 22.7 16 - 17 10.7 - 11.3
429	69 - 133	310 - 599	0.1	160 - 170
575	69 - 133	310 - 599	0.1	160 - 170
561	69 - 133	103 - 200	0.2	80 - 85

Table 1 - Typical Gap Detection Times

FUNCTIONAL DESCRIPTION (cont.)

ERROR CHECKING

Once a word gap is detected, the data word in the input register is transferred to the receive buffer and checked for errors.

When parity detection is enabled (PARITY ENB high), the received word is checked for odd parity. If there is a parity error, the 32nd bit of the received data word is set high.

If parity checking is disabled (PARITY ENB low) the 32nd bit of the data word is always the 32nd ARINC bit received.

The ERROR flag output is set high upon receipt of a word gap and the number of bits received since the previous word gap is less than or greater than 32. The ERROR flag is reset low when the next valid ARINC word is written into the receive buffer or when $\overline{\text{RESET}}$ is pulsed low.

READING RECEIVE BUFFER

When the data word is transferred to the receive buffer, the DATA RDY pin goes high. The data word can then be read in two 16-bit bytes by pulsing the $\overline{\text{READ}}$ input low as indicated in Figure 5. The first read cycle resets DATA RDY low and increments an internal counter to the second 16-bit byte. The relationship between each bit of an ARINC word received and each bit of the two 16-bit data bus bytes is specified in Figure 2.

When a new ARINC word is received it always overwrites the receive buffer. If the first byte of the previous word has not been read, then previous data is lost and the receive buffer will contain the new ARINC word. However, if the DATA RDY pin goes high between the reading of the first and second bytes, the first byte is no longer valid because the corresponding second byte has been overwritten by the new ARINC word. Also, the next read will be of the first byte of the new ARINC word since the internal byte counter is always reset to the first byte when new data is transferred to the receive buffer.

Read	Byte	Data Bus Bits	ARINC Bits
1st	Byte 1	D0 - D15	ARINC 1 - ARINC 16
2nd	Byte 2	D0 - D15	ARINC 17 - ARINC 32

FIGURE 2. ORDER OF RECEIVED DATA

RESET

A low on the $\overline{\text{RESET}}$ input sets a flip-flop which initializes the internal logic. When $\overline{\text{RESET}}$ goes high, the internal logic remains in the initialized state until the first word gap is detected preventing reception of a partial word.

TEST MODE

The built-in differential line receiver can be disabled allowing the data and clock detection circuitry to be driven directly with digital signals. The logical OR function of the TESTA and TESTB is defined in Truth Table 1. The two inputs can be used for testing the receiver logic and for inputting ARINC 429 type data derived from another source/ protocol. See Figure 4 for typical test input timing.

The device should always be initialized with $\overline{\text{RESET}}$ immediately after entering the test mode to clear a partial word that may have been received since the last word gap. Otherwise, an ERROR condition may occur and the first 32 bits of data on the test inputs may not be properly received.

Also, when entering the test mode, both TESTA and TESTB should be set high and held in that state for at least one word gap period (17 gap clocks) after $\overline{\text{RESET}}$ goes high.

When exiting the test mode, both test inputs should be held low and the device initialized with $\overline{\text{RESET}}$.

TRUTH TABLE 1.

RINA (-10)	RINB (-10)	TESTA	TESTB	RXA	RXB
-1.50V to +1.50V	-1.50V to +1.50V	0	0	0	0
-3.25V to -6.50V	+3.25V to +6.50V	0	0	0	1
+3.25V to +6.50V	-3.25V to -6.50V	0	0	1	0
X	X	0	1	0	1
X	X	1	0	1	0
X	X	1	1	0	0

X = don't care

TIMING DIAGRAMS

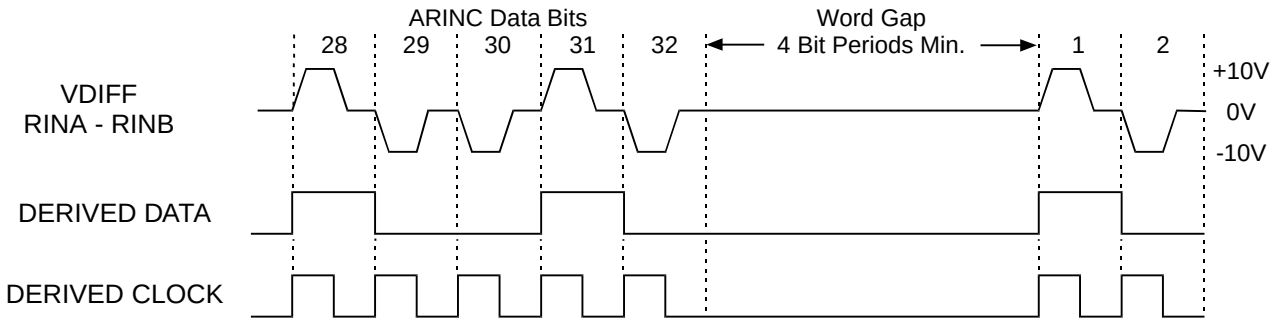


FIGURE 3 - RECEIVER INPUT TIMING FOR ARINC 429

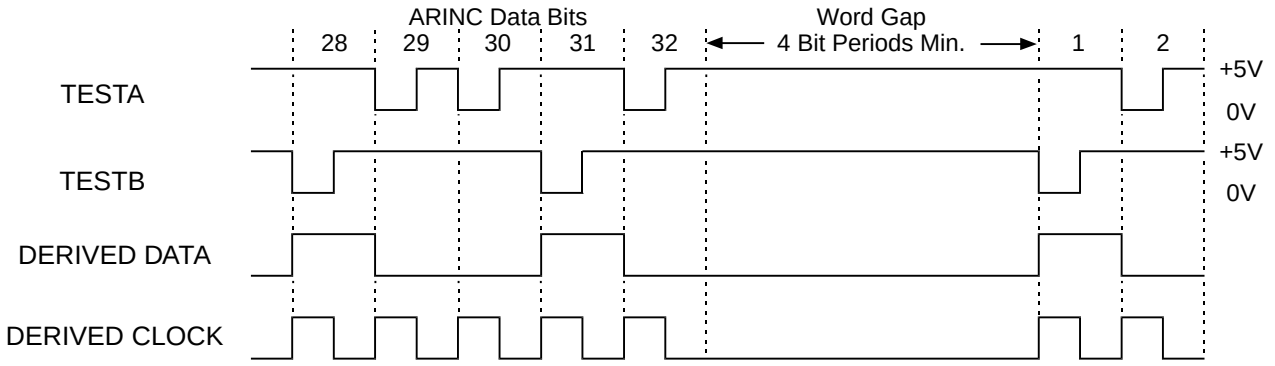


FIGURE 4 - TEST INPUT TIMING FOR ARINC 429

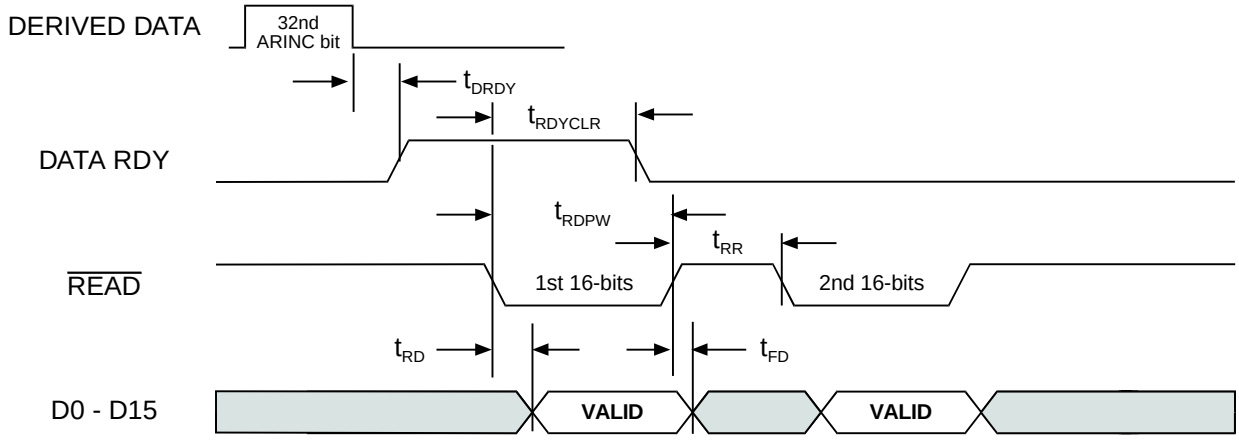


FIGURE 5 - RECEIVER PARALLEL DATABUS TIMING

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND

Supply voltages
V_{CC} ..... +7.0V

Voltage on inputs
RINA (-10) to RINB (-10) ..... +29V to - 29V
All other input pins.....-0.3 to Vcc +0.3

DC current per input pin ..... +10mA

Power dissipation at 25°C
plastic 28-pin SO..... 1.8W, derate 14.1mW/°C
plastic 28-pin PLCC .2.3W, derate 18.2mW/°C
plastic 32-pin SO.....1.6W, derate 15.4mW/°C

Solder Temperature
Leads ..... +280°C for 10 sec
Package body .....+220°C

Storage Temperature ..... -65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
V_{CC}.....+5V ± 10%

Temperature Range
Industrial Screening ..... -40°C to +85°C
Hi-Temp Screening ..... -55°C to +125°C
Military Screening.....-55°C to +125°C

Junction Temperature, Tj ..... ≤+175°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ARINC Bus Inputs (RINA, RINB, RINA-10 & RINB-10)						
Differential input voltage						
one or zero	V_{DIN}	differential voltage	6.5	10.0	13.0	volts
null	V_{NIN}	" " " "	-	-	2.75	volts
common mode	V_{COM}	with respect to GND	-	-	5.0	volts
Input resistance						
RINA (-10) to RINB(-10)	R_{DIFF}	supplies floating	30	75	-	Kohm
RINA (-10) or RINB(-10) to GND or V_{CC}	R_{SUP}	" " " '	19	40	-	Kohm
Input capacitance (Guaranteed but not tested)						
differential	C_{DIFF}	RINA (-10) to RINB (-10)	-	-	20	pF
to GND	C_G		-	-	20	pF
to V_{CC}	C_H		-	-	20	pF

DC ELECTRICAL CHARACTERISTICS (cont.)

Vcc = 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digital Inputs ($\overline{\text{RESET}}$, GAPCLK, $\overline{\text{READ}}$, PARITY ENA, TESTA & TESTB)						
Input voltage high low	 V_{IH} V_{IL}		 2.0 0.0	 - -	 V_{CC} 0.8	 volts volts
Input current source sink	 I_{IH} I_{IL}	 V_{IN} = 5.0V V_{IN} = 0.0V	 - -1.0	 - -	 1.0 -	 µA µA
Input capacitance	C_I		-	-	8.0	pF
Outputs (D0 to D15, ERROR & DATA RDY)						
Output voltage high low	 V_{OH} V_{OL}	 I_{OH} = -1.0 mA I_{OL} = 1.6 mA	 2.7 -	 - -	 - 0.4	 volts volts
Output tri-state current (D0 - D15 only)	 I_{IH} I_{IL}	 V_{OH} = 5.0V V_{OL} = 0.0V	 - -1.0	 - -	 1.0 -	 µA µA
Output capacitance	C_O		-	-	15	pF
Operating Supply Current						
V_{CC}	I_{CC}	V_{IN} = 0.0V, outputs open	-	-	6.5	mA

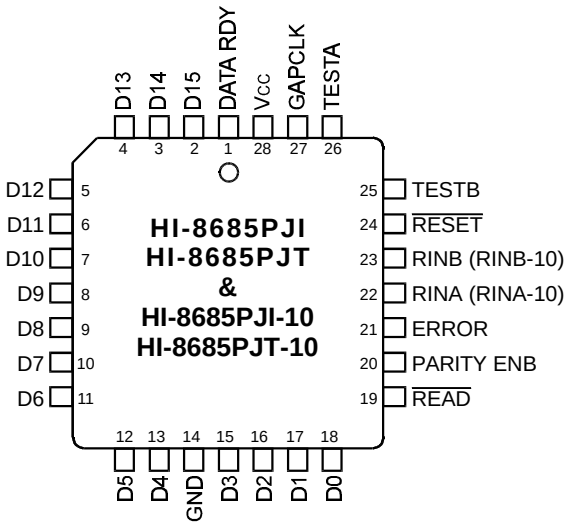
AC ELECTRICAL CHARACTERISTICS

Vcc = 5V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{READ}}$ pulse width	t_{RDPW}		50			ns
Data delay from $\overline{\text{READ}}$	t_{RD}				20	ns
$\overline{\text{READ}}$ to data floating	t_{FD}				20	ns
$\overline{\text{READ}}$ to DATA RDY clear	t_{RDYCLR}				25	ns
$\overline{\text{READ}}$ pulse to next $\overline{\text{READ}}$ pulse	t_{RR}		25			ns
GAPCLK frequency	f_{GC}			1		MHz
32nd ARINC bit to DATA RDY	t_{DRDY}		16		17	clocks

ADDITIONAL HI-8685 PIN CONFIGURATION

(See page 1 for additional pin configurations)



HI-8685
28-Pin Plastic PLCC

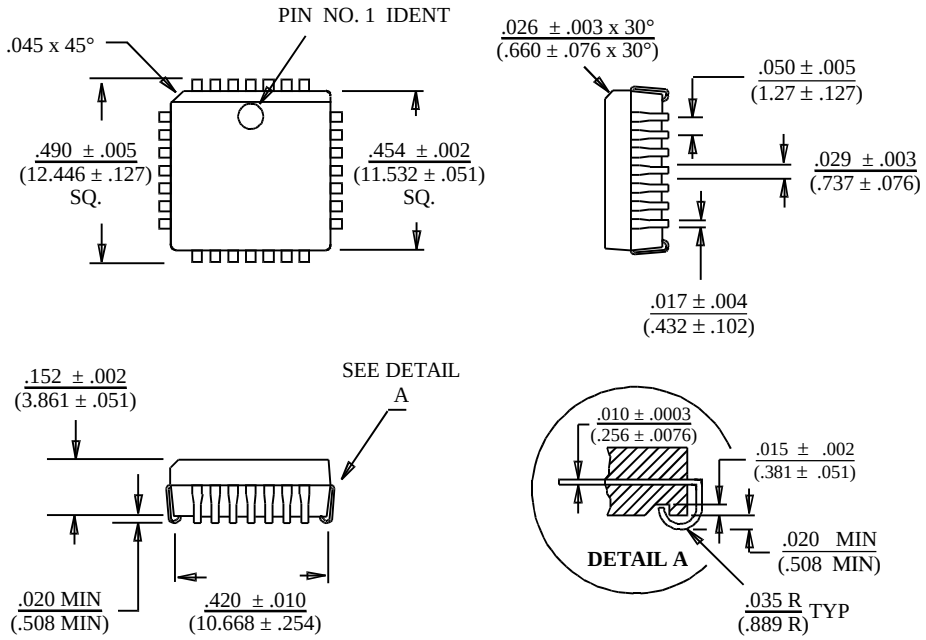
ORDERING INFORMATION

PART NUMBER	PACKAGE DESCRIPTION	BUILT-IN LINE RECV'R	EXT. 10KΩ REQUIRED	TEMPERATURE RANGE	FLOW	BURN IN	LEAD FINISH
HI-8685PJI	28 PIN PLASTIC PLCC	YES	NO	-40°C TO +85°C	I	NO	SOLDER
HI-8685PJT	28 PIN PLASTIC PLCC	YES	NO	-55°C TO +125°C	T	NO	SOLDER
HI-8685PSI	28 PIN PLASTIC SOIC - WB	YES	NO	-40°C TO +85°C	I	NO	SOLDER
HI-8685PST	28 PIN PLASTIC SOIC - WB	YES	NO	-55°C TO +125°C	T	NO	SOLDER
HI-8686PQI	32 PIN PLASTIC TQFP	YES	OPTIONAL	-40°C TO +85°C	I	NO	SOLDER
HI-8686PQT	32 PIN PLASTIC TQFP	YES	OPTIONAL	-55°C TO +125°C	T	NO	SOLDER
HI-8685PJI-10	28 PIN PLASTIC PLCC	YES	YES	-40°C TO +85°C	I	NO	SOLDER
HI-8685PJT-10	28 PIN PLASTIC PLCC	YES	YES	-55°C TO +125°C	T	NO	SOLDER
HI-8685PSI-10	28 PIN PLASTIC SOIC - WB	YES	YES	-40°C TO +85°C	I	NO	SOLDER
HI-8685PST-10	28 PIN PLASTIC SOIC - WB	YES	YES	-55°C TO +125°C	T	NO	SOLDER

Legend: WB - Wide Body

28-PIN PLASTIC PLCC

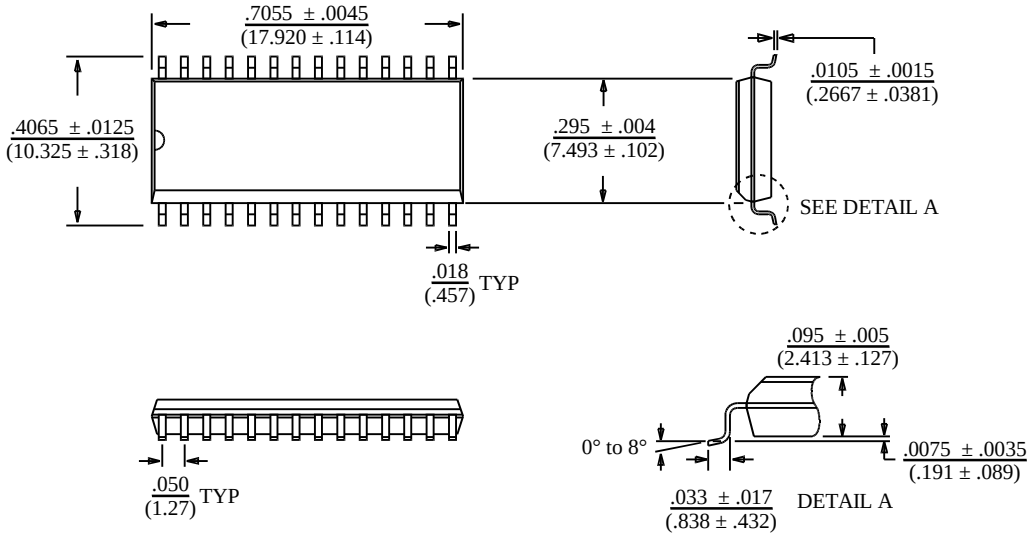
Package Type: 28J



28-PIN PLASTIC SMALL OUTLINE (SOIC) - WB

(Wide Body)

Package Type: 28HW



32 PIN PLASTIC THIN QUAD FLAT PACK (TQFP)

Package Type: 32PTQS