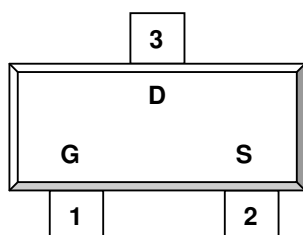


DESCRIPTION

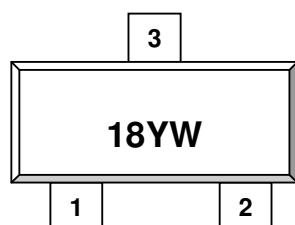
ST2318SRG is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION SOT-23



1.Gate 2.Source 3.Drain

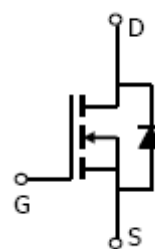
PART MARKING SOT-23



Y: Year Code W: Week Code

FEATURE

- 40V/3.9A, $R_{DS(ON)} = 42m\Omega$ (Typ.) @VGS = 10V
- 40V/3.5A, $R_{DS(ON)} = 53m\Omega$ @VGS = 4.5V
- 40V/2.0A, $R_{DS(ON)} = 75 m\Omega$ @VGS = 2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design





ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	40	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	3.9 3.0	A
Pulsed Drain Current		I _{DM}	10	A
Continuous Source Current (Diode Conduction)		I _S	1.20	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	1.20 0.8	W
Operation Junction Temperature		T _J	150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	100	°C/W



ST2318SRG
N Channel Enhancement Mode MOSFET

3.9A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

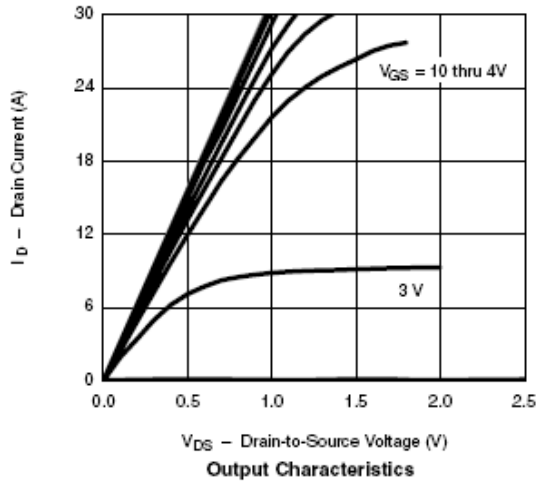
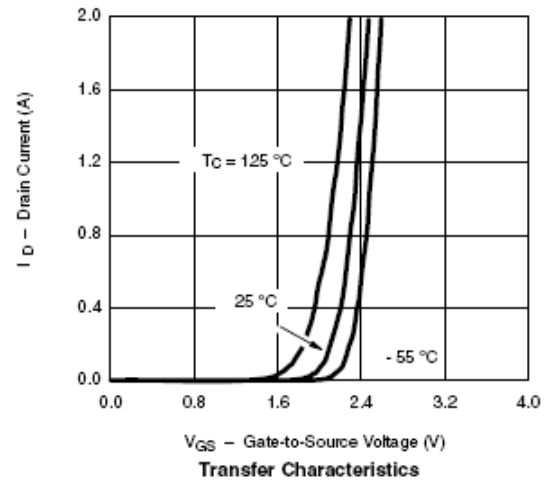
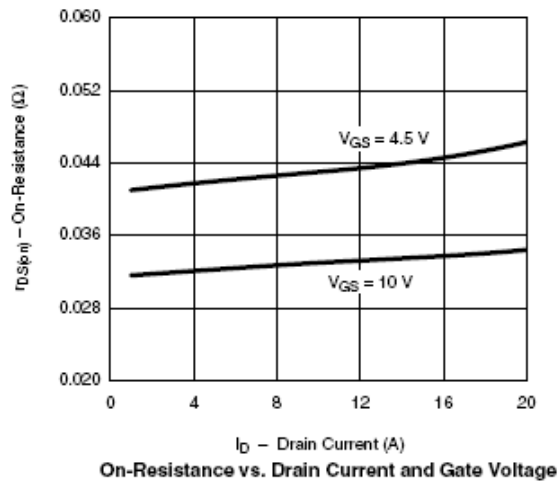
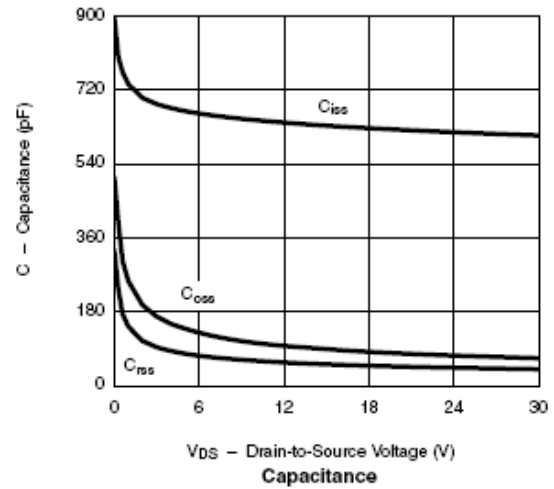
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.50		1.2	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$			1	uA
		$V_{DS}=40V, V_{GS}=0V$ $T_J=85^{\circ}C$			5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.9A$ $V_{GS}=4.5V, I_D=3.5A$ $V_{GS}=2.5V, I_D=2.0A$		0.042 0.053 0.075		Ω
Forward Transconductance	g_{fs}	$V_{DS}=15V, I_D=6.2A$		13		S
Diode Forward Voltage	V_{SD}	$I_S=2.3A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V$ $V_{GS}=10V$ $I_D\equiv 2.0A$		16	24	nC
Gate-Source Charge	Q_{gs}			3		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=15V$ $R_L=15\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		15	20	nS
Turn-Off Time	$t_{d(off)tf}$			6	12	
				10	20	
				40	80	

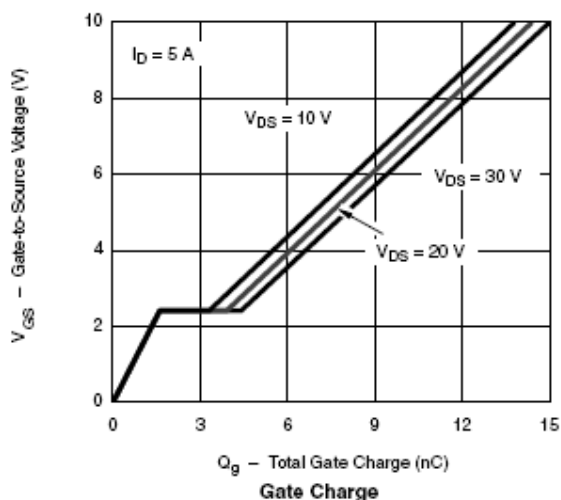
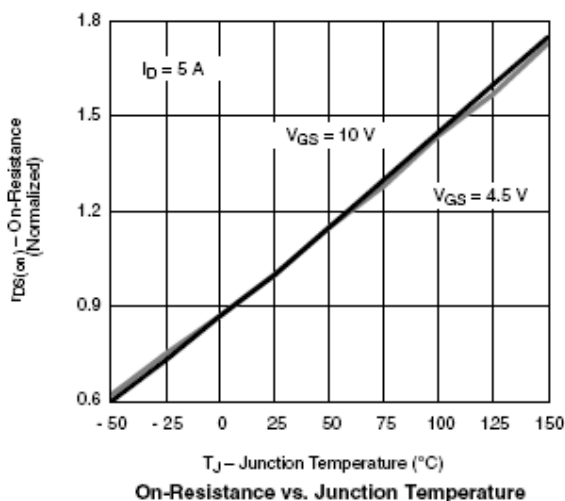
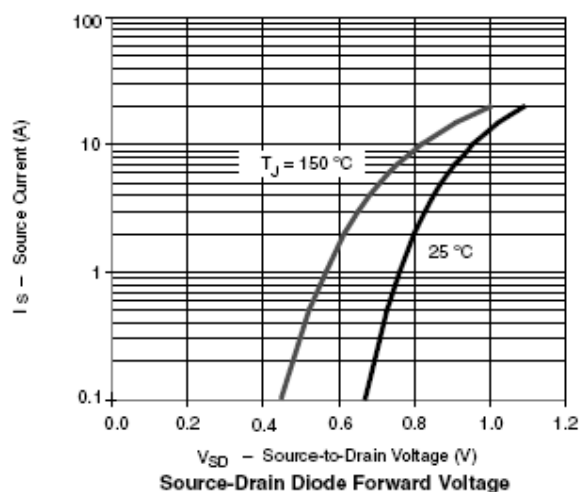
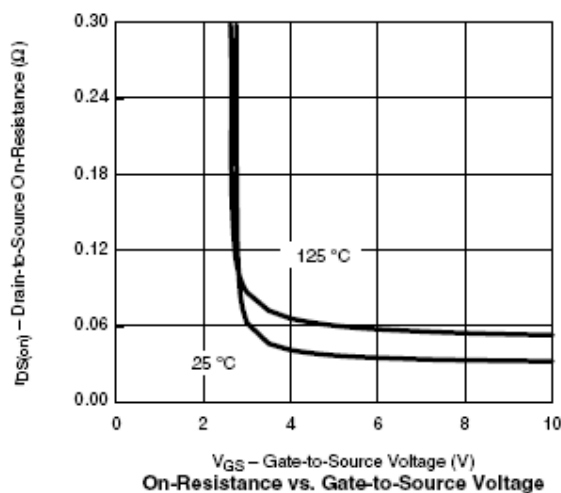


ST2318SRG
N Channel Enhancement Mode MOSFET

3.9A

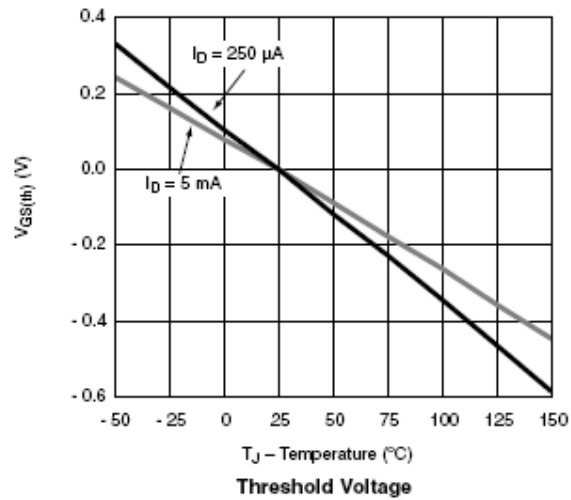
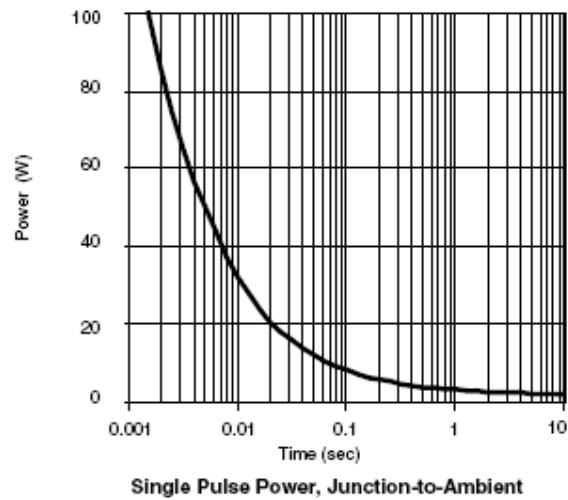
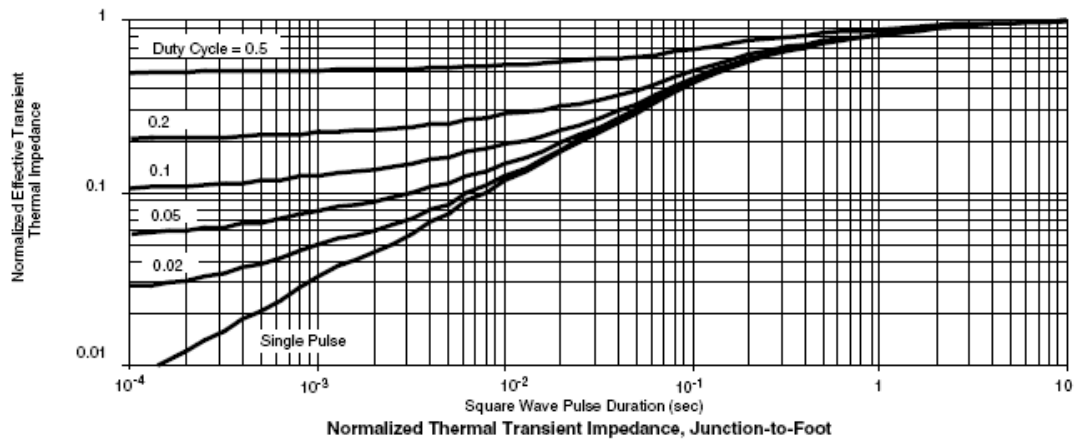
TYPICAL CHARACTERISTICS (25°C Unless noted)



TYPICAL CHARACTERISTICS (25°C Unless noted)


**ST2318SRG**

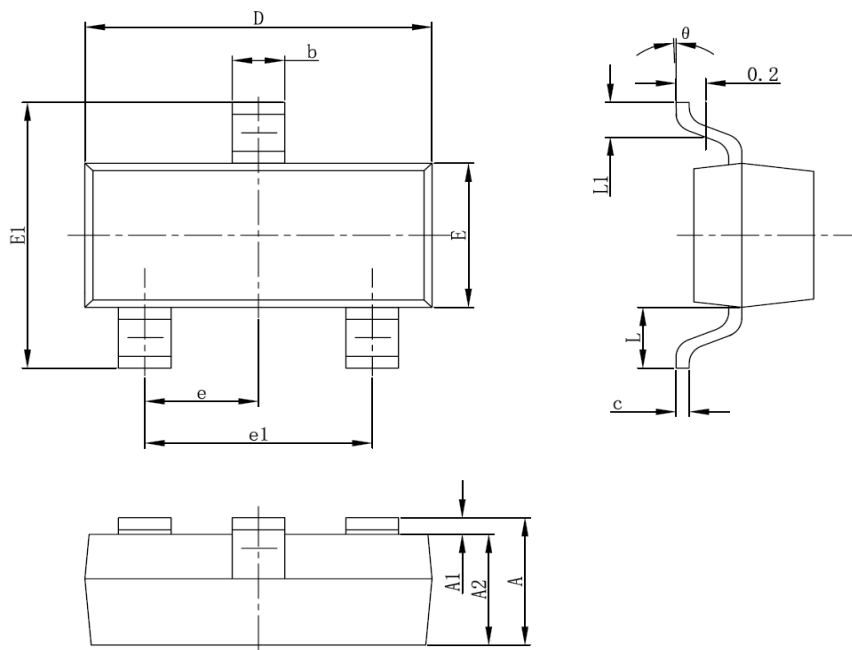
N Channel Enhancement Mode MOSFET

3.9A**TYPICAL CHARACTERISTICS (25°C Unless noted)**

STANSON TECHNOLOGY
120 Bentley Square, Mountain View, Ca 94040 USA
www.stansontech.com

ST2318SRG 2009. V1

SOT-23 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°