DRAM

MT4LC4M4B1, MT4C4M4B1
MT4LC4M4A1, MT4C4M4A1

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/mti/msp/html/datasheet.html

FEATURES

- Industry-standard x4 pinout, timing, functions, and packages
- High-performance, low-power CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or +5V ±0.5V)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE-RAS# (CBR)
- Optional self refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- FAST-PAGE-MODE (FPM) access
- 5V tolerant inputs and I/Os on 3.3V devices

OPTIONS — MARKING

- Voltage
  - 3.3V — LC
  - 5V — C
- Refresh Addressing
  - 2,048 (2K) rows — B1
  - 4,096 (4K) rows — A1
- Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic TSOP (300 mil) — TG
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Refresh Rates
  - Standard Refresh — None
  - Self Refresh (128ms period) — S*

NOTE: 1. The 4 Meg x 4 FPM DRAM base number differentiates the offerings in one place—MT4LC4M4B1. The fifth field distinguishes various options: B1 designates a 2K refresh and A1 designates a 4K refresh for FPM DRAMs.
2. The # symbol indicates signal is active LOW.

*Contact factory for availability

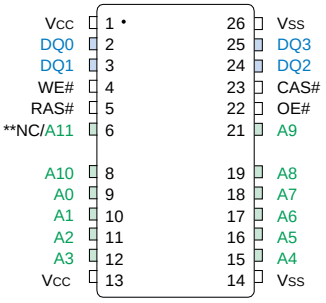
Part Number Example:
MT4LC4M4B1DJ

KEY TIMING PARAMETERS

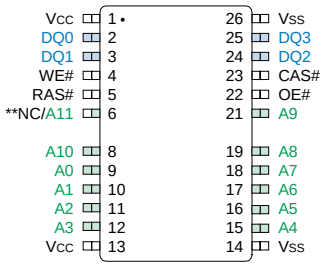
SPEED	tRC	tRAC	tPC	tAA	tCAC	tRP
-5	84ns	50ns	20ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ



24/26-Pin TSOP



**NC on 2K refresh and A11 on 4K refresh options.

4 MEG x 4 FPM DRAM PART NUMBERS

PART NUMBER	Vcc	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC4M4B1DJ-6	3.3V	2K	SOJ	Standard
MT4LC4M4B1DJ-6S	3.3V	2K	SOJ	Self
MT4LC4M4B1TG-6	3.3V	2K	TSOP	Standard
MT4LC4M4B1TG-6S	3.3V	2K	TSOP	Self
MT4LC4M4A1DJ-6	3.3V	4K	SOJ	Standard
MT4LC4M4A1DJ-6S	3.3V	4K	SOJ	Self
MT4LC4M4A1TG-6	3.3V	4K	TSOP	Standard
MT4C4M4A1TG-6S	3.3V	4K	TSOP	Self
MT4C4M4B1DJ-6	5V	2K	SOJ	Standard
MT4C4M4B1DJ-6S	5V	2K	SOJ	Self
MT4C4M4B1TG-6	5V	2K	TSOP	Standard
MT4C4M4B1TG-6S	5V	2K	TSOP	Self
MT4C4M4A1DJ-6	5V	4K	SOJ	Standard
MT4C4M4A1DJ-6S	5V	4K	SOJ	Self
MT4C4M4A1TG-6	5V	4K	TSOP	Standard
MT4C4M4A1TG-6S	5V	4K	TSOP	Self

GENERAL DESCRIPTION

The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address (the latter 11 bits for 2K and the latter 10 bits for 4K; address pins A10 and A11 are "Don't Care").

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pins remain open (High- Z) until the next CAS# cycle, regardless of OE#.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

The MT4LC4M4B1 and MT4LC4M4A1 must be refreshed periodically in order to retain stored data.

FAST PAGE MODE ACCESS

Page operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The page cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the page mode of operation, i.e., closes the page.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR, or HIDDEN) so that all combinations of RAS# addresses (2,048 for 2K and 4,096 for 4K) are executed within ^{t}REF (MAX), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

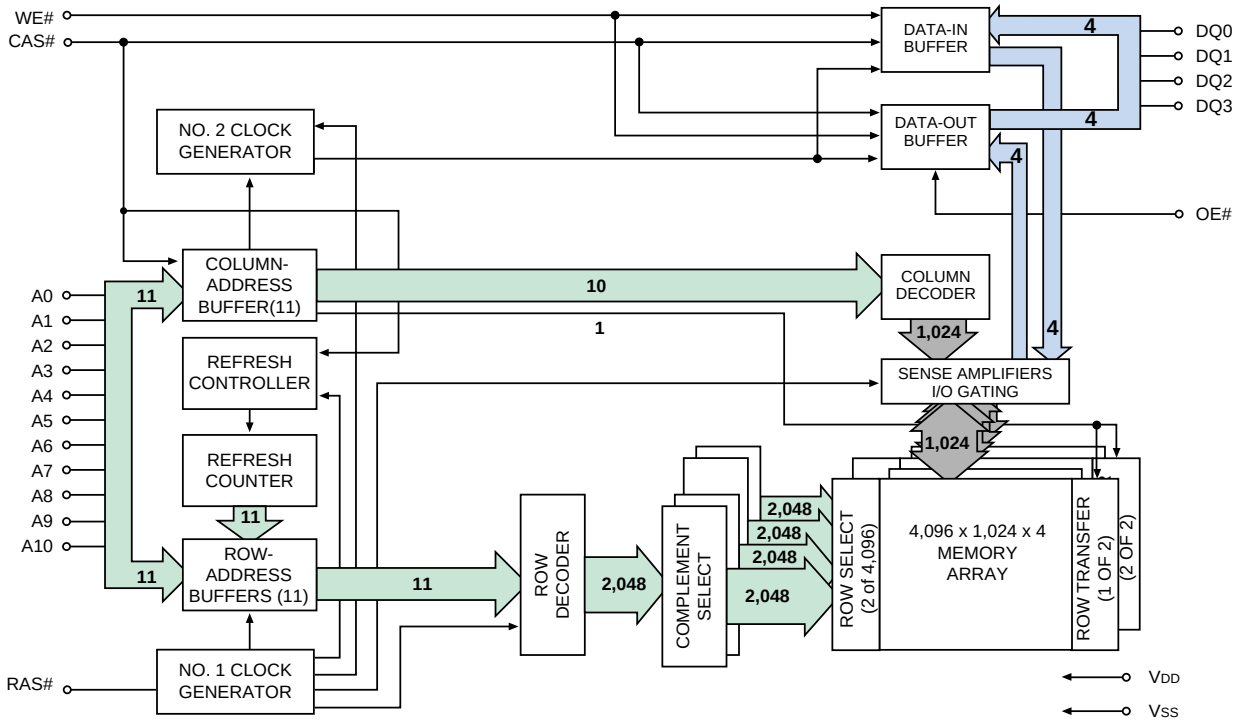
An optional self refresh mode is also available the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 31.25µs per row for a 4K refresh and 62.5µs per row for a 2K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes RAS#-ONLY or burst CBR refresh sequence, all rows must be refreshed with a refresh rate of ^{t}RC minimum prior to resuming normal operation.

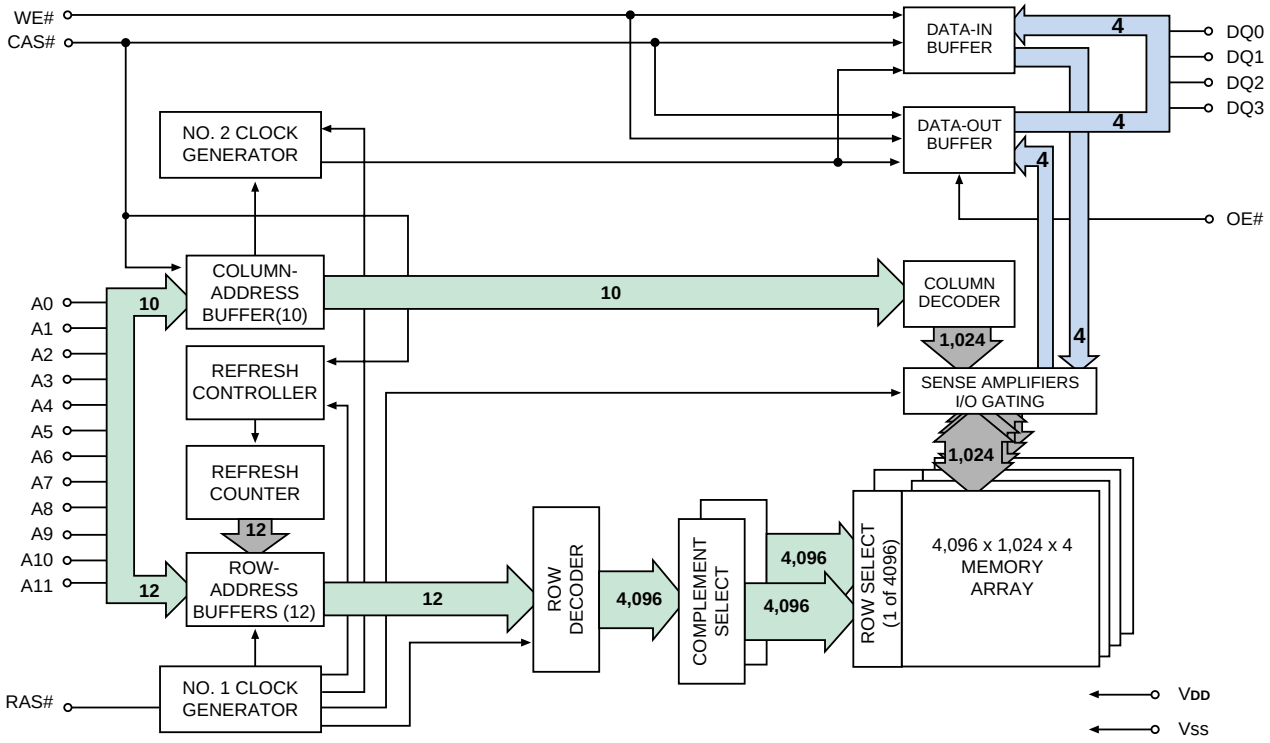
STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

FUNCTIONAL BLOCK DIAGRAM – 2K REFRESH



FUNCTIONAL BLOCK DIAGRAM – 4K REFRESH



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS}
- 3.3V ..... -1V to +4.6V
- 5V ..... -1V TO +7V

Voltage on NC, Inputs or I/O Pins Relative to V_{SS}
- 3.3V ..... -1V to +5.5V
- 5V ..... -1V TO +7V

Operating Temperature, T_A (ambient) .... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 5, 6) (V_{CC} (MIN) ≤ V_{CC} ≤ V_{CC} (MAX))

PARAMETER/CONDITION	SYMBOL	3.3V		5V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
SUPPLY VOLTAGE	V_{CC}	3	3.6	4.5	5.5	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2	5.5	2.4	Vcc+1	V	24
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-1.0	0.8	-0.5	0.8	V	24
INPUT LEAKAGE CURRENT: Any input at V_{IN} [0V ≤ V_{IN} ≤ V_{CC} (MAX)]; All other pins not under test = 0V	I_I	-2	2	-2	2	µA	
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA	V_{OH}	2.4	–	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA	V_{OL}	–	0.4	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} [0V ≤ V_{OUT} ≤ V_{CC} (MAX)]; DQ is disabled and in High-Z state	I_{OZ}	-5	5	-5	5	µA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 6) [Vcc (MIN) ≤ Vcc ≤ Vcc (MAX)]

PARAMETER/CONDITION	SYM	SPEED	3.3V		5V		UNITS	NOTES
			2K REFRESH	4K REFRESH	2K REFRESH	4K REFRESH		
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	ALL	1	1	1	1	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = V_{CC} - 0.2V)	I_{CC2}	ALL	500	500	500	500	mA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = V_{CC} - 0.2V)	I_{CC2}	ALL	150	150	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $^{t}RC = {}^{t}RC$ [MIN])	I_{CC3}	-5 -6	110 100	90 80	140 130	120 110	mA	23
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: $^{t}PC = {}^{t}PC$ [MIN])	I_{CC4}	-5 -6	110 100	100 90	110 100	100 90	mA	23
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: $^{t}RC = {}^{t}RC$ [MIN])	I_{CC5}	-5 -6	110 100	90 80	140 130	120 110	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: $^{t}RC = {}^{t}RC$ [MIN])	I_{CC6}	-5 -6	110 100	90 80	140 130	120 110	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^{t}RAS (MIN); WE# = V_{CC} - 0.2V; A0-A11, OE# and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC7}	ALL	300	300	300	300	µA	4, 7
		^{t}RC	62.5	31.25	62.5	31.25	µs	23
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# ≥ $^{t}RASS$ (MIN) and CAS# held LOW; WE# = V_{CC} - 0.2V; A0-A11, OE# and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	ALL	300	300	300	300	µA	4, 7

CAPACITANCE

(Note: 6)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Address pins	C_{I1}	5	pF
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF
Input/Output Capacitance: DQ	C_{IO}	7	pF

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) [Vcc (MIN) ≤ Vcc ≤ Vcc (MAX)]

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column address	^tAA		25		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Column address to WE# delay time	^tAWD	42		49		ns	18
Access time from CAS#	^tCAC		13		15	ns	
Column-address hold time	^tCAH	8		10		ns	
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	4
CAS# to output in Low-Z	^tCLZ	0		0		ns	22
CAS# precharge time	^tCP	8		10		ns	13
Access time from CAS# precharge	^tCPA		28		35	ns	
CAS# to RAS# precharge time	^tCRP	5		5		ns	
CAS# hold time	^tCSH	38		45		ns	
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	4
CAS# to WE# delay time	^tCWD	28		35		ns	18
WRITE command to CAS# lead time	^tCWL	8		10		ns	
Data-in hold time	^tDH	8		10		ns	19
Data-in setup time	^tDS	0		0		ns	19
Output disable	^tOD	0	12	0	15	ns	22
Output enable	^tOE		12		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	17, 22
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	20		25		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	47		56		ns	
Access time from RAS#	^tRAC		50		60	ns	
RAS# to column-address delay time	^tRAD	9		12		ns	15
Row-address hold time	^tRAH	9		10		ns	
RAS# pulse width	^tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	^tRASP	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	^tRASS	100		100		µs	
Random READ or WRITE cycle time	^tRC	84		104		ns	
RAS# to CAS# delay time	^tRCD	11		14		ns	14
READ command hold time (referenced to CAS#)	^tRCH	0		0		ns	16
READ command setup time	^tRCS	0		0		ns	
Refresh period (2,048 cycles)	^tREF		32		32	ms	
Refresh period (4,096 cycles)	^tREF		64		64	ms	

AC ELECTRICAL CHARACTERISTICS

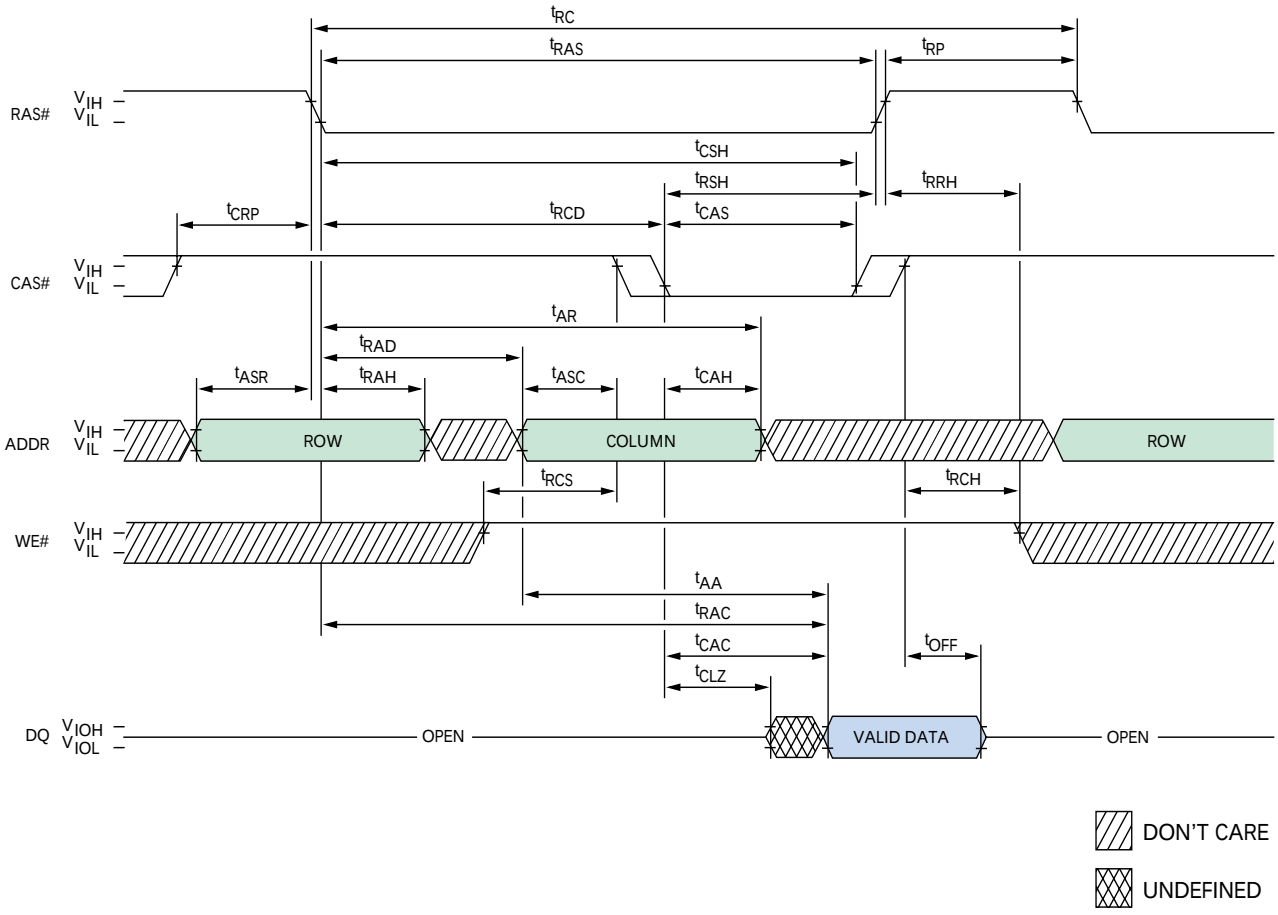
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) [Vcc (MIN) ≤ Vcc ≤ Vcc (MAX)]

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Refresh period "S" version	^{t}REF		128		128	ms	140
RAS# precharge time	^{t}RP	30		40		ns	
RAS# to CAS# precharge time	^{t}RPC	5		5		ns	
RAS# precharge time exiting Self Refresh	^{t}RPS	90		105		ns	
READ command hold time (referenced to RAS#)	^{t}RRH	0		0		ns	16
RAS# hold time	^{t}RSH	13		15		ns	
READ-WRITE cycle time	^{t}RWC	116		140		ns	
RAS# to WE# delay time	^{t}RWD	67		79		ns	19
WRITE command to RAS# lead time	^{t}RWL	13		15		ns	
Transition time (rise or fall)	^{t}T	2	50	2	50	ns	
WRITE command hold time	^{t}WCH	8		10		ns	
WRITE command hold time (referenced to RAS#)	^{t}WCR	38		45		ns	
WE# command setup time	^{t}WCS	0		0		ns	18
WRITE command pulse width	^{t}WP	5		5		ns	
WE# hold time (CBR Refresh)	^{t}WRH	8		10		ns	4, 23
WE# setup time (CBR Refresh)	^{t}WRP	8		10		ns	4, 23

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V or 5.0V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
14. The ^{t}RCD (MAX) limit is no longer specified. ^{t}RCD (MAX) was specified as a reference point only. If ^{t}RCD was greater than the specified ^{t}RCD (MAX) limit, then access time was controlled exclusively by ^{t}CAC (^{t}RAC [MIN] no longer applied). With or without the ^{t}RCD limit, ^{t}AA and ^{t}CAC must always be met.
15. The ^{t}RAD (MAX) limit is no longer specified. ^{t}RAD (MAX) was specified as a reference point only. If ^{t}RAD was greater than the specified ^{t}RAD (MAX) limit, then access time was controlled exclusively by ^{t}AA (^{t}RAC and ^{t}CAC no longer applied). With or without the ^{t}RAD (MAX) limit, ^{t}AA, ^{t}RAC, and ^{t}CAC must always be met.
16. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
17. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
18. ^{t}WCS, ^{t}RWD, ^{t}AWD, and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD, and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN), and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD, and ^{t}AWD are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. The 3ns minimum is a parameter guaranteed by design.
23. Column address changed once each cycle.
24. V_{IH} overshoot: V_{IH} (MAX) = V_{CC} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pu lse width cannot be greater than one third of the cycle rate.

READ CYCLE

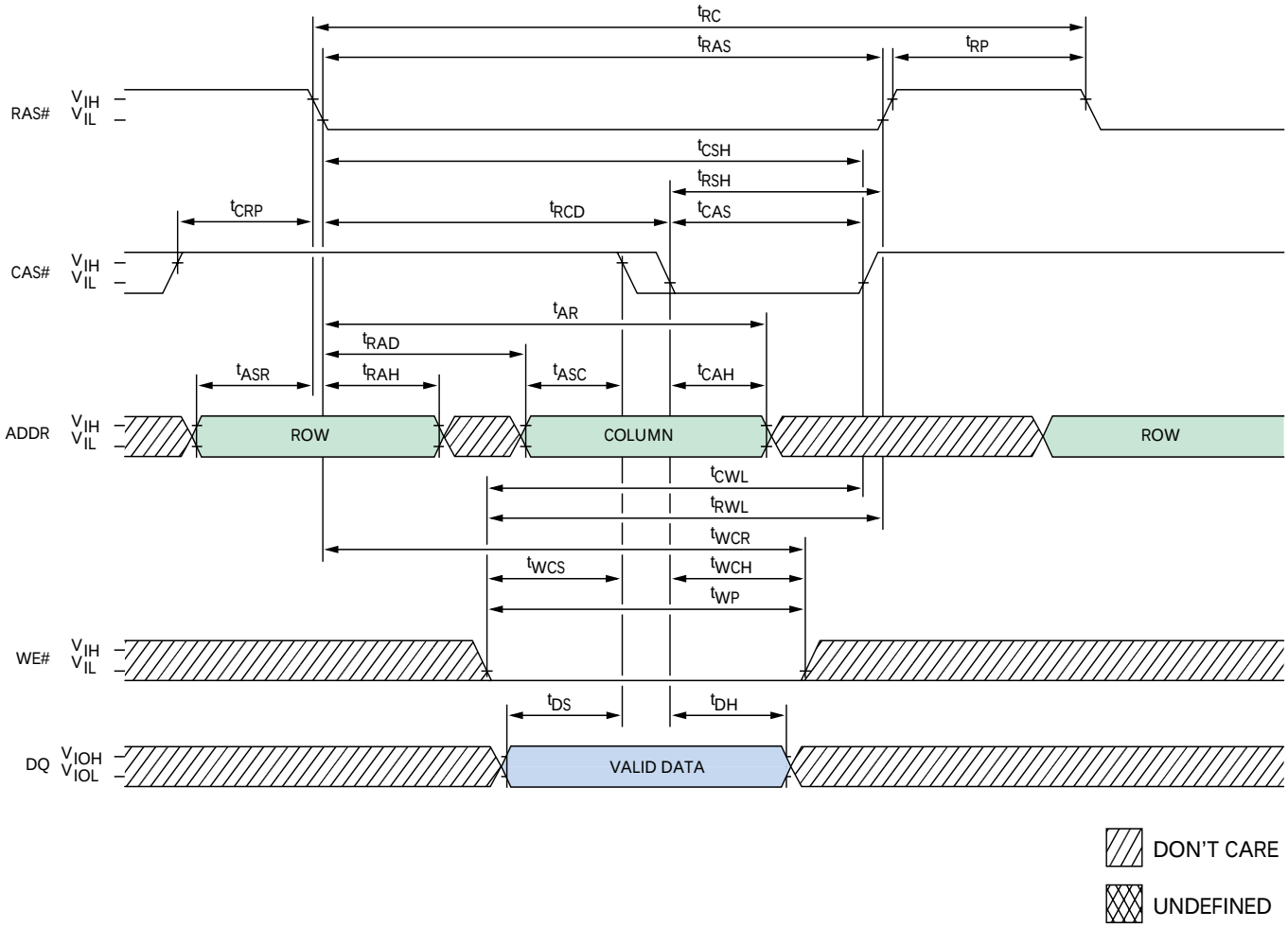


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	0	12	0	15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EARLY WRITE CYCLE

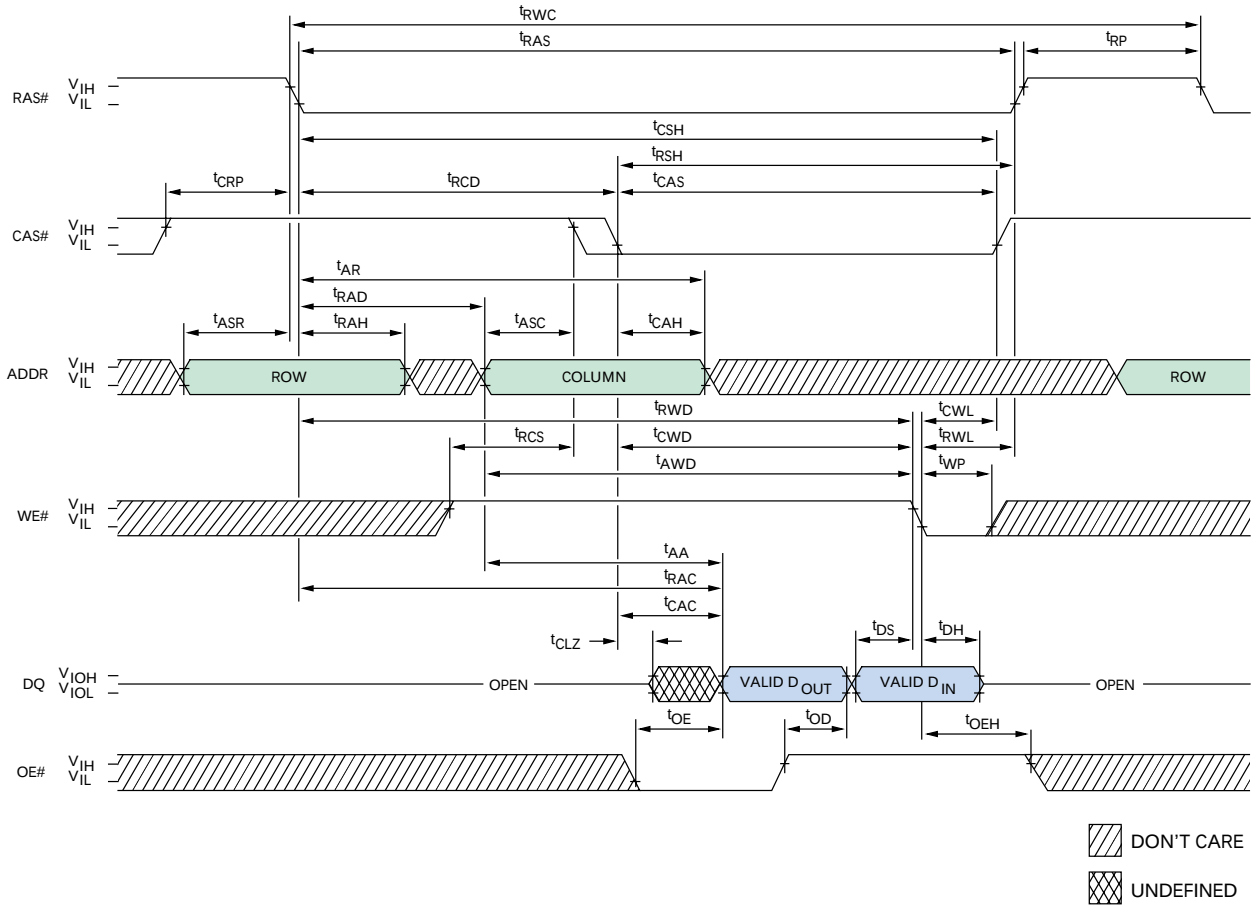


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD	9		12		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

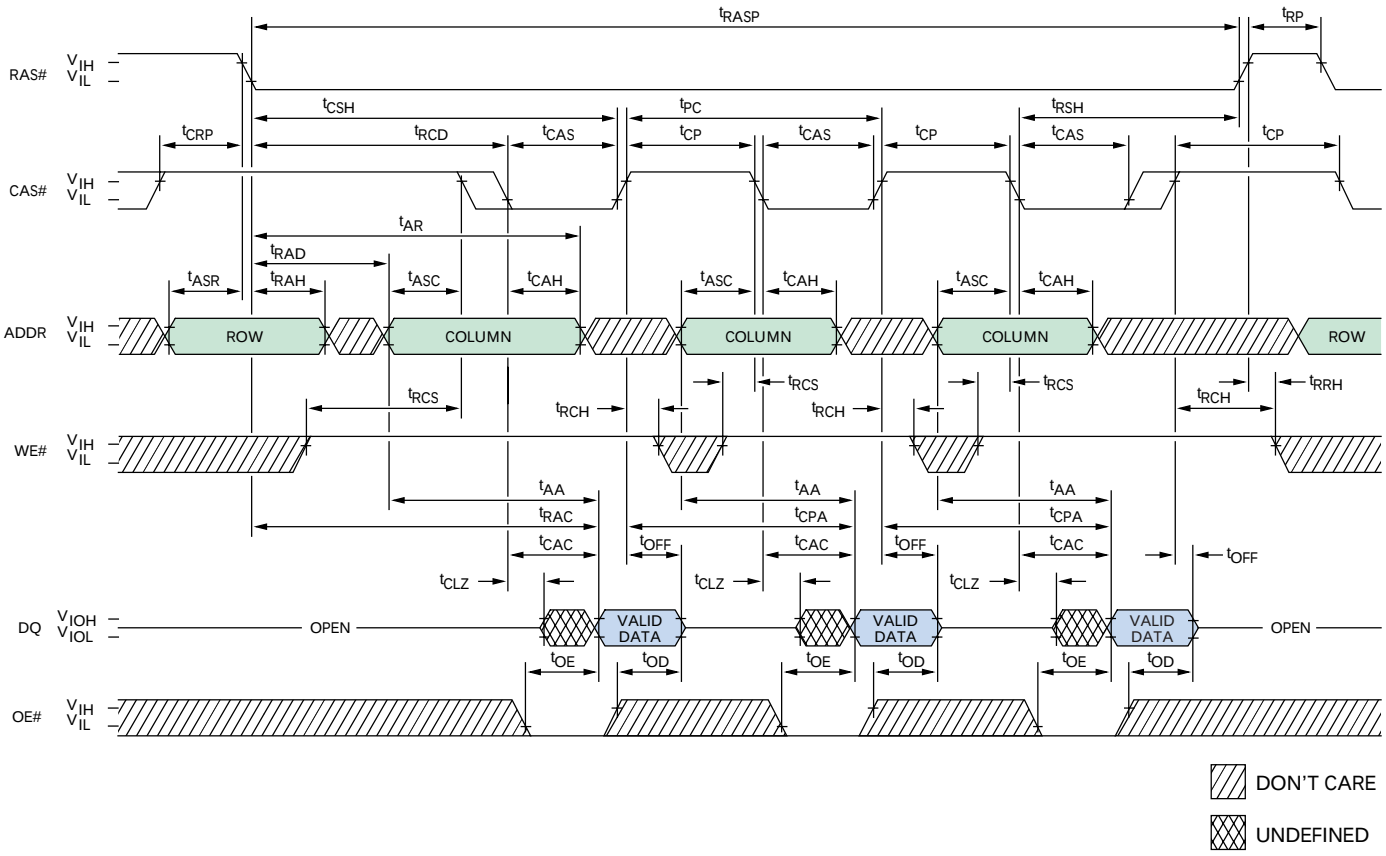


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

FAST-PAGE-MODE READ CYCLE

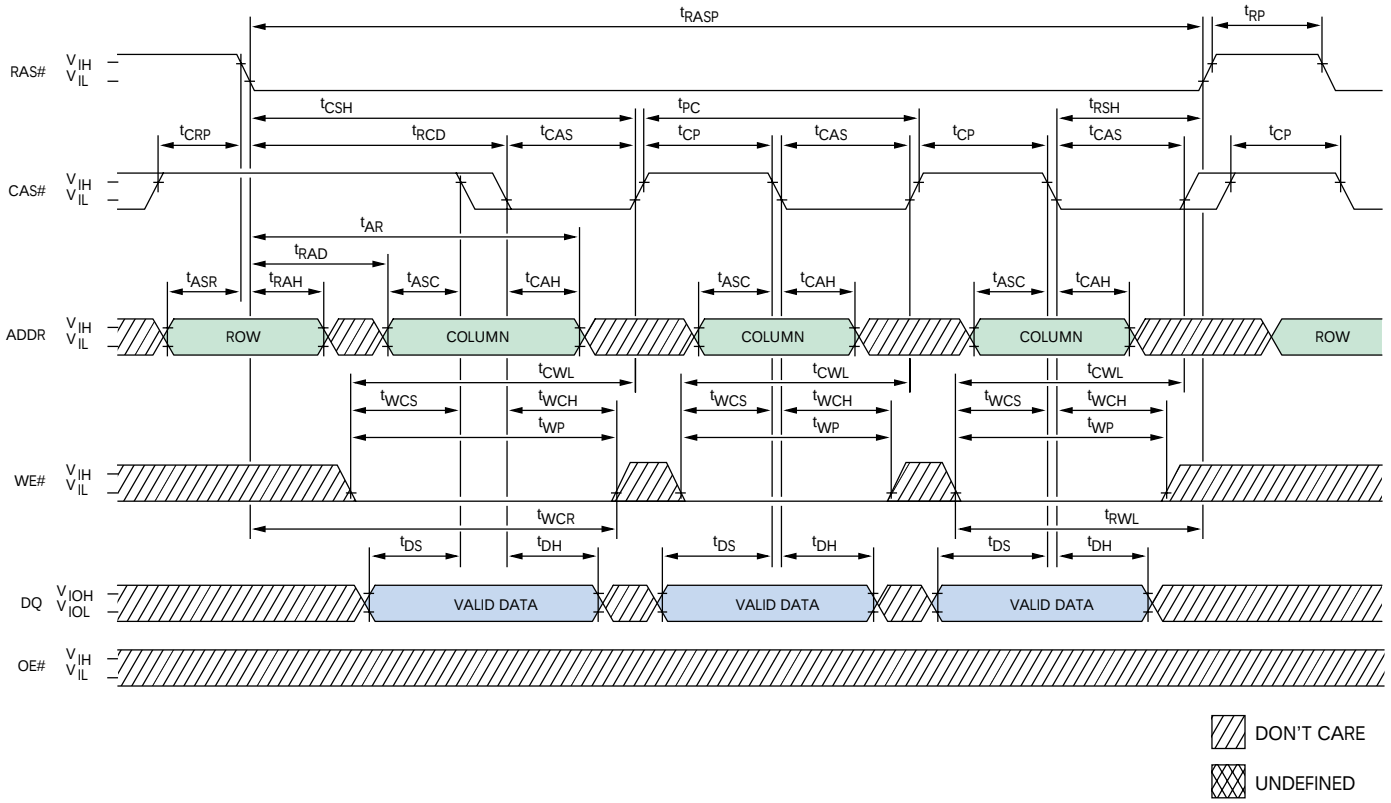


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

FAST-PAGE-MODE EARLY WRITE CYCLE

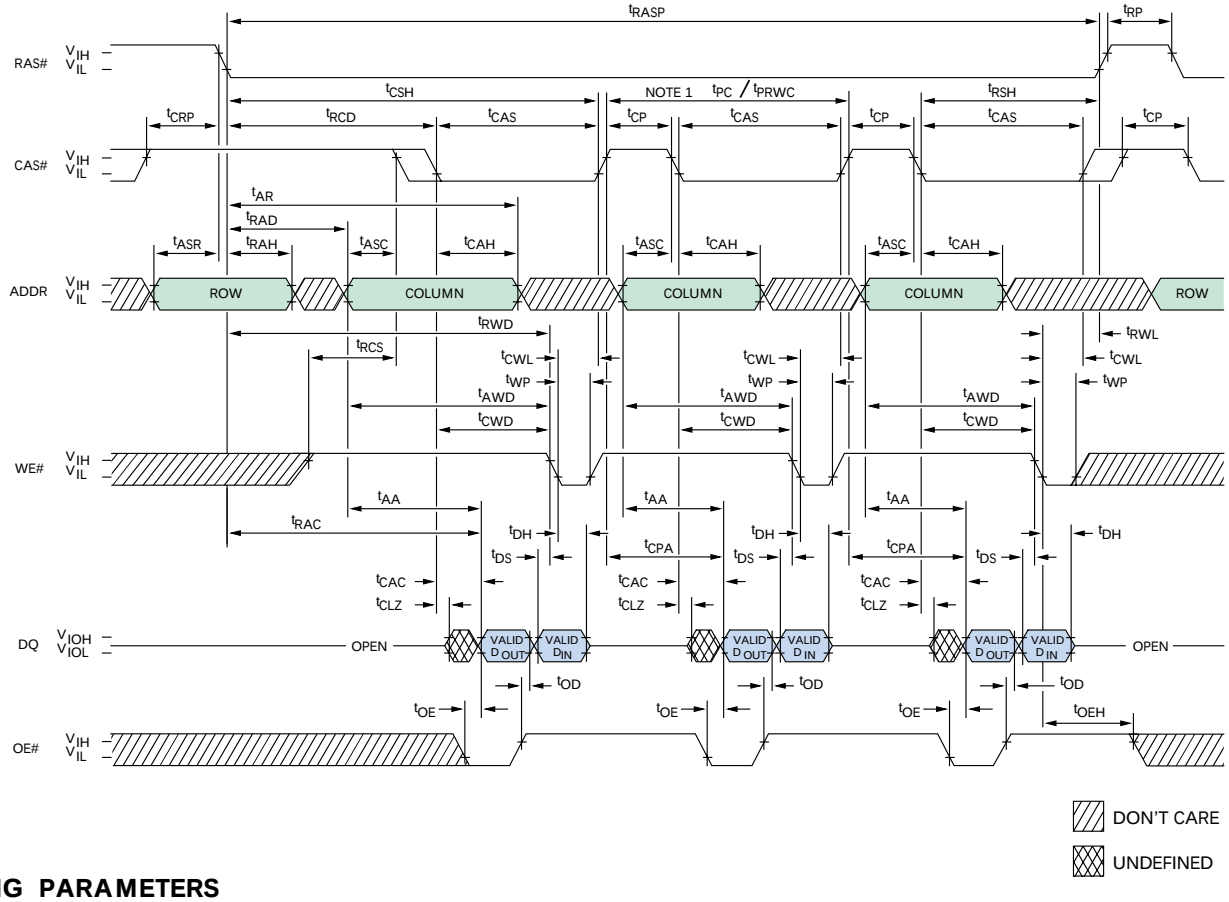


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns
tPC	20		25		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



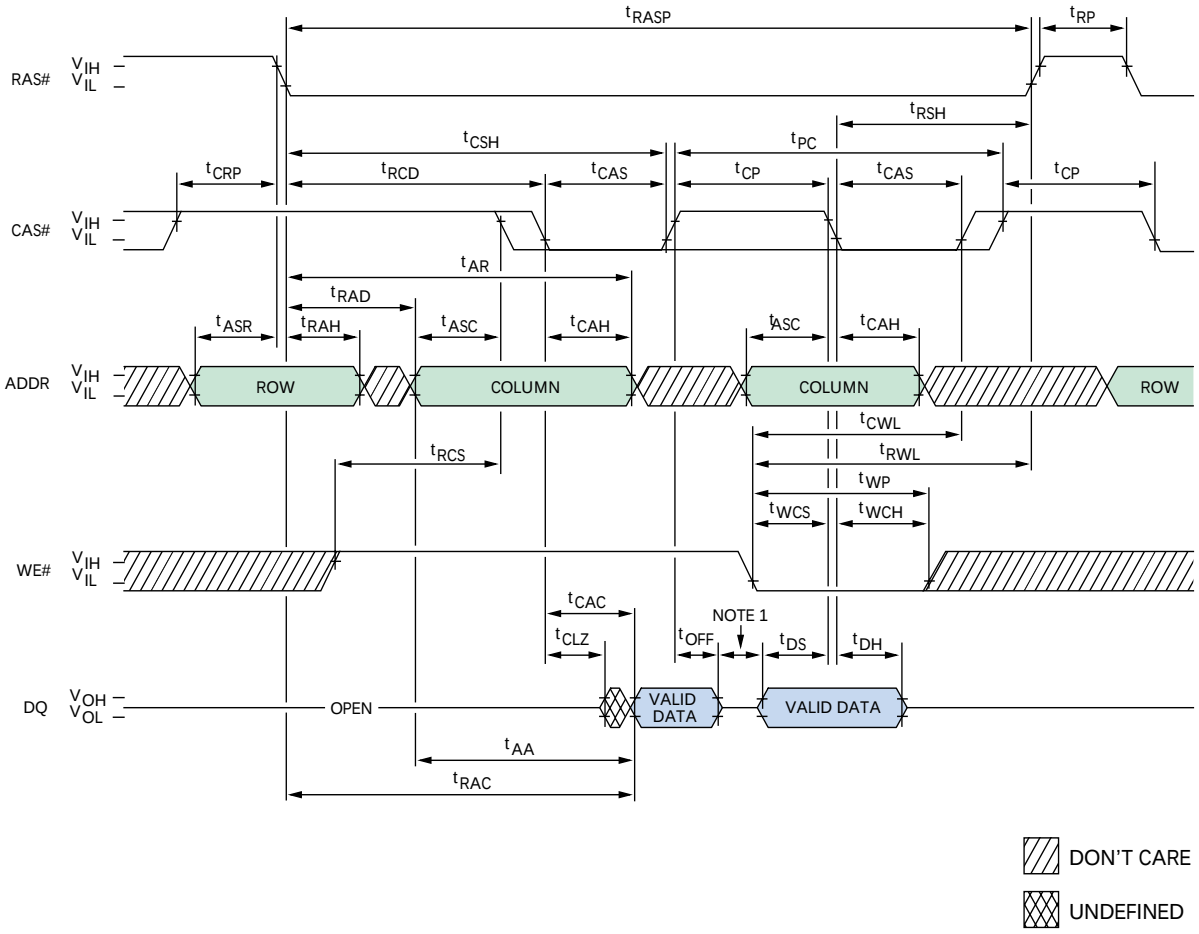
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tPC	20		25		ns
tPRWC	47		56		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE only.

FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



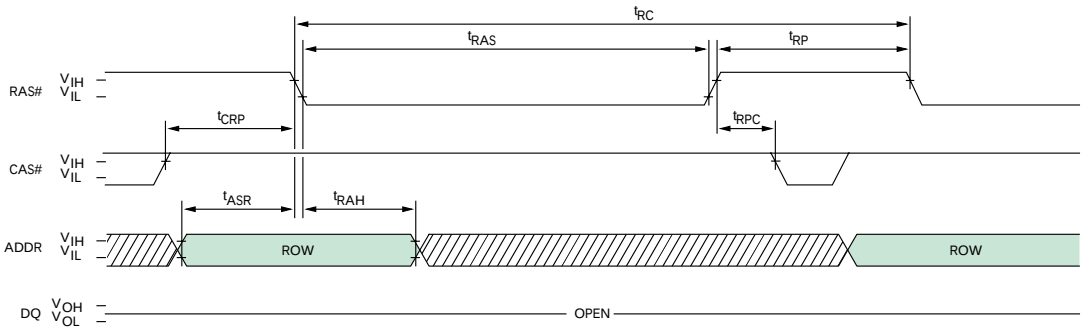
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

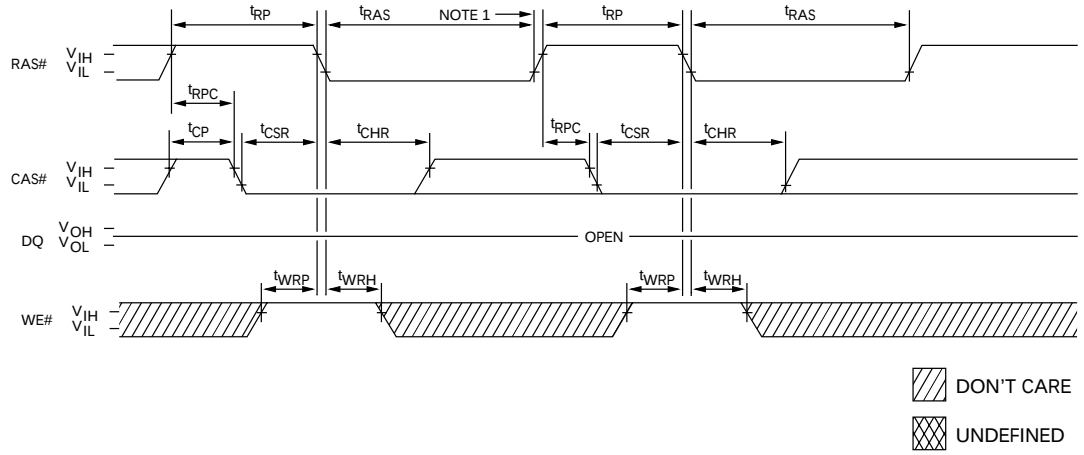
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWP	5		5		ns

NOTE: 1. Do not drive data prior to tristate.

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



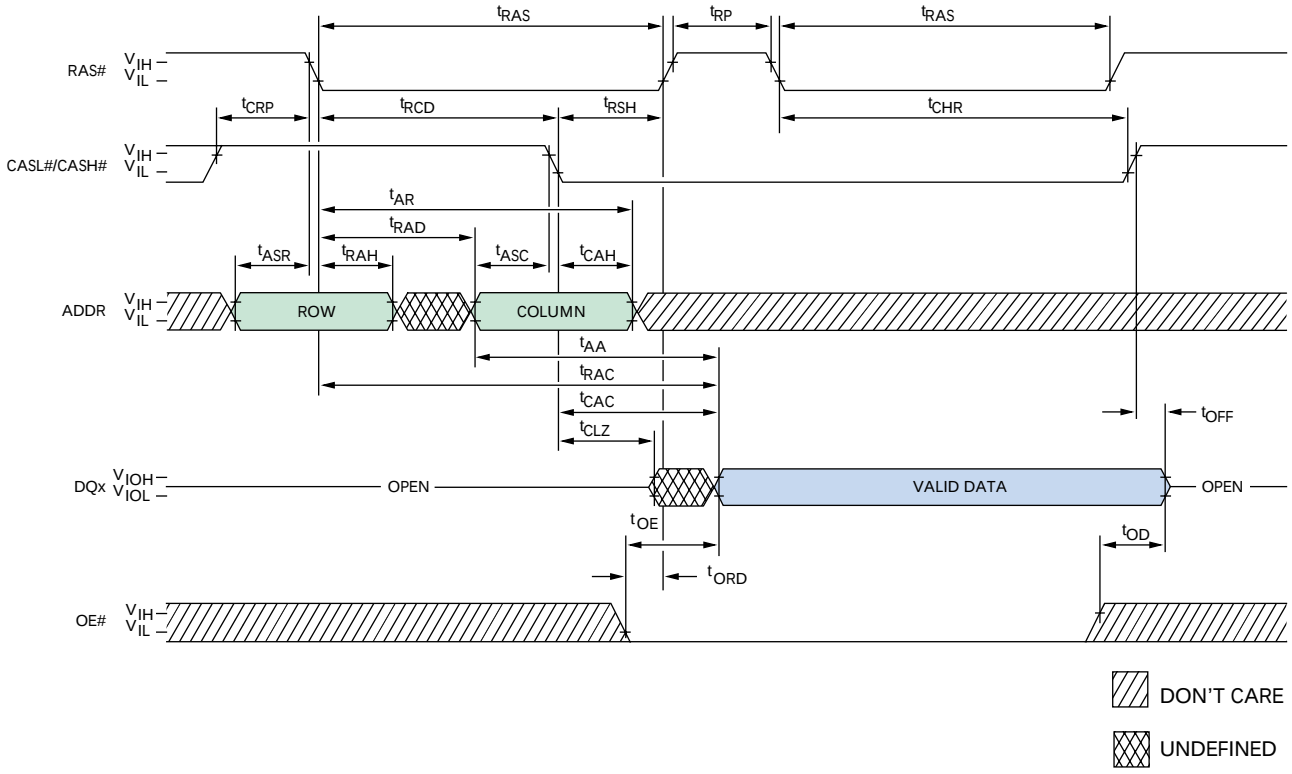
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	9		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. End of CBR REFRESH cycle.

HIDDEN REFRESH CYCLE[1]
(WE# = HIGH; OE# = LOW)



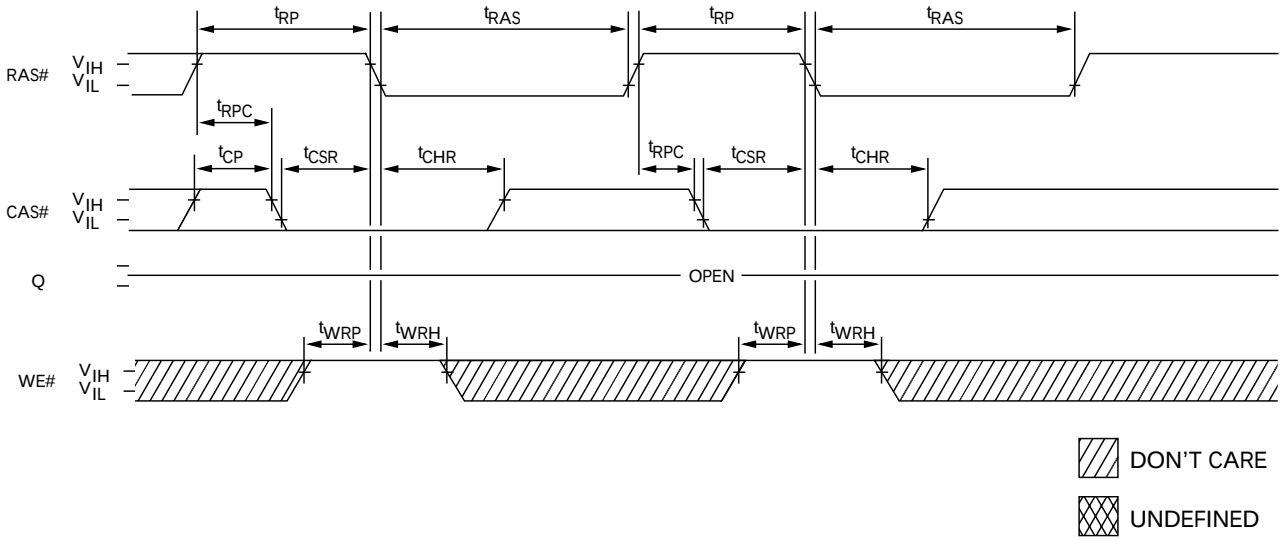
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



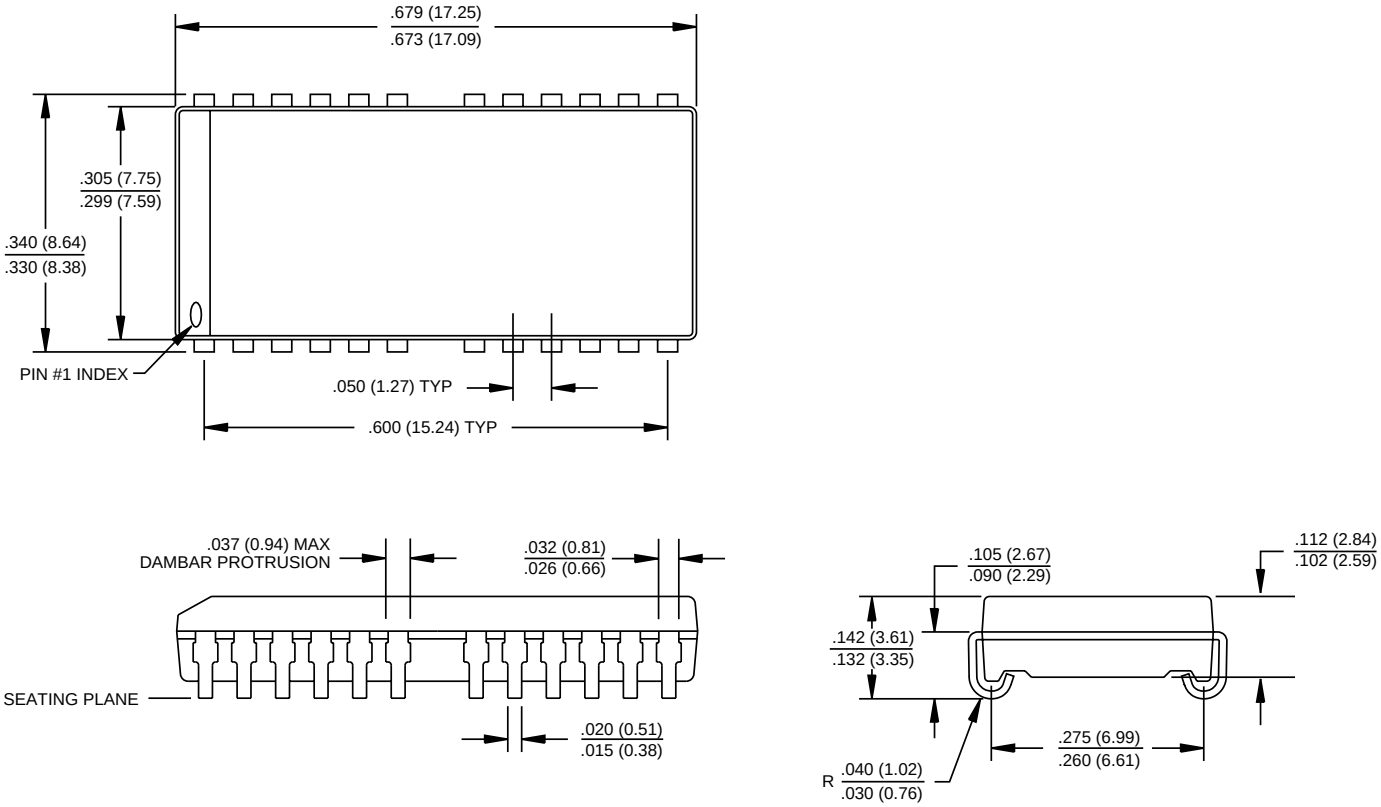
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCHD	15		15		ns
tCP	8		10		ns
tCSR	5		5		ns
tRASS	100		100		µs
tRP	30		40		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRPC	5		5		ns
tRPS	90		105		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed if RAS#-only or burst CBR refresh is used.

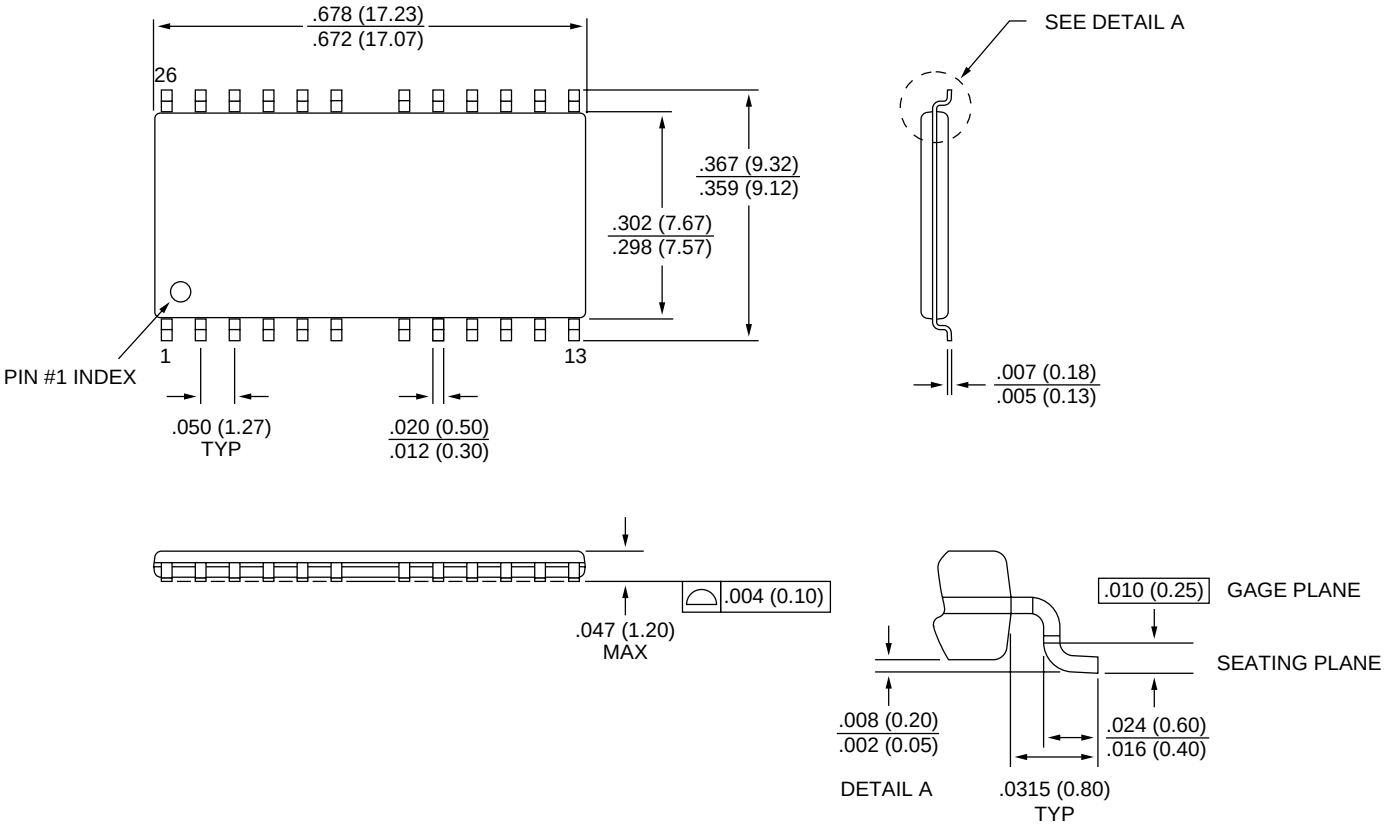
24/26-PIN PLASTIC SOJ (300 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24/26-PIN PLASTIC TSOP (300 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992