**Freescale Semiconductor**
Data Sheet

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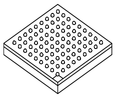
# MSC8113



FC-PBGA–431
20 mm × 20 mm

# Tri-Core Digital Signal Processor

- Three StarCore™ SC140 DSP extended cores, each with an SC140 DSP core, 224 Kbyte of internal SRAM M1 memory (1436 Kbyte total), 16 way 16 Kbyte instruction cache (ICache), four-entry write buffer, external cache support, programmable interrupt controller (PIC), local interrupt controller (LIC), and low-power Wait and Stop processing modes.
- 475 Kbyte M2 memory for critical data and temporary data buffering.
- 4 Kbyte boot ROM.
- M2-accessible multi-core MQBus connecting the M2 memory with all three cores, operating at the core frequency, with data bus access of up to 128-bit reads and up to 64-bit writes, central efficient round-robin arbiter for core access to the bus, and atomic operation control of M2 memory access by the cores and the local bus.
- Internal PLL configured are reset by configuration signal values.
- 60x-compatible system bus with 64 or 32 bit data and 32-bit address bus, support for multi-master designs, four-beat burst transfers (eight-beat in 32-bit data mode), port size of 64/32/16/8 bits controlled by the internal memory controller,.access to external memory or peripherals, access by an external host to internal resources, slave support with direct access to internal resources including M1 and M2 memories, and on-device arbitration for up to four master devices.
- Direct slave interface (DSI) using a 32/64-bit slave host interface with 21–25 bit addressing and 32/64-bit data transfers, direct access by an external host to internal and external resources, synchronous or asynchronous accesses with burst capability in synchronous mode, dual or single strobe mode, write and read buffers to improve host bandwidth, byte enable signals for 1/2/4/8-byte write granularity, sliding window mode for access using a reduced number of address pins, chip ID decoding to allow one $\overline{\mathrm{CS}}$ signal to control multiple DSPs, broadcast mode to write to multiple DSPs, and big-endian/little-endian/munged support.
- Three mode signal multiplexing: 64-bit DSI and 32-bit system bus, 32-bit DSI and 64-bit system bus, or 32-bit DSI and 32-bit system bus, and Ethernet port (MII/RMII).
- Flexible memory controller with three UPMs, a GPCM, a page-mode SDRAM machine, glueless interface to a variety of memories and devices, byte enables for 64- or 32-bit bus widths, 8 memory banks for external memories, and 2 memory banks for IPBus peripherals and internal memories.
- Multi-channel DMA controller with 16 time-multiplexed single channels, up to four external peripherals, $\overline{\mathrm{DONE}}$ or $\overline{\mathrm{DRACK}}$ protocol for two external peripherals,.service for up to 16 internal requests from up to 8 internal FIFOs per channel, FIFO generated watermarks and hungry requests, priority-based time-multiplexing between channels using 16 internal priority levels or round-robin time-multiplexing between channels, flexible channel configuration with connection to local bus or system bus, and flyby transfer support that bypasses the FIFO.
- Up to four independent TDM modules with programmable word size (2, 4, 8, or 16-bit), hardware-base A-law/µ-law conversion, up to 128 Mbps data rate for all channels, with glueless interface to E1 or T1 framers, and can interface with H-MVIP/H.110 devices, TSI, and codecs such as AC-97.
- Ethernet controller with support for 10/100 Mbps MII/RMII/SMII including full- and half-duplex operation, full-duplex flow controls, out-of-sequence transmit queues, programmable maximum frame length including jumbo frames and VLAN tags and priority, retransmission after collision, CRC generation and verification of inbound/outbound packets, address recognition (including exact match, broadcast address, individual hash check, group hash check, and promiscuous mode), pattern matching, insertion with expansion or replacement for transmit frames, VLAN tag insertion, RMON statistics, local bus master DMA for descriptor fetching and buffer access, and optional multiplexing with GPIO (MII/RMII/SMII) or DSI/system bus signals lines (MII/RMII).
- UART with full-duplex operation up to 6.25 Mbps.
- Up to 32 general-purpose input/output (GPIO) ports.
- I$^2$C interface that allows booting from EEPROM devices.
- Two timer modules, each with sixteen configurable 16-bit timers.
- Eight programmable hardware semaphores.
- Global interrupt controller (GIC) with interrupt consolidation and routing to $\overline{\mathrm{INT\_OUT}}$, $\overline{\mathrm{NMI\_OUT}}$, and the cores; twenty-four virtual maskable interrupts (8 per core) and three virtual $\overline{\mathrm{NMI}}$ (one per core) that can be generated by a simple write access.
- Optional booting external memory, external host, UART, TDM, or I$^2$C.

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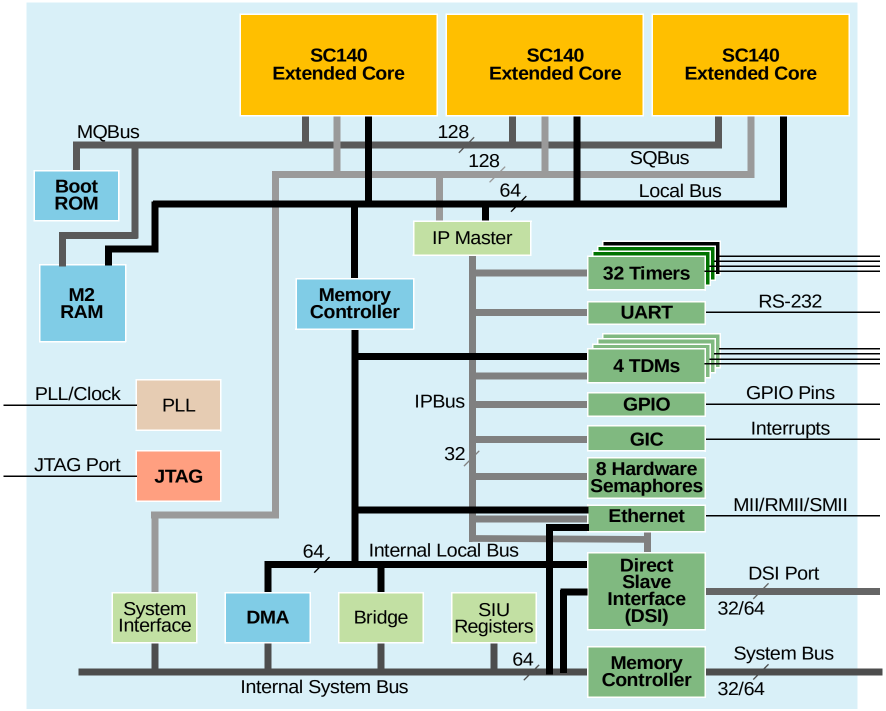
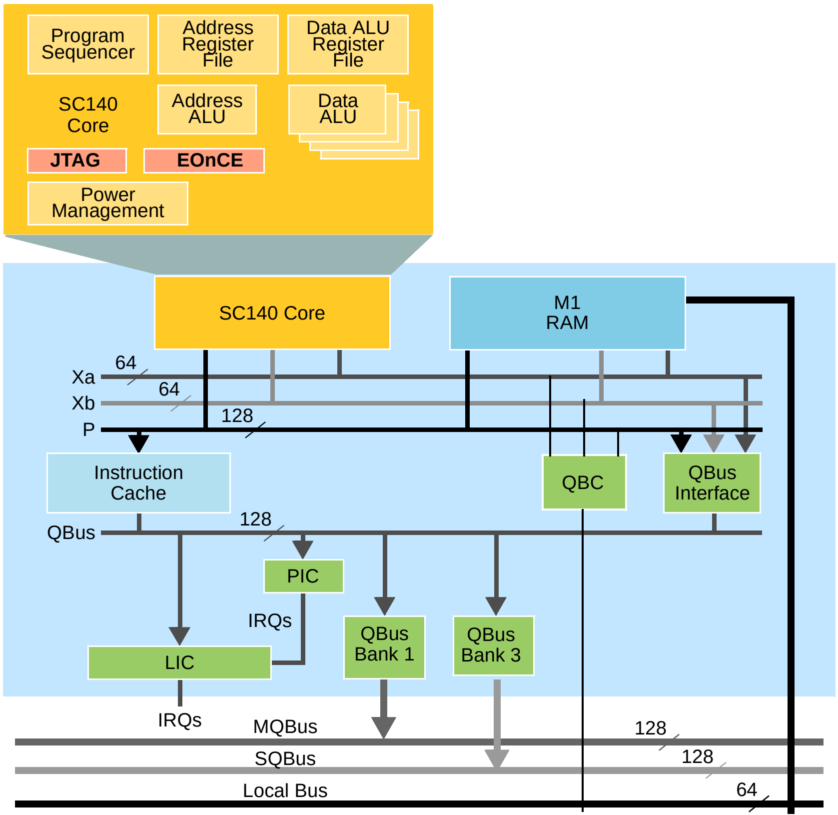


Figure 1. MSC8113 Block Diagram



**Notes: 1.** The arrows show the data transfer direction.

**2**. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

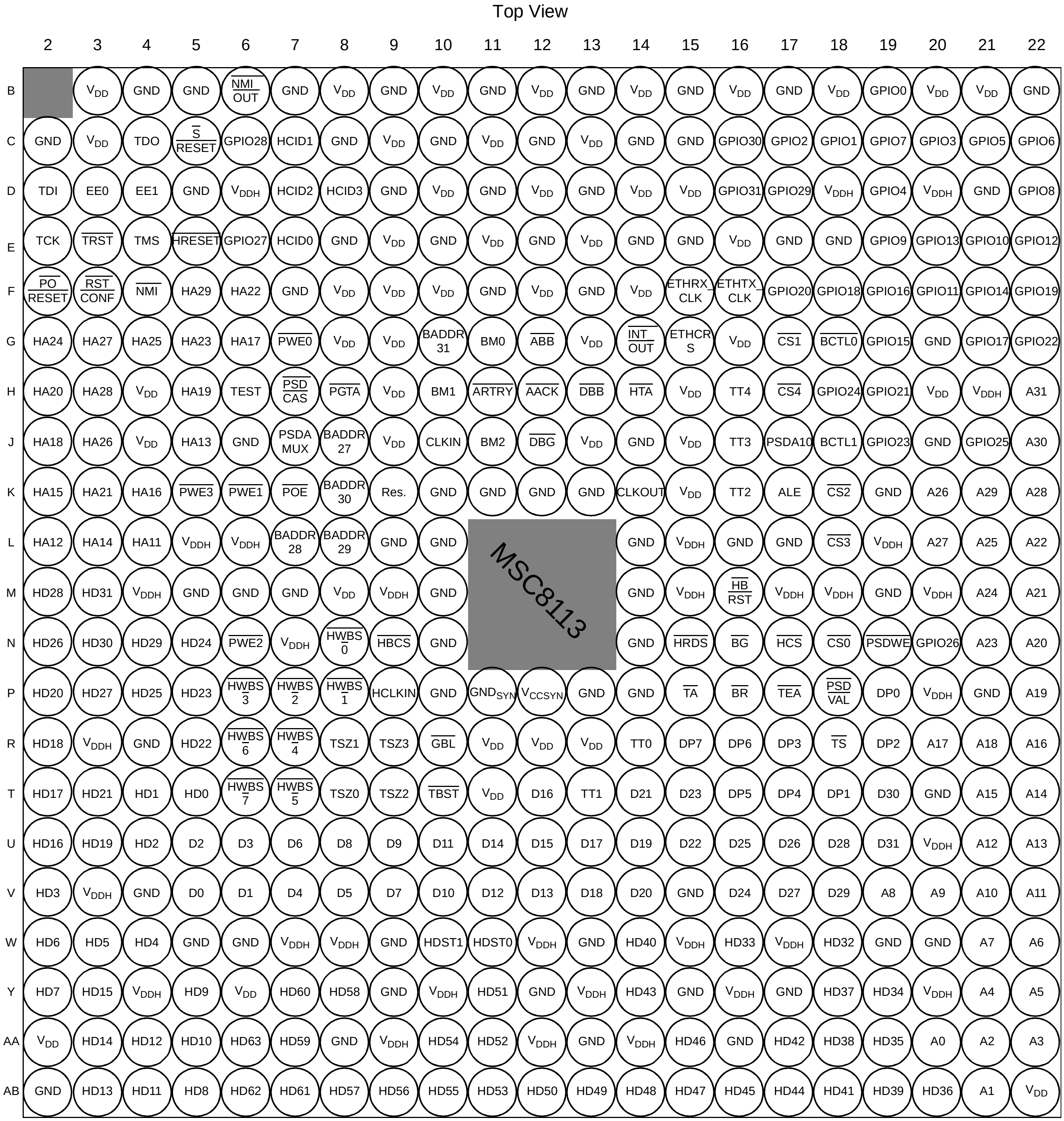
Figure 2. StarCore® SC140 DSP Extended Core Block Diagram

# 1 Pin Assignments

This section includes diagrams of the MSC8113 package ball grid array layouts and pinout allocation tables.

## 1.1 FC-PBGA Ball Layout Diagrams

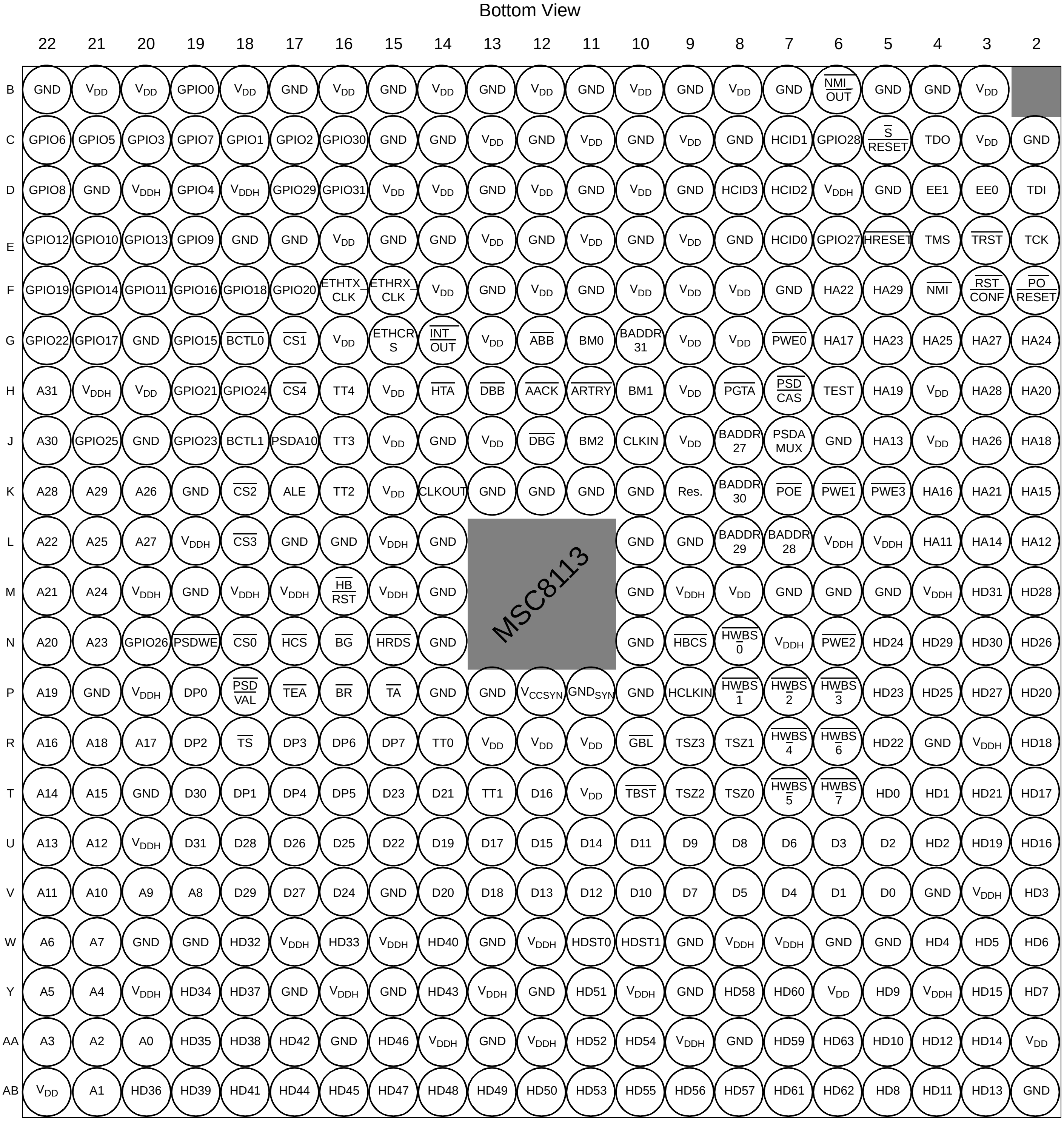
Top and bottom views of the FC-PBGA package are shown in **Figure 3** and **Figure 4** with their ball location index numbers.



Top View

| | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | | $V_{DD}$ | GND | GND | $\overline{\text{NMI\_OUT}}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GPIO0 | $V_{DD}$ | $V_{DD}$ | GND |
| C | GND | $V_{DD}$ | TDO | $\overline{\text{S}}$RESET | GPIO28 | HCID1 | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | GND | GPIO30 | GPIO2 | GPIO1 | GPIO7 | GPIO3 | GPIO5 | GPIO6 |
| D | TDI | EE0 | EE1 | GND | $V_{DDH}$ | HCID2 | HCID3 | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | $V_{DD}$ | GPIO31 | GPIO29 | $V_{DDH}$ | GPIO4 | $V_{DDH}$ | GND | GPIO8 |
| E | TCK | $\overline{\text{TRST}}$ | TMS | $\overline{\text{HRESET}}$ | GPIO27 | HCID0 | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | GND | $V_{DD}$ | GND | GND | GPIO9 | GPIO13 | GPIO10 | GPIO12 |
| F | $\overline{\text{PO}}$RESET | $\overline{\text{RST}}$CONF | $\overline{\text{NMI}}$ | HA29 | HA22 | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | ETHRX_CLK | ETHTX_CLK | GPIO20 | GPIO18 | GPIO16 | GPIO11 | GPIO14 | GPIO19 |
| G | HA24 | HA27 | HA25 | HA23 | HA17 | $\overline{\text{PWE0}}$ | $V_{DD}$ | $V_{DD}$ | BADDR31 | BM0 | $\overline{\text{ABB}}$ | $V_{DD}$ | $\overline{\text{INT\_OUT}}$ | ETHCRS | $V_{DD}$ | $\overline{\text{CS1}}$ | $\overline{\text{BCTL0}}$ | GPIO15 | GND | GPIO17 | GPIO22 |
| H | HA20 | HA28 | $V_{DD}$ | HA19 | TEST | $\overline{\text{PSD}}$CAS | $\overline{\text{PGTA}}$ | $V_{DD}$ | BM1 | $\overline{\text{ARTRY}}$ | $\overline{\text{AACK}}$ | $\overline{\text{DBB}}$ | $\overline{\text{HTA}}$ | $V_{DD}$ | TT4 | $\overline{\text{CS4}}$ | GPIO24 | GPIO21 | $V_{DD}$ | $V_{DDH}$ | A31 |
| J | HA18 | HA26 | $V_{DD}$ | HA13 | GND | PSDAMUX | BADDR27 | $V_{DD}$ | CLKIN | BM2 | $\overline{\text{DBG}}$ | $V_{DD}$ | GND | $V_{DD}$ | TT3 | PSDA10 | BCTL1 | GPIO23 | GND | GPIO25 | A30 |
| K | HA15 | HA21 | HA16 | $\overline{\text{PWE3}}$ | $\overline{\text{PWE1}}$ | $\overline{\text{POE}}$ | BADDR30 | Res. | GND | GND | GND | GND | CLKOUT | $V_{DD}$ | TT2 | ALE | $\overline{\text{CS2}}$ | GND | A26 | A29 | A28 |
| L | HA12 | HA14 | HA11 | $V_{DDH}$ | $V_{DDH}$ | BADDR28 | BADDR29 | GND | GND | | | | GND | $V_{DDH}$ | GND | GND | $\overline{\text{CS3}}$ | $V_{DDH}$ | A27 | A25 | A22 |
| M | HD28 | HD31 | $V_{DDH}$ | GND | GND | GND | $V_{DD}$ | $V_{DDH}$ | GND | | MSC8113 | | GND | $V_{DDH}$ | $\overline{\text{HB}}$RST | $V_{DDH}$ | $V_{DDH}$ | GND | $V_{DDH}$ | A24 | A21 |
| N | HD26 | HD30 | HD29 | HD24 | $\overline{\text{PWE2}}$ | $V_{DDH}$ | $\overline{\text{HWBS0}}$ | $\overline{\text{HBCS}}$ | GND | | | | GND | $\overline{\text{HRDS}}$ | $\overline{\text{BG}}$ | $\overline{\text{HCS}}$ | $\overline{\text{CS0}}$ | $\overline{\text{PSDWE}}$ | GPIO26 | A23 | A20 |
| P | HD20 | HD27 | HD25 | HD23 | $\overline{\text{HWBS3}}$ | $\overline{\text{HWBS2}}$ | $\overline{\text{HWBS1}}$ | HCLKIN | GND | $GND_{SYN}$ | $V_{CCSYN}$ | GND | GND | $\overline{\text{TA}}$ | $\overline{\text{BR}}$ | $\overline{\text{TEA}}$ | $\overline{\text{PSD}}$VAL | DP0 | $V_{DDH}$ | GND | A19 |
| R | HD18 | $V_{DDH}$ | GND | HD22 | $\overline{\text{HWBS6}}$ | $\overline{\text{HWBS4}}$ | TSZ1 | TSZ3 | $\overline{\text{GBL}}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | TT0 | DP7 | DP6 | DP3 | $\overline{\text{TS}}$ | DP2 | A17 | A18 | A16 |
| T | HD17 | HD21 | HD1 | HD0 | $\overline{\text{HWBS7}}$ | $\overline{\text{HWBS5}}$ | TSZ0 | TSZ2 | $\overline{\text{TBST}}$ | $V_{DD}$ | D16 | TT1 | D21 | D23 | DP5 | DP4 | DP1 | D30 | GND | A15 | A14 |
| U | HD16 | HD19 | HD2 | D2 | D3 | D6 | D8 | D9 | D11 | D14 | D15 | D17 | D19 | D22 | D25 | D26 | D28 | D31 | $V_{DDH}$ | A12 | A13 |
| V | HD3 | $V_{DDH}$ | GND | D0 | D1 | D4 | D5 | D7 | D10 | D12 | D13 | D18 | D20 | GND | D24 | D27 | D29 | A8 | A9 | A10 | A11 |
| W | HD6 | HD5 | HD4 | GND | GND | $V_{DDH}$ | $V_{DDH}$ | GND | HDST1 | HDST0 | $V_{DDH}$ | GND | HD40 | $V_{DDH}$ | HD33 | $V_{DDH}$ | HD32 | GND | GND | A7 | A6 |
| Y | HD7 | HD15 | $V_{DDH}$ | HD9 | $V_{DD}$ | HD60 | HD58 | GND | $V_{DDH}$ | HD51 | GND | $V_{DDH}$ | HD43 | GND | $V_{DDH}$ | GND | HD37 | HD34 | $V_{DDH}$ | A4 | A5 |
| AA | $V_{DD}$ | HD14 | HD12 | HD10 | HD63 | HD59 | GND | $V_{DDH}$ | HD54 | HD52 | $V_{DDH}$ | GND | $V_{DDH}$ | HD46 | GND | HD42 | HD38 | HD35 | A0 | A2 | A3 |
| AB | GND | HD13 | HD11 | HD8 | HD62 | HD61 | HD57 | HD56 | HD55 | HD53 | HD50 | HD49 | HD48 | HD47 | HD45 | HD44 | HD41 | HD39 | HD36 | A1 | $V_{DD}$ |

Figure 3. MSC8113 Package, Top View



Bottom View

|  | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B | GND | $V_{DD}$ | $V_{DD}$ | GPIO0 | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $\overline{\text{NMI\_OUT}}$ | GND | GND | $V_{DD}$ |  |
| C | GPIO6 | GPIO5 | GPIO3 | GPIO7 | GPIO1 | GPIO2 | GPIO30 | GND | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | HCID1 | GPIO28 | $\overline{\text{SRESET}}$ | TDO | $V_{DD}$ | GND |
| D | GPIO8 | GND | $V_{DDH}$ | GPIO4 | $V_{DDH}$ | GPIO29 | GPIO31 | $V_{DD}$ | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | HCID3 | HCID2 | $V_{DDH}$ | GND | EE1 | EE0 | TDI |
| E | GPIO12 | GPIO10 | GPIO13 | GPIO9 | GND | GND | $V_{DD}$ | GND | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | GND | HCID0 | GPIO27 | $\overline{\text{HRESET}}$ | TMS | $\overline{\text{TRST}}$ | TCK |
| F | GPIO19 | GPIO14 | GPIO11 | GPIO16 | GPIO18 | GPIO20 | ETHTX_CLK | ETHRX_CLK | $V_{DD}$ | GND | $V_{DD}$ | GND | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | GND | HA22 | HA29 | $\overline{\text{NMI}}$ | $\overline{\text{RSTCONF}}$ | $\overline{\text{PORESET}}$ |
| G | GPIO22 | GPIO17 | GND | GPIO15 | $\overline{\text{BCTL0}}$ | $\overline{\text{CS1}}$ | $V_{DD}$ | ETHCRS | $\overline{\text{INT\_OUT}}$ | $V_{DD}$ | $\overline{\text{ABB}}$ | BM0 | BADDR31 | $V_{DD}$ | $V_{DD}$ | $\overline{\text{PWE0}}$ | HA17 | HA23 | HA25 | HA27 | HA24 |
| H | A31 | $V_{DDH}$ | $V_{DD}$ | GPIO21 | GPIO24 | $\overline{\text{CS4}}$ | TT4 | $V_{DD}$ | $\overline{\text{HTA}}$ | $\overline{\text{DBB}}$ | $\overline{\text{AACK}}$ | $\overline{\text{ARTRY}}$ | BM1 | $V_{DD}$ | $\overline{\text{PGTA}}$ | $\overline{\text{PSDCAS}}$ | TEST | HA19 | $V_{DD}$ | HA28 | HA20 |
| J | A30 | GPIO25 | GND | GPIO23 | BCTL1 | PSDA10 | TT3 | $V_{DD}$ | GND | $V_{DD}$ | $\overline{\text{DBG}}$ | BM2 | CLKIN | $V_{DD}$ | BADDR27 | PSDAMUX | GND | HA13 | $V_{DD}$ | HA26 | HA18 |
| K | A28 | A29 | A26 | GND | $\overline{\text{CS2}}$ | ALE | TT2 | $V_{DD}$ | CLKOUT | GND | GND | GND | GND | Res. | BADDR30 | $\overline{\text{POE}}$ | $\overline{\text{PWE1}}$ | $\overline{\text{PWE3}}$ | HA16 | HA21 | HA15 |
| L | A22 | A25 | A27 | $V_{DDH}$ | $\overline{\text{CS3}}$ | GND | GND | $V_{DDH}$ | GND | MSC8113 |  |  | GND | GND | BADDR29 | BADDR28 | $V_{DDH}$ | $V_{DDH}$ | HA11 | HA14 | HA12 |
| M | A21 | A24 | $V_{DDH}$ | GND | $V_{DDH}$ | $V_{DDH}$ | $\overline{\text{HBRST}}$ | $V_{DDH}$ | GND |  |  |  | GND | $V_{DDH}$ | $V_{DD}$ | GND | GND | GND | $V_{DDH}$ | HD31 | HD28 |
| N | A20 | A23 | GPIO26 | $\overline{\text{PSDWE}}$ | $\overline{\text{CS0}}$ | $\overline{\text{HCS}}$ | $\overline{\text{BG}}$ | $\overline{\text{HRDS}}$ | GND |  |  |  | GND | $\overline{\text{HBCS}}$ | $\overline{\text{HWBS0}}$ | $V_{DDH}$ | $\overline{\text{PWE2}}$ | HD24 | HD29 | HD30 | HD26 |
| P | A19 | GND | $V_{DDH}$ | DP0 | $\overline{\text{PSDVAL}}$ | $\overline{\text{TEA}}$ | $\overline{\text{BR}}$ | $\overline{\text{TA}}$ | GND | GND | $V_{CCSYN}$ | $\text{GND}_{SYN}$ | GND | HCLKIN | $\overline{\text{HWBS1}}$ | $\overline{\text{HWBS2}}$ | $\overline{\text{HWBS3}}$ | HD23 | HD25 | HD27 | HD20 |
| R | A16 | A18 | A17 | DP2 | $\overline{\text{TS}}$ | DP3 | DP6 | DP7 | TT0 | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $\overline{\text{GBL}}$ | TSZ3 | TSZ1 | $\overline{\text{HWBS4}}$ | $\overline{\text{HWBS6}}$ | HD22 | GND | $V_{DDH}$ | HD18 |
| T | A14 | A15 | GND | D30 | DP1 | DP4 | DP5 | D23 | D21 | TT1 | D16 | $V_{DD}$ | $\overline{\text{TBST}}$ | TSZ2 | TSZ0 | $\overline{\text{HWBS5}}$ | $\overline{\text{HWBS7}}$ | HD0 | HD1 | HD21 | HD17 |
| U | A13 | A12 | $V_{DDH}$ | D31 | D28 | D26 | D25 | D22 | D19 | D17 | D15 | D14 | D11 | D9 | D8 | D6 | D3 | D2 | HD2 | HD19 | HD16 |
| V | A11 | A10 | A9 | A8 | D29 | D27 | D24 | GND | D20 | D18 | D13 | D12 | D10 | D7 | D5 | D4 | D1 | D0 | GND | $V_{DDH}$ | HD3 |
| W | A6 | A7 | GND | GND | HD32 | $V_{DDH}$ | HD33 | $V_{DDH}$ | HD40 | GND | $V_{DDH}$ | HDST0 | HDST1 | GND | $V_{DDH}$ | $V_{DDH}$ | GND | GND | HD4 | HD5 | HD6 |
| Y | A5 | A4 | $V_{DDH}$ | HD34 | HD37 | GND | $V_{DDH}$ | GND | HD43 | $V_{DDH}$ | GND | HD51 | $V_{DDH}$ | GND | HD58 | HD60 | $V_{DD}$ | HD9 | $V_{DDH}$ | HD15 | HD7 |
| AA | A3 | A2 | A0 | HD35 | HD38 | HD42 | GND | HD46 | $V_{DDH}$ | GND | $V_{DDH}$ | HD52 | HD54 | $V_{DDH}$ | GND | HD59 | HD63 | HD10 | HD12 | HD14 | $V_{DD}$ |
| AB | $V_{DD}$ | A1 | HD36 | HD39 | HD41 | HD44 | HD45 | HD47 | HD48 | HD49 | HD50 | HD53 | HD55 | HD56 | HD57 | HD61 | HD62 | HD8 | HD11 | HD13 | GND |

Figure 4. MSC8113 Package, Bottom View

## 1.2 Signal List By Ball Location

**Table 1** presents signal list sorted by ball number. -

**Table 1. MSC8113 Signal Listing by Ball Designator**

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| B3 | $V_{DD}$ | C18 | GPIO1/TIMER0/CHIP_ID1/$\overline{\text{IRQ5}}$/ETHTXD1 |
| B4 | GND | C19 | GPIO7/TDM3RCLK/$\overline{\text{IRQ5}}$/ETHTXD3 |
| B5 | GND | C20 | GPIO3/TDM3TSYN/$\overline{\text{IRQ1}}$/ETHTXD2 |
| B6 | $\overline{\text{NMI\_OUT}}$ | C21 | GPIO5/TDM3TDAT/$\overline{\text{IRQ3}}$/ETHRXD3 |
| B7 | GND | C22 | GPIO6/TDM3RSYN/$\overline{\text{IRQ4}}$/ETHRXD2 |
| B8 | $V_{DD}$ | D2 | TDI |
| B9 | GND | D3 | EE0 |
| B10 | $V_{DD}$ | D4 | EE1 |
| B11 | GND | D5 | GND |
| B12 | $V_{DD}$ | D6 | $V_{DDH}$ |
| B13 | GND | D7 | HCID2 |
| B14 | $V_{DD}$ | D8 | HCID3/HA8 |
| B15 | GND | D9 | GND |
| B16 | $V_{DD}$ | D10 | $V_{DD}$ |
| B17 | GND | D11 | GND |
| B18 | $V_{DD}$ | D12 | $V_{DD}$ |
| B19 | GPIO0/CHIP_ID0/$\overline{\text{IRQ4}}$/ETHTXD0 | D13 | GND |
| B20 | $V_{DD}$ | D14 | $V_{DD}$ |
| B21 | $V_{DD}$ | D15 | $V_{DD}$ |
| B22 | GND | D16 | GPIO31/TIMER3/SCL |
| C2 | GND | D17 | GPIO29/CHIP_ID3/ETHTX_EN |
| C3 | $V_{DD}$ | D18 | $V_{DDH}$ |
| C4 | TDO | D19 | GPIO4/TDM3TCLK/$\overline{\text{IRQ2}}$/ETHTX_ER |
| C5 | $\overline{\text{SRESET}}$ | D20 | $V_{DDH}$ |
| C6 | GPIO28/UTXD/DREQ2 | D21 | GND |
| C7 | HCID1 | D22 | GPIO8/TDM3RDAT/$\overline{\text{IRQ6}}$/ETHCOL |
| C8 | GND | E2 | TCK |
| C9 | $V_{DD}$ | E3 | $\overline{\text{TRST}}$ |
| C10 | GND | E4 | TMS |
| C11 | $V_{DD}$ | E5 | $\overline{\text{HRESET}}$ |
| C12 | GND | E6 | GPIO27/URXD/DREQ1 |
| C13 | $V_{DD}$ | E7 | HCID0 |
| C14 | GND | E8 | GND |
| C15 | GND | E9 | $V_{DD}$ |
| C16 | GPIO30/TIMER2/TMCLK/SDA | E10 | GND |
| C17 | GPIO2/TIMER1/CHIP_ID2/$\overline{\text{IRQ6}}$ | E11 | $V_{DD}$ |

### Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| E12 | GND | G6 | HA17 |
| E13 | $V_{DD}$ | G7 | $\overline{\text{PWE0}}$/$\overline{\text{PSDDQM0}}$/$\overline{\text{PBS0}}$ |
| E14 | GND | G8 | $V_{DD}$ |
| E15 | GND | G9 | $V_{DD}$ |
| E16 | $V_{DD}$ | G10 | $\overline{\text{IRQ3}}$/BADDR31 |
| E17 | GND | G11 | BM0/TC0/BNKSEL0 |
| E18 | GND | G12 | $\overline{\text{ABB}}$/$\overline{\text{IRQ4}}$ |
| E19 | GPIO9/TDM2TSYN/$\overline{\text{IRQ7}}$/ETHMDIO | G13 | $V_{DD}$ |
| E20 | GPIO13/TDM2RCLK/$\overline{\text{IRQ11}}$/ETHMDC | G14 | $\overline{\text{IRQ7}}$/$\overline{\text{INT\_OUT}}$ |
| E21 | GPIO10/TDM2TCLK/$\overline{\text{IRQ8}}$/ETHRX_DV/ETHCRS_DV/NC | G15 | ETHCRS/ETHRXD |
| E22 | GPIO12/TDM2RSYN/$\overline{\text{IRQ10}}$/ETHRXD1/ETHSYNC | G16 | $V_{DD}$ |
| F2 | $\overline{\text{PORESET}}$ | G17 | $\overline{\text{CS1}}$ |
| F3 | $\overline{\text{RSTCONF}}$ | G18 | $\overline{\text{BCTL0}}$ |
| F4 | $\overline{\text{NMI}}$ | G19 | GPIO15/TDM1TSYN/DREQ1 |
| F5 | HA29 | G20 | GND |
| F6 | HA22 | G21 | GPIO17/TDM1TDAT/$\overline{\text{DACK1}}$ |
| F7 | GND | G22 | GPIO22/TDM0TCLK/$\overline{\text{DONE2}}$/$\overline{\text{DRACK2}}$ |
| F8 | $V_{DD}$ | H2 | HA20 |
| F9 | $V_{DD}$ | H3 | HA28 |
| F10 | $V_{DD}$ | H4 | $V_{DD}$ |
| F11 | GND | H5 | HA19 |
| F12 | $V_{DD}$ | H6 | TEST |
| F13 | GND | H7 | $\overline{\text{PSDCAS}}$/PGPL3 |
| F14 | $V_{DD}$ | H8 | $\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$ |
| F15 | ETHRX_CLK/ETHSYNC_IN | H9 | $V_{DD}$ |
| F16 | ETHTX_CLK/ETHREF_CLK/ETHCLOCK | H10 | BM1/TC1/BNKSEL1 |
| F17 | GPIO20/TDM1RDAT | H11 | $\overline{\text{ARTRY}}$ |
| F18 | GPIO18/TDM1RSYN/DREQ2 | H12 | $\overline{\text{AACK}}$ |
| F19 | GPIO16/TDM1TCLK/$\overline{\text{DONE1}}$/$\overline{\text{DRACK1}}$ | H13 | $\overline{\text{DBB}}$/$\overline{\text{IRQ5}}$ |
| F20 | GPIO11/TDM2TDAT/$\overline{\text{IRQ9}}$/ETHRX_ER/ETHTXD | H14 | $\overline{\text{HTA}}$ |
| F21 | GPIO14/TDM2RDAT/$\overline{\text{IRQ12}}$/ETHRXD0/NC | H15 | $V_{DD}$ |
| F22 | GPIO19/TDM1RCLK/$\overline{\text{DACK2}}$ | H16 | TT4/$\overline{\text{CS7}}$ |
| G2 | HA24 | H17 | $\overline{\text{CS4}}$ |
| G3 | HA27 | H18 | GPIO24/TDM0RSYN/$\overline{\text{IRQ14}}$ |
| G4 | HA25 | H19 | GPIO21/TDM0TSYN |
| G5 | HA23 | H20 | $V_{DD}$ |

## Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| H21 | $V_{DDH}$ | K15 | $V_{DD}$ |
| H22 | A31 | K16 | TT2/$\overline{CS5}$ |
| J2 | HA18 | K17 | ALE |
| J3 | HA26 | K18 | $\overline{CS2}$ |
| J4 | $V_{DD}$ | K19 | GND |
| J5 | HA13 | K20 | A26 |
| J6 | GND | K21 | A29 |
| J7 | PSDAMUX/PGPL5 | K22 | A28 |
| J8 | BADDR27 | L2 | HA12 |
| J9 | $V_{DD}$ | L3 | HA14 |
| J10 | CLKIN | L4 | HA11 |
| J11 | BM2/TC2/BNKSEL2 | L5 | $V_{DDH}$ |
| J12 | $\overline{DBG}$ | L6 | $V_{DDH}$ |
| J13 | $V_{DD}$ | L7 | BADDR28 |
| J14 | GND | L8 | $\overline{IRQ5}$/BADDR29 |
| J15 | $V_{DD}$ | L9 | GND |
| J16 | TT3/$\overline{CS6}$ | L10 | GND |
| J17 | PSDA10/PGPL0 | L14 | GND |
| J18 | $\overline{BCTL1}$/$\overline{CS5}$ | L15 | $V_{DDH}$ |
| J19 | GPIO23/TDM0TDAT/$\overline{IRQ13}$ | L16 | GND |
| J20 | GND | L17 | GND |
| J21 | GPIO25/TDM0RCLK/$\overline{IRQ15}$ | L18 | $\overline{CS3}$ |
| J22 | A30 | L19 | $V_{DDH}$ |
| K2 | HA15 | L20 | A27 |
| K3 | HA21 | L21 | A25 |
| K4 | HA16 | L22 | A22 |
| K5 | $\overline{PWE3}$/$\overline{PSDDQM3}$/$\overline{PBS3}$ | M2 | HD28 |
| K6 | $\overline{PWE1}$/$\overline{PSDDQM1}$/$\overline{PBS1}$ | M3 | HD31 |
| K7 | $\overline{POE}$/$\overline{PSDRAS}$/PGPL2 | M4 | $V_{DDH}$ |
| K8 | $\overline{IRQ2}$/BADDR30 | M5 | GND |
| K9 | Reserved | M6 | GND |
| K10 | GND | M7 | GND |
| K11 | GND | M8 | $V_{DD}$ |
| K12 | GND | M9 | $V_{DDH}$ |
| K13 | GND | M10 | GND |
| K14 | CLKOUT | M14 | GND |

### Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| M15 | $V_{DDH}$ | P12 | $V_{CCSYN}$ |
| M16 | $\overline{\text{HBRST}}$ | P13 | GND |
| M17 | $V_{DDH}$ | P14 | GND |
| M18 | $V_{DDH}$ | P15 | $\overline{\text{TA}}$ |
| M19 | GND | P16 | $\overline{\text{BR}}$ |
| M20 | $V_{DDH}$ | P17 | $\overline{\text{TEA}}$ |
| M21 | A24 | P18 | $\overline{\text{PSDVAL}}$ |
| M22 | A21 | P19 | DP0/DREQ1/$\overline{\text{EXT\_BR2}}$ |
| N2 | HD26 | P20 | $V_{DDH}$ |
| N3 | HD30 | P21 | GND |
| N4 | HD29 | P22 | A19 |
| N5 | HD24 | R2 | HD18 |
| N6 | $\overline{\text{PWE2}}$/$\overline{\text{PSDDQM2}}$/$\overline{\text{PBS2}}$ | R3 | $V_{DDH}$ |
| N7 | $V_{DDH}$ | R4 | GND |
| N8 | $\overline{\text{HWBS0}}$/$\overline{\text{HDBS0}}$/$\overline{\text{HWBE0}}$/$\overline{\text{HDBE0}}$ | R5 | HD22 |
| N9 | $\overline{\text{HBCS}}$ | R6 | $\overline{\text{HWBS6}}$/$\overline{\text{HDBS6}}$/$\overline{\text{HWBE6}}$/$\overline{\text{HDBE6}}$/$\overline{\text{PWE6}}$/$\overline{\text{PSDDQM6}}$/$\overline{\text{PBS6}}$ |
| N10 | GND | R7 | $\overline{\text{HWBS4}}$/$\overline{\text{HDBS4}}$/$\overline{\text{HWBE4}}$/$\overline{\text{HDBE4}}$/$\overline{\text{PWE4}}$/$\overline{\text{PSDDQM4}}$/$\overline{\text{PBS4}}$ |
| N14 | GND | R8 | TSZ1 |
| N15 | $\overline{\text{HRDS}}$/HRW/$\overline{\text{HRDE}}$ | R9 | TSZ3 |
| N16 | $\overline{\text{BG}}$ | R10 | $\overline{\text{IRQ1}}$/$\overline{\text{GBL}}$ |
| N17 | $\overline{\text{HCS}}$ | R11 | $V_{DD}$ |
| N18 | $\overline{\text{CS0}}$ | R12 | $V_{DD}$ |
| N19 | $\overline{\text{PSDWE}}$/PGPL1 | R13 | $V_{DD}$ |
| N20 | GPIO26/TDM0RDAT | R14 | TT0/HA7 |
| N21 | A23 | R15 | $\overline{\text{IRQ7}}$/DP7/DREQ4 |
| N22 | A20 | R16 | $\overline{\text{IRQ6}}$/DP6/DREQ3 |
| P2 | HD20 | R17 | $\overline{\text{IRQ3}}$/DP3/DREQ2/$\overline{\text{EXT\_BR3}}$ |
| P3 | HD27 | R18 | $\overline{\text{TS}}$ |
| P4 | HD25 | R19 | $\overline{\text{IRQ2}}$/DP2/$\overline{\text{DACK2}}$/$\overline{\text{EXT\_DBG2}}$ |
| P5 | HD23 | R20 | A17 |
| P6 | $\overline{\text{HWBS3}}$/$\overline{\text{HDBS3}}$/$\overline{\text{HWBE3}}$/$\overline{\text{HDBE3}}$ | R21 | A18 |
| P7 | $\overline{\text{HWBS2}}$/$\overline{\text{HDBS2}}$/$\overline{\text{HWBE2}}$/$\overline{\text{HDBE2}}$ | R22 | A16 |
| P8 | $\overline{\text{HWBS1}}$/$\overline{\text{HDBS1}}$/$\overline{\text{HWBE1}}$/$\overline{\text{HDBE1}}$ | T2 | HD17 |
| P9 | HCLKIN | T3 | HD21 |
| P10 | GND | T4 | HD1/DSISYNC |
| P11 | $GND_{SYN}$ | T5 | HD0/SWTE |

### Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| T6 | HWBS7/HDBS7/HWBE7/HDBE7/PWE7/PSDDQM7/PBS7 | U21 | A12 |
| T7 | HWBS5/HDBS5/HWBE5/HDBE5/PWE5/PSDDQM5/PBS5 | U22 | A13 |
| T8 | TSZ0 | V2 | HD3/MODCK1 |
| T9 | TSZ2 | V3 | $V_{DDH}$ |
| T10 | TBST | V4 | GND |
| T11 | $V_{DD}$ | V5 | D0 |
| T12 | D16 | V6 | D1 |
| T13 | TT1 | V7 | D4 |
| T14 | D21 | V8 | D5 |
| T15 | D23 | V9 | D7 |
| T16 | IRQ5/DP5/DACK4/EXT_BG3 | V10 | D10 |
| T17 | IRQ4/DP4/DACK3/EXT_DBG3 | V11 | D12 |
| T18 | IRQ1/DP1/DACK1/EXT_BG2 | V12 | D13 |
| T19 | D30 | V13 | D18 |
| T20 | GND | V14 | D20 |
| T21 | A15 | V15 | GND |
| T22 | A14 | V16 | D24 |
| U2 | HD16 | V17 | D27 |
| U3 | HD19 | V18 | D29 |
| U4 | HD2/DSI64 | V19 | A8 |
| U5 | D2 | V20 | A9 |
| U6 | D3 | V21 | A10 |
| U7 | D6 | V22 | A11 |
| U8 | D8 | W2 | HD6 |
| U9 | D9 | W3 | HD5/CNFGS |
| U10 | D11 | W4 | HD4/MODCK2 |
| U11 | D14 | W5 | GND |
| U12 | D15 | W6 | GND |
| U13 | D17 | W7 | $V_{DDH}$ |
| U14 | D19 | W8 | $V_{DDH}$ |
| U15 | D22 | W9 | GND |
| U16 | D25 | W10 | HDST1/HA10 |
| U17 | D26 | W11 | HDST0/HA9 |
| U18 | D28 | W12 | $V_{DDH}$ |
| U19 | D31 | W13 | GND |
| U20 | $V_{DDH}$ | W14 | HD40/D40/ETHRXD0 |

## Table 1. MSC8113 Signal Listing by Ball Designator (continued)

| Des. | Signal Name | Des. | Signal Name |
|---|---|---|---|
| W15 | $V_{DDH}$ | AA9 | $V_{DDH}$ |
| W16 | HD33/D33/reserved | AA10 | HD54/D54/ETHTX_EN |
| W17 | $V_{DDH}$ | AA11 | HD52/D52 |
| W18 | HD32/D32/reserved | AA12 | $V_{DDH}$ |
| W19 | GND | AA13 | GND |
| W20 | GND | AA14 | $V_{DDH}$ |
| W21 | A7 | AA15 | HD46/D46/ETHTXT0 |
| W22 | A6 | AA16 | GND |
| Y2 | HD7 | AA17 | HD42/D42/ETHRXD2/reserved |
| Y3 | HD15 | AA18 | HD38/D38/reserved |
| Y4 | $V_{DDH}$ | AA19 | HD35/D35/reserved |
| Y5 | HD9 | AA20 | A0 |
| Y6 | $V_{DD}$ | AA21 | A2 |
| Y7 | HD60/D60/ETHCOL/reserved | AA22 | A3 |
| Y8 | HD58/D58/ETHMDC | AB2 | GND |
| Y9 | GND | AB3 | HD13 |
| Y10 | $V_{DDH}$ | AB4 | HD11 |
| Y11 | HD51/D51 | AB5 | HD8 |
| Y12 | GND | AB6 | HD62/D62 |
| Y13 | $V_{DDH}$ | AB7 | HD61/D61 |
| Y14 | HD43/D43/ETHRXD3/reserved | AB8 | HD57/D57/ETHRX_ER |
| Y15 | GND | AB9 | HD56/D56/ETHRX_DV/ETHCRS_DV |
| Y16 | $V_{DDH}$ | AB10 | HD55/D55/ETHTX_ER/reserved |
| Y17 | GND | AB11 | HD53/D53 |
| Y18 | HD37/D37/reserved | AB12 | HD50/D50 |
| Y19 | HD34/D34/reserved | AB13 | HD49/D49/ETHTXD3/reserved |
| Y20 | $V_{DDH}$ | AB14 | HD48/D48/ETHTXD2/reserved |
| Y21 | A4 | AB15 | HD47/D47/ETHTXD1 |
| Y22 | A5 | AB16 | HD45/D45 |
| AA2 | $V_{DD}$ | AB17 | HD44/D44 |
| AA3 | HD14 | AB18 | HD41/D41/ETHRXD1 |
| AA4 | HD12 | AB19 | HD39/D39/reserved |
| AA5 | HD10 | AB20 | HD36/D36/reserved |
| AA6 | HD63/D63 | AB21 | A1 |
| AA7 | HD59/D59/ETHMDIO | AB22 | $V_{DD}$ |
| AA8 | GND | | |

# 2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8113 Reference Manual*.

## 2.1 Maximum Ratings

> **CAUTION**
>
> **This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{DD}$).**

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

**Table 2** describes the maximum electrical ratings for the MSC8113.

**Table 2. Absolute Maximum Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core and PLL supply voltage | $V_{DD}$ | –0.2 to 1.6 | V |
| I/O supply voltage | $V_{DDH}$ | –0.2 to 4.0 | V |
| Input voltage | $V_{IN}$ | –0.2 to 4.0 | V |
| Maximum operating temperature: | $T_J$ | 105 | °C |
| Minimum operating temperature | $T_J$ | –40 | °C |
| Storage temperature range | $T_{STG}$ | –55 to +150 | °C |

**Notes:**
1. Functional operating conditions are given in **Table 3.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 3.5**, *Thermal Considerations* includes a formula for computing the chip junction temperature ($T_J$).

## 2.2 Recommended Operating Conditions

**Table 3** lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core and PLL supply voltage: | $V_{DD}$<br>$V_{CCSYN}$ | 1.07 to 1.13 | V |
| I/O supply voltage | $V_{DDH}$ | 3.135 to 3.465 | V |
| Input voltage | $V_{IN}$ | –0.2 to $V_{DDH}$+0.2 | V |
| Operating temperature range: | $T_J$ | –40 to 105 | °C |

## 2.3 Thermal Characteristics

**Table 4** describes thermal characteristics of the MSC8113 for the FC-PBGA packages.

**Table 4. Thermal Characteristics for the MSC8113**

| Characteristic | Symbol | FC-PBGA 20 × 20 mm[5] | | Unit |
|---|---|---|---|---|
| | | Natural Convection | 200 ft/min (1 m/s) airflow | |
| Junction-to-ambient[1, 2] | $R_{\theta JA}$ | 26 | 21 | °C/W |
| Junction-to-ambient, four-layer board[1, 3] | $R_{\theta JA}$ | 19 | 15 | °C/W |
| Junction-to-board (bottom)[4] | $R_{\theta JB}$ | 9 | | °C/W |
| Junction-to-case[5] | $R_{\theta JC}$ | 0.9 | | °C/W |
| Junction-to-package-top[6] | $\Psi_{JT}$ | 1 | | °C/W |

**Notes:**

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

**Section 3.5**, *Thermal Considerations* provides a detailed explanation of these characteristics.

## 2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8113. The measurements in **Table 5** assume the following system conditions:

- $T_A$ = 25 °C
- $V_{DD}$ = 1.1 V nominal = 1.07–1.13 $V_{DC}$
- $V_{DDH}$ = 3.3 V ± 5% $V_{DC}$
- GND = 0 $V_{DC}$

**Note:** The leakage current is measured for nominal $V_{DDH}$ and $V_{DD}$.

Table 5. DC Electrical Characteristics

| Characteristic | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage[1], all inputs except CLKIN | $V_{IH}$ | 2.0 | — | 3.465 | V |
| Input low voltage[1] | $V_{IL}$ | GND | 0 | 0.8 | V |
| CLKIN input high voltage | $V_{IHC}$ | 2.4 | 3.0 | 3.465 | V |
| CLKIN input low voltage | $V_{ILC}$ | GND | 0 | 0.8 | V |
| Input leakage current, $V_{IN} = V_{DDH}$ | $I_{IN}$ | –1.0 | 0.09 | 1 | µA |
| Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDH}$ | $I_{OZ}$ | –1.0 | 0.09 | 1 | µA |
| Signal low input current, $V_{IL}$ = 0.8 V[2] | $I_L$ | –1.0 | 0.09 | 1 | µA |
| Signal high input current, $V_{IH}$ = 2.0 V[2] | $I_H$ | –1.0 | 0.09 | 1 | µA |
| Output high voltage, $I_{OH}$ = –2 mA, except open drain pins | $V_{OH}$ | 2.0 | 3.0 | — | V |
| Output low voltage, $I_{OL}$= 3.2 mA | $V_{OL}$ | — | 0 | 0.4 | V |
| Internal supply current:<br>• Wait mode<br>• Stop mode | <br>$I_{DDW}$<br>$I_{DDS}$ | <br>—<br>— | <br>375[3]<br>290[3] | <br>—<br>— | <br>mA<br>mA |
| Typical power 400 MHz at 1.1 V[4]<br>Typical power 300 MHz at 1.1 V[4] | P | —<br>— | 826<br>676 | —<br>— | mW<br>mW |

**Notes:**
1. See **Figure 5** for undershoot and overshoot voltages.
2. Not tested. Guaranteed by design.
3. Measured for 1.1 V core at 25°C junction temperature.
4. The typical power values were calculated using a power calculator configured for three cores performing an EFR code with the device running at the specified operating frequency and a junction temperature of 25°C. No peripherals were included. The calculator was created using CodeWarrior® 2.5. These values are provided as examples only. Power consumption is application dependent and varies widely. To assure proper board design with regard to thermal dissipation and maintaining proper operating temperatures, evaluate power consumption for your application and use the design guidelines in **Section 3** of this document and in *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601).

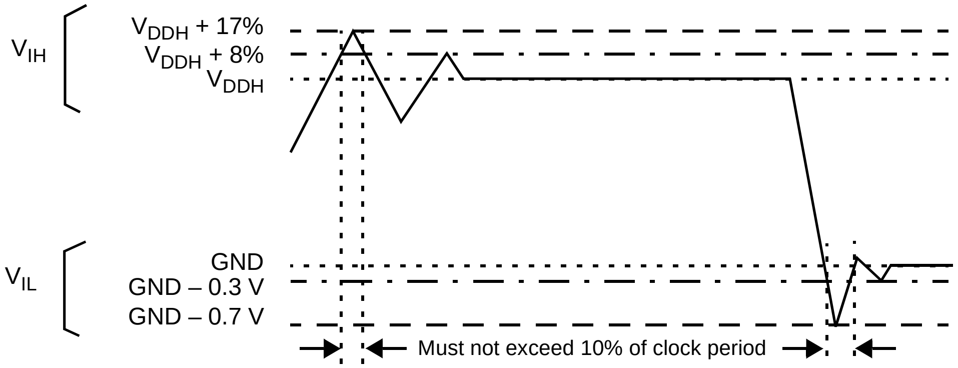


Figure 5. Overshoot/Undershoot Voltage for $V_{IH}$ and $V_{IL}$

## 2.5 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs. When systems such as DSP farms are developed using the DSI, use a device loading of 4 pF per pin. AC timings are based on a 20 pF load, except where noted otherwise, and a 50 Ω transmission line. For loads smaller than 20 pF, subtract 0.06 ns per pF down to 10 pF load. For loads larger than 20 pF, add 0.06 ns for SIU/Ethernet/DSI delay and 0.07 ns for GPIO/TDM/timer delay. When calculating overall loading, also consider additional RC delay.

### 2.5.1 Output Buffer Impedances

**Table 6. Output Buffer Impedances**

| Output Buffers | Typical Impedance (Ω) |
|---|---|
| System bus | 50 |
| Memory controller | 50 |
| Parallel I/O | 50 |
| **Note:** These are typical values at 65°C. The impedance may vary by ±25% depending on device process and operating temperature. | |

### 2.5.2 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.5.3** describes the clocking characteristics. **Section 2.5.4** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8113 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence. See **Table 11** for timing.
- If possible, bring up the $V_{DD}$ and $V_{DDH}$ levels together. For designs with separate power supplies, bring up the $V_{DD}$ levels and then the $V_{DDH}$ levels (see **Figure 7**).
- CLKIN should start toggling at least 16 cycles (starting after $V_{DDH}$ reaches its nominal level) before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see **Figure 6** and **Figure 7**).
- CLKIN must not be pulled high during $V_{DDH}$ power-up. CLKIN can toggle during this period.

The following figures show acceptable start-up sequence examples. **Figure 6** shows a sequence in which $V_{DD}$ and $V_{DDH}$ are raised together. **Figure 7** shows a sequence in which $V_{DDH}$ is raised after $V_{DD}$ and CLKIN begins to toggle as $V_{DDH}$ rises.

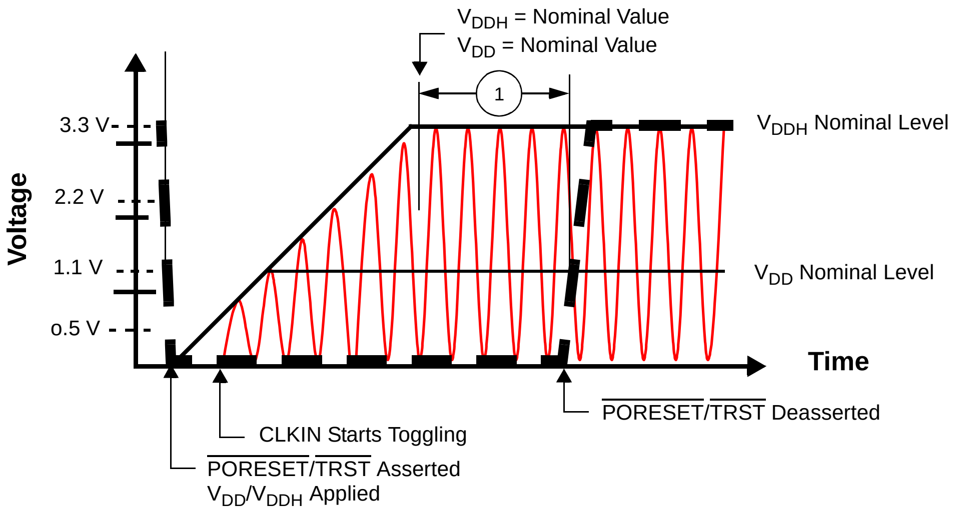


**Figure 6. Start-Up Sequence: $V_{DD}$ and $V_{DDH}$ Raised Together**

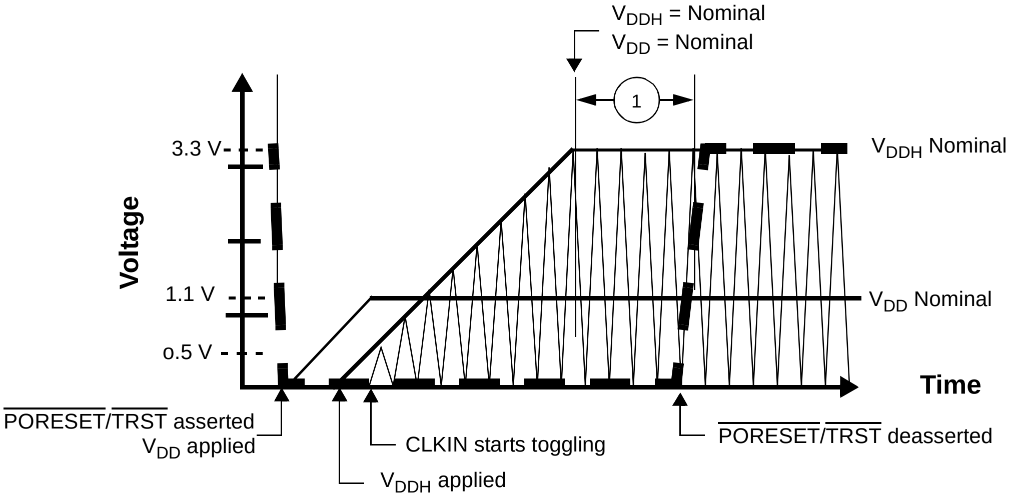


**Figure 7. Start-Up Sequence: $V_{DD}$ Raised Before $V_{DDH}$ with CLKIN Started with $V_{DDH}$**

In all cases, the power-up sequence must follow the guidelines shown in **Figure 8**.

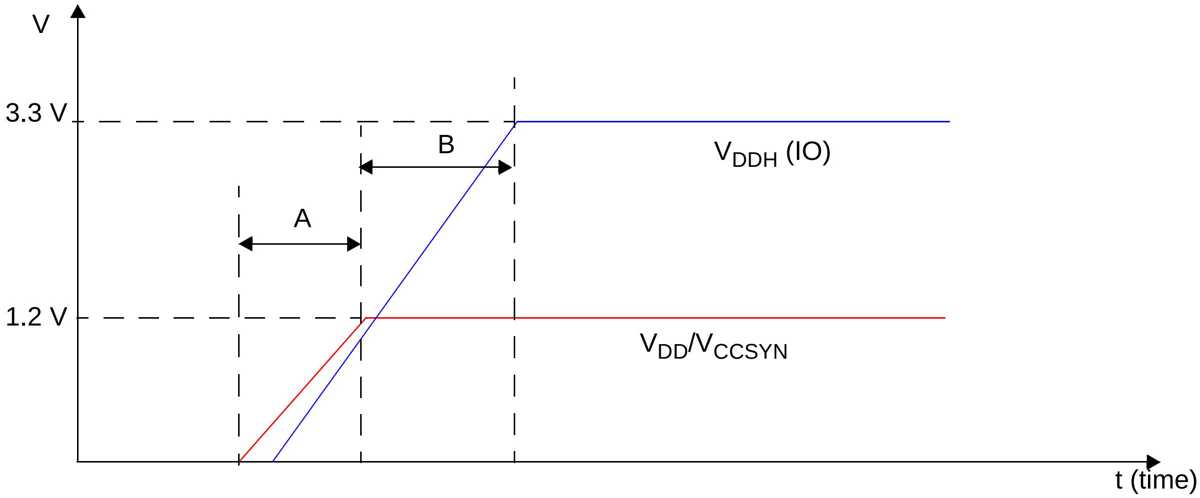


**Figure 8. Power-Up Sequence for $V_{DDH}$ and $V_{DD}/V_{CCSYN}$**

The following rules apply:

1. During time interval A, $V_{DDH}$ should always be equal to or less than the $V_{DD}/V_{CCSYN}$ voltage level. The duration of interval A should be kept below 10 ms.
2. The duration of timing interval B should be kept as small as possible and less than 10 ms.

## 2.5.3 Clock and Timing Signals

The following sections include a description of clock signal characteristics. **Table 7** shows the maximum frequency values for internal (Core, Reference, Bus, and DSI) and external (CLKIN and CLKOUT) clocks. The user must ensure that maximum frequency values are not exceeded.

**Table 7. Maximum Frequencies**

| Characteristic | Maximum in MHz |
|---|---|
| Core frequency | 300/400 |
| Reference frequency (REFCLK) | 100/133 |

### Table 7. Maximum Frequencies

| Characteristic | Maximum in MHz |
|---|---|
| Internal bus frequency (BLCK) | 100/133 |
| DSI clock frequency (HCLKIN)<br>• Core frequency = 300 MHz<br>• Core frequency = 400 MHz | <br>HCLKIN ≤ (min{70 MHz, CLKOUT})<br>HCLKIN ≤ (min{100 MHz, CLKOUT}) |
| External clock frequency (CLKIN or CLKOUT) | 100/133 |

### Table 8. Clock Frequencies

| Characteristics | Symbol | 300 MHz Device | | 400 MHz Device | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| CLKIN frequency | $F_{CLKIN}$ | 20 | 100 | 20 | 133.3 |
| BCLK frequency | $F_{BCLK}$ | 40 | 100 | 40 | 133.3 |
| Reference clock (REFCLK) frequency | $F_{REFCLK}$ | 40 | 100 | 40 | 133.3 |
| Output clock (CLKOUT) frequency | $F_{CLKOUT}$ | 40 | 100 | 40 | 133.3 |
| SC140 core clock frequency | $F_{CORE}$ | 200 | 300 | 200 | 400 |
| **Note:** The rise and fall time of external clocks should be 3 ns maximum | | | | | |

### Table 9. System Clock Parameters

| Characteristic | Min | Max | Unit |
|---|---|---|---|
| Phase jitter between BCLK and CLKIN | — | 0.3 | ns |
| CLKIN frequency | 20 | see **Table 8** | MHz |
| CLKIN slope | — | 3 | ns |
| PLL input clock (after predivider) | 20 | 100 | MHz |
| PLL output frequency (VCO output)<br>• 300 MHz core<br>• 400 MHz core | 800 | <br>1200<br>1600 | MHz<br>MHz<br>MHz |
| CLKOUT frequency jitter[1] | — | 200 | ps |
| CLKOUT phase jitter[1] with CLKIN phase jitter of ±100 ps. | — | 500 | ps |
| **Notes:** **1.** Peak-to-peak.<br>**2.** Not tested. Guaranteed by design. | | | |

## 2.5.4 Reset Timing

The MSC8113 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- Bus monitor reset
- Host reset command through JTAG

All MSC8113 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 10** describes the reset sources.

**Table 10. Reset Sources**

| Name | Direction | Description |
|---|---|---|
| Power-on reset ($\overline{\text{PORESET}}$) | Input | Initiates the power-on reset flow that resets the MSC8113 and configures various attributes of the MSC8113. On $\overline{\text{PORESET}}$, the entire MSC8113 device is reset. SPLL states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The clock mode (MODCK bits), reset configuration mode, boot mode, Chip ID, and use of either a DSI 64 bits port or a System Bus 64 bits port are configured only when $\overline{\text{PORESET}}$ is asserted. |
| External hard reset ($\overline{\text{HRESET}}$) | Input/ Output | Initiates the hard reset flow that configures various attributes of the MSC8113. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the SC140 extended cores are reset, and system configuration is sampled. The most configurable features are reconfigured. These features are defined in the 32-bit hard reset configuration word described in *Hard Reset Configuration Word* section of the *Reset* chapter in the *MSC8113 Reference Manual*. |
| External soft reset ($\overline{\text{SRESET}}$) | Input/ Output | Initiates the soft reset flow. The MSC8113 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8113 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the SC140 extended cores are reset, and system configuration is maintained. |
| Software watchdog reset | Internal | When the MSC8113 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence. |
| Bus monitor reset | Internal | When the MSC8113 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence. |
| Host reset command through the TAP | Internal | When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated. |

**Table 11** summarizes the reset actions that occur as a result of the different reset sources.

**Table 11. Reset Actions for Each Reset Source**

| Reset Action/Reset Source | Power-On Reset ($\overline{\text{PORESET}}$) | Hard Reset ($\overline{\text{HRESET}}$) | Soft Reset ($\overline{\text{SRESET}}$) | |
|---|---|---|---|---|
| | External only | External or Internal (Software Watchdog or Bus Monitor) | External | JTAG Command: EXTEST, CLAMP, or HIGHZ |
| Configuration pins sampled (Refer to **Section 2.5.4.1** for details). | Yes | No | No | No |
| SPLL state reset | Yes | No | No | No |
| System reset configuration write through the DSI | Yes | No | No | No |
| System reset configuration write though the system bus | Yes | Yes | No | No |
| $\overline{\text{HRESET}}$ driven | Yes | Yes | No | No |
| SIU registers reset | Yes | Yes | No | No |
| IPBus modules reset (TDM, UART, Timers, DSI, IPBus master, GIC, HS, and GPIO) | Yes | Yes | Yes | Yes |
| $\overline{\text{SRESET}}$ driven | Yes | Yes | Yes | Depends on command |
| SC140 extended cores reset | Yes | Yes | Yes | Yes |
| MQBS reset | Yes | Yes | Yes | Yes |

### 2.5.4.1 Power-On Reset ($\overline{\text{PORESET}}$) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 16 CLKIN cycles after $V_{DD}$ and $V_{DDH}$ are both at their nominal levels.

### 2.5.4.2 Reset Configuration

The MSC8113 has two mechanisms for writing the reset configuration:

- Through the direct slave interface (DSI)
- Through the system bus. When the reset configuration is written through the system bus, the MSC8113 acts as a configuration master or a configuration slave. If configuration slave is selected, but no special configuration word is written, a default configuration word is applied.

Fourteen signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the Reset Configuration Mode and boot and operating conditions:

- $\overline{\text{RSTCONF}}$
- CNFGS
- DSISYNC
- DSI64
- CHIP_ID[0–3]
- BM[0–2]
- SWTE
- MODCK[1–2]

### 2.5.4.3 Reset Timing Tables

**Table 12** and **Figure 9** describe the reset timing for a reset configuration write through the direct slave interface (DSI) or through the system bus.

**Table 12. Timing for a Reset Configuration Write through the DSI or System Bus**

| No. | Characteristics | Expression | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | Required external $\overline{\text{PORESET}}$ duration minimum<br>• CLKIN = 20 MHz<br>• CLKIN = 100 MHz (300 MHz core)<br>• CLKIN = 133 MHz (400 MHz core) | 16/CLKIN | <br>800<br>160<br>120 | <br>—<br>—<br>— | <br>ns<br>ns<br>ns |
| 2 | Delay from deassertion of external $\overline{\text{PORESET}}$ to deassertion of internal $\overline{\text{PORESET}}$<br>• CLKIN = 20 MHz to 133 MHz | 1024/CLKIN | 6.17 | 51.2 | µs |
| 3 | Delay from de-assertion of internal $\overline{\text{PORESET}}$ to SPLL lock<br>• CLKIN = 20 MHz (RDF = 1)<br>• CLKIN = 100 MHz (RDF = 1) (300 MHz core)<br>• CLKIN = 133 MHz (RDF = 2) (400 MHz core) | 6400/(CLKIN/RDF) (PLL reference clock-division factor) | <br>320<br>64<br>96 | <br>320<br>64<br>96 | <br>µs<br>µs<br>µs |
| 5 | Delay from SPLL to $\overline{\text{HRESET}}$ deassertion<br>• REFCLK = 40 MHz to 133 MHz | 512/REFCLK | 3.08 | 12.8 | µs |
| 6 | Delay from SPLL lock to $\overline{\text{SRESET}}$ deassertion<br>• REFCLK = 40 MHz to 133 MHz | 515/REFCLK | 3.10 | 12.88 | µs |
| 7 | Setup time from assertion of $\overline{\text{RSTCONF}}$, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] before deassertion of $\overline{\text{PORESET}}$ | | 3 | — | ns |
| 8 | Hold time from deassertion of $\overline{\text{PORESET}}$ to deassertion of $\overline{\text{RSTCONF}}$, CNFGS, DSISYNC, DSI64, CHIP_ID[0–3], BM[0–2], SWTE, and MODCK[1–2] | | 5 | — | ns |
| **Note:** | Timings are not tested, but are guaranteed by design. | | | | |

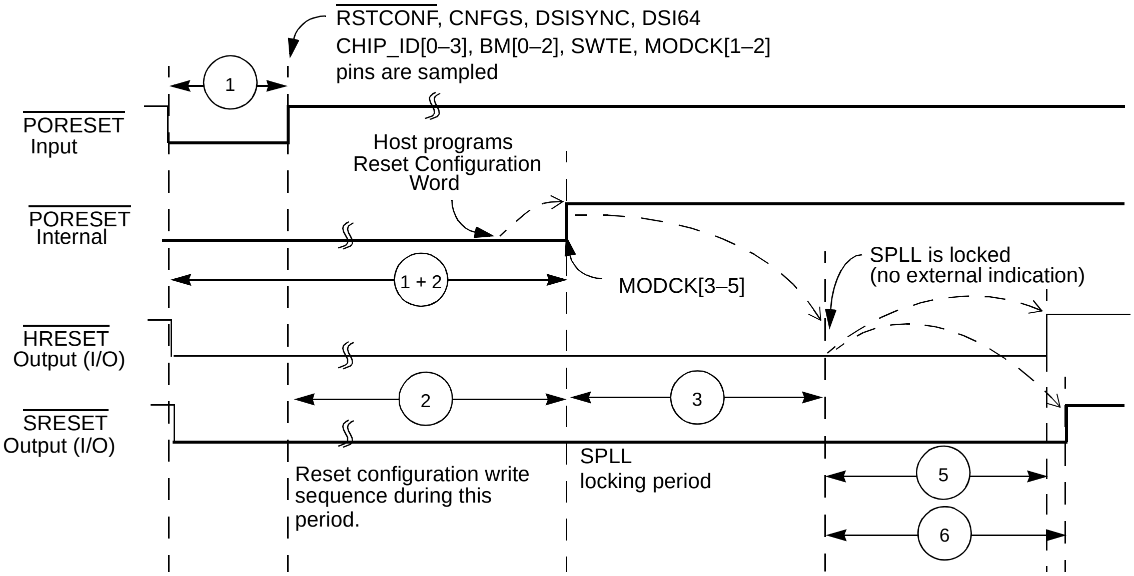


Figure 9. Timing Diagram for a Reset Configuration Write

## 2.5.5 System Bus Access Timing

### 2.5.5.1 Core Data Transfers

Generally, all MSC8113 bus and system output signals are driven from the rising edge of the reference clock (REFCLK). The REFCLK is the CLKIN signal. Memory controller signals, however, trigger on four points within a REFCLK cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge of REFCLK (and T3 at the falling edge), but the spacing of T2 and T4 depends on the PLL clock ratio selected, as **Table 13** shows.

Table 13. Tick Spacing for Memory Controller Signals

| BCLK/SC140 clock | Tick Spacing (T1 Occurs at the Rising Edge of REFCLK) | | |
|---|---|---|---|
| | T2 | T3 | T4 |
| 1:4, 1:6, 1:8, 1:10 | 1/4 REFCLK | 1/2 REFCLK | 3/4 REFCLK |
| 1:3 | 1/6 REFCLK | 1/2 REFCLK | 4/6 REFCLK |
| 1:5 | 2/10 REFCLK | 1/2 REFCLK | 7/10 REFCLK |

**Figure 10** is a graphical representation of **Table 13**.

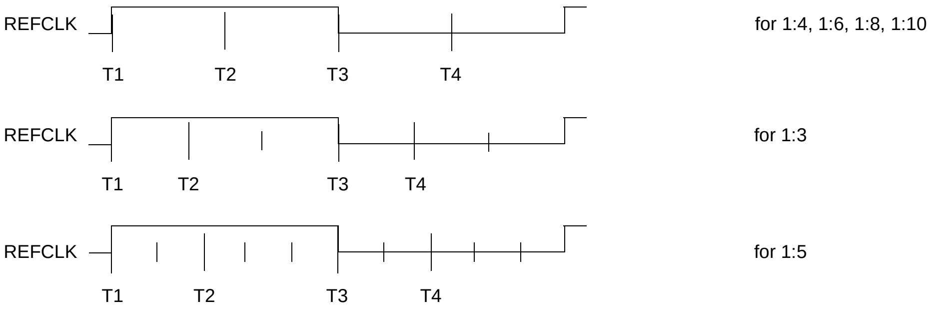


Figure 10. Internal Tick Spacing for Memory Controller Signals

The UPM machine and GPCM machine outputs change on the internal tick selected by the memory controller configuration. The AC timing specifications are relative to the internal tick. SDRAM machine outputs change only on the REFCLK rising edge.

### Table 14. AC Timing for SIU Inputs

| No. | Characteristic | Ref = CLKIN at 1.1 V and 100/133 MHz | Units |
|---|---|---|---|
| 10 | Hold time for all signals after the 50% level of the REFCLK rising edge | 0.5 | ns |
| 11a | $\overline{\text{ARTRY}}$/$\overline{\text{ABB}}$ set-up time before the 50% level of the REFCLK rising edge | 3.1 | ns |
| 11b | $\overline{\text{DBG}}$/$\overline{\text{DBB}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{TC}}$ set-up time before the 50% level of the REFCLK rising edge | 3.6 | ns |
| 11c | $\overline{\text{AACK}}$ set-up time before the 50% level of the REFCLK rising edge | 3.0 | ns |
| 11d | $\overline{\text{TA}}$/$\overline{\text{TEA}}$/$\overline{\text{PSDVAL}}$ set-up time before the 50% level of the REFCLK rising edge<br>• Data-pipeline mode<br>• Non-pipeline mode | 3.5<br>4.4 | ns<br>ns |
| 12 | Data bus set-up time before REFCLK rising edge in Normal mode<br>• Data-pipeline mode<br>• Non-pipeline mode | 1.9<br>4.2 | ns<br>ns |
| 13[1] | Data bus set-up time before the 50% level of the REFCLK rising edge in ECC and PARITY modes<br>• Data-pipeline mode<br>• Non-pipeline mode | 2.0<br>8.2 | ns<br>ns |
| 14[1] | DP set-up time before the 50% level of the REFCLK rising edge<br>• Data-pipeline mode<br>• Non-pipeline mode | 2.0<br>7.9 | ns<br>ns |
| 15a | $\overline{\text{TS}}$ and Address bus set-up time before the 50% level of the REFCLK rising edge<br>• Extra cycle mode (SIUBCR[EXDD] = 0)<br>• No extra cycle mode (SIUBCR[EXDD] = 1) | 4.2<br>5.5 | ns<br>ns |
| 15b | Address attributes: TT/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ set-up time before the 50% level of the REFCLK rising edge<br>• Extra cycle mode (SIUBCR[EXDD] = 0)<br>• No extra cycle mode (SIUBCR[EXDD] = 1) | 3.7<br>4.8 | ns<br>ns |
| 16 | PUPMWAIT signal set-up time before the 50% level of the REFCLK rising edge | 3.7 | ns |
| 17 | $\overline{\text{IRQx}}$ setup time before the 50% level; of the REFCLK rising edge[3] | 4.0 | ns |
| 18 | $\overline{\text{IRQx}}$ minimum pulse width[3] | 6.0 + $T_{REFCLK}$ | ns |

**Notes:**
1. Timings specifications 13 and 14 in non-pipeline mode are more restrictive than MSC8102 timings.
2. Values are measured from the 50% TTL transition level relative to the 50% level of the REFCLK rising edge.
3. Guaranteed by design.

### Table 15. AC Timing for SIU Outputs

| No. | Characteristic | Bus Speed in MHz[3] Ref = CLKIN at 1.1 V and 100/ 133 MHz | Units |
|---|---|---|---|
| 30[2] | Minimum delay from the 50% level of the REFCLK for all signals | 0.9 | ns |
| 31 | $\overline{\text{PSDVAL}}$/$\overline{\text{TEA}}$/$\overline{\text{TA}}$ max delay from the 50% level of the REFCLK rising edge | 6.0 | ns |
| 32a | Address bus max delay from the 50% level of the REFCLK rising edge<br>• Multi-master mode (SIUBCR[EBM] = 1)<br>• Single-master mode (SIUBCR[EBM] = 0) | <br>6.4<br>5.3 | <br>ns<br>ns |
| 32b | Address attributes: TT[0–1]/$\overline{\text{TBST}}$/TSZ/$\overline{\text{GBL}}$ max delay from the 50% level of the REFCLK rising edge | 6.4 | ns |
| 32c | Address attributes: TT[2–4]/TC max delay from the 50% level of the REFCLK rising edge | 6.9 | ns |
| 32d | BADDR max delay from the 50% level of the REFCLK rising edge | 5.2 | ns |
| 33a | Data bus max delay from the 50% level of the REFCLK rising edge<br>• Data-pipeline mode<br>• Non-pipeline mode | <br>4.8<br>7.1 | <br>ns<br>ns |
| 33b | DP max delay from the 50% level of the REFCLK rising edge<br>• Data-pipeline mode<br>• Non-pipeline mode | <br>6.0<br>7.5 | <br>ns<br>ns |
| 34 | Memory controller signals/ALE/$\overline{\text{CS[0–4]}}$ max delay from the 50% level of the REFCLK rising edge | 5.1 | ns |
| 35a | $\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$/$\overline{\text{DBB}}$ max delay from the 50% level of the REFCLK rising edge | 6.0 | ns |
| 35b | $\overline{\text{AACK}}$/$\overline{\text{ABB}}$/$\overline{\text{TS}}$/$\overline{\text{CS[5–7]}}$ max delay from the 50% level of the REFCLK rising edge | 5.5 | ns |

**Notes:**

1. Values are measured from the 50% level of the REFCLK rising edge to the 50% signal level and assume a 20 pF load except where otherwise specified.
2. Except for specification 30, which is specified for a 10 pF load, all timings in this table are specified for a 20 pF load. Decreasing the load results in a timing decrease at the rate of 0.3 ns per 5 pF decrease in load. Increasing the load results in a timing increase at the rate of 0.15 ns per 5 pF increase in load.
3. The maximum bus frequency depends on the mode:
   - In 60x-compatible mode connected to another MSC8113 device, the frequency is determined by adding the input and output longest timing values, which results in the total delay for 20 pF output capacitance. You must also account for other influences that can affect timing, such as on-board clock skews, on-board noise delays, and so on.
   - In single-master mode, the frequency depends on the timing of the devices connected to the MSC8113.
   - To achieve maximum performance on the bus in single-master mode, disable the $\overline{\text{DBB}}$ signal by writing a 1 to the SIUMCR[BDD] bit. See the SIU chapter in the *MSC8113 Reference Manual* for details.

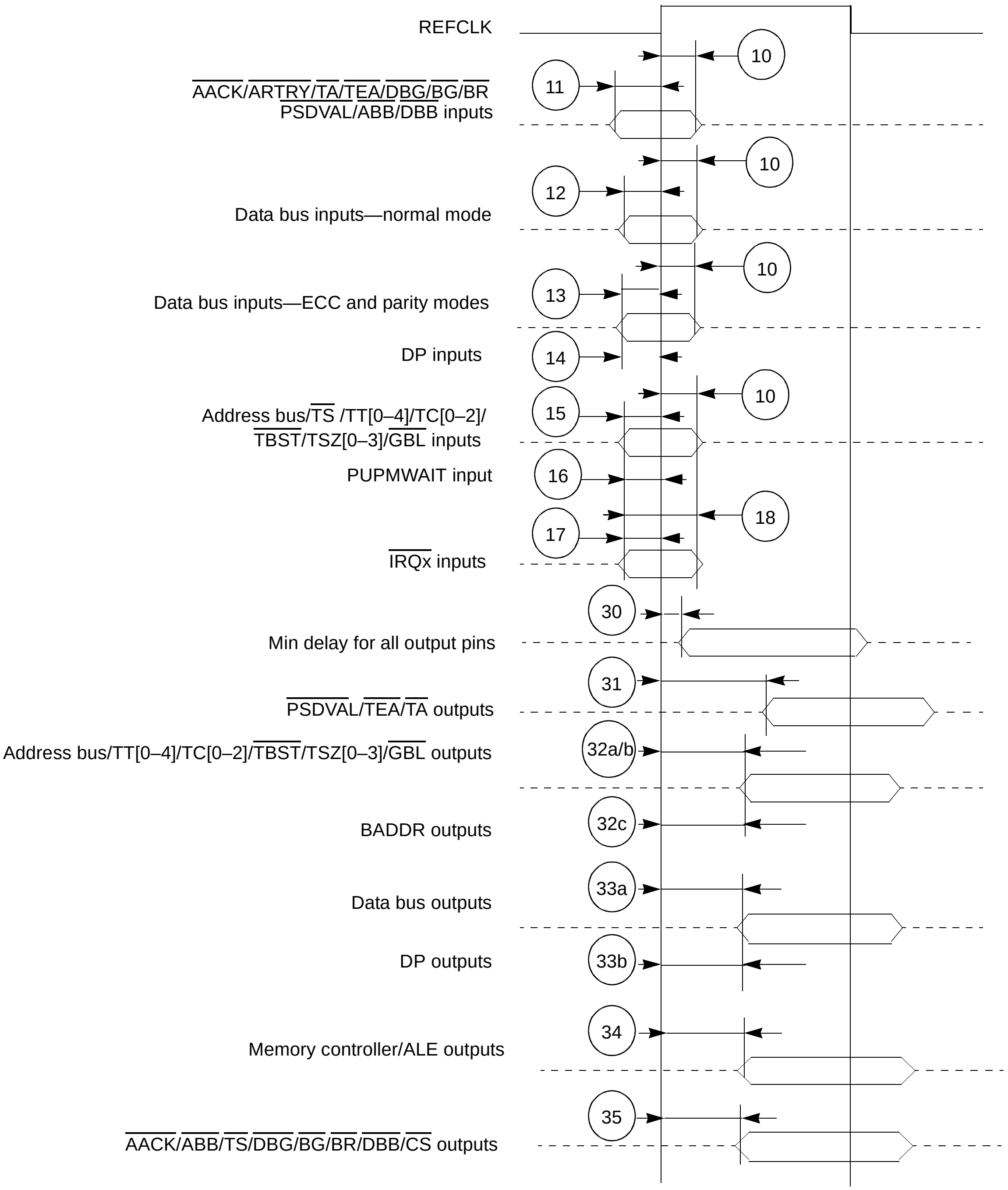


**Figure 11. SIU Timing Diagram**

### 2.5.5.2 CLKIN to CLKOUT Skew

**Table 17** describes the CLKOUT-to-CLKIN skew timing.

**Table 16. CLKOUT Skew**

| No. | Characteristic | Min[1] | Max[1] | Units |
|---|---|---|---|---|
| 20 | Rise-to-rise skew | 0.0 | 0.95 | ns |
| 21 | Fall-to-fall skew | –1.5 | 1.0 | ns |
| 23 | CLKOUT phase (1.1 V, 133 MHz)<br>• Phase high<br>• Phase low | <br>2.2<br>2.2 | <br>—<br>— | <br>ns<br>ns |
| 24 | CLKOUT phase (1.1 V, 100 MHz)<br>• Phase high<br>• Phase low | <br>3.3<br>3.3 | <br>—<br>— | <br>ns<br>ns |

**Notes:**
1. A positive number indicates that CLKOUT precedes CLKIN, A negative number indicates that CLKOUT follows CLKIN.
2. Skews are measured in clock mode 29, with a CLKIN:CLKOUT ratio of 1:1. The same skew is valid for all clock modes.
3. CLKOUT skews are measured using a load of 10 pF.
4. CLKOUT skews and phase are not measured for 500/166 Mhz parts because these parts only use CLKIN mode.

For designs that use the CLKOUT synchronization mode, use the skew values listed in **Table 16** to adjust the rise-to-fall timing values specified for CLKIN synchronization. **Figure 12** shows the relationship between the CLKOUT and CLKIN timings.

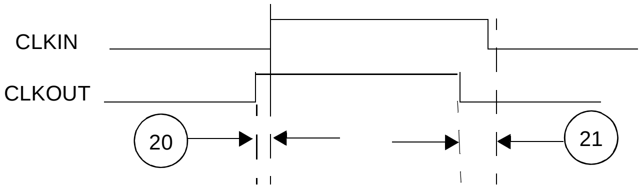


**Figure 12. CLKOUT and CLKIN Signals.**

### 2.5.5.3 DMA Data Transfers

**Table 17** describes the DMA signal timing.

**Table 17. DMA Signals**

| No. | Characteristic | Ref = CLKIN | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| 37 | DREQ set-up time before the 50% level of the falling edge of REFCLK | 5.0 | — | ns |
| 38 | DREQ hold time after the 50% level of the falling edge of REFCLK | 0.5 | — | ns |
| 39 | $\overline{\text{DONE}}$ set-up time before the 50% level of the rising edge of REFCLK | 5.0 | — | ns |
| 40 | $\overline{\text{DONE}}$ hold time after the 50% level of the rising edge of REFCLK | 0.5 | — | ns |
| 41 | $\overline{\text{DACK}}$/$\overline{\text{DRACK}}$/$\overline{\text{DONE}}$ delay after the 50% level of the REFCLK rising edge | 0.5 | 7.5 | ns |

The DREQ signal is synchronized with REFCLK. To achieve fast response, a synchronized peripheral should assert DREQ according to the timings in **Table 17**. **Figure 13** shows synchronous peripheral interaction.

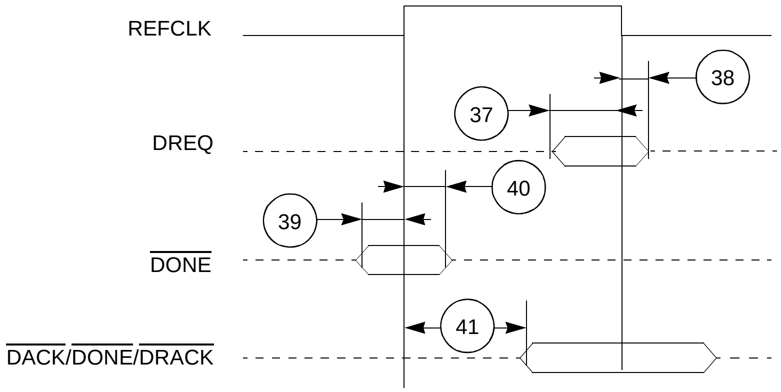


**Figure 13. DMA Signals**

## 2.5.6 DSI Timing

The timings in the following sections are based on a 20 pF capacitive load.

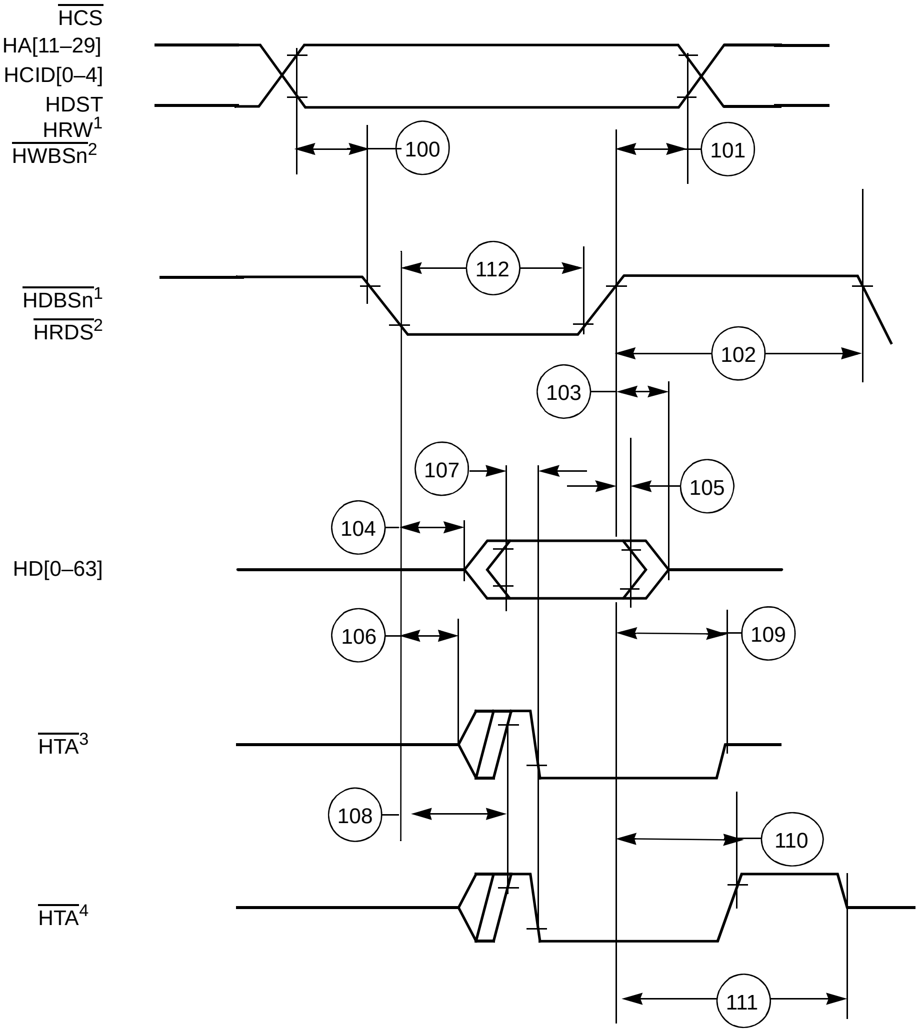
### 2.5.6.1 DSI Asynchronous Mode

**Table 18. DSI Asynchronous Mode Timing**

| No. | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 100 | Attributes[1] set-up time before strobe ($\overline{\text{HWBS[n]}}$) assertion | 1.5 | — | ns |
| 101 | Attributes[1] hold time after data strobe deassertion | 1.3 | — | ns |
| 102 | Read/Write data strobe deassertion width:<br>• DCR[HTAAD] = 1<br>— Consecutive access to the same DSI<br>— Different device with DCR[HTADT] = 01<br>— Different device with DCR[HTADT] = 10<br>— Different device with DCR[HTADT] = 11<br>• DCR[HTAAD] = 0 | <br><br>$1.8 + T_{REFCLK}$<br>$5 + T_{REFCLK}$<br>$5 + (1.5 \times T_{REFCLK})$<br>$5 + (2.5 \times T_{REFCLK})$<br>$1.8 + T_{REFCLK}$ | — | <br><br>ns<br>ns<br>ns<br>ns<br>ns |
| 103 | Read data strobe deassertion to output data high impedance | — | 8.5 | ns |
| 104 | Read data strobe assertion to output data active from high impedance | 2.0 | — | ns |
| 105 | Output data hold time after read data strobe deassertion | 2.2 | — | ns |
| 106 | Read/Write data strobe assertion to $\overline{\text{HTA}}$ active from high impedance | 2.2 | — | ns |
| 107 | Output data valid to $\overline{\text{HTA}}$ assertion | 3.2 | — | ns |
| 108 | Read/Write data strobe assertion to $\overline{\text{HTA}}$ valid[2] | — | 7.4 | ns |
| 109 | Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance.<br>(DCR[HTAAD] = 0, $\overline{\text{HTA}}$ at end of access released at logic 0) | — | 6.5 | ns |
| 110 | Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ deassertion.<br>(DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1) | — | 6.5 | ns |
| 111 | Read/Write data strobe deassertion to output $\overline{\text{HTA}}$ high impedance.<br>(DCR[HTAAD] = 1, $\overline{\text{HTA}}$ at end of access released at logic 1<br>• DCR[HTADT] = 01<br>• DCR[HTADT] = 10<br>• DCR[HTADT] = 11 | — | <br><br>$5 + T_{REFCLK}$<br>$5 + (1.5 \times T_{REFCLK})$<br>$5 + (2.5 \times T_{REFCLK})$ | <br><br>ns<br>ns<br>ns |
| 112 | Read/Write data strobe assertion width | $1.8 + T_{REFCLK}$ | — | ns |
| 201 | Host data input set-up time before write data strobe deassertion | 1.0 | — | ns |
| 202 | Host data input hold time after write data strobe deassertion | 1.7 | — | ns |

**Notes:**
1. *Attributes* refers to the following signals: $\overline{\text{HCS}}$, HA[11–29], HCID[0–4], HDST, HRW, $\overline{\text{HRDS}}$, and $\overline{\text{HWBSn}}$.
2. This specification is tested in dual-strobe mode. Timing in single-strobe mode is guaranteed by design.
3. All values listed in this table are tested or guaranteed by design.

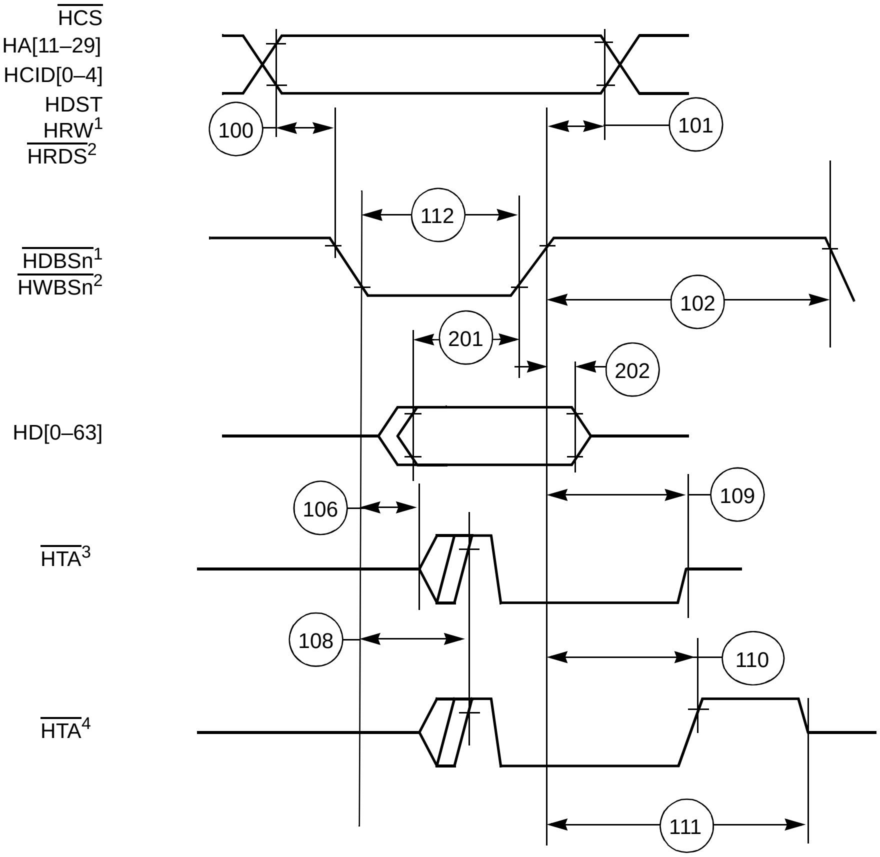
**Figure 14** shows DSI asynchronous read signals timing.



**Notes:**
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. $\overline{\text{HTA}}$ released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. $\overline{\text{HTA}}$ released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

**Figure 14. Asynchronous Single- and Dual-Strobe Modes Read Timing Diagram**

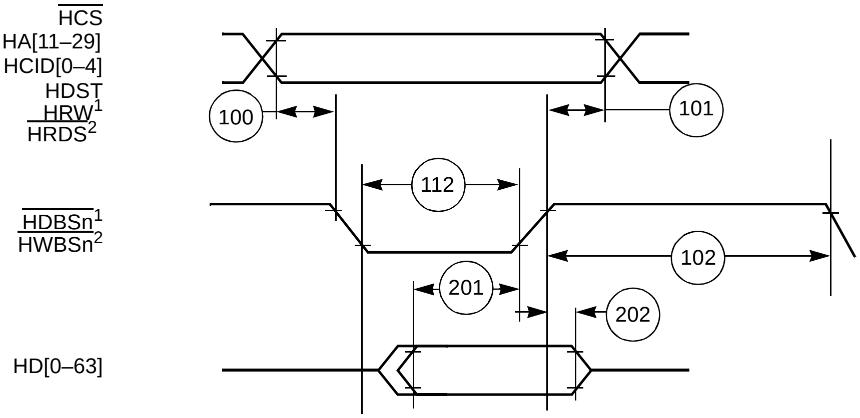
**Figure 15** shows DSI asynchronous write signals timing.



**Notes:**
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.
3. HTA released at logic 0 (DCR[HTAAD] = 0) at end of access; used with pull-down implementation.
4. HTA released at logic 1 (DCR[HTAAD] = 1) at end of access; used with pull-up implementation.

Figure 15. Asynchronous Single- and Dual-Strobe Modes Write Timing Diagram

**Figure 16** shows DSI asynchronous broadcast write signals timing.



**Notes:**
1. Used for single-strobe mode access.
2. Used for dual-strobe mode access.

Figure 16. Asynchronous Broadcast Write Timing Diagram

### 2.5.6.2 DSI Synchronous Mode

**Table 19. DSI Inputs in Synchronous Mode**

| No. | Characteristic | Expression | 1.1 V Core | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 120 | HCLKIN cycle time[1,2] | HTC | 10.0 | 55.6 | ns |
| 121 | HCLKIN high pulse width | (0.5 ± 0.1) × HTC | 4.0 | 33.3 | ns |
| 122 | HCLKIN low pulse width | (0.5 ± 0.1) × HTC | 4.0 | 33.3 | ns |
| 123 | HA[11–29] inputs set-up time | — | 1.2 | — | ns |
| 124 | HD[0–63] inputs set-up time | — | 0.6 | — | ns |
| 125 | HCID[0–4] inputs set-up time | — | 1.3 | — | ns |
| 126 | All other inputs set-up time | — | 1.2 | — | ns |
| 127 | All inputs hold time | — | 1.5 | — | ns |

**Notes:**
1. Values are based on a frequency range of 18–100 MHz.
2. Refer to **Table 7** for HCLKIN frequency limits.

**Table 20. DSI Outputs in Synchronous Mode**

| No. | Characteristic | 1.1 V Core | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| 128 | HCLKIN high to HD[0–63] output active | 2.0 | — | ns |
| 129 | HCLKIN high to HD[0–63] output valid | — | 7.6 | ns |
| 130 | HD[0–63] output hold time | 1.7 | — | ns |
| 131 | HCLKIN high to HD[0–63] output high impedance | — | 8.3 | ns |
| 132 | HCLKIN high to $\overline{\text{HTA}}$ output active | 2.2 | — | ns |
| 133 | HCLKIN high to $\overline{\text{HTA}}$ output valid | — | 7.4 | ns |
| 134 | $\overline{\text{HTA}}$ output hold time | 1.7 | — | ns |
| 135 | HCLKIN high to $\overline{\text{HTA}}$ high impedance | — | 7.5 | ns |

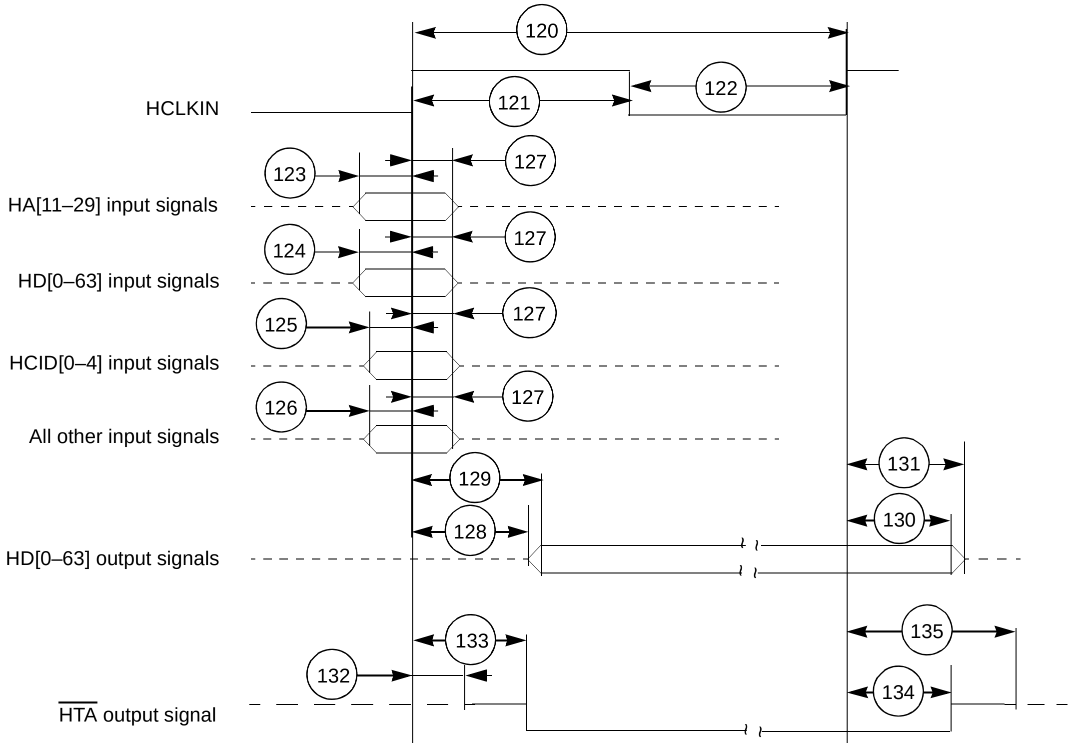


Figure 17. DSI Synchronous Mode Signals Timing Diagram

## 2.5.7 TDM Timing

Table 21. TDM Timing

| No. | Characteristic | Expression | 1.1 V Core | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 300 | TDMxRCLK/TDMxTCLK | TC[1] | 16 | — | ns |
| 301 | TDMxRCLK/TDMxTCLK high pulse width | (0.5 ± 0.1) × TC | 7 | — | ns |
| 302 | TDMxRCLK/TDMxTCLK low pulse width | (0.5 ± 0.1) × TC | 7 | — | ns |
| 303 | TDM receive all input set-up time | | 1.3 | — | ns |
| 304 | TDM receive all input hold time | | 1.0 | — | ns |
| 305 | TDMxTCLK high to TDMxTDAT/TDMxRCLK output active[2,3] | | 2.8 | — | ns |
| 306 | TDMxTCLK high to TDMxTDAT/TDMxRCLK output | | — | 10.0 | ns |
| 307 | All output hold time[4] | | 2.5 | — | ns |
| 308 | TDMxTCLK high to TDmXTDAT/TDMxRCLK output high impedance[2,3] | | — | 10.7 | ns |
| 309 | TDMxTCLK high to TDMXTSYN output valid[2] | | — | 9.7 | ns |
| 310 | TDMxTSYN output hold time[4] | | 2.5 | — | ns |

**Notes:**
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz. Devices operating at 300 MHz are limited to a maximum TDMxRCLK/TDMxTCLK frequency of 50 MHz.
2. Values are based on 20 pF capacitive load.
3. When configured as an output, TDMxRCLK acts as a second data link. See the *MSC8113 Reference Manual* for details.
4. Values are based on 10 pF capacitive load.

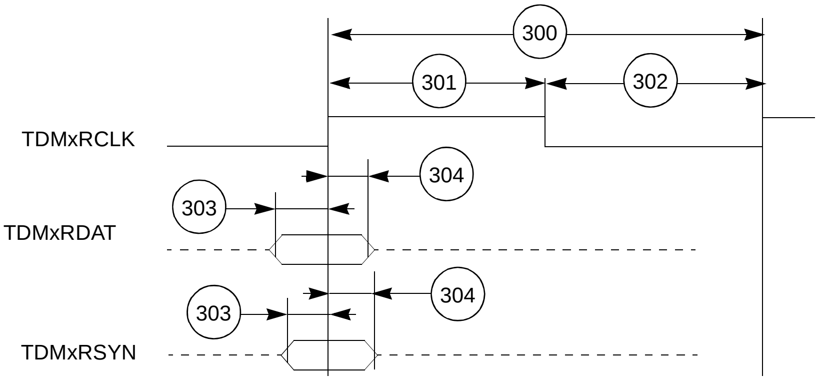


Figure 18. TDM Inputs Signals

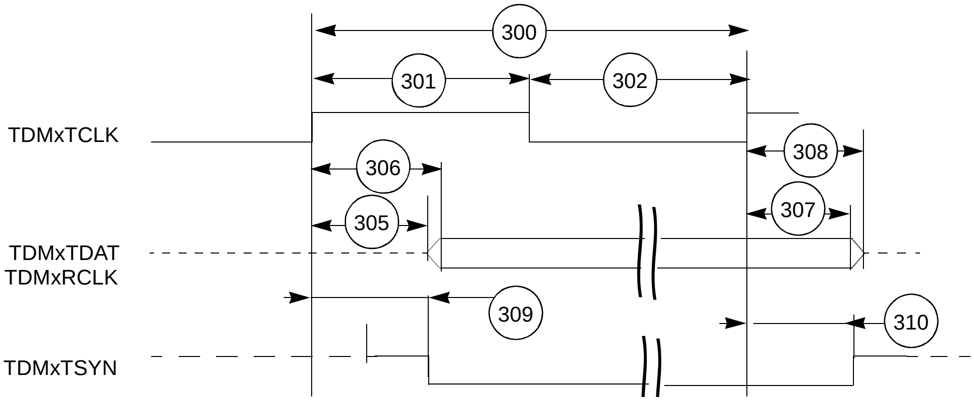


Figure 19. TDM Output Signals

### 2.5.8 UART Timing

**Table 22. UART Timing**

| No. | Characteristics | Expression | Min | Max | Unit |
|---|---|---|---|---|---|
| 400 | URXD and UTXD inputs high/low duration | 16 × $T_{REFCLK}$ | 160.0 | — | ns |
| 401 | URXD and UTXD inputs rise/fall time | | | 10 | ns |
| 402 | UTXD output rise/fall time | | | 10 | ns |

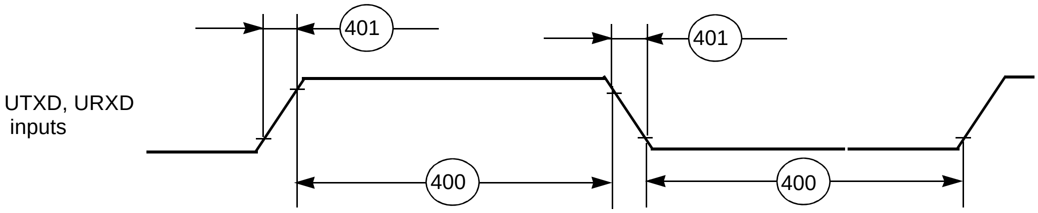


Figure 20. UART Input Timing

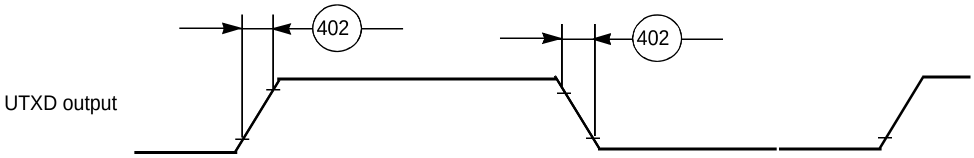


Figure 21. UART Output Timing

### 2.5.9 Timer Timing

**Table 23. Timer Timing**

| No. | Characteristics | Ref = CLKIN | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 500 | TIMERx frequency | 10.0 | — | ns |
| 501 | TIMERx Input high period | 4.0 | — | ns |
| 502 | TIMERx Output low period | 4.0 | — | ns |
| 503 | TIMERx Propagations delay from its clock input | 3.1 | 9.5 | ns |

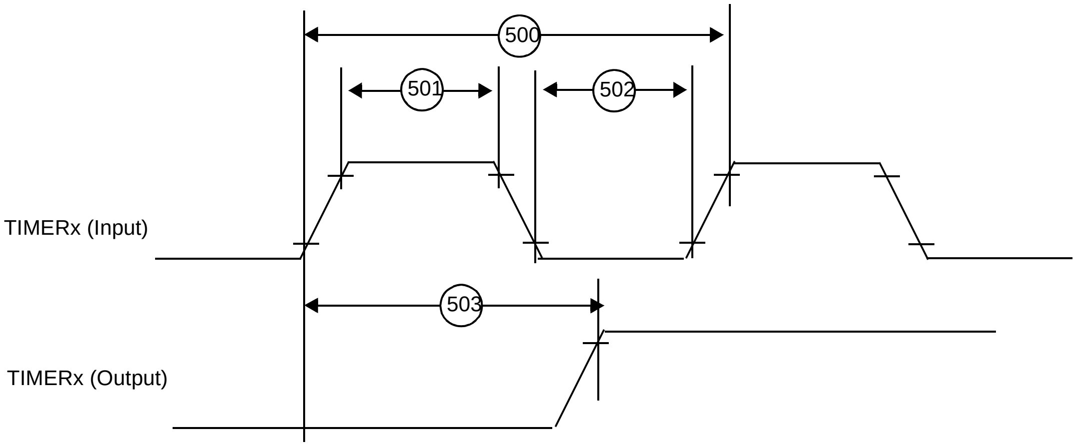


Figure 22. Timer Timing

## 2.5.10 Ethernet Timing

### 2.5.10.1 Management Interface Timing

Table 24. Ethernet Controller Management Interface Timing

| No. | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 801 | ETHMDIO to ETHMDC rising edge set-up time | 10 | — | ns |
| 802 | ETHMDC rising edge to ETHMDIO hold time | 10 | — | ns |

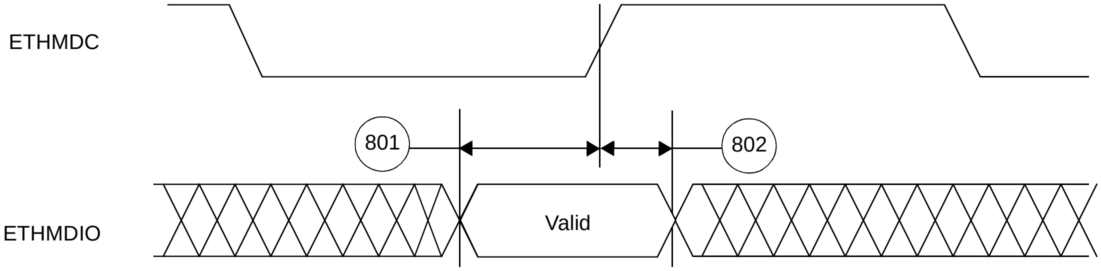


Figure 23. MDIO Timing Relationship to MDC

## 2.5.10.2 MII Mode Timing

**Table 25. MII Mode Signal Timing**

| No. | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 803 | ETHRX_DV, ETHRXD[0–3], ETHRX_ER to ETHRX_CLK rising edge set-up time | 3.5 | — | ns |
| 804 | ETHRX_CLK rising edge to ETHRX_DV, ETHRXD[0–3], ETHRX_ER hold time | 3.5 | — | ns |
| 805 | ETHTX_CLK to ETHTX_EN, ETHTXD[0–3], ETHTX_ER output delay | 1 | 14.6 | ns |

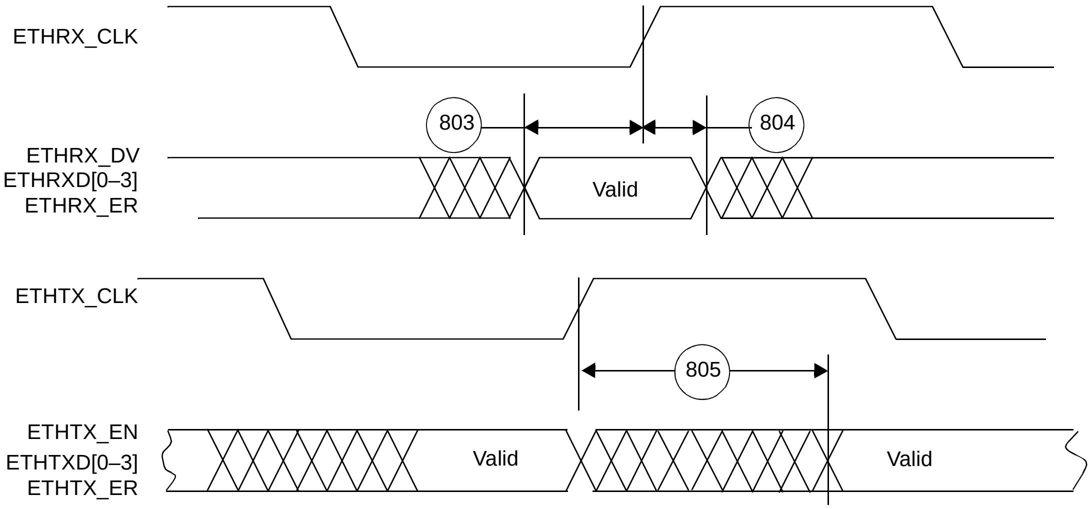


**Figure 24. MII Mode Signal Timing**

## 2.5.10.3 RMII Mode

**Table 26. RMII Mode Signal Timing**

| No. | Characteristics | 1.1 V Core | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 806 | ETHTX_EN,ETHRXD[0–1], ETHCRS_DV, ETHRX_ER to ETHREF_CLK rising edge set-up time | 1.6 | — | ns |
| 807 | ETHREF_CLK rising edge to ETHRXD[0–1], ETHCRS_DV, ETHRX_ER hold time | 1.6 | — | ns |
| 811 | ETHREF_CLK rising edge to ETHTXD[0–1], ETHTX_EN output delay. | 3 | 12.5 | ns |

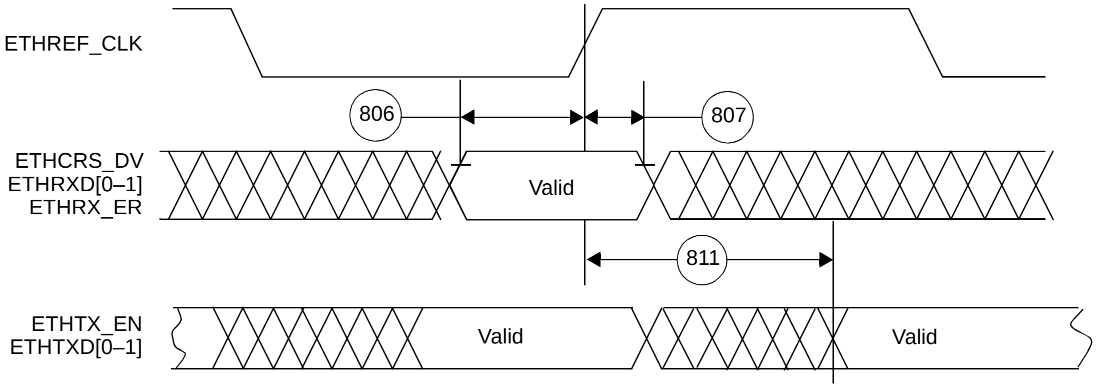


**Figure 25. RMII Mode Signal Timing**

### 2.5.10.4 SMII Mode

**Table 27. SMII Mode Signal Timing**

| No. | Characteristics | Min | Max | Unit |
|---|---|---|---|---|
| 808 | ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge set-up time | 1.0 | — | ns |
| 809 | ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time | 1.0 | — | ns |
| 810 | ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay | 1.5[1] | 6.0[2] | ns |
| **Notes:** **1.** Measured using a 5 pF load.<br>**2.** Measured using a 15 pF load. | | | | |

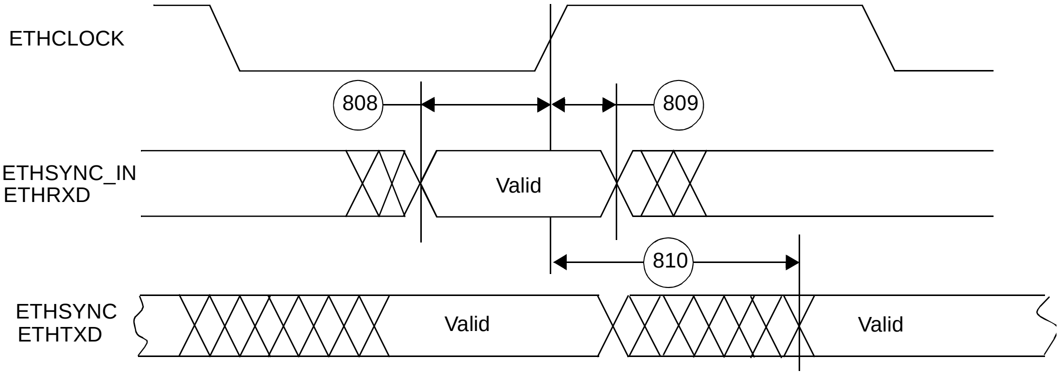


Figure 26. SMII Mode Signal Timing

## 2.5.11 GPIO Timing

**Table 28. GPIO Timing**

| No. | Characteristics | Ref = CLKIN | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 601 | REFCLK edge to GPIO out valid (GPIO out delay time) | — | 6.1 | ns |
| 602 | REFCLK edge to GPIO out not valid (GPIO out hold time) | 1.1 | — | ns |
| 603 | REFCLK edge to high impedance on GPIO out | — | 5.4 | ns |
| 604 | GPIO in valid to REFCLK edge (GPIO in set-up time) | 3.5 | — | ns |
| 605 | REFCLK edge to GPIO in not valid (GPIO in hold time) | 0.5 | — | ns |

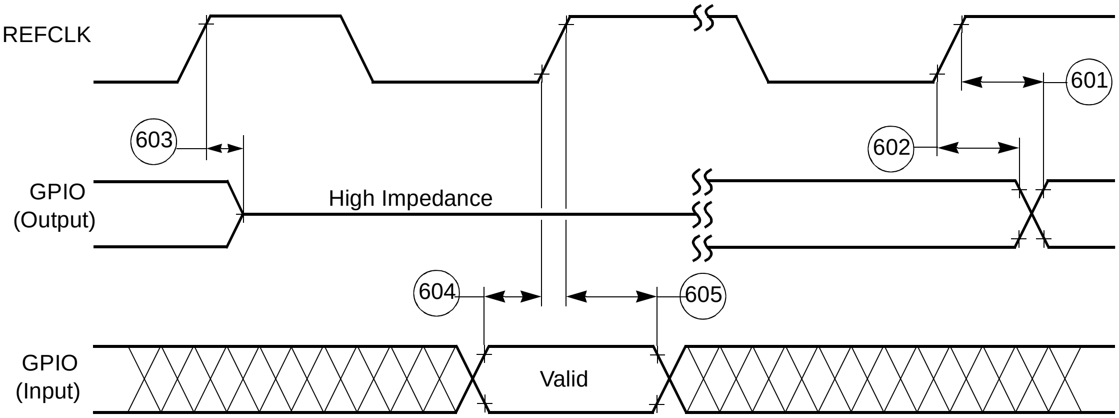


Figure 27. GPIO Timing

### 2.5.12 EE Signals

**Table 29. EE Pin Timing**

| Number | Characteristics | Type | Min |
|---|---|---|---|
| 65 | EE0 (input) | Asynchronous | 4 core clock periods |
| 66 | EE1 (output) | Synchronous to Core clock | 1 core clock period |

**Notes:** **1.** The core clock is the SC140 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
**2.** Refer to **Table 1-4** on page 1-6 for details on EE pin functionality.

**Figure 28** shows the signal behavior of the EE pins.

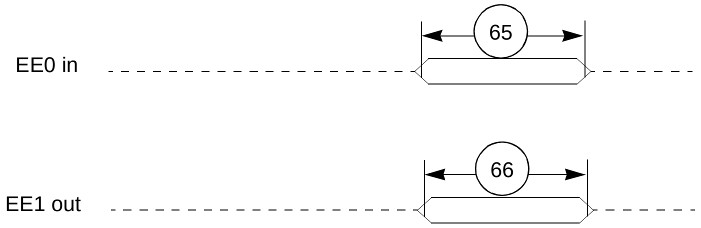


Figure 28. EE Pin Timing

### 2.5.13 JTAG Signals

**Table 30. JTAG Timing**

| No. | Characteristics | All frequencies Min | All frequencies Max | Unit |
|---|---|---|---|---|
| 700 | TCK frequency of operation (1/($T_C \times 4$); maximum 25 MHz) | 0.0 | 25 | MHz |
| 701 | TCK cycle time | 40.0 | — | ns |
| 702 | TCK clock pulse width measured at $V_M$ = 1.6 V<br>• High<br>• Low | <br>20.0<br>16.0 | <br>—<br>— | <br>ns<br>ns |
| 703 | TCK rise and fall times | 0.0 | 3.0 | ns |
| 704 | Boundary scan input data set-up time | 5.0 | — | ns |
| 705 | Boundary scan input data hold time | 20.0 | — | ns |
| 706 | TCK low to output data valid | 0.0 | 30.0 | ns |
| 707 | TCK low to output high impedance | 0.0 | 30.0 | ns |
| 708 | TMS, TDI data set-up time | 5.0 | — | ns |
| 709 | TMS, TDI data hold time | 20.0 | — | ns |
| 710 | TCK low to TDO data valid | 0.0 | 20.0 | ns |
| 711 | TCK low to TDO high impedance | 0.0 | 20.0 | ns |
| 712 | $\overline{\text{TRST}}$ assert time | 100.0 | — | ns |
| 713 | $\overline{\text{TRST}}$ set-up time to TCK low | 30.0 | — | ns |
| **Note:** | All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port. | | | |

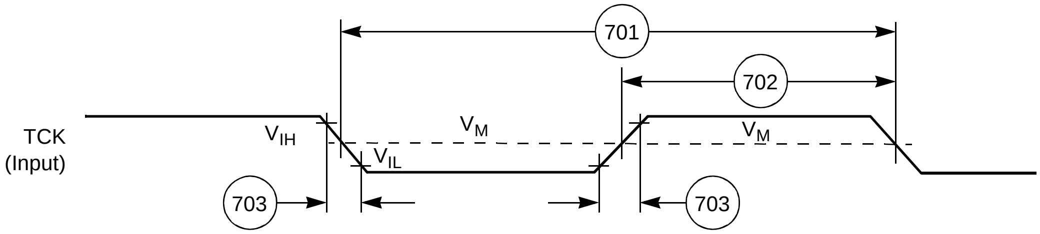


Figure 29. Test Clock Input Timing Diagram

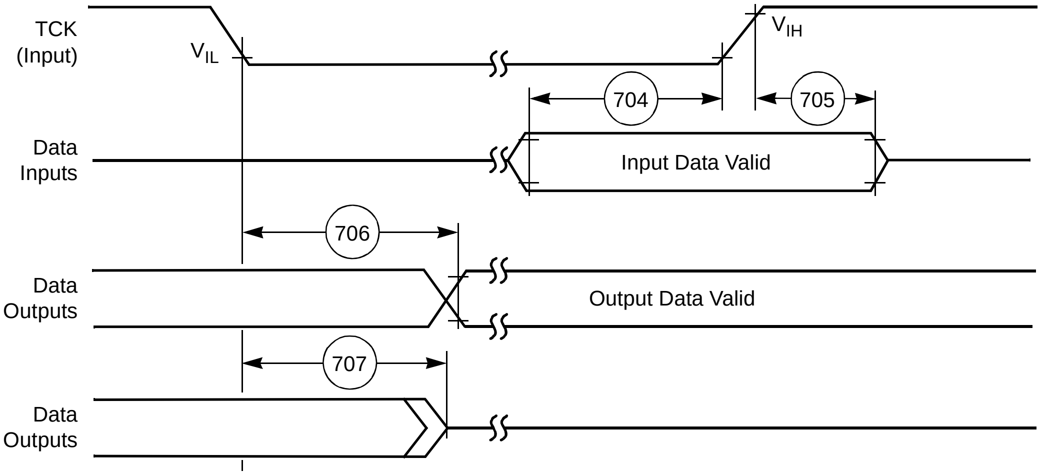


Figure 30. Boundary Scan (JTAG) Timing Diagram

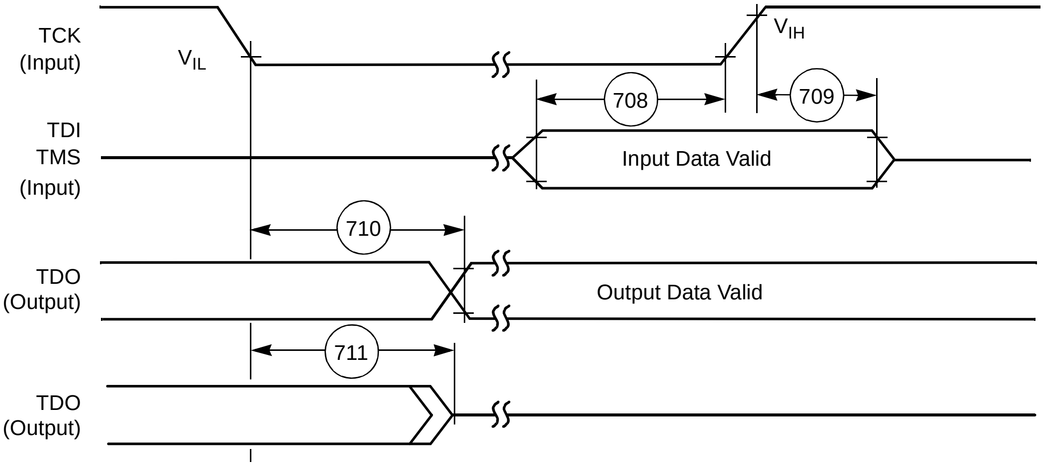


Figure 31. Test Access Port Timing Diagram

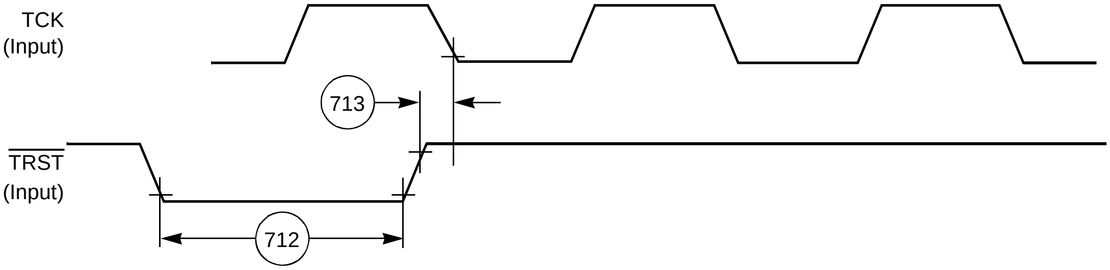


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

# 3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8113 device is designed into a system.

## 3.1 Start-up Sequencing Recommendations

Use the following guidelines for start-up and power-down sequences:

- Assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ before applying power and keep the signals driven low until the power reaches the required minimum power levels. This can be implemented via weak pull-down resistors.
- CLKIN can be held low or allowed to toggle during the beginning of the power-up sequence. However, CLKIN must start toggling before the deassertion of $\overline{\text{PORESET}}$ and after both power supplies have reached nominal voltage levels.
- If possible, bring up $V_{DD}/V_{CCSYN}$ and $V_{DDH}$ together. If it is not possible, raise $V_{DD}/V_{CCSYN}$ first and then bring up $V_{DDH}$. $V_{DDH}$ should not exceed $V_{DD}/V_{CCSYN}$ until $V_{DD}/V_{CCSYN}$ reaches its nominal voltage level. Similarly, bring both voltage levels down together. If that is not possible reverse the power-up sequence, with $V_{DDH}$ going down first and then $V_{DD}/V_{CCSYN}$.

**Note:** This recommended power sequencing for the MSC8113 is different from the MSC8102.

External voltage applied to any input line must not exceed the I/O supply $V_{DDH}$ by more than 0.8 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule. However, each such input can draw up to 80 mA per input pin per device in the system during start-up.

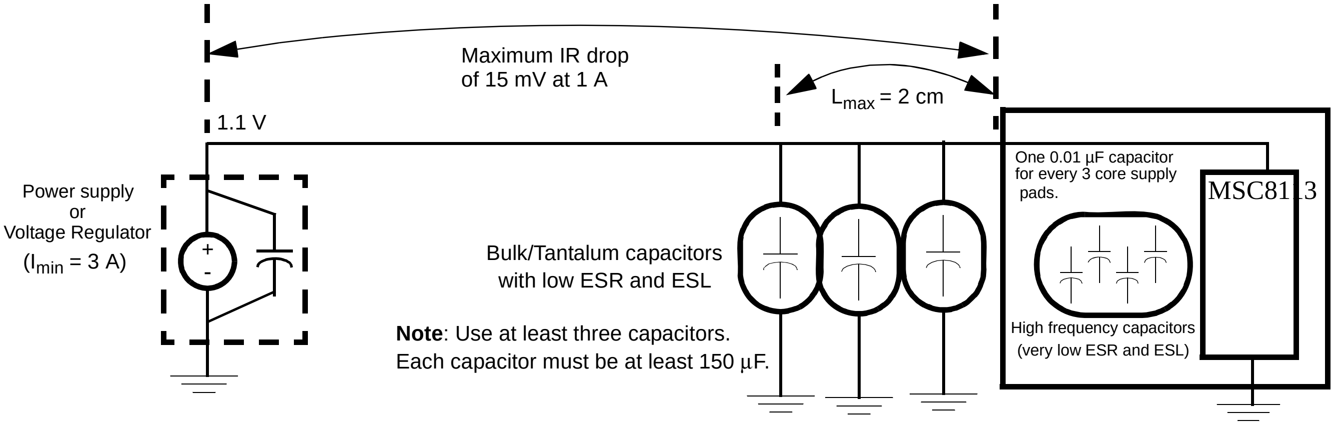
After power-up, $V_{DDH}$ must not exceed $V_{DD}/V_{CCSYN}$ by more than 2.6 V.

## 3.2 Power Supply Design Considerations

When implementing a new design, use the guidelines described in the *MSC8113 Design Checklist* (AN3374 for optimal system performance. *MSC8122 and MSC8126 Power Circuit Design Recommendations and Examples* (AN2937) provides detailed design information.

**Figure 33** shows the recommended power decoupling circuit for the core power supply. The voltage regulator and the decoupling capacitors should supply the required device current without any drop in voltage on the device pins. The voltage on the package pins should not drop below the minimum specified voltage level even for a very short spikes. This can be achieved by using the following guidelines:

- For the core supply, use a voltage regulator rated at 1.1 V with nominal rating of at least 3 A. This rating does not reflect actual average current draw, but is recommended because it resists changes imposed by transient spikes and has better voltage recovery time than supplies with lower current ratings.
- Decouple the supply using low-ESR capacitors mounted as close as possible to the socket. **Figure 33** shows three capacitors in parallel to reduce the resistance. Three capacitors is a recommended minimum number. If possible, mount at least one of the capacitors directly below the MSC8113 device.



**Note**: Use at least three capacitors.
Each capacitor must be at least 150 µF.

Figure 33. Core Power Supply Decoupling

Each $V_{CC}$ and $V_{DD}$ pin on the MSC8113 device should have a low-impedance path to the board power supply. Similarly, each GND pin should have a low-impedance path to the ground plane. The power supply pins drive distinct groups of logic on the chip. The $V_{CC}$ power supply should have at least four 0.1 µF by-pass capacitors to ground located as closely as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip $V_{CC}$, $V_{DD}$, and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as $V_{CC}$ and GND planes.

All output pins on the MSC8113 have fast rise and fall times. PCB trace interconnection length should be minimized to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PCB trace lengths of six inches are recommended. For the DSI control signals in synchronous mode, ensure that the layout supports the DSI AC timing requirements and minimizes any signal crosstalk. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{CC}$, $V_{DD}$, and GND circuits. Pull up all unused inputs or signals that will be inputs during reset.

Special care should be taken to minimize the noise levels on the PLL supply pins. There is one pair of PLL supply pins: $V_{CCSYN}$-$GND_{SYN}$. To ensure internal clock stability, filter the power to the $V_{CCSYN}$ input with a circuit similar to the one in **Figure 34**. For optimal noise filtering, place the circuit as close as possible to $V_{CCSYN}$. The 0.01-µF capacitor should be closest to $V_{CCSYN}$, followed by the 10-µF capacitor, the 10-nH inductor, and finally the 10-Ω resistor to $V_{DD}$. These traces should be kept short and direct. Provide an extremely low impedance path to the ground plane for $GND_{SYN}$. Bypass $GND_{SYN}$ to $V_{CCSYN}$ by a 0.01-µF capacitor located as close as possible to the chip package. For best results, place this capacitor on the backside of the PCB aligned with the depopulated void on the MSC8113 located in the square defined by positions, L11, L12, L13, M11, M12, M13, N11, N12, and N13.

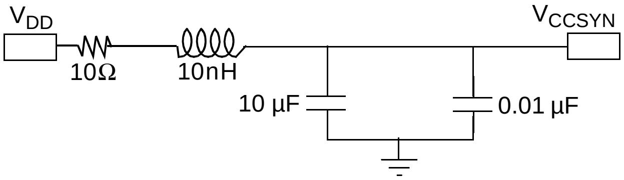


**Figure 34.** $V_{CCSYN}$ **Bypass**

## 3.3 Connectivity Guidelines

Unused output pins can be disconnected, and unused input pins should be connected to the non-active value, via resistors to $V_{DDH}$ or GND, except for the following:

- If the DSI is unused (DDR[DSIDIS] is set), $\overline{\text{HCS}}$ and $\overline{\text{HBCS}}$ must pulled up and all the rest of the DSI signals can be disconnected.
- When the DSI uses synchronous mode, $\overline{\text{HTA}}$ must be pulled up. In asynchronous mode, $\overline{\text{HTA}}$ should be pulled either up or down, depending on design requirements.
- $\overline{\text{HDST}}$ can be disconnected if the DSI is in big-endian mode, or if the DSI is in little-endian mode and the DCR[DSRFA] bit is set.
- When the DSI is in 64-bit data bus mode and DCR[BEM] is cleared, pull up $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ and $\overline{\text{HWBS[4–7]}}$/$\overline{\text{HDBS[4–7]}}$/$\overline{\text{HWBE[4–7]}}$/$\overline{\text{HDBE[4–7]}}$/$\overline{\text{PWE[4–7]}}$/$\overline{\text{PSDDQM[4–7]}}$/$\overline{\text{PBS[4–7]}}$.
- When the DSI is in 32-bit data bus mode and DCR[BEM] is cleared, $\overline{\text{HWBS[1–3]}}$/$\overline{\text{HDBS[1–3]}}$/$\overline{\text{HWBE[1–3]}}$/$\overline{\text{HDBE[1–3]}}$ must be pulled up.
- When the DSI is in asynchronous mode, $\overline{\text{HBRST}}$ and HCLKIN should either be disconnected or pulled up.
- The following signals must be pulled up: $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, $\overline{\text{PSDVAL}}$, and $\overline{\text{AACK}}$.
- In single-master mode (BCR[EBM] = 0) with internal arbitration (PPC_ACR[EARB] = 0):
  - — $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ can be left unconnected.
  - — $\overline{\text{EXT\_BG[2–3]}}$, $\overline{\text{EXT\_DBG[2–3]}}$, and $\overline{\text{GBL}}$ can be left unconnected if they are multiplexed to the system bus functionality. For any other functionality, connect the signal lines based on the multiplexed functionality.
  - — $\overline{\text{BR}}$ must be pulled up.
  - — $\overline{\text{EXT\_BR[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.

- If there is an external bus master (BCR[EBM] = 1):
  - $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{DBG}}$, and $\overline{\text{TS}}$ must be pulled up.
  - $\overline{\text{EXT\_BR[2–3]}}$, $\overline{\text{EXT\_BG[2–3]}}$, and $\overline{\text{EXT\_DBG[2–3]}}$ must be pulled up if multiplexed to the system bus functionality.
- In single-master mode, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ can be selected as $\overline{\text{IRQ}}$ inputs and be connected to the non-active value. In other modes, they must be pulled up.

**Note:** The MSC8113 does not support DLL-enabled mode. For the following two clock schemes, ensure that the DLL is disabled (that is, the DLLDIS bit in the Hard Reset Configuration Word is set).

- If no system synchronization is required (for example, the design does not use SDRAM), you can use any of the available clock modes.
- In the CLKIN synchronization mode, use the following connections:
  - Connect the oscillator output through a buffer to CLKIN.
  - Connect the CLKIN buffer output to the slave device (for example, SDRAM) making sure that the delay path between the clock buffer to the MSC8113 and the SDRAM is equal (that is, has a skew less than 100 ps).
  - Valid clock modes in this scheme are: 0, 7, 15, 19, 21, 23, 28, 29, 30, and 31.

**Note:** See the Clock chapter in the *MSC8113 Reference Manual* for details.

- If the 60x-compatible system bus is not used and SIUMCR[PBSE] is set, $\overline{\text{PPBS}}$ can be disconnected. Otherwise, it should be pulled up.
- The following signals: SWTE, DSISYNC, DSI64, MODCK[1–2], CNFGS, CHIPID[0–3], RSTCONF and BM[0–2] are used to configure the MSC8113 and are sampled on the deassertion of the $\overline{\text{PORESET}}$ signal. Therefore, they should be tied to GND or $V_{DDH}$ or through a pull-down or a pull-up resistor until the deassertion of the $\overline{\text{PORESET}}$ signal.
- When they are used, $\overline{\text{INT\_OUT}}$ (if SIUMCR[INTODC] is cleared), $\overline{\text{NMI\_OUT}}$, and $\overline{\text{IRQxx}}$ (if not full drive) signals must be pulled up.
- When the Ethernet controller is enabled and the SMII mode is selected, GPIO10 and GPIO14 must not be connected externally to any signal line.

**Note:** For details on configuration, see the *MSC8113 User's Guide* and *MSC8113 Reference Manual*. For additional information, refer to the *MSC8113 Design Checklist* (ANxxxx).

## 3.4 External SDRAM Selection

The external bus speed implemented in a system determines the speed of the SDRAM used on that bus. However, because of differences in timing characteristics among various SDRAM manufacturers, you may have use a faster speed rated SDRAM to assure efficient data transfer across the bus. For example, for 133 MHz operation, you may have to use 133 or 166 MHz SDRAM. Always perform a detailed timing analysis using the MSC8113 bus timing values and the manufacturer specifications for the SDRAM to ensure correct operation within your system design. The output delay listed in SDRAM specifications is usually given for a load of 30 pF. Scale the number to your specific board load using the typical scaling number provided by the SDRAM manufacturer.

## 3.5 Thermal Considerations

An estimation of the chip-junction temperature, $T_J$, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 1}$$

where

$T_A$ = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC8113 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm$^2$ with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If $T_J$ appears to be too high, either lower the ambient temperature or the power dissipation of the chip. You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case that is painted black. The MSC8113 device case surface is too shiny (low emissivity) to yield an accurate infrared temperature measurement. Use the following equation to determine $T_J$:

$$T_J = T_T + (\theta_{JA} \times P_D) \qquad \text{Eqn. 2}$$

where

$T_T$ = thermocouple (or infrared) temperature on top of the package (°C)
$\theta_{JA}$ = thermal characterization parameter (°C/W)
$P_D$ = power dissipation in the package (W)

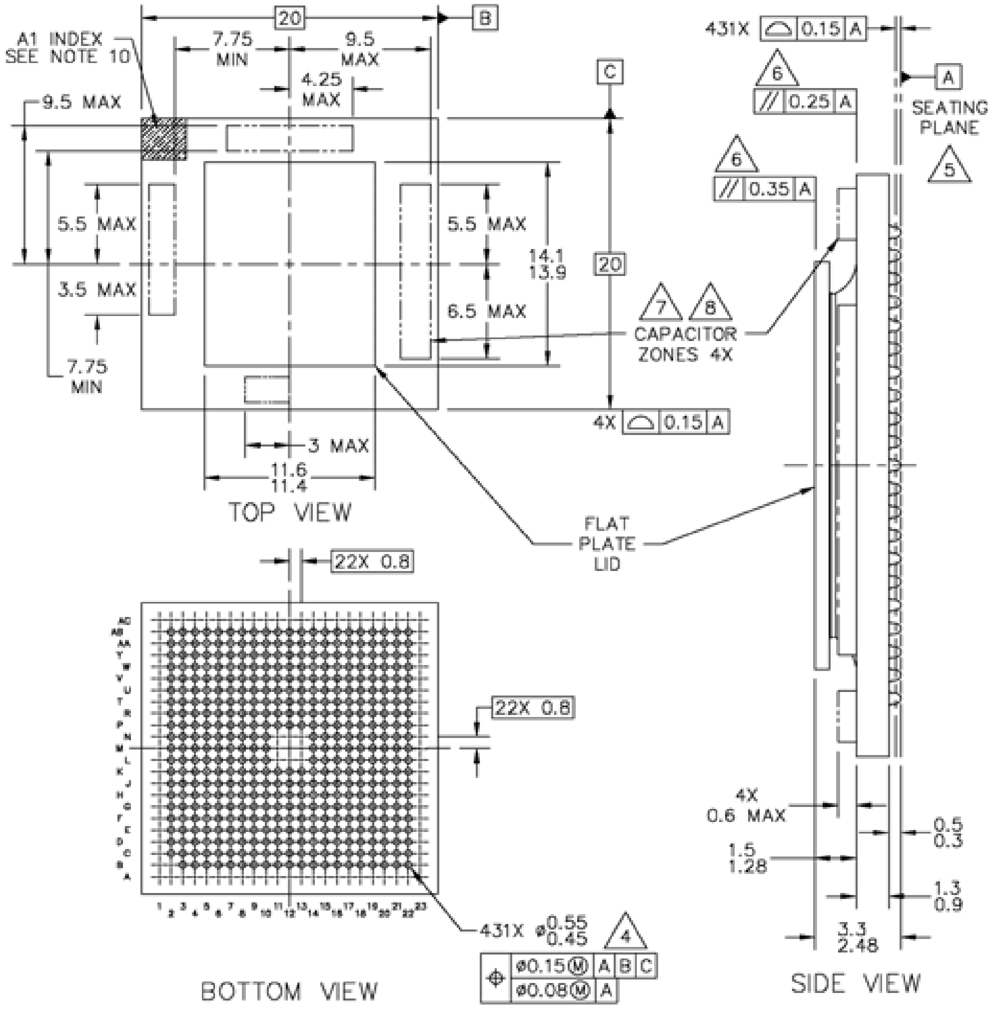
**Note:** See *MSC8102, MSC8122, and MSC8126 Thermal Management Design Guidelines* (AN2601/D).

# 4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

| Part | Package Type | Core Voltage | Operating Temperature | Core Frequency (MHz) | Order Number | |
|---|---|---|---|---|---|---|
| | | | | | Lead-Free | Lead-Bearing |
| MSC8113 | Flip Chip Plastic Ball Grid Array (FC-PBGA) | 1.1 V | –40° to 105°C | 300 | MSC8113TVT3600V | MSC8113TMP3600V |
| | | | | 400 | MSC8113TVT4800V | MSC8113TMP4800V |

# 5 Package Information



**Notes:**
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Features are symmetrical about the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to Datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement shall exclude any effect of mark on top surface of package.
7. Capacitors may not be present on all devices.
8. Caution must be taken not to short capacitors or exposed metal capacitor pads on package top.
9. FC CBGA (Ceramic) package code: 5238.
   FC PBGA (Plastic) package code: 5263.
10. Pin 1 indicator can be in the form of number 1 marking or an “L” shape marking.

**Figure 35. MSC8113 Mechanical Information, 431-pin FC-PBGA Package**

# 6 Product Documentation

- *MSC8113 Technical Data Sheet* (MSC8113). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8113 device.
- *MSC8113 Reference Manual* (MSC8113RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8113 device.
- *SC140 DSP Core Reference Manual*. Covers the SC140 core architecture, control registers, clock registers, program control, and instruction set.

# 7 Revision History

Table 31 provides a revision history for this data sheet.

**Table 31. Document Revision History**

| Revision | Date | Description |
|---|---|---|
| 0 | May 2008 | • Initial public release. |
| 1 | Dec. 2008 | • Added **Figure 8** and associated text that was omitted from the previous revision on p. 17.<br>• Clarified the wording of note 2 in **Table 15** on p. 23. |

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