

## ATM LIGHT SAR CONTROLLER

### DESCRIPTION

The  $\mu$ PD98409 (NEASCOT-S40C™) is a high-performance SAR chip for segmentation and reassembly of ATM cells. Provided with a PCI (Peripheral Component Interconnect) bus interface control memory and supporting a MPEG packet transfer engine function to mitigate the workload of the CPU in transferring compressed image data, this chip has ideal specifications for use in a set top box (STB) to interface with an ATM network. The  $\mu$ PD98409 conforms to ATM Forum recommendations and has AAL5-SAR sublayer and ATM layer functions.

### FEATURES

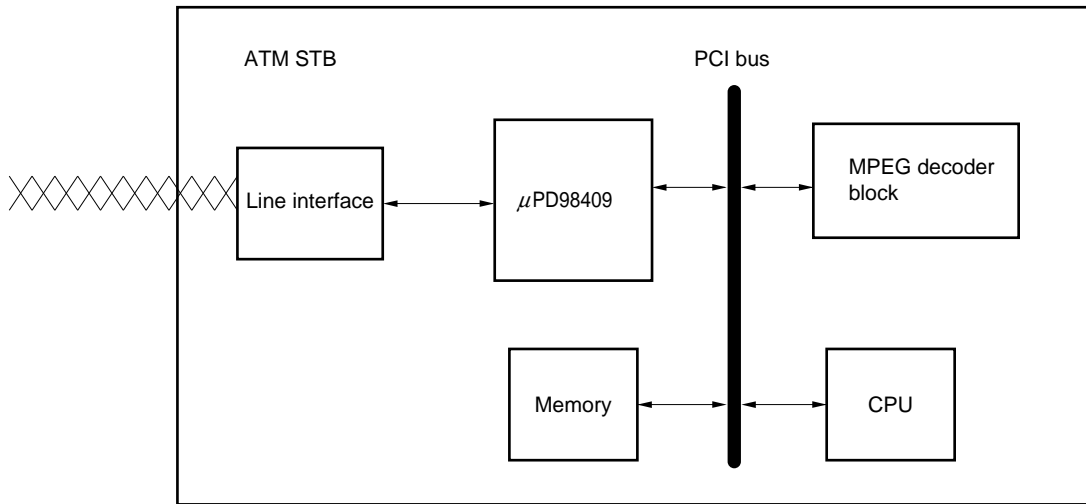
- Conforms to ATM Forum
- PCI bus interface (5/3.3 V, 32/64 bits, 33 MHz)  
Conforms to PCI Local Bus Specification Revision 2.1
- AAL-5 SAR sublayer and ATM layer functions
- Hardware support of AAL-5 processing (non-AAL-5 processing can be supported in software)
- Supports up to 64 virtual channels (VC) (64-VC control memory)
- Two traffic shapers for transmission scheduling
- MPEG packet transfer engine mitigating the workload of compressed image data transfer by CPU
- Receive FIFO of 12 cells
- PHY device I/F: UTOPIA Level-1 interface (octet/cell level handshake)
- JTAG boundary scan test functions
- 0.35- $\mu$ m CMOS process, +5/+3.3-V power supply
  - Bus interface +5 V : +5/+3.3-V power supply
  - Bus interface +3.3 V : +3.3-V single power supply

### ORDERING INFORMATION

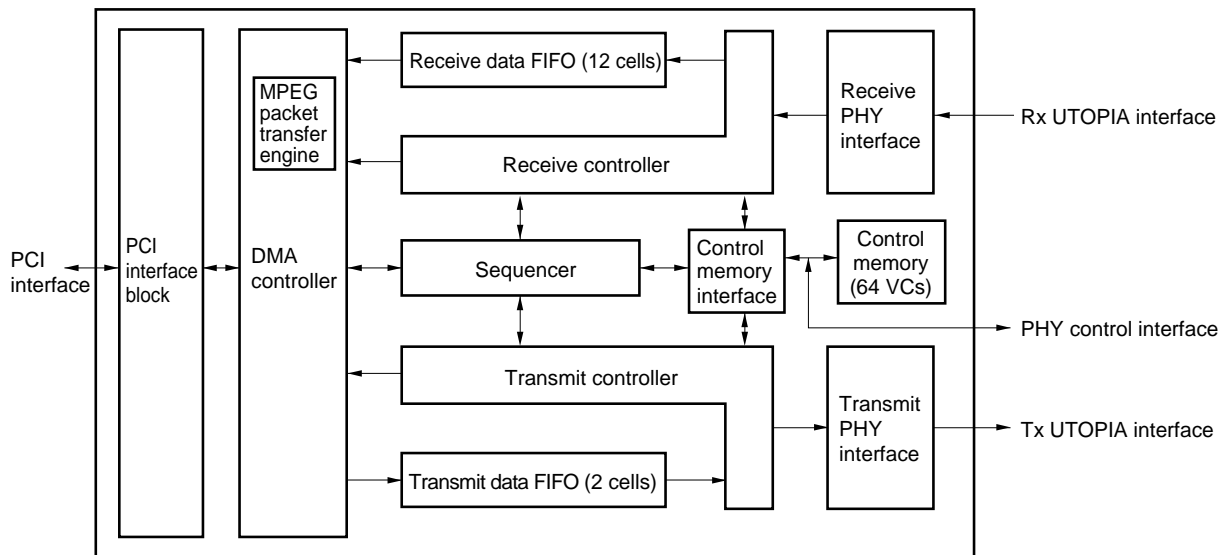
Part Number	Package
$\mu$ PD98409GN-LMU	240-pin plastic QFP (0.5-mm fine pitch) (32 × 32 mm)

The information in this document is subject to change without notice.

EXAMPLE OF SYSTEM CONFIGURATION

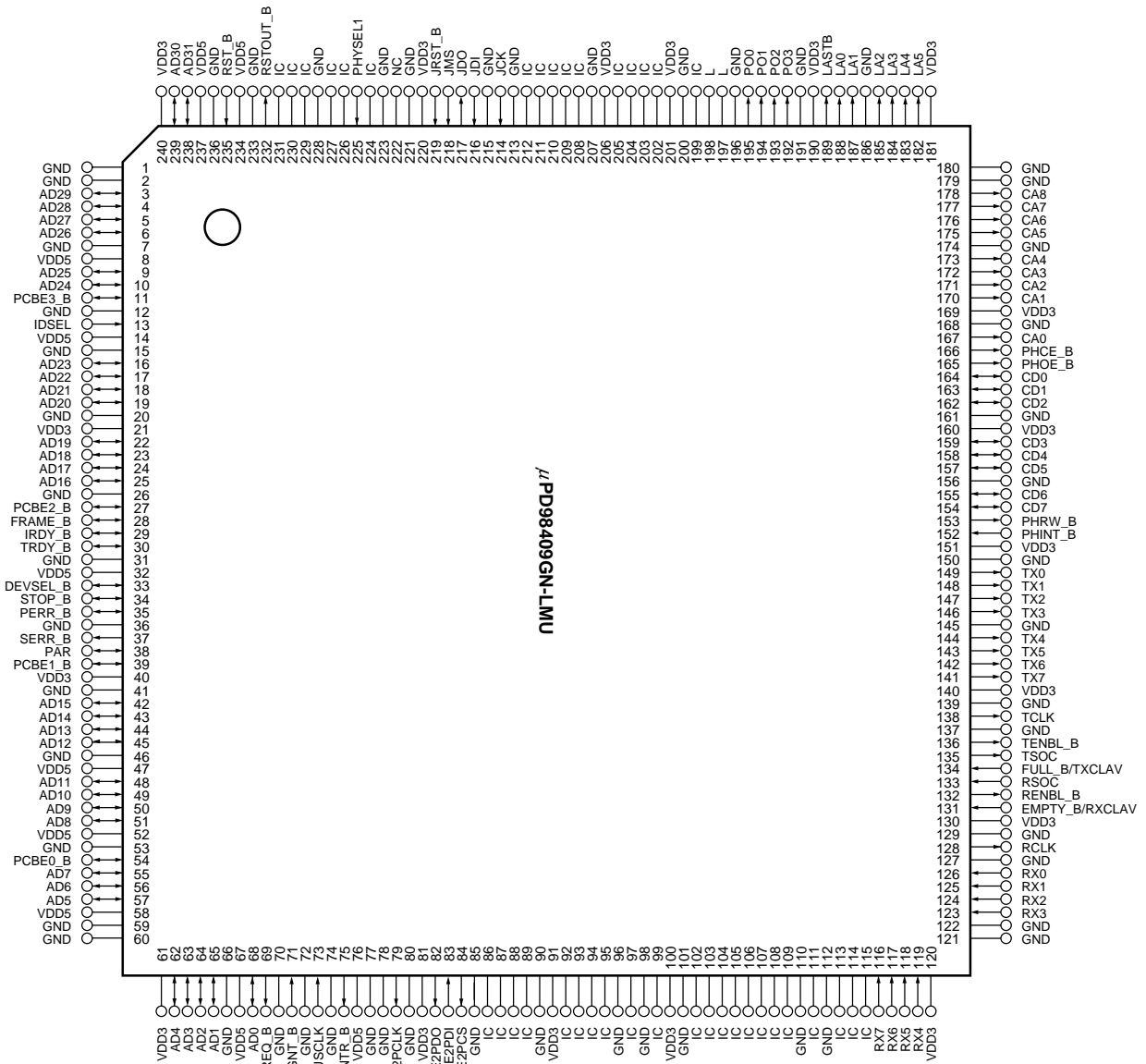


BLOCK DIAGRAM



**PIN CONFIGURATION (Top View)**

- 240-pin plastic QFP (0.5-mm fine pitch) (32 × 32 mm)



NC : No connection. Leave this pin open.

IC : Input pin with pull-down resistor for internal test. It is recommended to fix this pin to the low level.

L : Fix this pin to the low level.

## PIN NAMES

AD31_AD0	: Address/Data	PHINT_B	: PHY Interrupt
BUSCLK	: Bus Clock	PHOE_B	: PHY Output Enable
CA8-CA0	: PHY Device Address	PHRW_B	: PHY Read/Write
CD7-CD0	: PHY Device Data	PHYSEL1	: PHY Select
DEVSEL_B	: Device Select	PO3-PO0	: Generic Output Port
E2PCLK	: Clock for EEPROM™	RCLK	: Receive Clock
E2PCS	: EEPROM Chip Select	RENBL_B	: Receive Enable
E2PDI	: Serial Data Input from EEPROM	REQ_B	: Request
E2PDO	: Serial Data Output to EEPROM	RSOC	: Receive Start of Cell
EMPTY_B/RxCLAV	: PHY Empty / Rx Cell Available	RST_B	: Reset
FRAME_B	: Cycle Frame	RSTOUT_B	: Reset Output
FULL_B/TxCLAV	: PHY Buffer Full / Tx Cell Available	Rx7-Rx0	: Receive Data Bus
GND	: Ground	SERR_B	: System Error
GNT_B	: Grant	STOP_B	: Stop
IDSEL	: ID Select	TCLK	: Transmit Clock
INTR_B	: Interrupt	TENBL_B	: Transmit Enable
IRDY_B	: Initiator Ready	TRDY_B	: Target Ready
JCK	: JTAG Test Pin	TSOC	: Transmit Start of Cell
JDI	: JTAG Test Pin	Tx7-Tx0	: Transmit Data Bus
JDO	: JTAG Test Pin	V <sub>DD3</sub>	: +3.3 V Power Supply
JMS	: JTAG Test Pin	V <sub>DD5</sub>	: +5 V Power Supply
JRST_B	: JTAG Test Pin		
LA5-LA0	: Internal Test Pin		
LASTB	: Internal Test Pin		
PAR	: Parity		
PCBE_B3-PCBE_B0	: Bus Command and Byte Enables		
PERR_B	: Parity Error		
PHCE_B	: PHY Chip Enable		

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**1. PIN FUNCTION**

The pin function of the μPD98409 is described below. A detailed explanation of how to use each pin, and the points to be noted in using the pins are given in μPD98409 User's Manual (Document Number: S12776E). Be sure to refer to this user's manual.

The following describes the I/O levels in the tables.

- LV-TTL input : Can be connected to 5 V CMOS output
- TTL output : Can be connected to 5 V TTL input, V<sub>OH</sub> = 3.3 V, I<sub>OL</sub> = 6 mA
- CMOS output : 3.3 V CMOS output, V<sub>OH</sub> = 3.3 V, I<sub>OL</sub> = 12 mA
- PCI input : 5/3.3 V PCI input
- PCI output : 5/3.3 V PCI output

**1.1 PHY Device Interface Pin**

PHY device interfaces include a UTOPIA interface through which the μPD98409 transfers ATM cells with a PHY device, and a PHY control interface by which the μPD98409 controls the PHY device.

**1.1.1 UTOPIA interface**

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Pin Name	Pin No.	I/O	I/O Level	Function
Rx7-Rx0	116 - 119, 123 - 126	I	LV-TTL	Receive Data Bus. Rx7 through Rx0 constitute an 8-bit input bus which inputs data received from a network in byte format from a PHY device. The μPD98409 loads data in at the rising edge of RCLK.
RSOC	133	I	LV-TTL	Receive Start Cell. The RSOC signal is input in synchronization with the first byte of the cell data from a PHY device. This signal remains high while the first byte of the header is input to Rx7 through Rx0.
RENBL_B	132	O	TTL	Receive Enable. The RENBL_B signal indicates to a PHY device that the μPD98409 is ready to receive data in the next clock cycle.
EMPTY_B/ RxCLAV	131	I	LV-TTL	PHY Output Buffer Empty/Rx Cell Available. This signal notifies the μPD98409 that there is no cell data to be transferred in the receive FIFO and that no receive data can be supplied to the PHY device. When the UTOPIA interface is in the octet-level handshake mode, this signal serves as EMPTY_B, indicating that the data on Rx7 through Rx0 are invalid in the current clock cycle. In the cell-level handshake mode, it serves as RxCLAV, indicating that there is no cell to be supplied next after the transfer of the current cell is completed.
RCLK	128	O	TTL	Receive Clock. This is a synchronization clock used to transfer cell data with the PHY device at the receive side. The system clock input to the BUSCLK pin is output from this pin as is.
Tx7-Tx0	141 - 144, 146 - 149	O	TTL	Transmit Data Bus. Tx7 through Tx0 constitute an 8-bit output bus which outputs transmit data in byte format to a PHY device. The μPD98409 outputs data at the rising edge of TCLK.
TSOC	135	O	TTL	Transmit Start of Cell. The TSOC signal is output in synchronization with the first byte of transmit cell data.

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Pin Name	Pin No.	I/O	I/O Level	Function
TENBL_B	136	O	TTL	Transmit Enable. The TENBL_B signal indicates to a PHY device that data has been output to Tx7 through Tx0 in the current clock cycle.
FULL_B/ TxCLAV	134	I	LV-TTL	PHY Buffer Full/Tx Cell Available. This signal notifies the μPD98409 that the input buffer of the PHY device is full and that the device can receive no more data. When the UTOPIA interface is in the octet-level handshake mode, the PHY device inputs an inactive level to receive cell data. In the cell-level handshake mode, the PHY device inputs a signal that indicates that the PHY device can receive all the next one cell of data after the current cell has been completely transferred.
TCLK	138	O	TTL	Transmit Clock. This is a synchronization clock used to transfer cell data with the PHY device at the transmission side. The system clock input to the BUSCLK pin is output from this pin as is.

1.1.2 PHY device control interface

Pin Name	Pin No.	I/O	I/O Level	Function
PHRW_B	153	O	TTL	PHY Read/Write. The μPD98409 indicates the direction in which the PHY device is controlled, by using PHRW_B. 1: Read 0: Write
PHOE_B	165	O	TTL	PHY Output Enable. The μPD98409 enables output from the PHY device by making PHOE_B low
PHCE_B	166	O	TTL	PHY Chip Enable. The μPD98409 makes PHCE_B low to access a PHY device.
PHINT_B	152	I	LV-TTL	PHY Interrupt. This is an interrupt input signal from a PHY device. The PHY device indicates to the μPD98409 that it has an interrupt source, by inputting a low level to PHINT_B.
RSTOUT_B	232	O	TTL	Reset Output. This is a signal to reset a PHY device. The μPD98409 makes this pin low for the duration of 11 to 22 clock cycles when a low level is input to the RST_B pin or a software reset is executed.
CD7-CD0	154, 155, 157 - 159, 162 - 164	I/O 3-state	LV-TTL in TTL out	PHY device data. CD7 through CD0 constitute an 8-bit data bus. These pins are three-state I/O pins. They are used to transfer data with a PHY device.
CA8-CA0	178 - 175, 173 - 170, 167	O	TTL	PHY device address. CA8 through CA0 constitute a 9-bit address bus that outputs an address to a PHY device during read/write operation.

1.2 Bus Interface Pins

The μPD98409 employs a 32-bit PCI bus interface as a bus interface with the host. This interface conforms to “PCI Local Bus Specification Revision 2.1”.

(1/2)

Pin Name	Pin No.	I/O	I/O Level	Function
AD31-AD0	238, 239, 3 - 6, 9, 10, 16 - 19, 22 - 25, 42 - 45, 48 - 51, 55 - 57, 62 - 65, 68	I/O 3-state	PCI	Address/data. AD31 through AD0 are 32 bits of multiplexed address and data bus signals. When the μPD98409 operates as the bus master, it drives an address at the first one clock, and transfers data at the second clock and onward.
PCBE3_B PCBE2_B PCBE1_B PCBE0_B	11, 27, 39, 54	I/O 3-state	PCI	Bus command and byte enable. These signals define “bus commands” (generated bus transaction) in an address phase. In a data phase, they indicate which byte lane holds valid data. The PCBE3_B pin corresponds to byte 3 (bits 31 through 24), and PCBE0_B pin corresponds to byte 0 (bits 7 through 0).
PAR	38	I/O 3-state	PCI	Parity. This signal inputs/outputs an even parity on the AD31 through AD0 and PCBE3_B through PCBE0_B pins including the PAR signal. When the μPD98409 operates as the master, the PAR signal is output in the address and write data phases. When the μPD98409 operates as a target, the PAR signal is output in the read data phase.
FRAME_B	28	I/O Sustained 3-state	PCI	Frame. This signal indicates the start and period of bus transaction. When this signal becomes active, it indicates the start of bus transaction. While it is active, data is transferred. When the next data transfer phase is for the last data of the transaction, this signal becomes inactive.
TRDY_B	30	I/O Sustained 3-state	PCI	Target ready. This signal goes low when the target device is ready to complete the transaction of the current data phase. This signal is used in pairs with IRDY_B. When both IRDY_B and TRDY_B are low, read/write data transfer is executed.
IRDY_B	29	I/O Sustained 3-state	PCI	Initiator ready. This signal goes low when the initiator is ready to complete the transaction of the current data phase. This signal is used in pairs with TRDY_B. When both IRDY_B and TRDY_B are low, read/write data transfer is executed. If both FRAME_B and IRDY_B are inactive, the bus cycle is not executed, and wait cycles are inserted until both IRDY_B and TRDY_B become active.



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Pin Name	Pin No.	I/O	I/O Level	Function
STOP_B	34	I/O Sustained 3-state	PCI	Stop. This signal goes low when the target device requests the master device to stop the current transaction.
DEVSEL_B	33	I/O Sustained 3-state	PCI	Device select. This signal goes low when the μPD98409 operates as a target and recognizes an address after the FRAME_B signal has become active. When the μPD98409 operates as the master, it samples this signal to check to see whether a target device has been selected.
IDSEL	13	I	PCI	Initialization device select. This signal inputs a high level when the configuration register of the μPD98409 is read/written.
REQ_B	69	O <sup>Note</sup>	PCI	Request. The μPD98409 requests the arbiter for the bus mastership by making this signal low.
GNT_B	71	I	PCI	Grant. This signal goes low when the arbiter grants the μPD98409 the bus mastership.
PERR_B	35	I/O Sustained 3-state	PCI	Parity error. This signal indicates that the μPD98409 has detected a parity error. It is enabled when the "Parity Error Response" bit of the configuration register is set to 1.
SERR_B	37	O	N-ch open-drain	System error. This signal indicates that the μPD98409 has detected an address parity error. It is enabled when both the "Parity Error Response" and "System Error Enable" bits of the configuration register are set to 1.
INTR_B	75	O	N-ch open-drain	Interrupt output. Pull up this pin because it outputs an open-drain signal. INTR_B informs the CPU that the interrupt bit (not masked) of the GSR register is set.
BUSCLK	73	I	PCI	PCI bus clock. Bus clock input pin. It inputs a clock of up to 33 MHz.
RST_B	235	I	PCI	Reset. The RST_B signal initializes the μPD98409 (on starting). When a low level is input to RST_B, the internal state machine and registers of the μPD98409 are reset, and all the 3-state signals go into a high-impedance state. When this signal is input while the μPD98409 is operating, the operating status at that time is lost. Keep the input to RST_B low at least for the duration of 1 clock cycle. Do not access the μPD98409 at least for 20 clocks after it has been reset.

**Note** Although the "PCI Local Bus Specification Revision 2.1" specifies that the REQ\_B pin go into a high-impedance state while a low level is input to the RST\_B pin, the REQ\_B pin of the μPD98409 outputs a high level.

### 1.3 Serial EEPROM Interface Pins

The μPD98409 has an interface for serial EEPROM supporting the MICROWIRE™ interface. Some of the contents of the PCI configuration register can be loaded from the EEPROM connected.

As the EEPROM, “NM93C46L” of National Semiconductor Corp. is recommended.

Pin Name	Pin No.	I/O	I/O Level	Function
E2PCS	84	O	TTL	EEPROM chip select. A chip select signal for EEPROM. Leave this pin open when it is not used.
E2PDI	83	I	TTL Internally pulled up	EEPROM data input. This pin is connected to the data output pin of the EEPROM. Pull up or open this pin when it is not used.
E2PDO	82	O	TTL	EEPROM data output. This pin is connected to the data input pin of the EEPROM. Pull up or open this pin when it is not used.
E2PCLK	79	O	TTL	EEPROM clock. This pin supplies a clock necessary for data transfer with the EEPROM. It outputs the clock input to the BUSCLK pin divided by 36. Leave this pin open when it is not used.

### 1.4 JTAG Boundary Scan Pins

(These functions can be supported by request.)

Pin Name	Pin No.	I/O	I/O Level	Function
JDI	216	I	LV-TTL	JTAG Test Data Input. The JDI pin is used to input data to the JTAG boundary scan circuit register. Normally, fix this pin to high or low level.
JDO	217	O 3-state	TTL	JTAG Test Data Output. The JDO pin is used to output data from the JTAG boundary scan circuit register. It changes output at the falling edge of the clock input to the JCK pin. Normally, leave this pin open.
JCK	214	I	LV-TTL	JTAG Test Clock. This pin is used to supply a clock to the JTAG boundary scan circuit register. Normally, fix this pin to a high or low level.
JMS	218	I	LV-TTL	JTAG Test Mode Select. Normally, fix this pin to a high or low level.
JRST_B	219	I	LV-TTL	JTAG Test Reset. This pin initializes the JTAG boundary scan circuit register. Normally, fix this pin to a low level.

1.5 Other Pins

Pin Name	Pin No.	I/O	I/O Level	Function
PHYSEL1	225	I	LV-TTL	Internal test pin. Input a low level to this pin.
PO3-PO0	192 - 195	O	CMOS	General-purpose output port. General-purpose output port pins. These pins output the value written to the GPOR register.
LA5-LA0	182 - 185, 187, 188	O	TTL	Internal test pins. Leave these pins open during normal operation.
LASTB	189	O	TTL	Internal test pin. Leave this pin open during normal operation.

1.6 Power and Ground Pins

Pin Name	Pin No.	I/O	Function
V <sub>DD3</sub>	21, 40, 61, 81, 91, 100, 120, 130, 140, 151, 160, 169, 181, 190, 201, 206, 220, 240	—	+3.3-V power supply. These pins supply +3.3 V to the chip.
V <sub>DD5</sub>	8, 14, 32, 47, 52, 58, 67, 76, 234, 237	—	+5 V power supply. These pins supply +5 V to the chip when a +5-V bus interface is used. Supply +3.3 V to these pins when a +3.3-V bus interface is used.
GND	1, 2, 7, 12, 15, 20, 26, 31, 36, 41, 46, 53, 59, 60, 66, 70, 72, 74, 77, 78, 80, 85, 90, 96, 98, 101, 110, 112, 121, 122, 127, 129, 137, 139, 145, 150, 156, 161, 168, 174, 179, 180, 186, 191, 196, 200, 207, 213, 215, 221, 223, 228, 233, 236	—	Ground. Connect to ground.

## 2. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD3}$		-0.5 to +4.6	V
	$V_{DD5}^{Note}$	$V_{DD3} \leq V_{DD5}$	-0.5 to +6.6	V
Input voltage	$V_I$	Except pin PCI, $V_I < V_{DD3} + 3.0$ V	-0.5 to +6.6	V
		PCI pin	-5.5 to +11.0	V
Output voltage	$V_O$	Except PCI pin and PO0-PO3, $V_O < V_{DD3} + 3.0$ V	-0.5 to +6.6	V
		PO3-PO0, $V_O < V_{DD3} + 0.5$ V	-0.5 to +4.6	V
		PCI pin	-0.5 to +6.6	V
Output current	$I_O$	Except PCI pin and PO0-PO3	20	mA
		PO3-PO0	40	mA
		PCI pin	20	mA
Operating ambient temperature	$T_A$		0 to +70	°C
Storage temperature	$T_{stg}$		-65 to +150	°C

**Note**  $V_{DD5}$ : Dedicated power supply for clamping diode

**Caution** If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

### Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{DD3}$		3.0	3.3	3.6	V
	$V_{DD5}^{Note}$	+3.3 V PCI	3.0	3.3	3.6	V
	$V_{DD5}^{Note}$	+5 V PCI	4.75	5.00	5.25	V
Operating ambient temperature	$T_A$		0		+70	°C
High-level input voltage	$V_{IH1}$	Input pins except PCI	2.0		5.5	V
	$V_{IH2}$	RST_B pin	2.2		$V_{DD5} + 0.5$	V
	$V_{IH3}$	PCI pins except RST_B	2.0		$V_{DD5} + 0.5$	V
Low-level input voltage	$V_{IL1}$	Input pins except PCI	0		+0.8	V
	$V_{IL2}$	PCI pin	-0.5		+0.8	V

**Note**  $V_{DD5}$ : Dedicated power supply for clamping diode

**DC Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>DD3</sub> = +3.3 V ±0.3 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.0 mA <sup>Note 1</sup>	2.4			V
	V <sub>OH2</sub>	I <sub>OH</sub> = -12.0 mA <sup>Note 2</sup>	2.4			V
Low-level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 3.0 mA <sup>Note 3</sup>			0.55	V
	V <sub>OL2</sub>	I <sub>OL</sub> = 6.0 mA <sup>Note 4</sup>			0.55	V
	V <sub>OL3</sub>	I <sub>OL</sub> = 6.0 mA <sup>Note 5</sup>			0.40	V
	V <sub>OL4</sub>	I <sub>OL</sub> = 12.0 mA <sup>Note 6</sup>			0.40	V
Supply current	I <sub>DD</sub>	f <sub>CLK</sub> = 33 MHz, normal transmission/ reception		250	400	mA
Input leakage current (normal input)	I <sub>I1</sub>	V <sub>I</sub> = V <sub>DD3</sub>		±10 <sup>-4</sup>	±10	μA
★ Input leakage current (E2PDI pin with pull-up resistor)	I <sub>I2</sub>	V <sub>I</sub> = GND	10	80	200	μA

- Notes**
1. V<sub>OH1</sub> applies to all output pins except pins PO3-PO0.
  2. V<sub>OH2</sub> applies to pins PO3-PO0.
  3. V<sub>OL1</sub> applies to PCI output pins AD31-AD0, PCBE3\_B-PCBE0\_B, PAR, REQ\_B and INTR\_B.
  4. V<sub>OL2</sub> applies to PCI output pins FRAME\_B, TRDY\_B, IRDY\_B, DEVSEL\_B, STOP\_B, SERR\_B, and PERR\_B.
  5. V<sub>OL3</sub> applies to pins other than PCI output pins and pins other than pins PO3-PO0.
  6. V<sub>OL4</sub> applies to pins PO3-PO0.

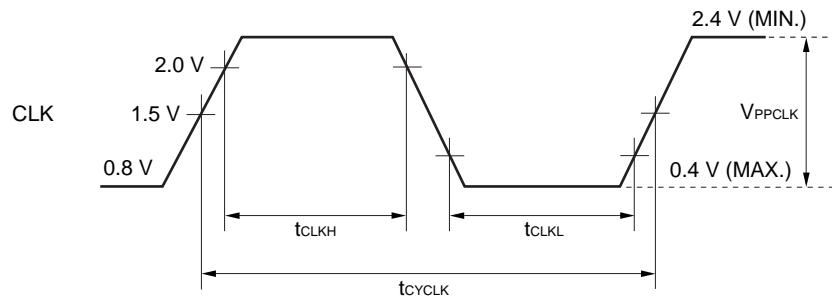
**Capacitance (T<sub>A</sub> = +25°C, V<sub>DD3</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	f = 1 MHz		10	20	pF
Output capacitance	C <sub>OUT</sub>	f = 1 MHz		10	20	pF
I/O capacitance	C <sub>I/O</sub>	f = 1 MHz		10	20	pF

AC Characteristics (T<sub>A</sub> = 0 to +70°C, V<sub>DD3</sub> = +3.3 V ± 0.3 V)

BUSCLK input

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK cycle time	t <sub>CYCLK</sub>		30		125	ns
CLK high-level width	t <sub>CLKH</sub>		11			ns
CLK low-level width	t <sub>CLKL</sub>		11			ns
CLK amplitude	V <sub>PPCLK</sub>		2			V
CLK through rate	slew <sub>CLK</sub>		1		4	V/ns



RST input

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RST low-level width	t <sub>RSTL</sub>		t <sub>CYCLK</sub>			ns
RST through rate	slew <sub>RST</sub>		50			mV/ns

PCI Bus Interface

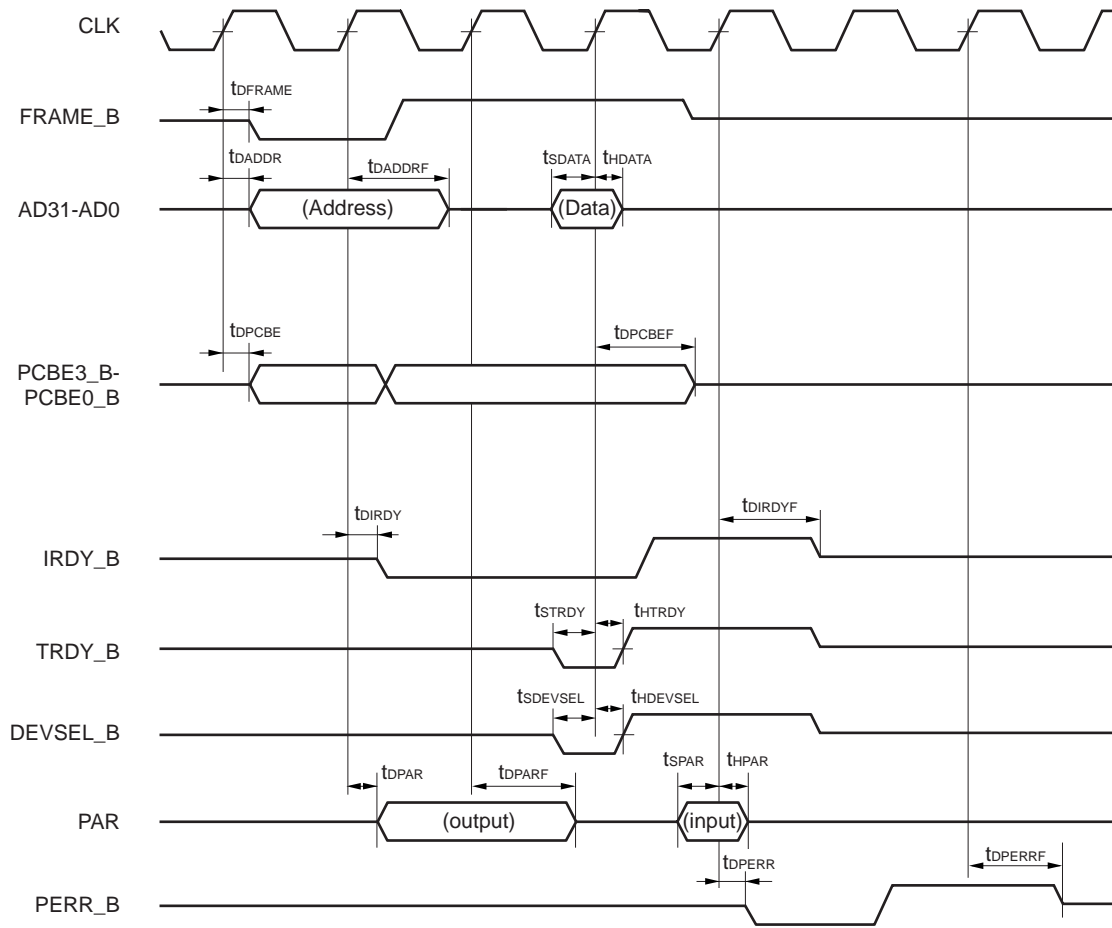
Bus master read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK↑→FRAME_B valid time	tDFRAME		2		11	ns
CLK↑→AD (Address) valid time	tDADDR		2		11	ns
CLK↑→AD (Address) float time	tDADDRF				28	ns
AD (Data) setup time	tSDATA		7			ns
AD (Data) hold time	tHDATA		2 <sup>Note 1</sup>			ns
CLK↑→PCBE_B valid time	tDPCBE		2		11	ns
CLK↑→PCBE_B float time	tDPCBEF				28	ns
CLK↑→IRDY_B valid time	tDIRDY		2		11	ns
CLK↑→IRDY_B float time	tDIRDYF				28	ns
TRDY_B setup time	tSTRDY		9 <sup>Note 2</sup>			ns
TRDY_B hold time	tHTRDY		2 <sup>Note 1</sup>			ns
DEVSEL_B setup time	tSDEVSEL		7			ns
DEVSEL_B hold time	tHDEVSEL		2 <sup>Note 1</sup>			ns
CLK↑→PAR valid time	tDPAR		2		11	ns
CLK↑→PAR float time	tDPARF				28	ns
PAR setup time	tSPAR		7			ns
PAR hold time	tHPAR		2 <sup>Note 1</sup>			ns
CLK↑→PERR_B valid time	tDPERR		2		11	ns
CLK↑→PERR_B float time	tDPERRF				28	ns

**Notes** 1. Relaxed specification from PCI Local Bus Specification Revision 2.1 0 ns → 2 ns

2. Relaxed specification from PCI Local Bus Specification Revision 2.1 7 ns → 9 ns

Bus master read



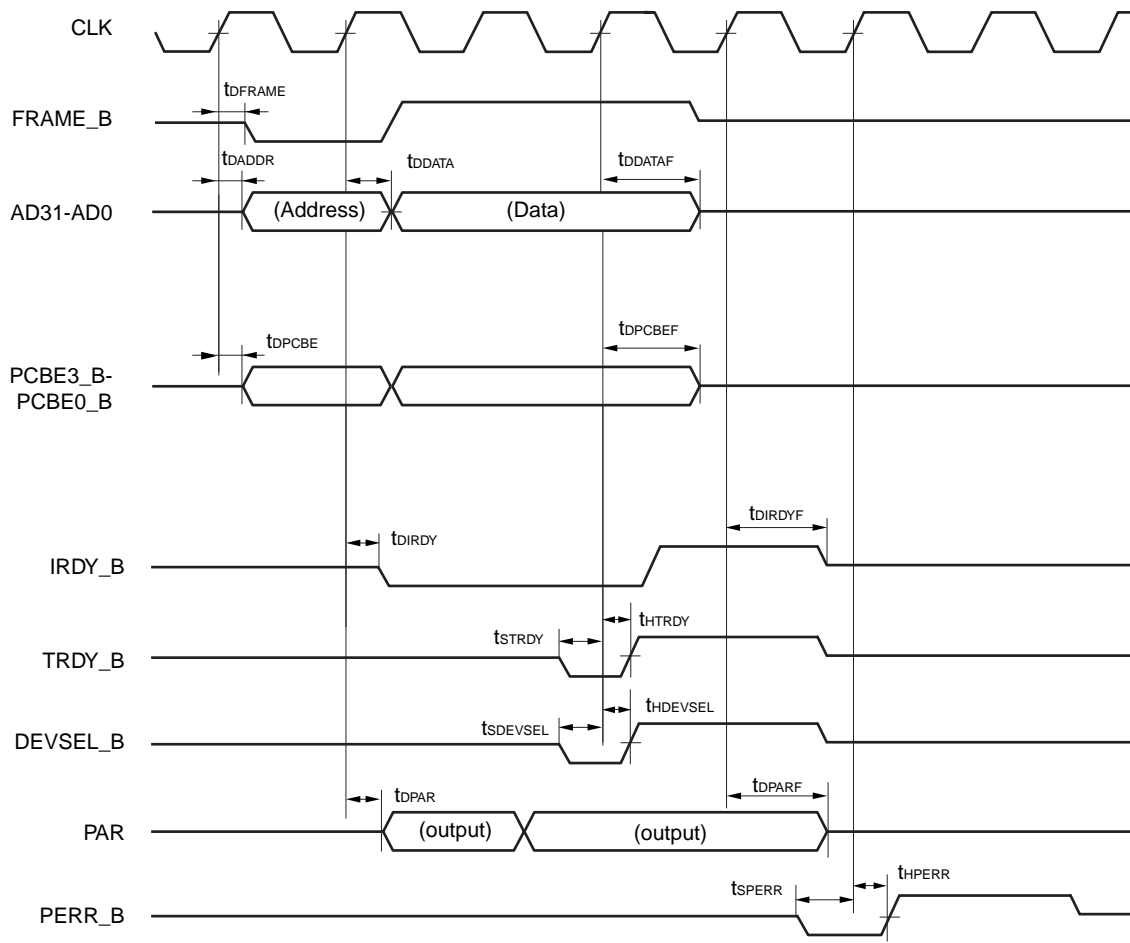


**Bus master write**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK↑ → FRAME_B valid time	tDFRAME		2		11	ns
CLK↑ → AD (Address) valid time	tDADDR		2		11	ns
CLK↑ → data valid time	tDDATA		2		11	ns
CLK↑ → data float time	tDDATAF				28	ns
CLK↑ → PCBE_B valid time	tDPCBE		2		11	ns
CLK↑ → PCBE_B float time	tDPCBEF				28	ns
CLK↑ → IRDY_B valid time	tDIRDY		2		11	ns
CLK↑ → IRDY_B float time	tDIRDYF				28	ns
TRDY_B setup time	tSTRDY		9 <sup>Note 2</sup>			ns
TRDY_B hold time	tHTRDY		2 <sup>Note 1</sup>			ns
DEVSEL_B setup time	tSDEVSEL		7			ns
DEVSEL_B hold time	tHDEVSEL		2 <sup>Note 1</sup>			ns
CLK↑ → PAR valid time	tDPAR		2		11	ns
CLK↑ → PAR float time	tDPARF				28	ns
PERR_B setup time	tSPERR		7			ns
PERR_B hold time	tHPERR		2 <sup>Note 1</sup>			ns

- Notes**
1. Relaxed specification from PCI Local Bus Specification Revision 2.1 0 ns → 2 ns
  2. Relaxed specification from PCI Local Bus Specification Revision 2.1 7 ns → 9 ns

Bus master write

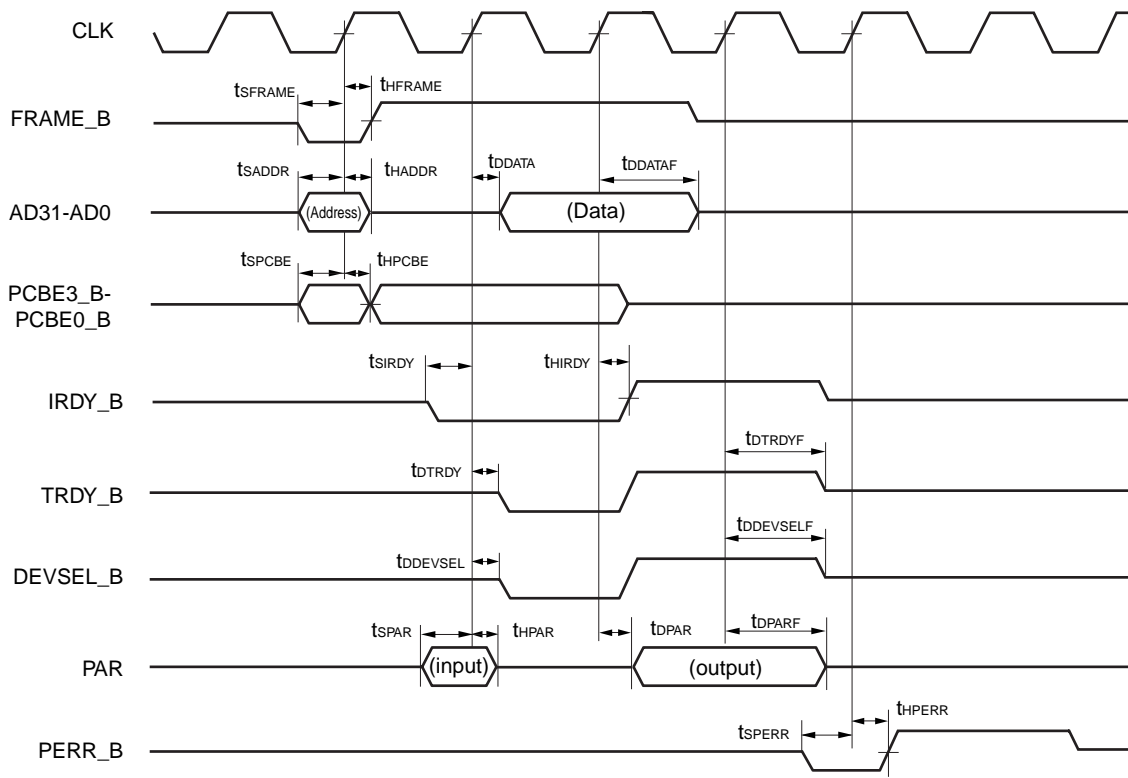


**Target read**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FRAME_B setup time	t <sub>SFRAME</sub>		7			ns
FRAME_B hold time	t <sub>HFRAME</sub>		2 <sup>Note 1</sup>			ns
AD (Address) setup time	t <sub>SADDR</sub>		7			ns
AD (Address) hold time	t <sub>HADDR</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → AD (Data) valid time	t <sub>DDATA</sub>		2		11	ns
CLK↑ → AD (Data) float time	t <sub>DDATAF</sub>				28	ns
PCBE_B setup time	t <sub>SPCBE</sub>		7			ns
PCBE_B hold time	t <sub>HPCBE</sub>		2 <sup>Note 1</sup>			ns
IRDY_B setup time	t <sub>SIRDY</sub>		9 <sup>Note 2</sup>			ns
IRDY_B hold time	t <sub>HIRDY</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → TRDY_B valid time	t <sub>DTRDY</sub>		2		11	ns
CLK↑ → TRDY_B float time	t <sub>DTRDYF</sub>				28	ns
CLK↑ → DEVSEL_B valid time	t <sub>DDEVSEL</sub>		2		11	ns
CLK↑ → DEVSEL_B float time	t <sub>DDEVSELF</sub>				28	ns
PAR setup time	t <sub>SPAR</sub>		7			ns
PAR hold time	t <sub>HPAR</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → PAR valid time	t <sub>DPAR</sub>		2		11	ns
CLK↑ → PAR float time	t <sub>DPARF</sub>				28	ns
PERR_B setup time	t <sub>SPERR</sub>		7			ns
PERR_B hold time	t <sub>HPERR</sub>		2 <sup>Note 1</sup>			

- Notes**
1. Relaxed specification from PCI Local Bus Specification Revision 2.1 0 ns → 2 ns
  2. Relaxed specification from PCI Local Bus Specification Revision 2.1 7 ns → 9 ns

Target read

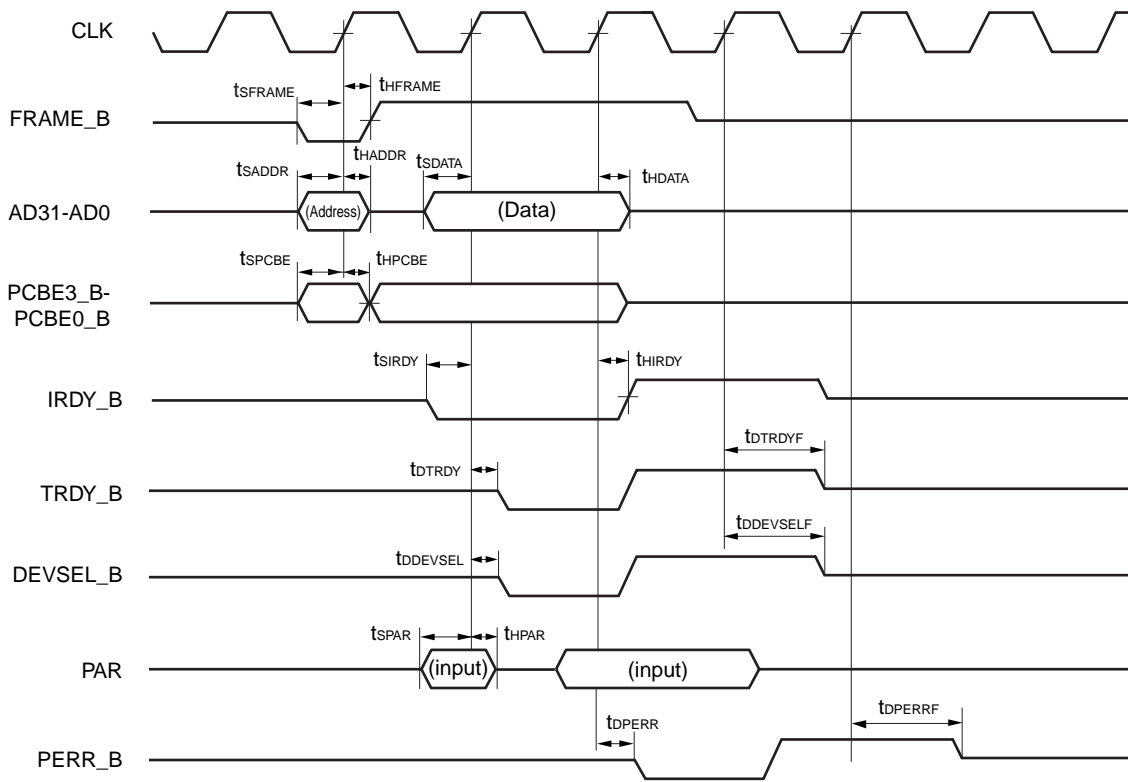


Target write

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FRAME_B setup time	t <sub>SFRAME</sub>		7			ns
FRAME_B hold time	t <sub>HFRAME</sub>		2 <sup>Note 1</sup>			ns
AD (Address) setup time	t <sub>SADDR</sub>		7			ns
AD (Address) hold time	t <sub>HADDR</sub>		2 <sup>Note 1</sup>			ns
AD (Data) setup time	t <sub>SDATA</sub>		7			ns
AD (Data) hold time	t <sub>HDATA</sub>		2 <sup>Note 1</sup>			ns
PCBE_B setup time	t <sub>SPCBE</sub>		7			ns
PCBE_B hold time	t <sub>HPCBE</sub>		2 <sup>Note 1</sup>			ns
IRDY_B setup time	t <sub>SIRDY</sub>		9 <sup>Note 2</sup>			ns
IRDY_B hold time	t <sub>HIRDY</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → TRDY_B valid time	t <sub>DTRDY</sub>		2		11	ns
CLK↑ → TRDY_B float time	t <sub>DTRDYF</sub>				28	ns
CLK↑ → DEVSEL_B valid time	t <sub>DDEVSEL</sub>		2		11	ns
CLK↑ → DEVSEL_B float time	t <sub>DDEVSELF</sub>				28	ns
PAR setup time	t <sub>SPAR</sub>		7			ns
PAR hold time	t <sub>HPAR</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → PERR_B valid time	t <sub>DPERR</sub>		2		11	ns
CLK↑ → PERR_B float time	t <sub>DPERRF</sub>				28	ns

- Notes**
1. Relaxed specification from PCI Local Bus Specification Revision 2.1 0 ns → 2 ns
  2. Relaxed specification from PCI Local Bus Specification Revision 2.1 7 ns → 9 ns

Target write

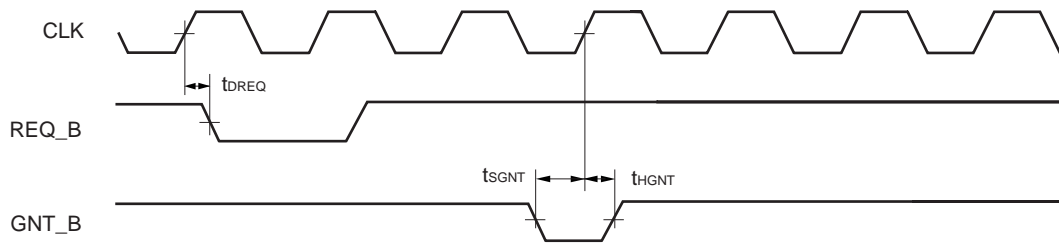


**Bus arbitration**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK↑ → REQ_B valid time	tDREQ		2		12	ns
GNT_B setup time	tSGNT		10			ns
GNT_B hold time	tHGNT		2 <sup>Note</sup>			ns

**Note** Relaxed specification from PCI Local Bus Specification Revision 2.1 0 ns → 2 ns

**Bus arbitration**



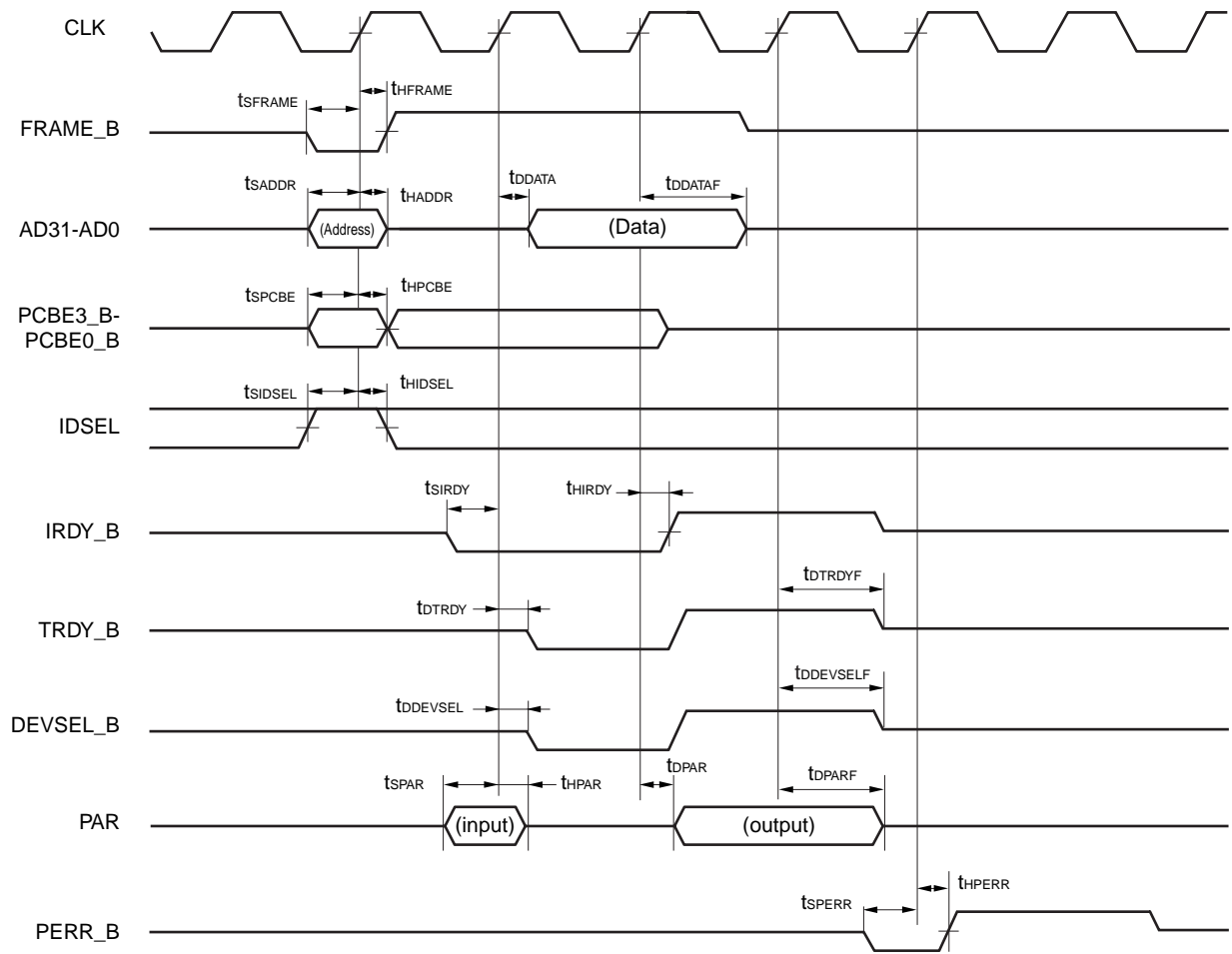
Configuration read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FRAME_B setup time	t <sub>SFRAME</sub>		7			ns
FRAME_B hold time	t <sub>HFRAME</sub>		2 <sup>Note 1</sup>			ns
AD (Address) setup time	t <sub>SADDR</sub>		7			ns
AD (Address) hold time	t <sub>HADDR</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → AD (Data) valid time	t <sub>DDATA</sub>		2		11	ns
CLK↑ → AD (Data) float time	t <sub>DDATAF</sub>				28	ns
PCBE_B setup time	t <sub>SPCBE</sub>		7			ns
PCBE_B hold time	t <sub>HPCBE</sub>		2 <sup>Note 1</sup>			ns
IDSEL setup time	t <sub>SIDSEL</sub>		7			ns
IDSEL hold time	t <sub>HIDSEL</sub>		2 <sup>Note 1</sup>			ns
IRDY_B setup time	t <sub>SIRDY</sub>		9 <sup>Note 2</sup>			ns
IRDY_B hold time	t <sub>HIRDY</sub>		2 <sup>Note 1</sup>			ns
CLK↑ → TRDY_B valid time	t <sub>DTRDY</sub>		2		11	ns
CLK↑ → TRDY_B float time	t <sub>DTRDYF</sub>				28	ns
CLK↑ → DEVSEL_B valid time	t <sub>DDEVSEL</sub>		2		11	ns
CLK↑ → DEVSEL_B float time	t <sub>DDEVSELF</sub>				28	ns
CLK↑ → PAR valid time	t <sub>DPAR</sub>		2		11	ns
CLK↑ → PAR float time	t <sub>DPARF</sub>				28	ns
PAR setup time	t <sub>SPAR</sub>		7			ns
PAR hold time	t <sub>HPAR</sub>		2 <sup>Note 1</sup>			ns
PERR_B setup time	t <sub>SPERR</sub>		7			ns
PERR_B hold time	t <sub>HPERR</sub>		2 <sup>Note 1</sup>			ns

- Notes**
1. Relaxed specification from PCI Local Bus Specification Revision 2.1 0 ns → 2 ns
  2. Relaxed specification from PCI Local Bus Specification Revision 2.1 7 ns → 9 ns



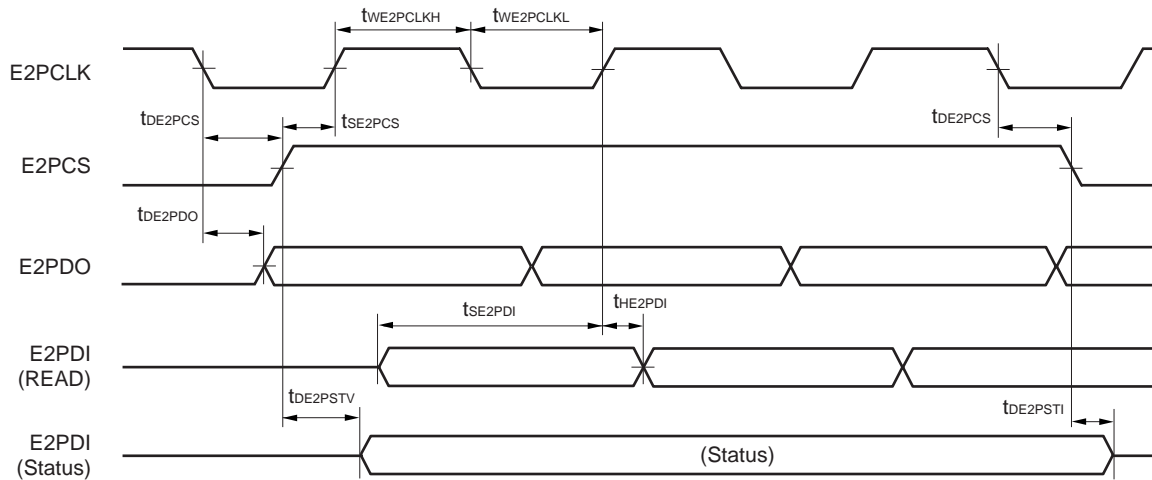
Configuration read



EEPROM Interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
E2PCLK high-level width	$t_{WE2PCLKH}$		$t_{CYCLK} \times 18 - 50$	$t_{CYCLK} \times 18$	$t_{CYCLK} \times 18 + 50$	ns
E2PCLK low-level width	$t_{WE2PCLKL}$		$t_{CYCLK} \times 18 - 50$	$t_{CYCLK} \times 18$	$t_{CYCLK} \times 18 + 50$	ns
E2PCLK↓ → E2PCS valid time	$t_{DE2PCS}$		50			ns
E2PCS↑ → E2PCLK	$t_{SE2PCS}$		50			ns
P2PCLK↓ → E2PDO valid time	$t_{DE2PDO}$				300	ns
E2PDI → E2PCLK setup time	$t_{SE2PDI}$		500			ns
E2PCLK → E2PDI hold time	$t_{HE2PDI}$		70			ns
E2PCS↑ → E2PDI (Status) valid delay time	$t_{DE2PSTV}$				500	ns
E2PCS↓ → E2PDI (Status) invalid delay time	$t_{DE2PSTI}$		0		100	ns

EEPROM interface



**UTOPIA Interface**

**Transmission operation**

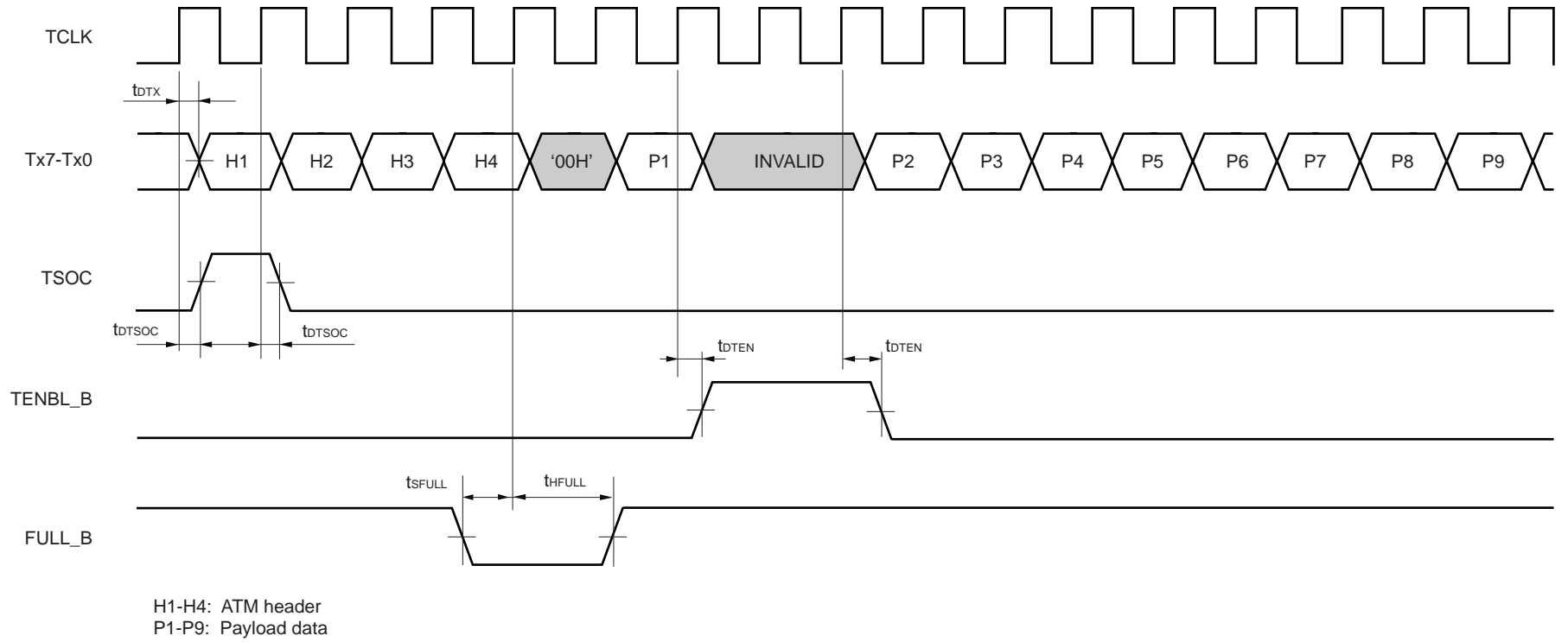
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCLK↑ → Tx delay time	t <sub>DTX</sub>		3		18	ns
TCLK↑ → TSOC delay time	t <sub>DTSOC</sub>		3		18	ns
TCLK↑ → TENBL_B delay time	t <sub>DTEN</sub>		3		18	ns
FULL_B setup time	t <sub>SFULL</sub>		8			ns
FULL_B hold time	t <sub>HFULL</sub>		1			ns

**Reception operation**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rx setup time	t <sub>SRX</sub>		8			ns
Rx hold time	t <sub>HRX</sub>		1			ns
RSOC setup time	t <sub>SRSOC</sub>		8			ns
RSOC hold time	t <sub>HRSOC</sub>		1			ns
RCLK↑ → RENBL_B delay time	t <sub>DREN</sub>		3		18	ns
EMPTY_B setup time	t <sub>SEMP</sub>		8			ns
EMPTY_B hold time	t <sub>HEMP</sub>		1			ns

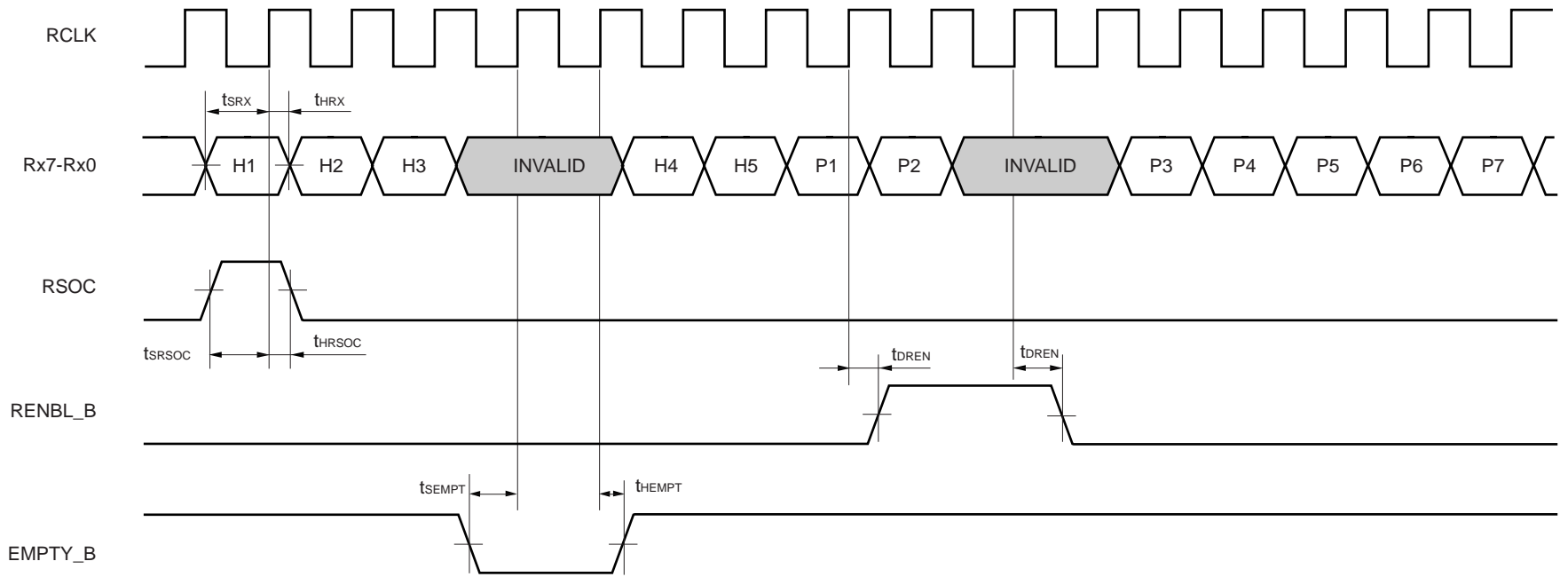
## UTOPIA interface (1)

### Transmission operation



UTOPIA interface (2)

Reception operation



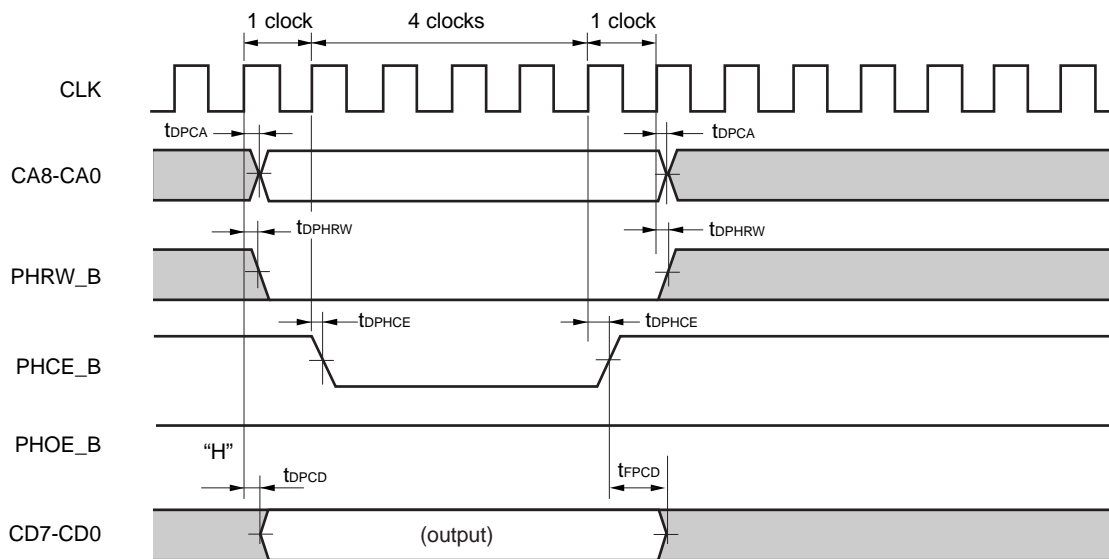
H1-H4: ATM header  
 P1-P7: Payload data

PHY Status Access

Write

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK↑ → CA delay time	t <sub>DPCA</sub>				20	ns
CLK↑ → PHRW_B delay time	t <sub>DPHRW</sub>				20	ns
CLK↑ → PHCE_B delay time	t <sub>DPHCE</sub>				20	ns
CLK↑ → CD delay time	t <sub>DPCD</sub>				20	ns
PHCE_B↑ → CD float time	t <sub>FPCD</sub>		1t <sub>CYCLK</sub> - 10		1t <sub>CYCLK</sub> + 10	ns

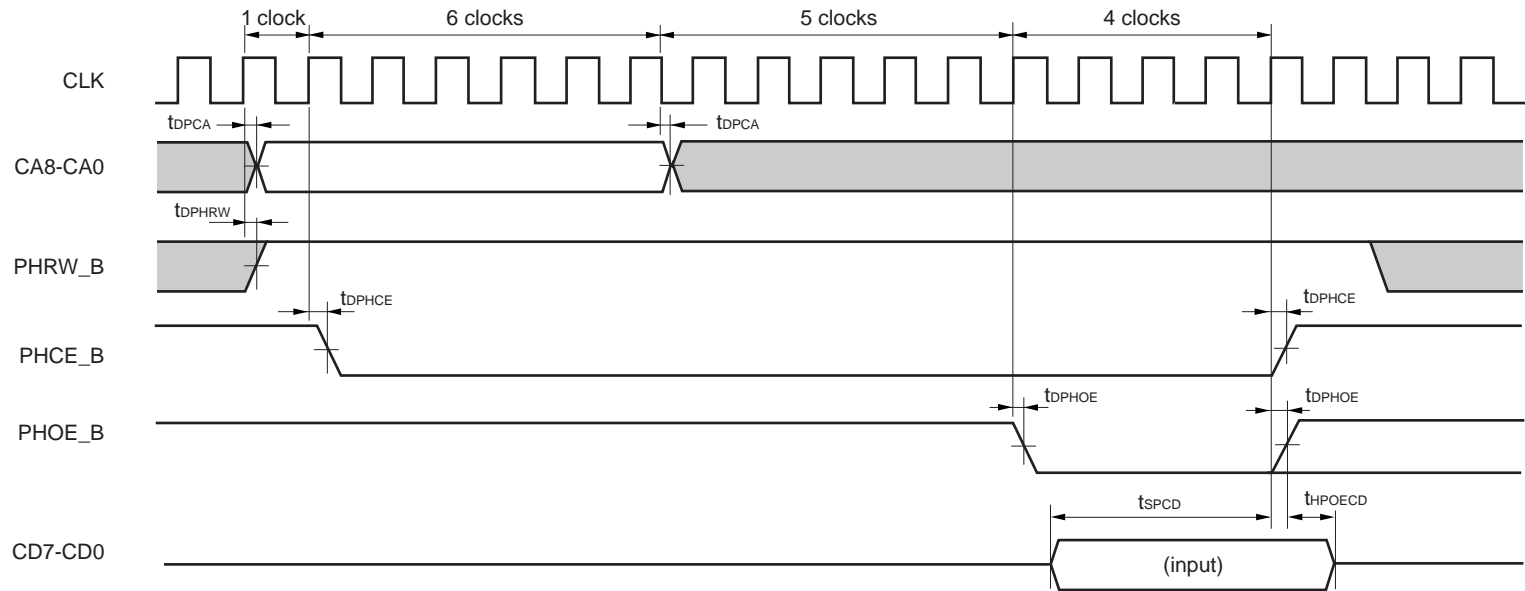
Write timing



Read

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CD setup time	t <sub>SPCD</sub>		0			ns
CD hold time	t <sub>HPOECD</sub>		0			ns
CLK↑ → CA delay time	t <sub>DPCA</sub>				20	ns
CLK↑ → PHRW_B delay time	t <sub>DPHRW</sub>				20	ns
CLK↑ → PHCE_B delay time	t <sub>DPHCE</sub>				20	ns
CLK↑ → PHOE_B delay time	t <sub>DPHOE</sub>				20	ns

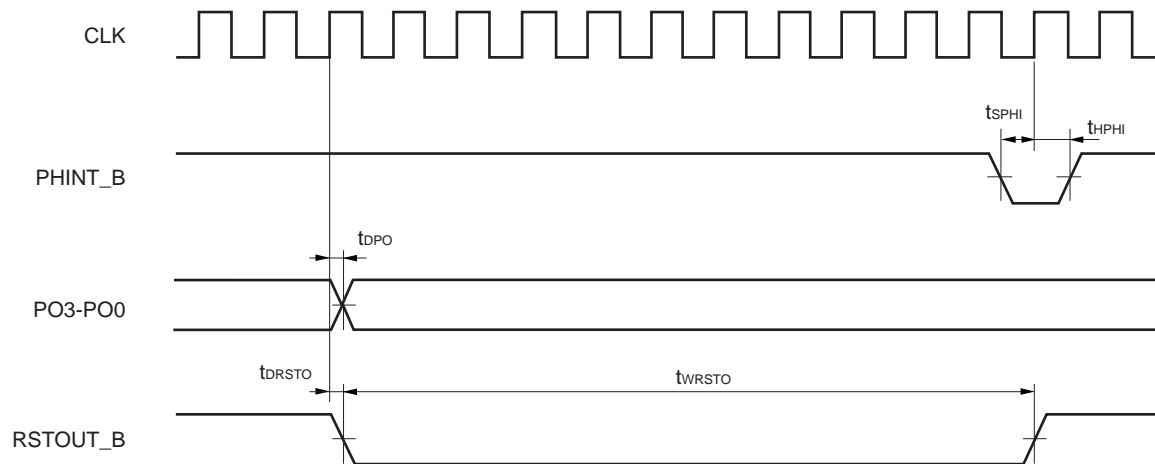
Read timing



Others

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PHINT_B setup time	$t_{SPHI}$		8			ns
PHINT_B hold time	$t_{HPHI}$		1			ns
CLK↑ → PO delay time	$t_{DPO}$		2		25	ns
CLK↑ → RSTOUT_B delay time	$t_{DRSTO}$		2		25	ns
RSTOUT_B output pulse width	$t_{WRSTO}$		11		22	$t_{CYCLK}$

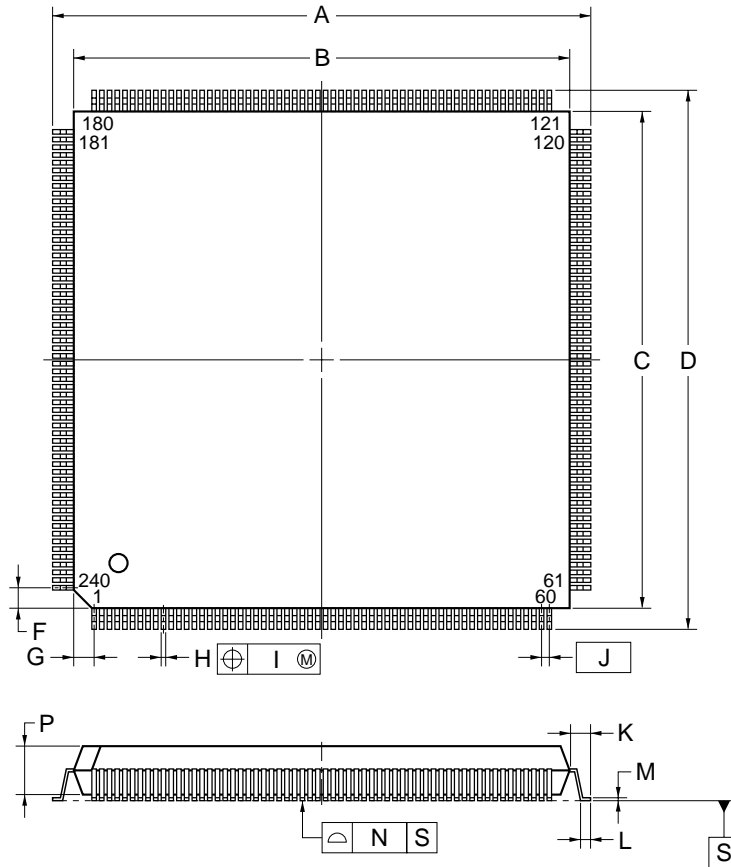
Other timing





3. PACKAGE DRAWING

240 PIN PLASTIC QFP (FINE PITCH) (32x32)



NOTE

- Controlling dimension — millimeter.
- Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	34.6±0.2	1.362±0.008
B	32.0±0.2	1.260±0.008
C	32.0±0.2	1.260±0.008
D	34.6±0.2	1.362±0.008
F	1.25	0.049
G	1.25	0.049
H	0.22 <sup>+0.05</sup> <sub>-0.04</sub>	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.3±0.2	0.051 <sup>+0.009</sup> <sub>-0.008</sub>
L	0.5±0.2	0.020 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>	0.007 <sup>+0.001</sup> <sub>-0.003</sub>
N	0.10	0.004
P	3.2±0.1	0.126±0.004
Q	0.4±0.1	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
R	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>
S	3.8 MAX.	0.150 MAX.

P240GN-50-LMU, MMU-2

**4. SOLDERING CONDITIONS**

Solder the product under the following recommended conditions.

For details of the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and soldering conditions other than those recommended, consult NEC.

**Surface Mount Type**

μPD98409GN-LMU: 240-pin plastic QFP (0.5-mm fine pitch) (32 × 32 mm)

Soldering Method	Soldering Conditions	Symbol of Recommended Condition
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: once, Number of days: 3 <sup>Note</sup> (Afterwards, prebaking is necessary at 125°C for 20 hours.) <b>&lt;Precaution&gt;</b> Products other than in heat-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	IR35-203-1
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per side of device)	—

**Note** Number of days in storage after the dry pack has been opened. The storage conditions are at 25°C, 65%RH max.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.