BQ294502, BQ294504, BQ294506, BQ294512, BQ294522
BQ294524, BQ294532, BQ294533, BQ294534, BQ294582, BQ294592
SLUSAJ3K – SEPTEMBER 2011 – REVISED AUGUST 2022

BQ2945xy Overvoltage Protection For 2-Series and 3-Series Cell Li-Ion Batteries

1 Features

- 2-series and 3-series cell overvoltage monitor for secondary protection
- Fixed programmable delay timer
- Fixed OVP threshold
  - Available range from 3.85 V to 4.6 V
- Fixed OVP delay option: 4 s or 6.5 s
- High-accuracy overvoltage protection: ±10 mV
- Low power consumption I_{CC} ≈ 1 µA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- Low leakage current per cell input < 100 nA
- Small package footprint
  - 6-pin SON

2 Applications

- Second-level protection in Li-ion battery packs in:
  - Tablets
  - Slates
  - Power tools
  - Notebook computers
  - Portable equipment and instrumentation

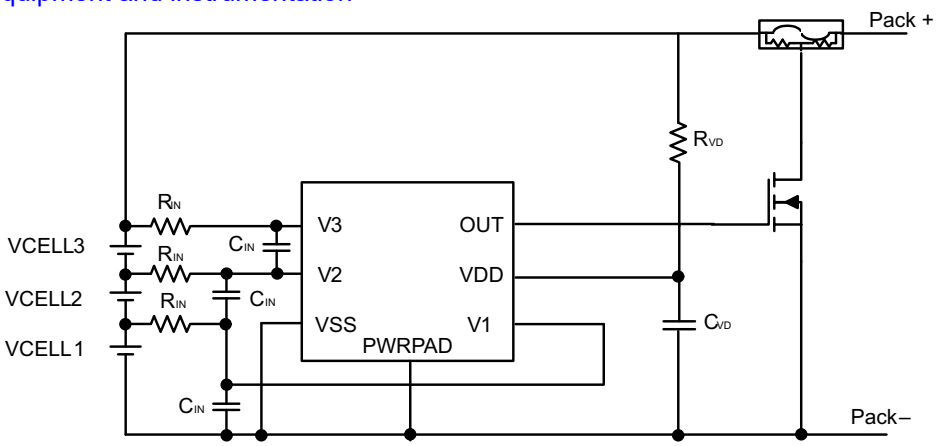
3 Description

The BQ2945xy family of products is a secondary-level voltage monitor and protector for Li-ion battery pack systems. Each cell is monitored independently for an overvoltage condition. Based on the configuration, an output is triggered after a fixed delay if any of the two or three cells has an overvoltage condition. This output is triggered into a high state after an overvoltage condition satisfies the specified delay timer.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
BQ2945xy	SON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (June 2022) to Revision K (August 2022)	Page
• Changed the BQ294534 device to Production Data	3
• Changed the BQ294534 device to Production Data in the *Electrical Characteristics*	5

Changes from Revision I (May 2021) to Revision J (June 2022)	Page
• Added the PRODUCT PREVIEW BQ294534 device	3
• Added the PRODUCT PREVIEW BQ294534 device to the *Electrical Characteristics*	5

Changes from Revision H (December 2017) to Revision I (May 2021)	Page
• Changed the BQ294506 device to Production Data	3

Changes from Revision G (November 2017) to Revision H (December 2017)	Page
• Added the BQ294506 device	3
• Added the BQ294506 device to the *Electrical Characteristics*	5

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5 Device Comparison Table

T_A	PART NUMBER	OVP (V)	DELAY TIME (s)
–40°C to +110°C	BQ294502	4.35	4
	BQ294504	4.35	6.5
	BQ294506	4.38	4
	BQ294512	4.4	4
	BQ294522	4.45	4
	BQ294524	4.45	6.5
	BQ294532	4.5	4
	BQ294533	4.5	6.5
	BQ294534	4.55	4
	BQ294582	4.225	4
	BQ294592	4.3	4

6 Pin Configuration and Functions

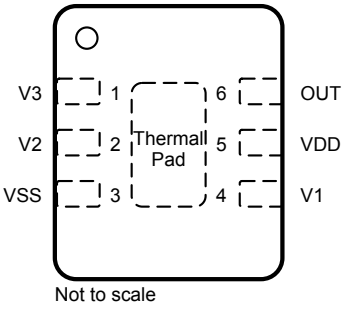


Figure 6-1. DRV Package 6-Pin SON Top View

Table 6-1. Pin Functions

NUMBER	NAME	TYPE(1)	DESCRIPTION
1	V3	IA	Sense input for positive voltage of the third cell from the bottom of the stack.
2	V2	IA	Sense input for positive voltage of the second cell from the bottom of the stack.
3	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack.
4	V1	IA	Sense input for positive voltage of the lowest cell in the stack.
5	VDD	P	Power supply
6	OUT	OA[1]	Output drive for external N-channel FET.
—	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed-circuit-board (PCB) for proper operation.

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD–VSS	–0.3	30	V
Input voltage	V1–VSS or V2–VSS or V3–VSS+	–0.3	30	V
	V3–V2 or V2–V1	–0.3	8	V
Output voltage	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See Section 7.4.		
Lead temperature (soldering, 10 s), T_{SOLDER}			300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See Figure 8-3.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD} (1)		3	25	V
Input voltage	V3–V2 or V2–V1 or V1–VSS	0	5	V
Operating ambient temperature, T_A		–40	110	°C

(1) See Section 9.2.

7.4 Thermal Information

THERMAL METRIC(1)		BQ2945xy DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	90.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	110.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	96.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

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7.5 Electrical Characteristics

Typical values stated where T_A = 25°C and VDD = 10.8 V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE PROTECTION THRESHOLD VCx						
V_{OV}	$V_{(PROTECT)}$ – Overvoltage Detection	BQ294502, fixed delay 4 s		4.35		V
		BQ294504, fixed delay 6.5 s		4.35		
		BQ294506, fixed delay 4 s		4.38		
		BQ294512, fixed delay 4 s		4.4		
		BQ294522, fixed delay 4 s		4.45		
		BQ294524, fixed delay 6.5 s		4.45		
		BQ294532, fixed delay 4 s		4.5		
		BQ294533, fixed delay 6.5 s		4.5		
		BQ294534, fixed delay 4 s		4.55		
		BQ294582, fixed delay 4 s		4.225		
		BQ294592, fixed delay 4 s		4.3		
V_{HYS}	Overvoltage Detection Hysteresis	V_{HYS}	250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C, BQ2945xy	–10		10	mV
		T_A = 25°C, BQ294506 only	–7		7	mV
$V_{OA\ –DRIFT}$	OV Detection Accuracy due to Temperature	T_A = –40°C T_A = 0°C T_A = 60°C T_A = 110°C	–40 –20 –24 –54		44 20 24 54	mV
		T_A = 10°C to 45°C, BQ294506 only	–15		15	mV
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	Supply Current	(V3–V2) = (V2–V1) = (V1–VSS) = 4 V (See Figure 8-3 for reference.)		1	2	µA
		(V3–V2) = (V2–V1) = (V1–VSS) = 2.8 V with T_A = –40°C to 60°C			1.25	
I_{IN}	Input Current at Vx Pins	Measured at V3, V2, and V1 = 4 V (V2–V1) = (V1–VSS) = 4 V T_A = 0°C to 60°C (See Figure 8-3 for reference.)	–0.1		0.1	µA
OUTPUT DRIVE OUT						
V_{OUT}	Output Drive Voltage	(V3–V2) or (V2–V1) or (V1–VSS) > V_{OV} V_{DD} = 7.2 V, I_{OH} = 100 µA, T_A = –40°C to +110°C	6			V
		Two of the three cells are short circuit and only one cell is powered (V3–V2) or (V2–V1) or (V1–VSS) > V_{OV} V_{DD} = Vx (Cell voltage), I_{OH} = 100 µA, T_A = –40°C to +110°C		VDD – 0.2		V
		(V3–V2), (V2–V1), and (V1–VSS) < V_{OV}, I_{OL} = 100 µA, T_A = 25°C T_A = –40°C to +110°C		250	400	mV
$I_{OUT(Short)}$	OUT Short Circuit Current	OUT = 0 V (V3–V2) or (V2–V1) or (V1–VSS) > V_{OV}			4.5	mA
t_R	Output Rise Time	CL = 1 nF, $V_{OH(OUT)}$ = 0 V to 5 V(1)		5		µs
Z_O	Output Impedance			2	5	kΩ
FIXED DELAY TIMER						
t_{DELAY}	Fault Detection Delay Time	Fixed Delay, BQ2945xy with delay set to 4s typ	3.2	4	4.8	s
		Fixed Delay, BQ2945xy with delay set to 6.5 s	5.2	6.5	7.8	

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7.5 Electrical Characteristics (continued)

Typical values stated where T_A = 25°C and VDD = 10.8 V, MIN/MAX values stated where T_A = –40°C to +110°C and V_{DD} = 3 V to 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode	Fixed Delay (Internal settings)		15		ms

(1) Specified by design. It is not 100% tested in production.

7.6 Typical Characteristics

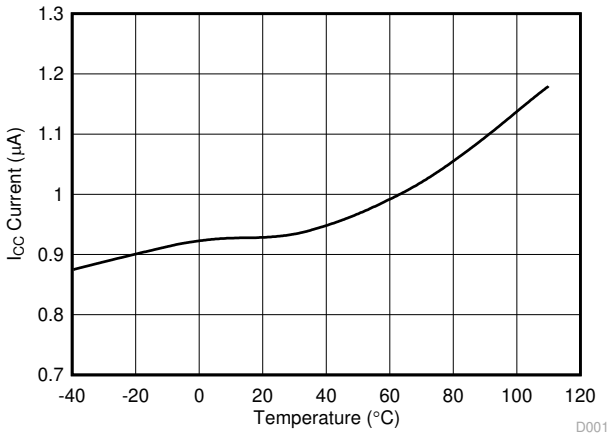


Figure 7-1. I_{CC} Current Consumption vs Temperature

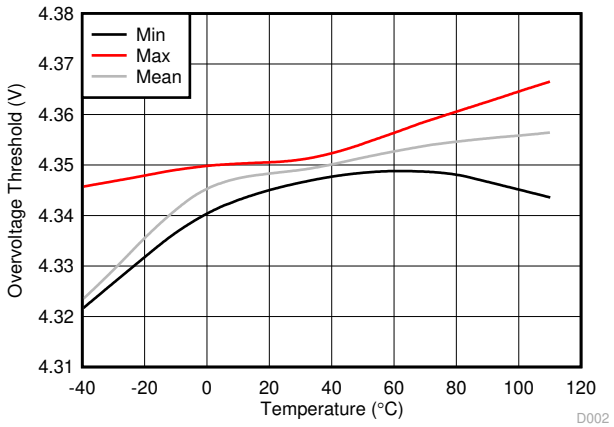


Figure 7-2. BQ294502 Overvoltage Threshold (OVT) vs Temperature

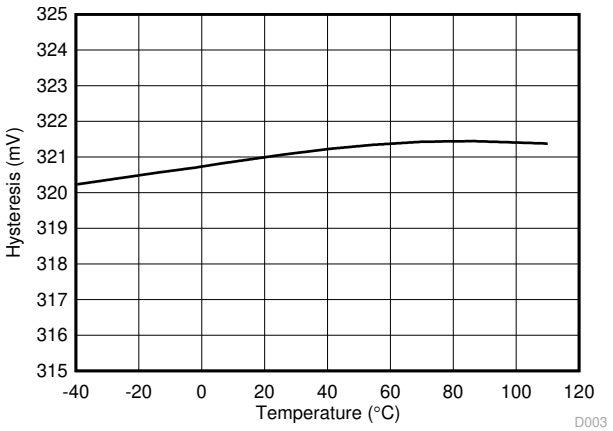


Figure 7-3. Hysteresis V_{HYS} vs Temperature

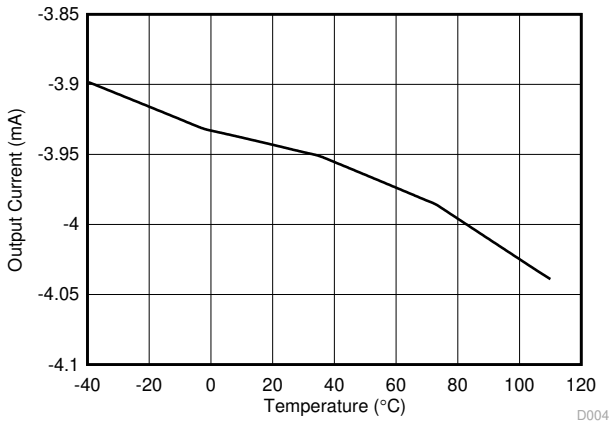


Figure 7-4. Output Current I_{OUT} vs Temperature

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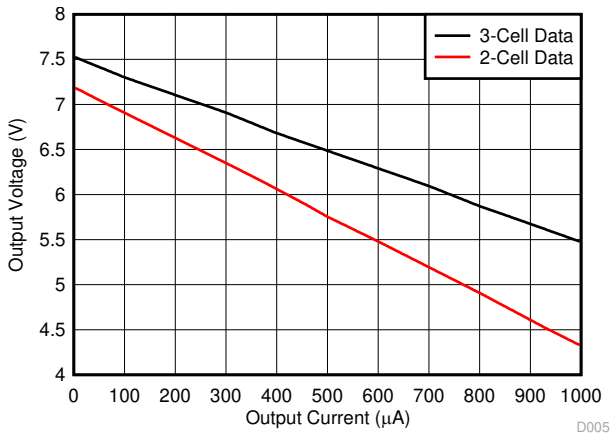


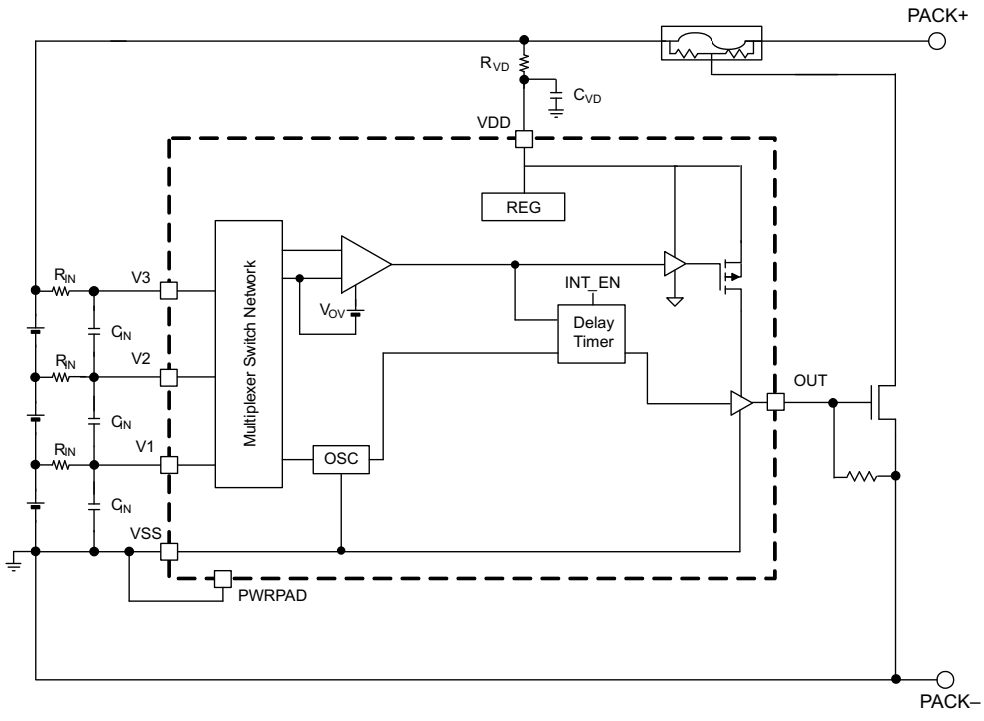
Figure 7-5. Output Voltage vs Output Current

8 Detailed Description

8.1 Overview

The BQ2945xy is a second-level overvoltage (OV) protector. Each cell is monitored independently by comparing the actual cell voltage to a protection voltage threshold, V_{OV}. The protection threshold is preprogrammed at the factory with a range from 3.85 V to 4.65 V.

8.2 Functional Block Diagram



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8.3 Feature Description

The voltage sensing for each cell is done independently using a multiplexer. The method of overvoltage detection is comparing the voltage to an overvoltage protection voltage V_{OV}. Once the voltage exceeds the programmed fixed value, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for either a 4-s or 6.5-s delay. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if *all* of the cell inputs (Vx) are below the OVP threshold minus the Vhys.

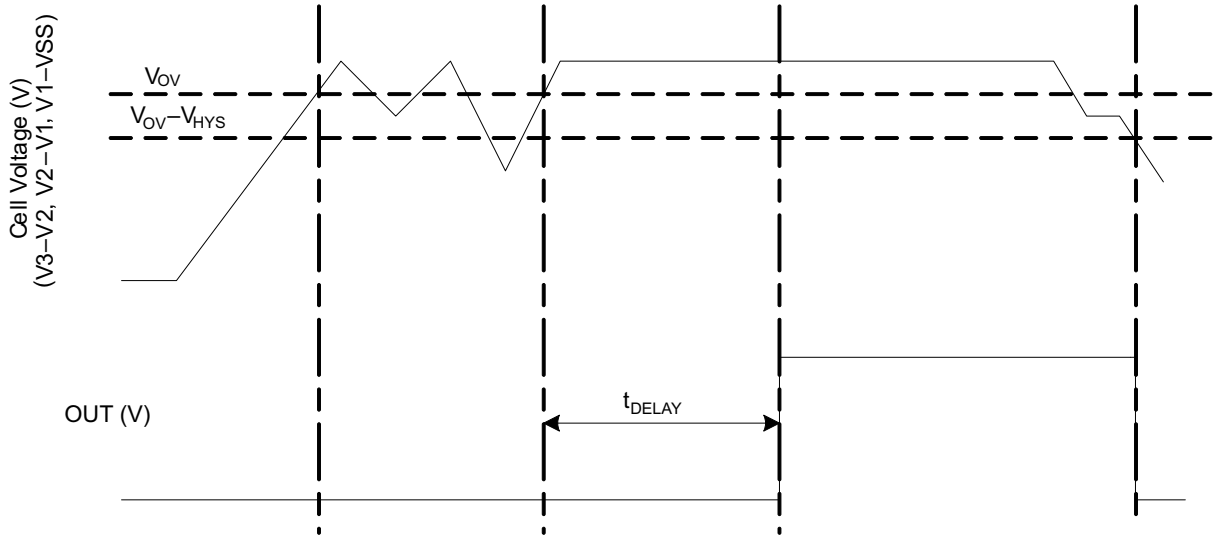


Figure 8-1. Timing for Overvoltage Sensing

8.3.1 Sense Positive Input for VX

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

The gate of an external N-channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. OUT resets to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.3.4 Thermal Pad, PWRPAD

For correct operation, the power pad (PWRPAD) is connected to the V_{SS} terminal on the PCB.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, VOV, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1) and (V3–V2). The OUT pin is inactive in this mode.

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, V_{OV} for the configured OV delay time, t_{DELAY}. The OUT pin pulls high internally. An external FET then turns on, shorting the fuse to ground, which enables the battery or charger power to blow the fuse. When all of the cell voltages fall below (V_{OV}–V_{HYS}), the device returns to NORMAL mode.

8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, set VDD to at least 10 V higher than V3 (see Figure 8-2). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

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CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 8-2 shows the timing for CTM.

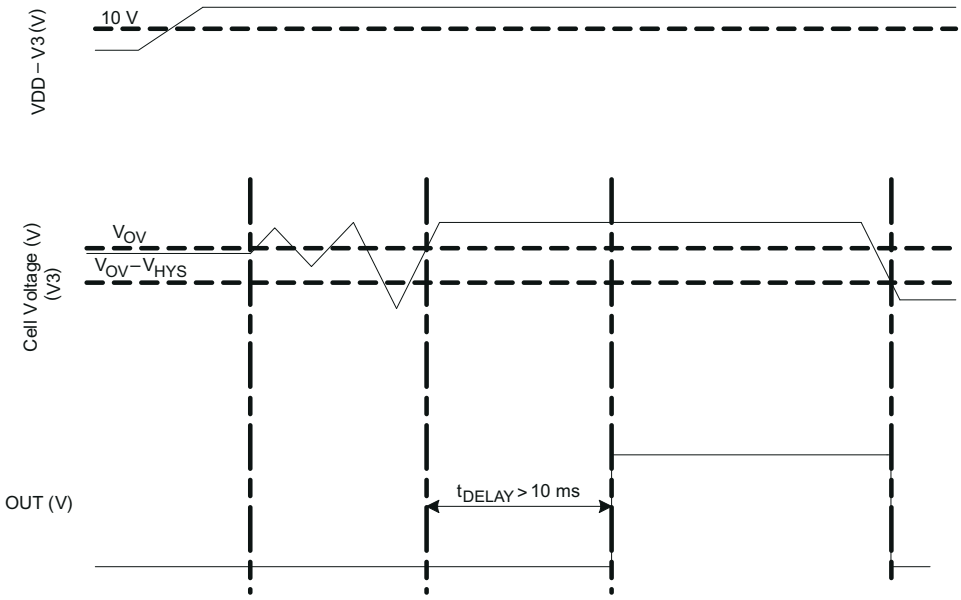


Figure 8-2. Timing for Customer Test Mode

Figure 8-3 shows the measurement for current consumption for the product for both VDD and Vx.

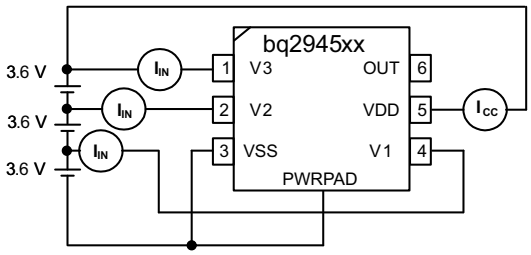


Figure 8-3. Configuration for IC Current Consumption Test

9 Application and Implementation

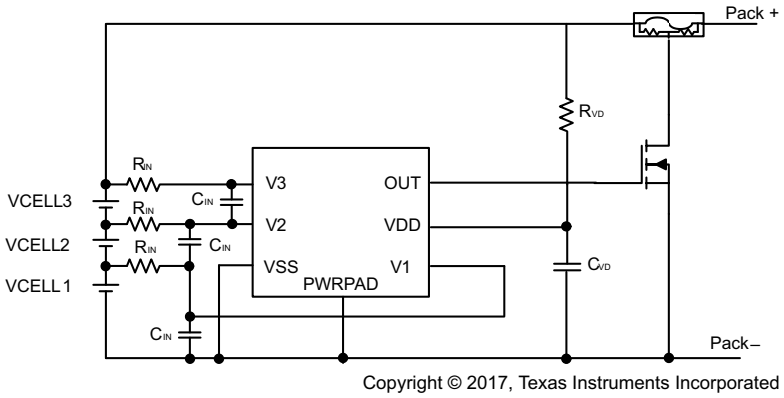
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The BQ2945xy devices are second-level protectors used for overvoltage protection for the battery pack in the application. The device, when configuring the OUT pin with active high, drives an NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery or charger power to blow the fuse and cut the power path.

9.2 Typical Application



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Figure 9-1. Application Configuration Schematic

9.2.1 Design Requirements

Changes to the ranges stated in Table 9-1 impact the accuracy of the cell measurements. Figure 9-1 shows each external component.

Table 9-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	TYP	MAX	UNIT
Voltage monitor filter resistance	RIN	100	1000	4700	Ω
Voltage monitor filter capacitance	CIN	0.1		1	µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

9.2.2 Detailed Design Procedure

1. Determine the overvoltage threshold and delay time. Select the proper device from the table in Section 5 or contact TI for a different configuration.
2. Determine the number of cell in series. The device supports 2-series to 3-series cell configurations. For a 2-series configuration, the V3 pin is shorted to V2.
3. To connect to the device, follow the application configuration schematic (see Figure 9-1).

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9.2.3 Application Curves

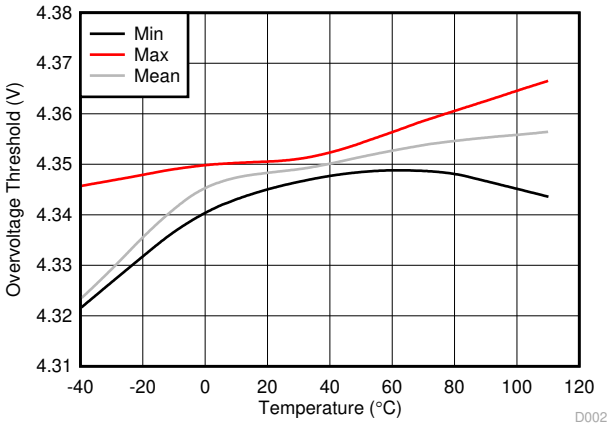


Figure 9-2. OVT vs Temperature

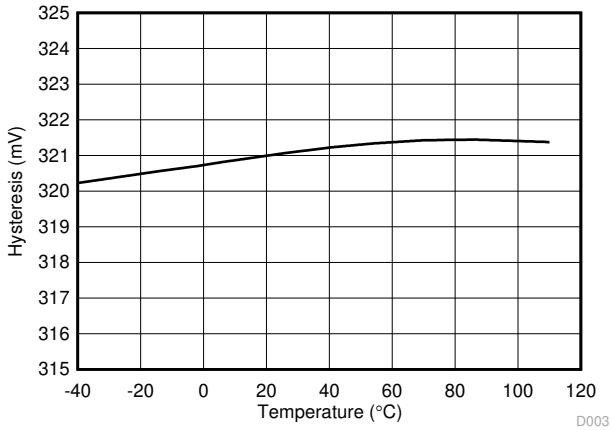


Figure 9-3. V_{HYS} vs Temperature

9.3 System Examples

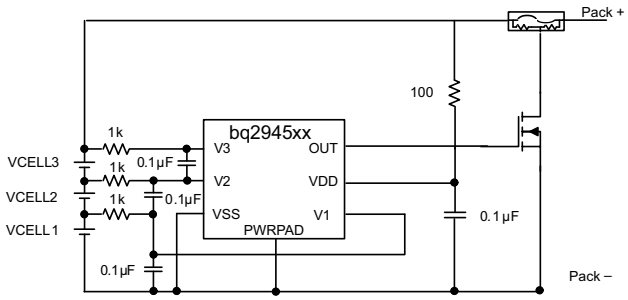


Figure 9-4. 3-Series Cell Configuration with Fixed Delay

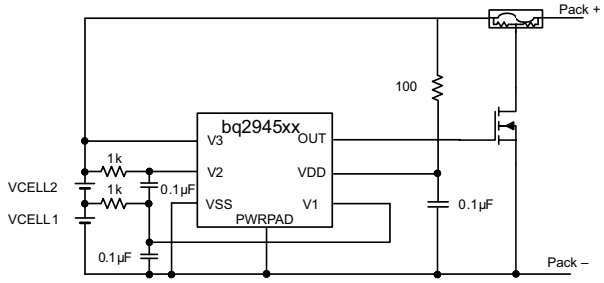


Figure 9-5. 2-Series Cell Configuration with Internal Fixed Delay

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10 Power Supply Recommendations

The maximum power of this device is 25 V on VDD.

11 Layout

11.1 Layout Guidelines

- Ensure the RC filters for the V1 and VDD pins are placed as close as possible to the target terminal, reducing the tracing loop area.
- Route the VSS pin to the CELL– terminal.
- Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack– is sufficient to withstand the current during a fuse blown event.

11.2 Layout Example

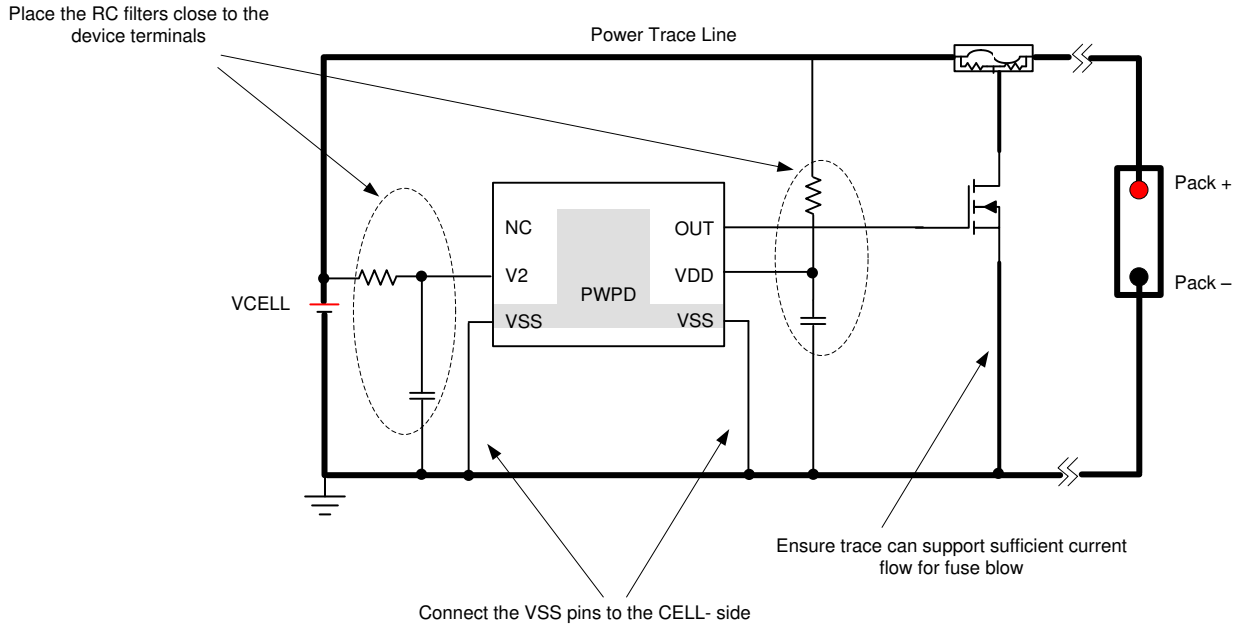


Figure 11-1. Layout Schematic

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Documentation

- *Semiconductor and IC Package Thermal Metrics Application Report*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294502DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294502DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4502	Samples
BQ294504DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	Samples
BQ294504DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4504	Samples
BQ294506DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4506	Samples
BQ294506DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4506	Samples
BQ294512DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294512DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4512	Samples
BQ294522DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294522DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4522	Samples
BQ294524DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4524	Samples
BQ294524DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4524	Samples
BQ294532DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4532	Samples
BQ294532DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4532	Samples
BQ294533DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4533	Samples
BQ294533DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4533	Samples
BQ294534DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	4534	Samples
BQ294582DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4582	Samples
BQ294582DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4582	Samples
BQ294592DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ294592DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4592	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

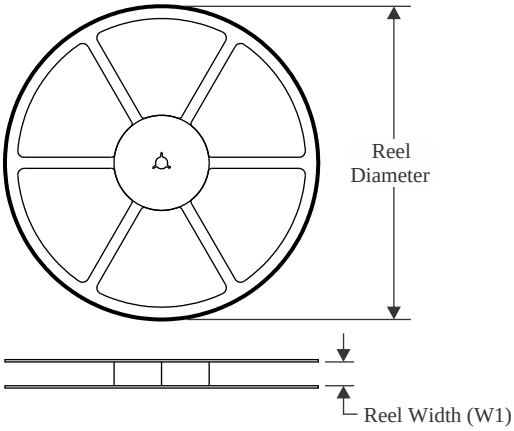
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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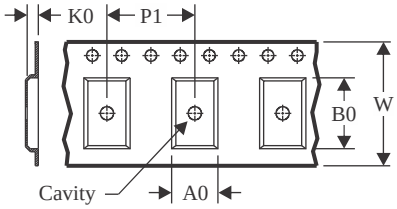
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

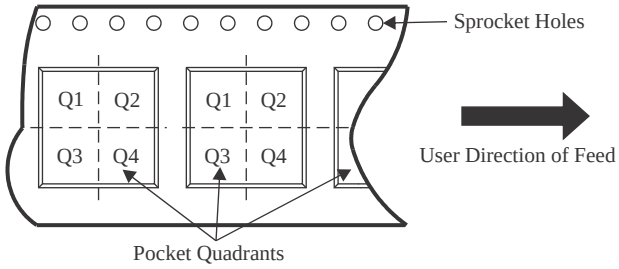


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

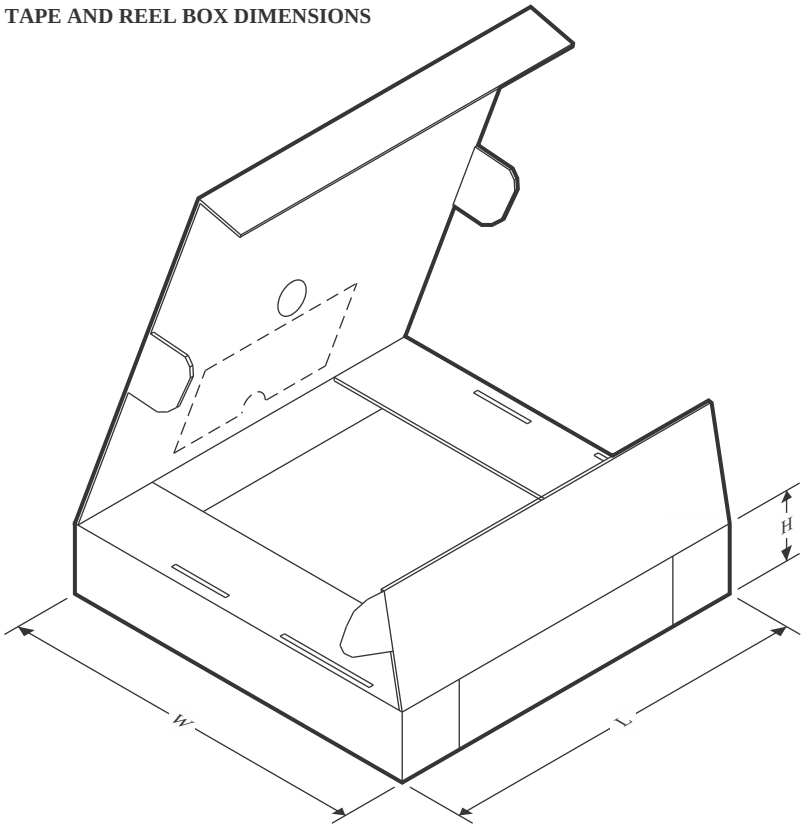


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294502DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294502DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294502DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294502DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294504DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294506DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294506DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294506DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294506DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294512DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294512DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294522DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294522DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294524DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294524DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294532DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294533DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294533DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294534DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294582DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ294592DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



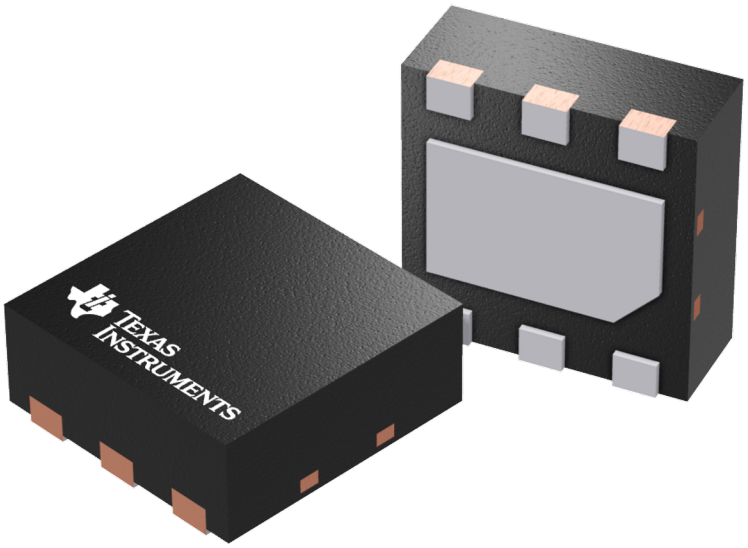
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294502DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294502DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294502DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294502DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294504DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294504DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294504DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294506DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294506DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294506DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294506DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294512DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294512DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294522DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294522DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294524DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294524DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294524DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294532DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294532DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294532DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294533DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294533DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294534DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294582DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294582DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294582DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294582DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294592DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
BQ294592DRVT	WSON	DRV	6	250	210.0	185.0	35.0
BQ294592DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



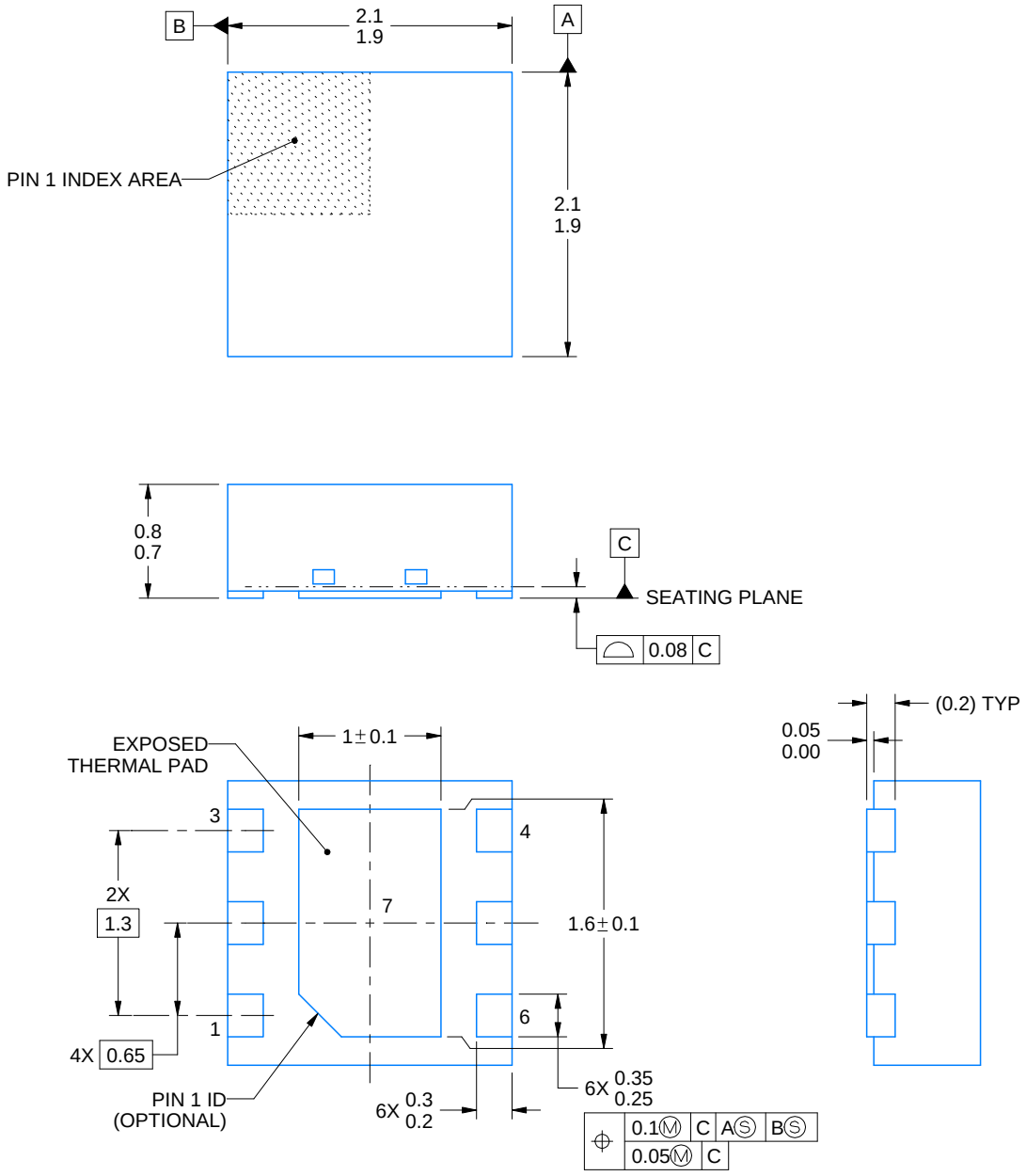
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

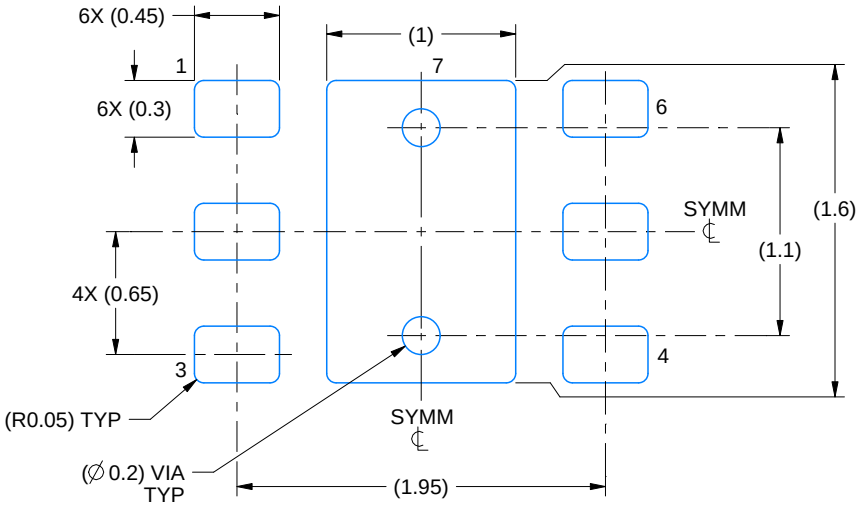
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

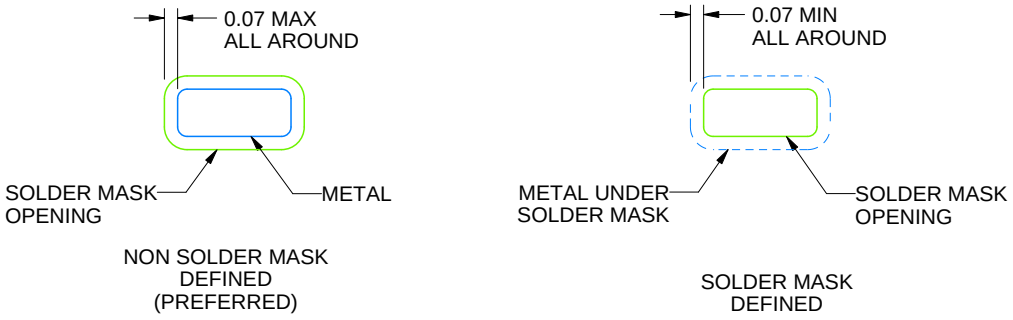


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

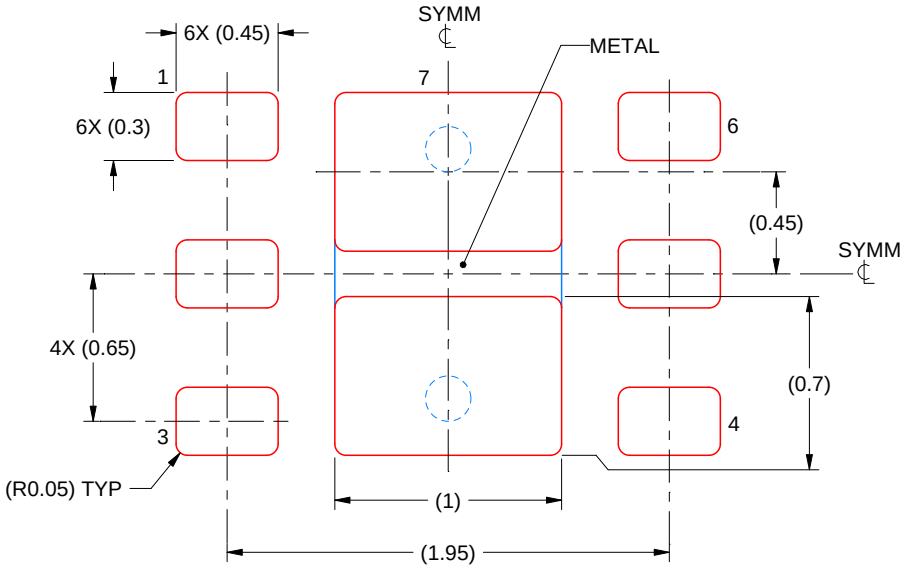
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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