NCV4275A

Linear Voltage Regulator, LDO, 450 mA, with Reset

The NCV4275A is an integrated low dropout regulator designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The output is regulated at 5.0 V or 3.3 V and is rated to 450 mA of output current. It also provides a number of features, including overcurrent protection, overtemperature protection and a programmable microprocessor reset. The NCV4275A is available in the DPAK and D^2PAK surface mount packages. The output is stable over a wide output capacitance and ESR range. The NCV4275A is pin for pin compatible with NCV4275.

Features

- 5.0 V and 3.3 V, ±2% Output Voltage Options
- 450 mA Output Current
- Very Low Current Consumption
- Active Reset Output
- Reset Low Down to V_Q = 1.0 V
- 500 mV (max) Dropout Voltage
- Fault Protection
  - +45 V Peak Transient Voltage
  - −42 V Reverse Voltage
  - Short Circuit Protection
  - Thermal Overload Protection
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- Pin Compatible with NCV4275
- These are Pb−Free Devices

Applications

- Auto Body Electronics

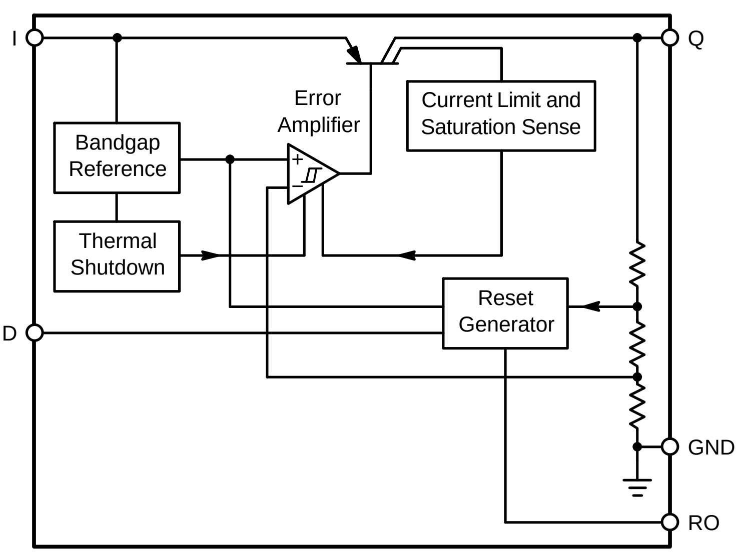

Figure 1. Block Diagram

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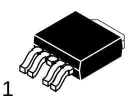
MARKING DIAGRAMS



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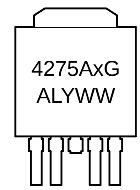
DPAK, 5−PIN
DT SUFFIX
CASE 175AA



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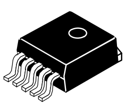

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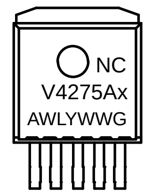
D^2PAK, 5−PIN
DS SUFFIX
CASE 936A



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x	= 5 (5.0 V Output) or 3 (3.3 V Output)
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

Pin	1. I
	2. RO
Tab,	3. GND*
	4. D
	5. Q

* Tab is connected to Pin 3 on all packages

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 17 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Description
1	I	Input; Battery Supply Input Voltage. Bypass to ground with a ceramic capacitor.
2	RO	Reset Output; Open Collector Active Reset (accurate when I > 1.0 V).
3, Tab	GND	Ground; Pin 3 internally connected to tab.
4	D	Reset Delay; timing capacitor to GND for Reset Delay function.
5	Q	Output; ±2.0%, 450 mA output. Bypass with 22 μF capacitor, ESR < 4.5 Ω (5.0 V Version), 3.5 Ω (3.3 V Version) to ground.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage	V_I	−42	45	V
Input Peak Transient Voltage	V_I	−	45	V
Output Voltage	V_Q	−1.0	16	V
Reset Output Voltage	V_{RO}	−0.3	25	V
Reset Output Current	I_{RO}	−5.0	5.0	mA
Reset Delay Voltage	V_D	−0.3	7.0	V
Reset Delay Current	I_D	−2.0	2.0	mA
ESD Susceptibility (Note 1) − Human Body Model − Machine Model − Charge Device Model	ESD_{HBM} ESD_{MM} ESD_{CDM}	4.0 200 1000	− − −	kV V V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{stg}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device incorporates ESD protection and is tested by the following methods: ESD Human Body Model tested per AEC−Q100−002, ESD Machine Model tested per AEC−Q100−003, ESD Charged Device Model tested per AEC−Q100−011, Latch−up tested per AEC−Q100−004.

OPERATING RANGE

Input Voltage Operating Range, 5.0 V Output	V_I	5.5	42	V
Input Voltage Operating Range, 3.3 V Output	V_I	4.4	42	V
Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

LEAD TEMPERATURE SOLDERING REFLOW AND MSL (Note 2)

Lead Free, 60 sec−150 sec above 217°C	T_{SLD}	−	265 Peak	°C
Moisture Sensitivity Level	MSL	1		

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
DPAK 5−PIN PACKAGE			
	Min Pad Board (Note 3)	1″ Pad Board (Note 4)	
Junction−to−Tab ($R_{\theta JT}$)	4.2	4.7	°C/W
Junction−to−Ambient ($R_{\theta JA}$)	100.9	46.8	°C/W
D²PAK 5−PIN PACKAGE			
	0.4 sq. in. Spreader Board (Note 5)	1.2 sq. in. Spreader Board (Note 6)	
Junction−to−Tab ($R_{\theta JT}$)	3.8	4.0	°C/W
Junction−to−Ambient ($R_{\theta JA}$)	74.8	41.6	°C/W

2. PR_R IPC / JEDEC J−STD−020C
3. 1 oz. copper, 0.26 inch^2 (168 mm^2) copper area, 0.062″ thick FR4.
4. 1 oz. copper, 1.14 inch^2 (736 mm^2) copper area, 0.062″ thick FR4.
5. 1 oz. copper, 0.373 inch^2 (241 mm^2) copper area, 0.062″ thick FR4.
6. 1 oz. copper, 1.222 inch^2 (788 mm^2) copper area, 0.062″ thick FR4.

ELECTRICAL CHARACTERISTICS (V_I = 13.5 V; −40°C < T_J < 150°C; unless otherwise noted.)

Characteristic	Symbol	Test Conditions	5.0V Output Voltage			3.3V Output Voltage			Unit
			Min	Typ	Max	Min	Typ	Max	
Output									
Output Voltage	V_Q	100 μA ≤ I_Q ≤ 400 mA 6.0V ≤ V_I ≤ 28V (5.0V Version) 4.4V ≤ V_I ≤ 28V (3.3V version)	4.9	5.0	5.1	3.23	3.3	3.37	V
Output Voltage	V_Q	100 μA ≤ I_Q ≤ 200 mA 6.0V ≤ V_I ≤ 40V (5.0V Version) 4.4V ≤ V_I ≤ 40V (3.3V version)	4.9	5.0	5.1	3.23	3.3	3.37	V
Output Current Limitation	I_Q	V_Q = 0.9 x $V_{Q,typ}$	450	700	−	450	700	−	mA
Quiescent Current $I_q = I_I - I_Q$	I_q	I_Q = 1.0 mA	−	140	200	−	135	200	μA
		I_Q = 1.0 mA, T_J = 25°C	−	140	150	−	135	150	μA
		I_Q = 250 mA	−	10	15	−	10	15	mA
		I_Q = 400 mA	−	23	35	−	23	35	mA
Dropout Voltage	V_{dr}	I_Q = 300 mA $V_{dr} = V_I - V_Q$ (Note 7)	−	250	500	−	1100	1170	mV
Load Regulation	ΔV_Q	I_Q = 5.0 mA to 400 mA	−30	15	30	−30	15	30	mV
Line Regulation	ΔV_Q	ΔV_I = 8.0 V to 32 V, I_Q = 5.0 mA	−15	5.0	15	−15	5.0	15	mV
Power Supply Ripple Rejection	PSRR	f_r = 100 Hz, V_r = 0.5 V_{pp}	−	60	−	−	60	−	dB
Temperature Output Voltage Drift	dV_Q/dT	−−	−	0.5	−	−	0.5	−	mV/K
Reset Timing D and Output RO									
Reset Switching Threshold	$V_{Q,rt}$	−−	4.53	4.65	4.8	3.0	3.1	3.2	V
Reset Output Low Voltage	V_{ROL}	R_{ext} ≥ 5.0 kΩ, V_Q ≥ 1.0V	−	0.2	0.4	−	0.2	0.4	V
Reset Output Leakage Current	I_{ROH}	V_{ROH} = 5.0V	−	0	10	−	0	10	μA
Reset Charging Current	$I_{D,C}$	V_D = 1.0V	3.0	5.5	9.0	2.0	4.0	9.0	μA
Upper Timing Threshold	V_{DU}	−−	1.5	1.8	2.2	0.7	1.3	1.6	V
Lower Timing Threshold	V_{DL}	−−	0.2	0.4	0.7	0.2	0.4	0.7	V
Reset Delay Time	t_{rd}	C_D = 47nF	10	16	22	10	16	22	ms
Reset Reaction Time	t_{rr}	C_D = 47nF	−	1.5	4.0	−	1.5	4.0	μs
Thermal Shutdown									
Shutdown Temperature (Note 8)	T_{SD}	−−	150	−	210	150	−	210	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Measured when output voltage V_Q falls 100 mV below the regulated voltage at V_I = 13.5 V. $V_{dr} = V_I - V_Q$. For output voltage set < 4.4 V, V_{dr} will be constrained by the minimum input voltage.
8. Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

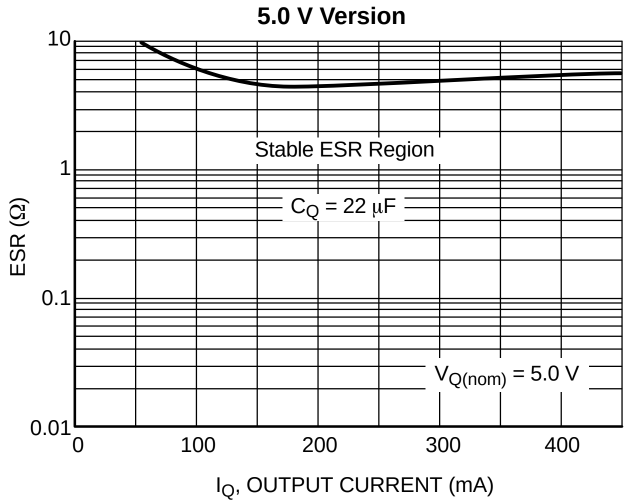


Figure 2. Output Stability with Output Capacitor ESR

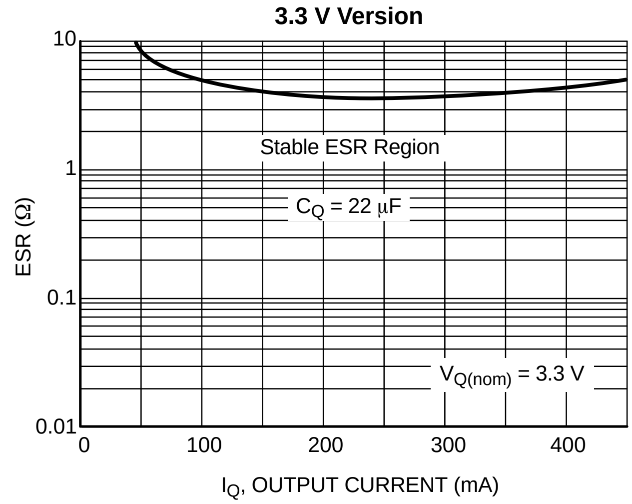


Figure 3. Output Stability with Output Capacitor ESR

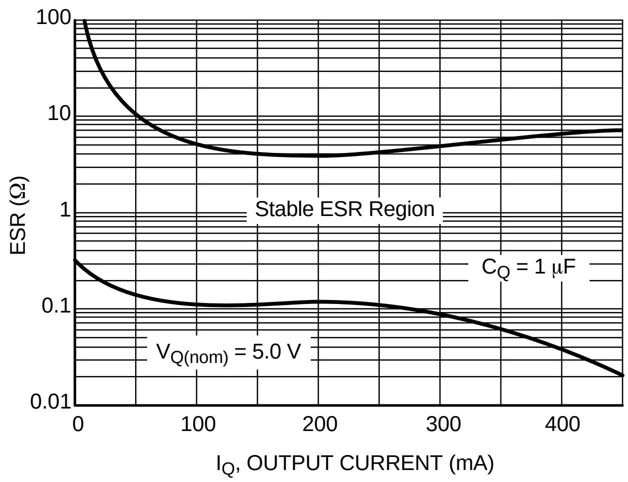


Figure 4. Output Stability with Output Capacitor ESR

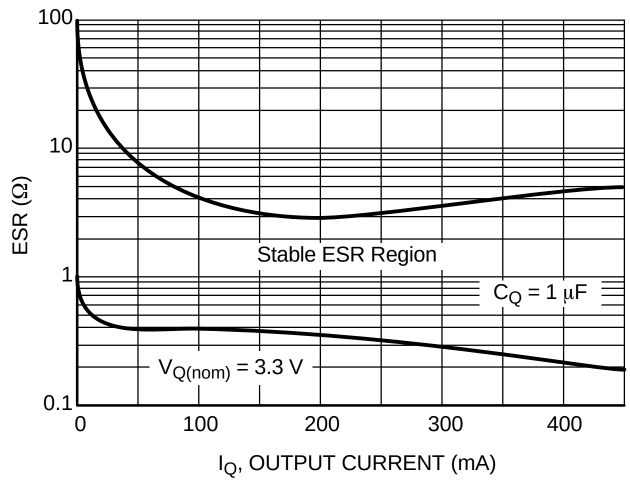


Figure 5. Output Stability with Output Capacitor ESR

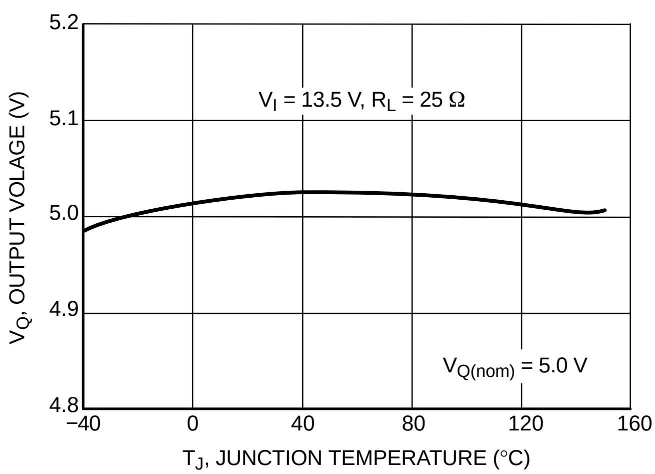


Figure 6. Output Voltage V_Q vs. Temperature T_J

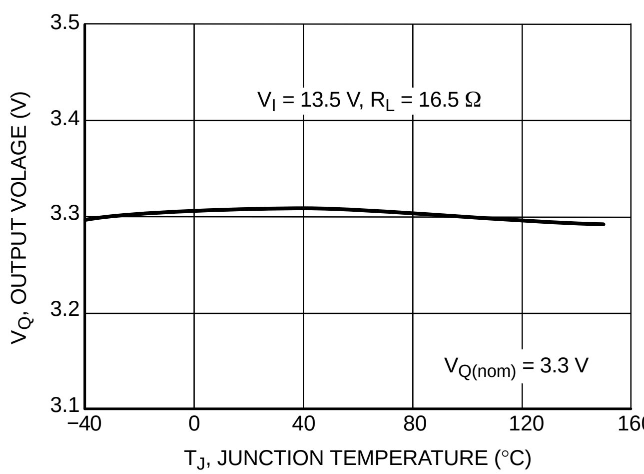


Figure 7. Output Voltage V_Q vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS

5.0 V Version

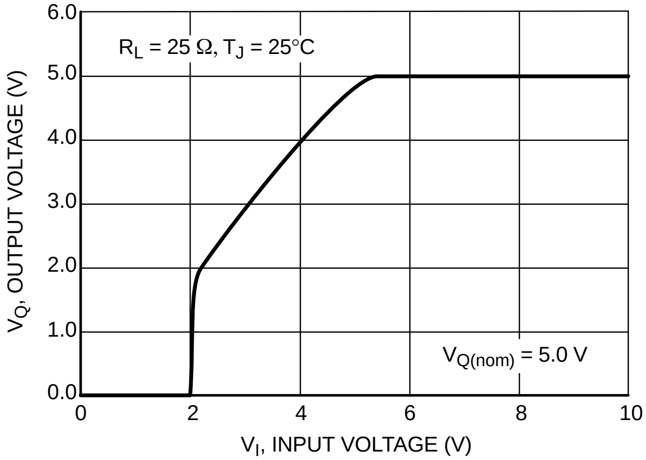


Figure 8. Output Voltage V_Q vs. Input Voltage V_I

3.3 V Version

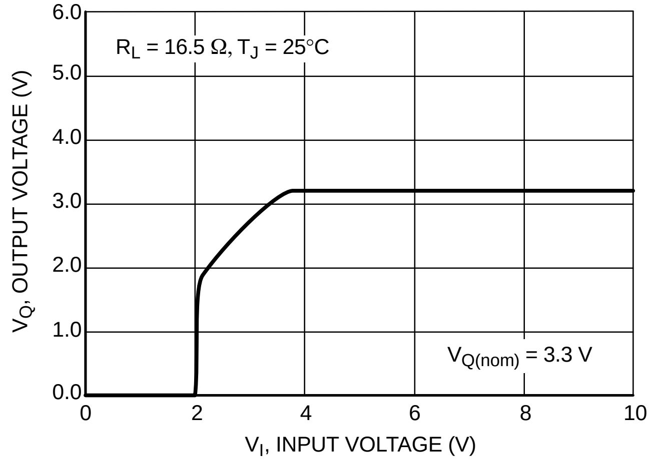


Figure 9. Output Voltage V_Q vs. Input Voltage V_I

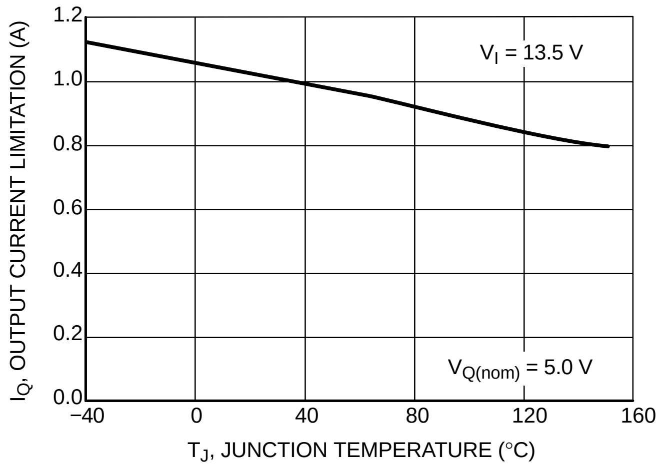


Figure 10. Output Current I_Q vs. Temperature T_J

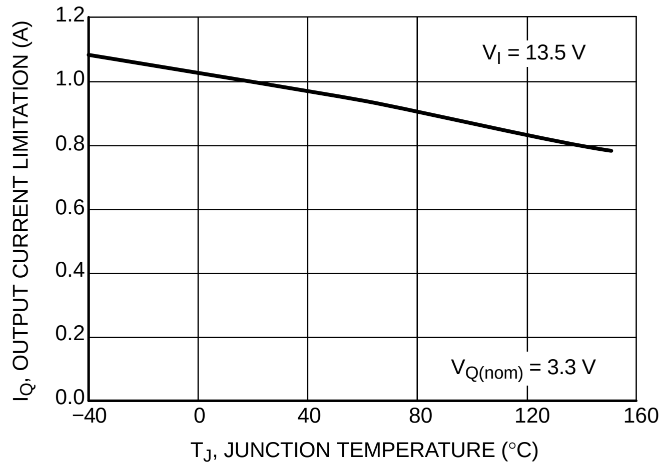


Figure 11. Output Current I_Q vs. Temperature T_J

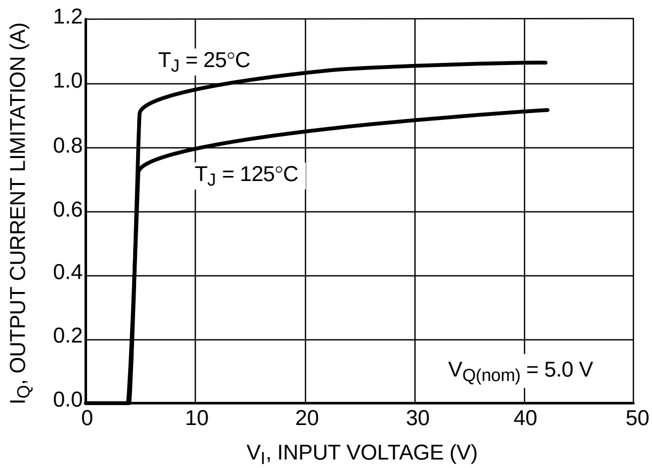


Figure 12. Output Current I_Q vs. Input Voltage V_I

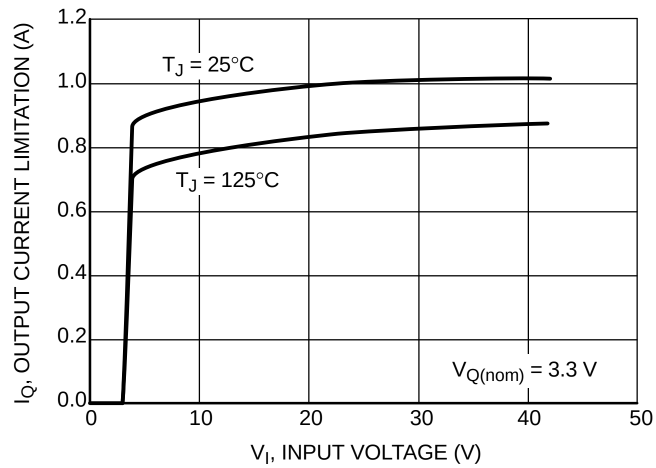


Figure 13. Output Current I_Q vs. Input Voltage V_I

TYPICAL PERFORMANCE CHARACTERISTICS

5.0 V Version

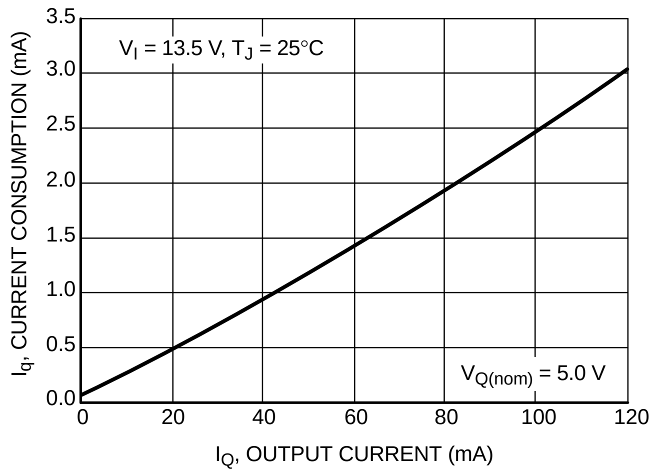


Figure 14. Current Consumption I_q vs. Output Current I_Q

3.3 V Version

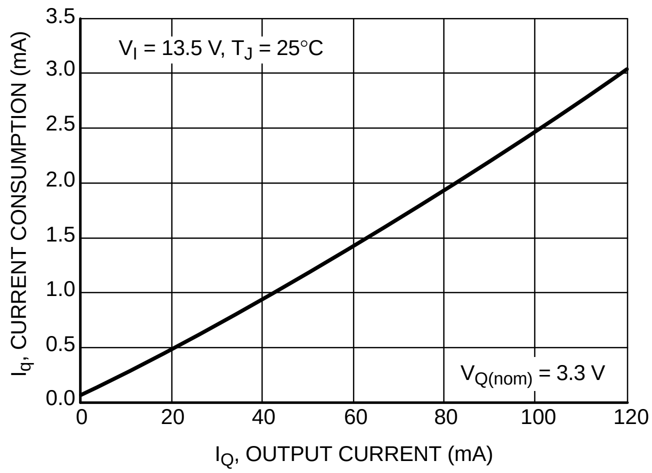


Figure 15. Current Consumption I_q vs. Output Current I_Q

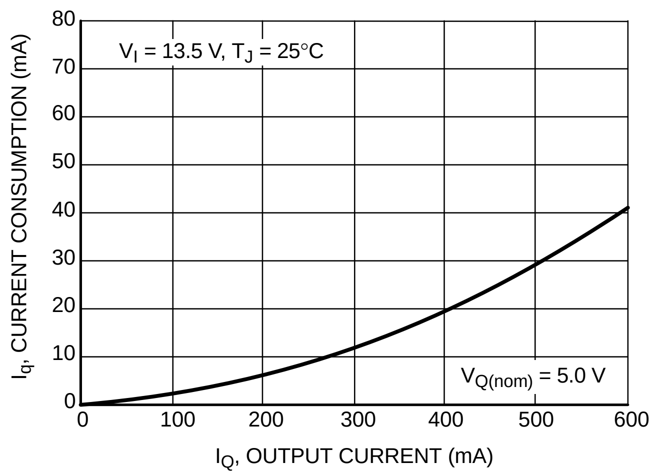


Figure 16. Current Consumption I_q vs. Output Current I_Q

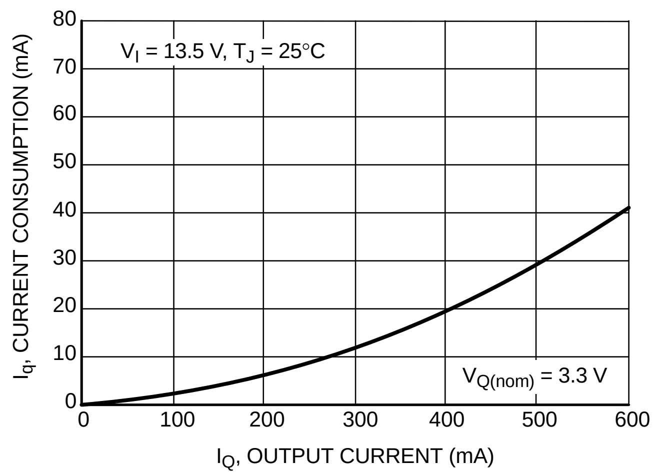


Figure 17. Current Consumption I_q vs. Output Current I_Q

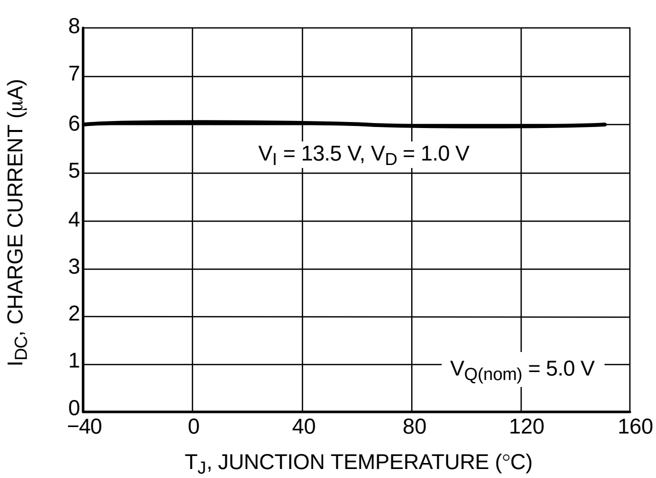


Figure 18. Charge Current $I_{D,C}$ vs. Temperature T_J

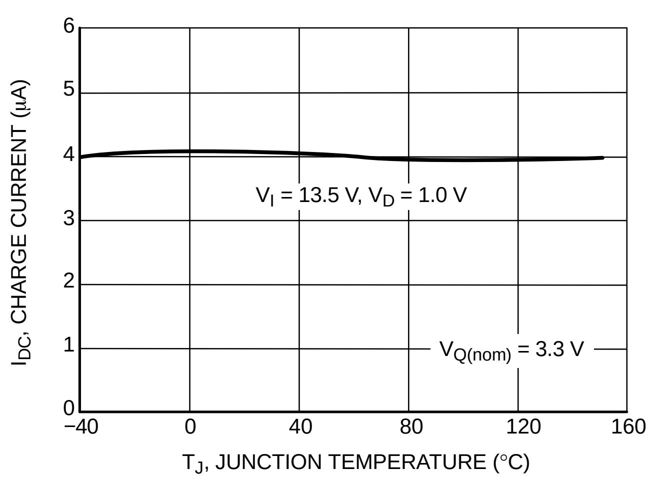


Figure 19. Charge Current $I_{D,C}$ vs. Temperature T_J

TYPICAL PERFORMANCE CHARACTERISTICS

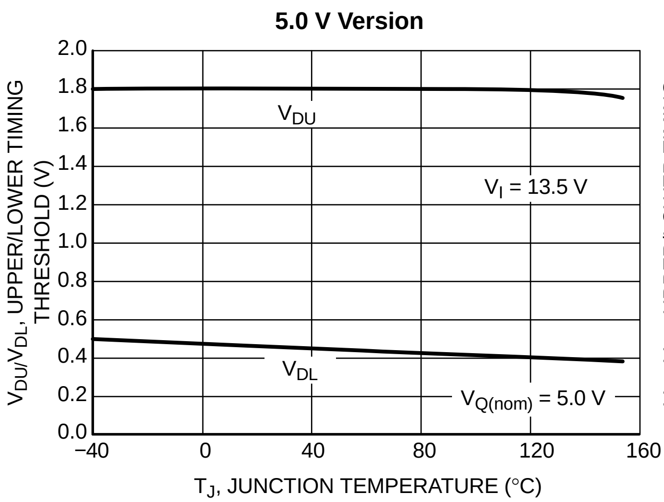


Figure 20. Delay Switching Threshold V_{DU}, V_{DL} vs. Temperature T_J

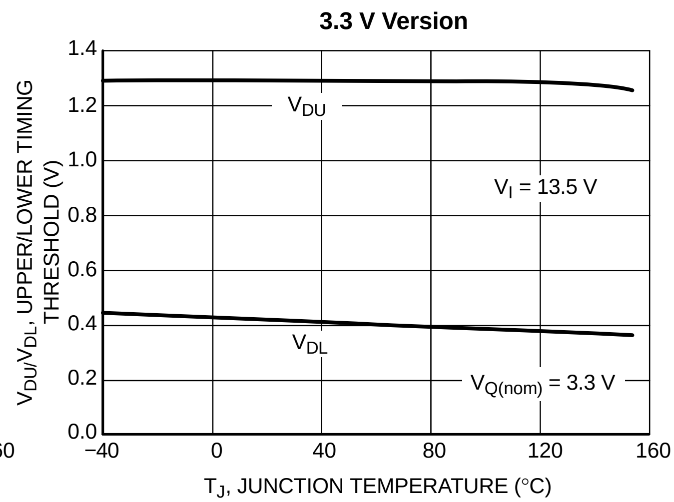


Figure 21. Delay Switching Threshold V_{DU}, V_{DL} vs. Temperature T_J

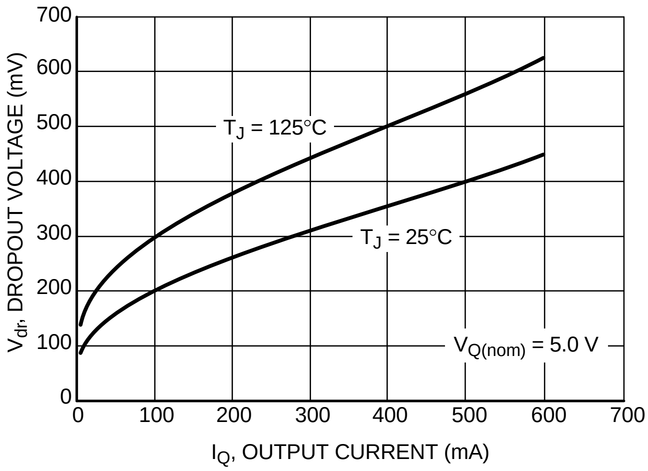


Figure 22. Drop Voltage V_{dr} vs. Output Current I_Q

APPLICATION INFORMATION

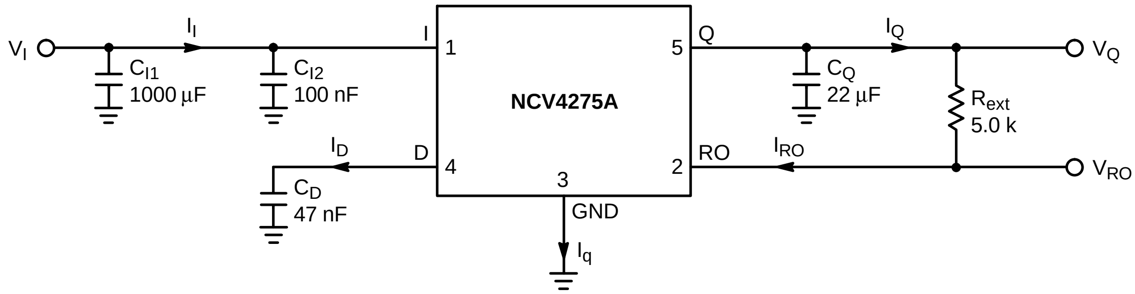


Figure 23. Test Circuit

Circuit Description

The NCV4275A is an integrated low dropout regulator that provides 5.0 V or 3.3 V, 450 mA protected output and a signal for power on reset. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible drop out voltage and best possible temperature stability. The output current capability is 450 mA, and the base drive quiescent current is controlled to prevent over saturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures. The delay time for the reset output is adjustable by selection of the timing capacitor. See Figure 23, Test Circuit, for circuit element nomenclature illustration.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_Q) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitors (C_{I1} and C_{I2}) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0 Ω in series with C_{I2} can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum, aluminum or ceramic capacitors can be used. The range of stability versus capacitance, load current and capacitive ESR is illustrated in Figures 2 to 5. Minimum ESR for C_Q = 22 µF is native ESR of ceramic capacitors. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the capacitance and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figure 23, Test Circuit, should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed for $C_Q \geq 22$ µF and an ESR ≤ 4.5 Ω (5.0 V Version), 3.5 Ω (3.3 V Version).

ESR characteristics were measured with ceramic capacitors and additional resistors to emulate ESR. Murata ceramic capacitors were used, GRM32ER71A226ME20 (22 µF, 10 V, X7R, 1210), GRM31MR71E105KA01 (1 µF, 25 V, X7R, 1206).

Reset Output

The reset output is used as the power on indicator to the microcontroller. This signal indicates when the output voltage is suitable for reliable operation of the controller. It pulls low when the output is not considered to be ready. RO is pulled up to V_Q by an external resistor, typically 5.0 kΩ in value. The input and output conditions that control the Reset Output and the relative timing are illustrated in Figure 24, Reset Timing.

Output voltage regulation must be maintained for the delay time before the reset output signals a valid condition. The delay for the reset output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0.0 V to the upper timing threshold voltage V_{DU}. The charging current for this is $I_{D,C}$ and D pin voltage in steady state is typically 3.2 V for 5.0 V regulator and typically 2.4 V for 3.3 V regulator. By using typical IC parameters with a 47 nF capacitor on the D pin, the following time delay for 5.0 V regulator is derived:

$$t_{RD} = C_D V_{DU} / I_{D,C}$$

$$t_{RD} = 47\ \text{nF}\ (1.8\ \text{V}) / 5.5\ \mu\text{A} = 15.4\ \text{ms}$$

Other time delays can be obtained by changing the capacitor value.

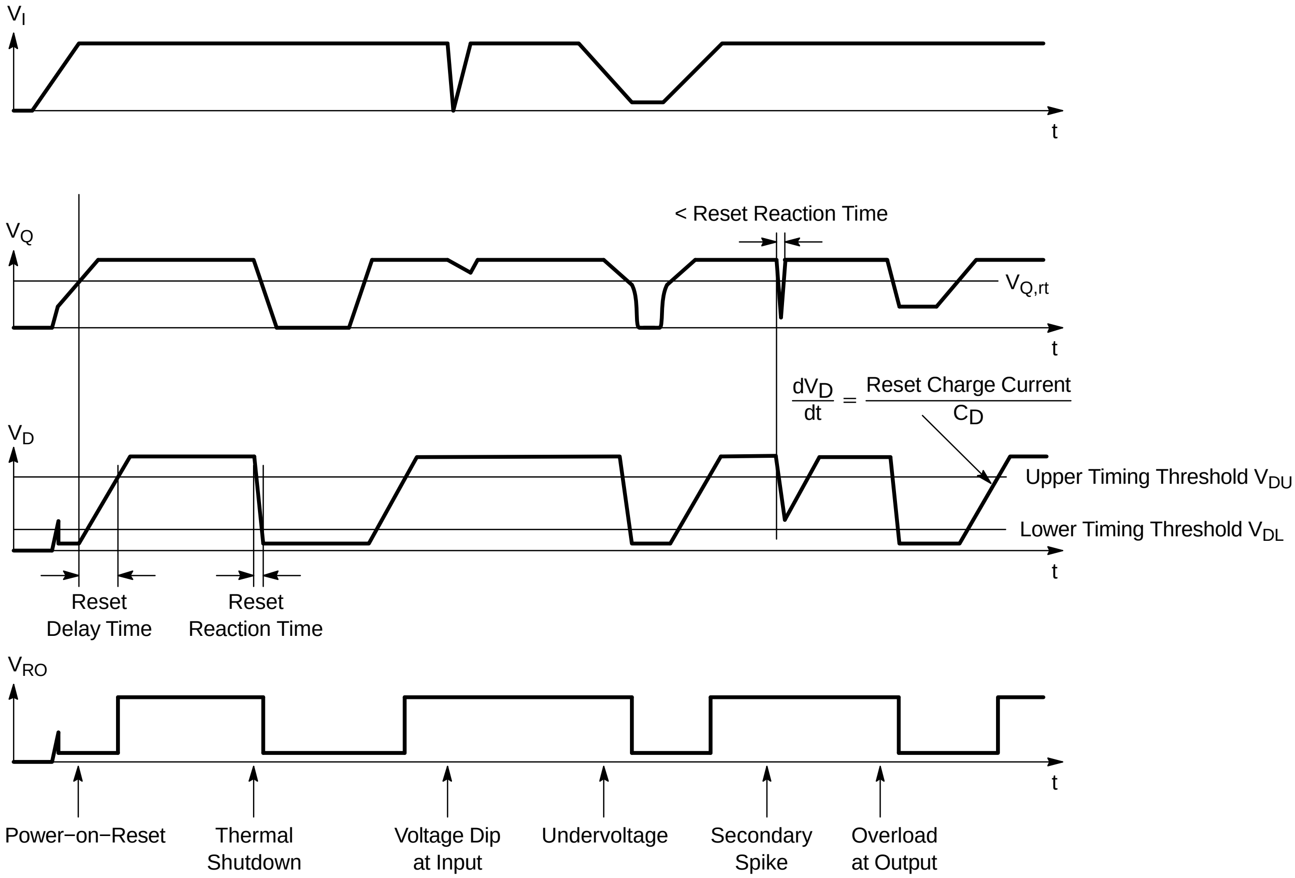


Figure 24. Reset Timing

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 25) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \quad (1)$$

where

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application,

I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

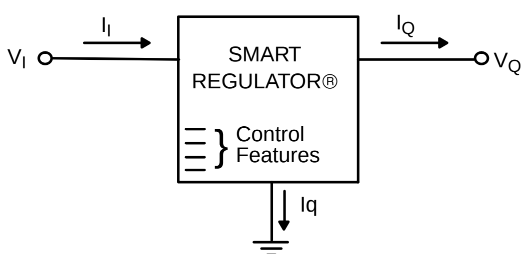


Figure 25. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

Thermal Model

A discussion of thermal modeling is in the ON Semiconductor web site: http://www.onsemi.com/pub/collateral/BR1487−D.PDF.

Table 1. DPAK 5−Lead Thermal RC Network Models

Drain Copper Area (1 oz thick)			**168 mm^2**	**736 mm^2**		**168 mm^2**	**736 mm^2**	
(SPICE Deck Format)			**Cauer Network**			**Foster Network**		
			168 mm^2	736 mm^2	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	1.00E−06	1.00E−06	W−s/C	1.36E−08	1.361E−08	sec
C_C2	**node1**	**Gnd**	1.00E−05	1.00E−05	W−s/C	7.41E−07	7.411E−07	sec
C_C3	**node2**	**Gnd**	6.00E−05	6.00E−05	W−s/C	1.04E−05	1.029E−05	sec
C_C4	**node3**	**Gnd**	1.00E−04	1.00E−04	W−s/C	3.91E−05	3.737E−05	sec
C_C5	**node4**	**Gnd**	4.36E−04	3.64E−04	W−s/C	1.80E−03	1.376E−03	sec
C_C6	node5	Gnd	6.77E−02	1.92E−02	W−s/C	3.77E−01	2.851E−02	sec
C_C7	node6	Gnd	1.51E−01	1.27E−01	W−s/C	3.79E+00	9.475E−01	sec
C_C8	node7	Gnd	4.80E−01	1.018	W−s/C	2.65E+01	1.173E+01	sec
C_C9	node8	Gnd	3.740	2.955	W−s/C	8.71E+01	8.59E+01	sec

(SPICE Deck Format)			Cauer Network			Foster Network		
C_C10	node9	Gnd	10.322	0.438	W−s/C			sec
			168 mm^2	736 mm^2		R's	R's	
R_R1	**Junction**	**node1**	0.015	0.015	C/W	0.0123	0.0123	C/W
R_R2	**node1**	**node2**	0.08	0.08	C/W	0.0585	0.0585	C/W
R_R3	**node2**	**node3**	0.4	0.4	C/W	0.0304	0.0287	C/W
R_R4	**node3**	**node4**	0.2	0.2	C/W	0.3997	0.3772	C/W
R_R5	**node4**	**node5**	2.97519	2.6171	C/W	3.115	2.68	C/W
R_R6	node5	node6	8.2971	1.6778	C/W	3.571	1.38	C/W
R_R7	node6	node7	25.9805	7.4246	C/W	12.851	5.92	C/W
R_R8	node7	node8	46.5192	14.9320	C/W	35.471	7.39	C/W
R_R9	node8	node9	17.7808	19.2560	C/W	46.741	28.94	C/W
R_R10	node9	Gnd	0.1	0.1758	C/W			C/W

NOTE: Bold face items represent the package without the external thermal system.

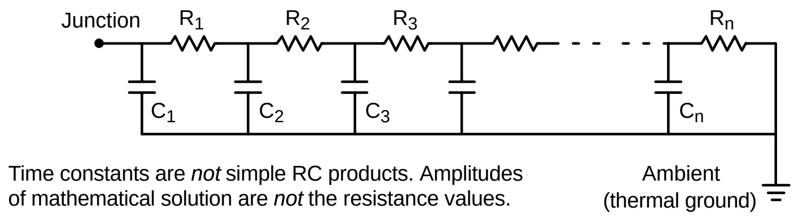


Figure 26. Grounded Capacitor Thermal Network (“Cauer” Ladder)

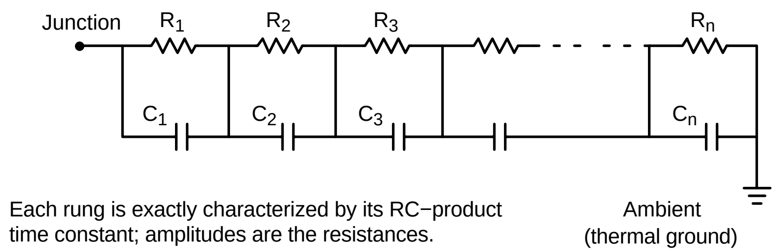


Figure 27. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

Table 2. D2PAK 5−Lead Thermal RC Network Models

Drain Copper Area (1 oz thick)			241 mm^2	788 mm^2		241 mm^2	788 mm^2	
(SPICE Deck Format)			Cauer Network			Foster Network		
			241 mm^2	653 mm^2	Units	Tau	Tau	Units
C_C1	**Junction**	**Gnd**	1.00E−06	1.00E−06	W−s/C	1.361E−08	1.361E−08	sec
C_C2	**node1**	**Gnd**	1.00E−05	1.00E−05	W−s/C	7.411E−07	7.411E−07	sec
C_C3	**node2**	**Gnd**	6.00E−05	6.00E−05	W−s/C	1.005E−05	1.007E−05	sec
C_C4	**node3**	**Gnd**	1.00E−04	1.00E−04	W−s/C	3.460E−05	3.480E−05	sec
C_C5	**node4**	**Gnd**	2.82E−04	2.87E−04	W−s/C	7.868E−04	8.107E−04	sec
C_C6	node5	Gnd	5.58E−03	5.95E−03	W−s/C	7.431E−03	7.830E−03	sec
C_C7	node6	Gnd	4.25E−01	4.61E−01	W−s/C	2.786E+00	2.012E+00	sec
C_C8	node7	Gnd	9.22E−01	2.05	W−s/C	2.014E+01	2.601E+01	sec
C_C9	node8	Gnd	1.73	4.88	W−s/C	1.134E+02	1.218E+02	sec
C_C10	node9	Gnd	7.12	1.31	W−s/C			sec
			241 mm^2	653 mm^2		R’s	R’s	
R_R1	**Junction**	**node1**	0.015	0.0150	C/W	0.0123	0.0123	C/W
R_R2	**node1**	**node2**	0.08	0.0800	C/W	0.0585	0.0585	C/W
R_R3	**node2**	**node3**	0.4	0.4000	C/W	0.0257	0.0260	C/W
R_R4	**node3**	**node4**	0.2	0.2000	C/W	0.3413	0.3438	C/W
R_R5	**node4**	**node5**	1.85638	1.8839	C/W	1.77	1.81	C/W
R_R6	node5	node6	1.23672	1.2272	C/W	1.54	1.52	C/W
R_R7	node6	node7	9.81541	5.3383	C/W	4.13	3.46	C/W
R_R8	node7	node8	33.1868	18.9591	C/W	6.27	5.03	C/W
R_R9	node8	node9	27.0263	13.3369	C/W	60.80	29.30	C/W
R_R10	node9	gnd	1.13944	0.1191	C/W			C/W

NOTE: Bold face items represent the package without the external thermal system.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

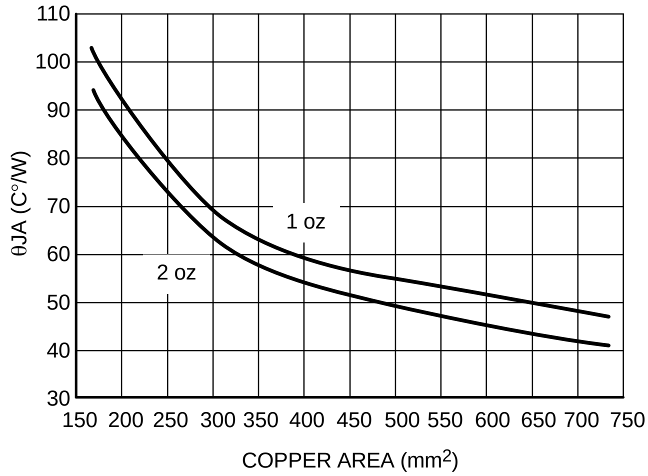


Figure 28. θJA vs. Copper Spreader Area, DPAK 5−Lead

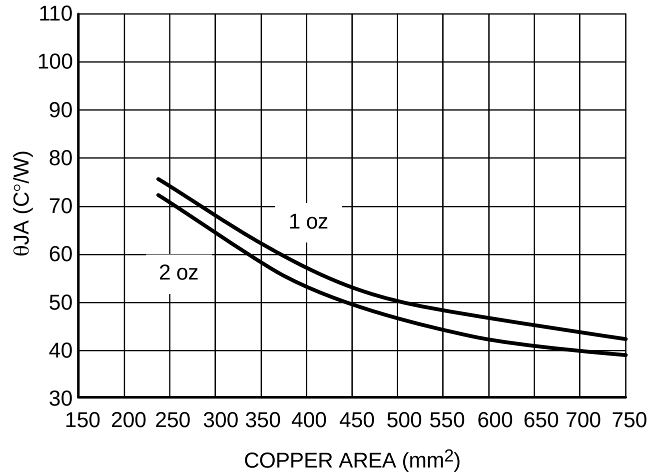


Figure 29. θJA vs. Copper Spreader Area, D^2PAK 5−Lead

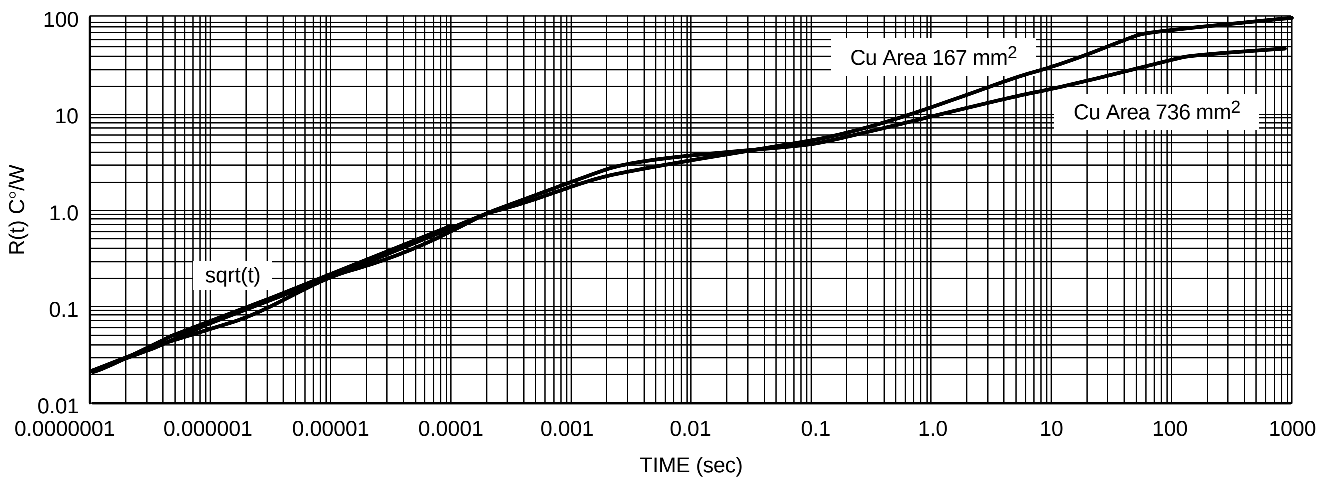


Figure 30. Single−Pulse Heating Curves, DPAK 5−Lead

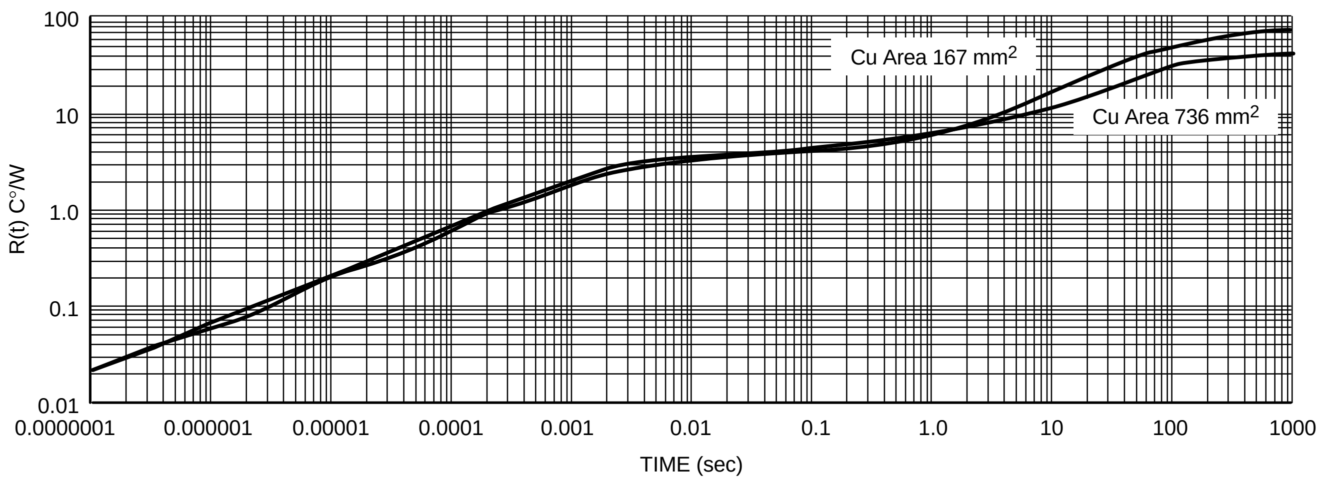


Figure 31. Single−Pulse Heating Curves, D^2PAK 5−Lead

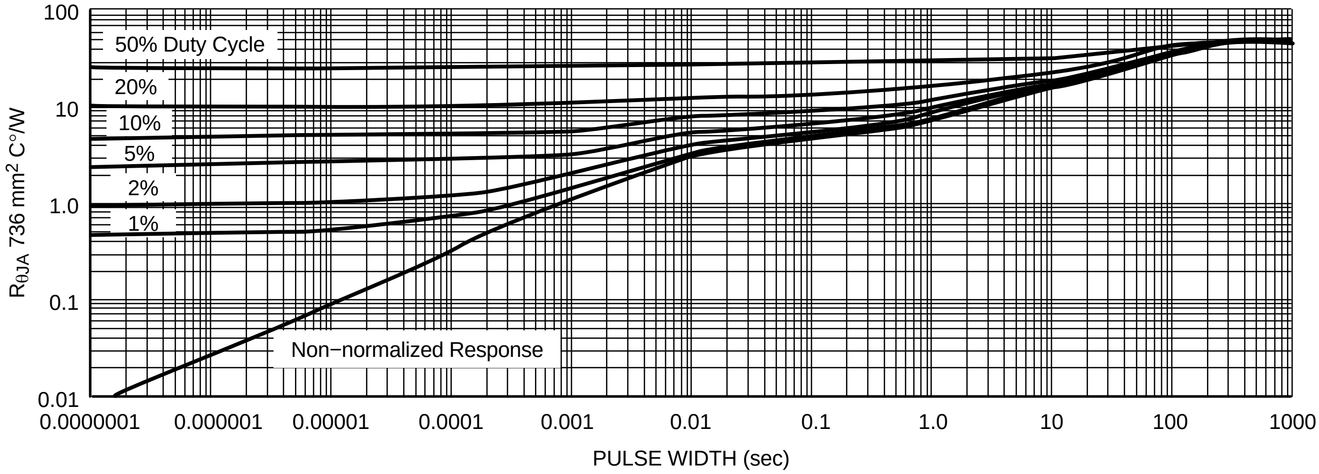


Figure 32. Duty Cycle for 1” Spreader Boards, DPAK 5−Lead

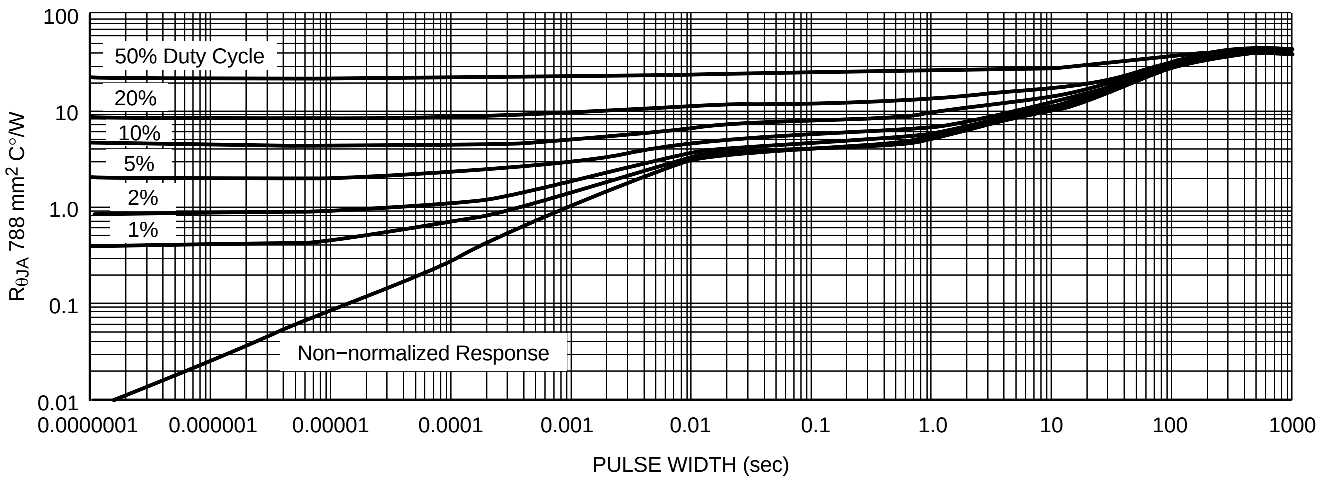


Figure 33. Duty Cycle for 1” Spreader Boards, D²PAK 5−Lead

EMC−Characteristics: Conducted Susceptibility

All EMC−Characteristics are based on limited samples and no part of production test according to 47A/658/CD IEC62132−4 (direct Power Injection).

Test Conditions

Supply Voltage V_{in} = 12 V
Temperature T_A = 23°C ±5°C
Load R_L = 100 Ω

Direct Power Injection

33 dBm (Note 1) forward power CW for global pin (Note 2)

17 dBm (Note 1) forward power CW for local pin (Note 3)

Acceptance Criteria

Amplitude Dev. max 4% of Output Voltage
Reset outputs remain in correct state ±1 V

1. dBm means dB mili−Watts, P(dBm) = 10 log (P(mW)).
2. A global pin carries a signal or power which enters or leaves the application board.
3. A local pin carries a signal or power which does not leave the application board. It remains on the application board as a signal between two components.

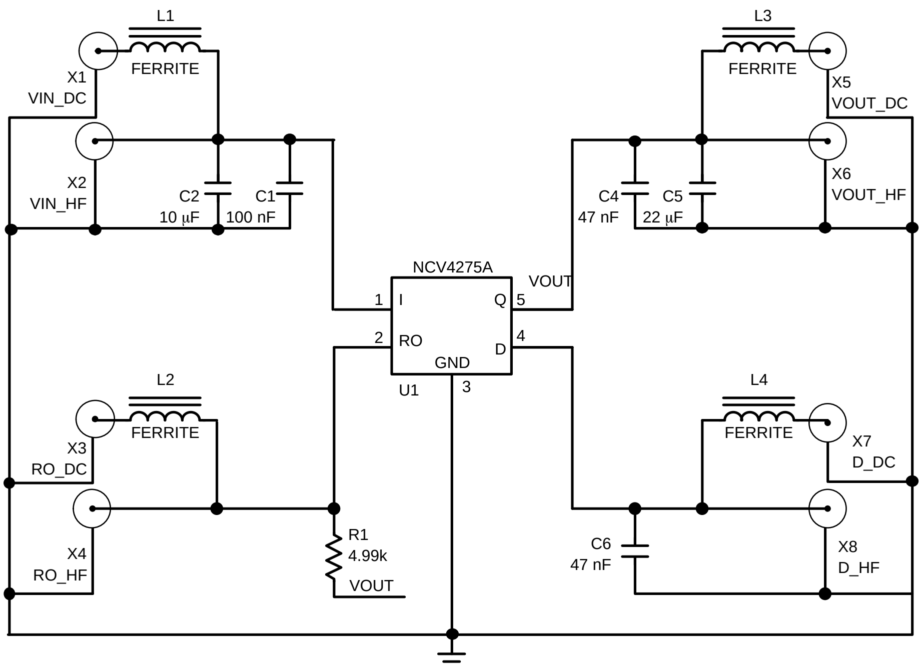


Figure 34. Test Circuit

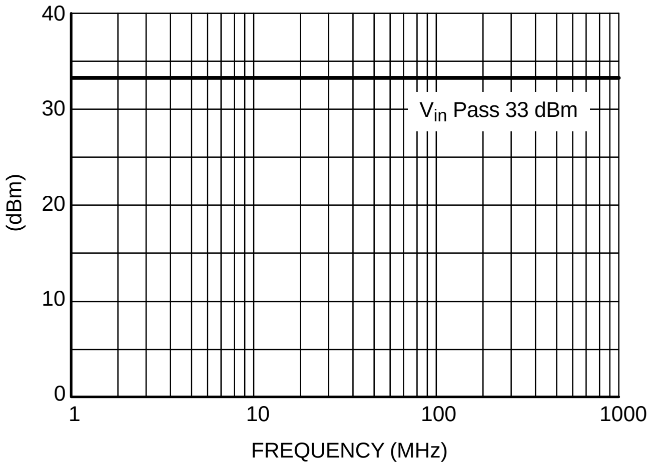


Figure 35. Typical V_{in} Pin Susceptibility

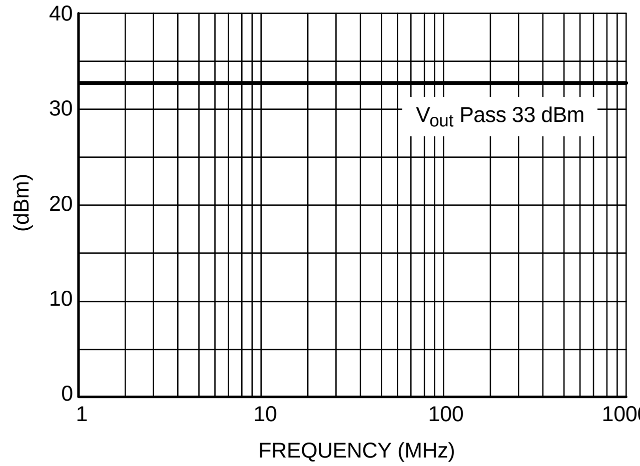


Figure 36. Typical V_{out} Pin Susceptibility

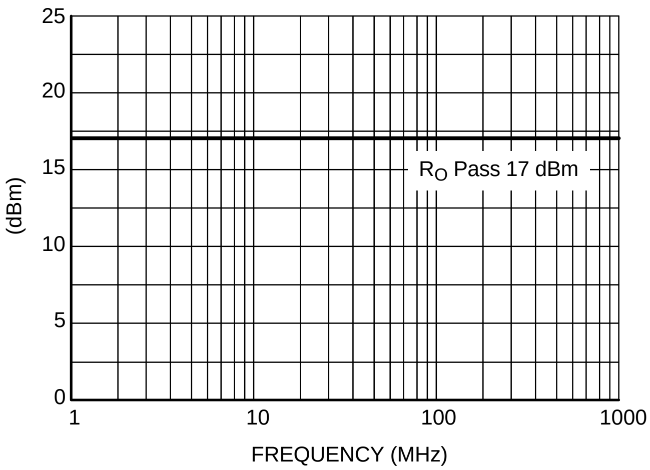


Figure 37. Typical R_O Pin Susceptibility

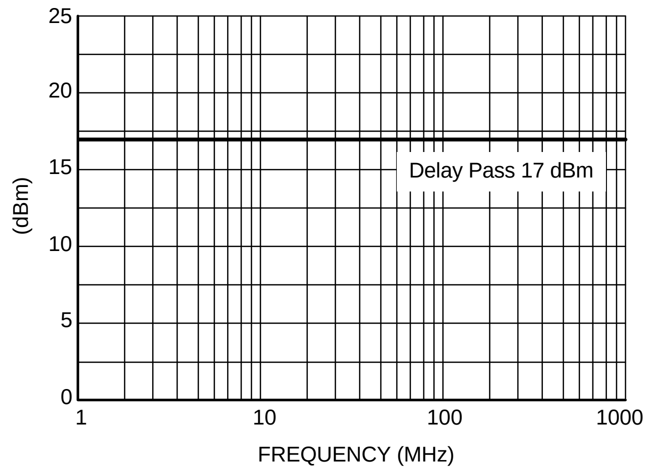
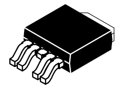


Figure 38. Typical Delay Pin Susceptibility

ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV4275ADS50G	5.0 V	D^2PAK (Pb−Free)	50 Units/Rail
NCV4275ADS50R4G			800 Tape & Reel
NCV4275ADT50RKG		DPAK (Pb−Free)	2500 Tape & Reel
NCV4275ADS33G	3.3 V	D^2PAK (Pb−Free)	50 Units/Rail
NCV4275ADS33R4G			800 Tape & Reel
NCV4275ADT33RKG		DPAK (Pb−Free)	2500 Tape & Reel

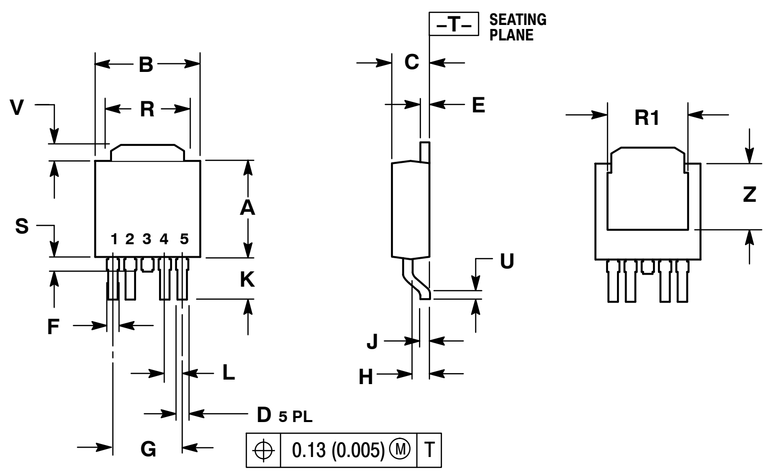
†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

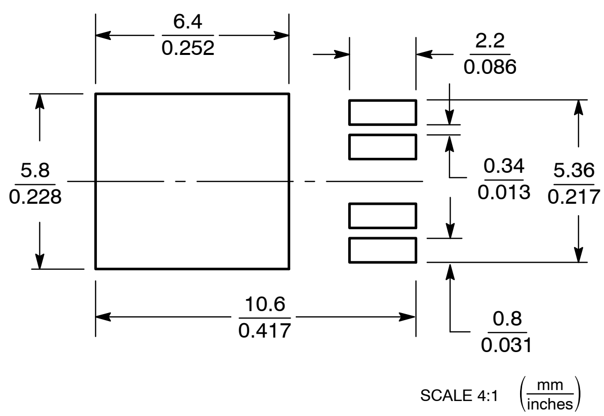
DATE 15 MAY 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

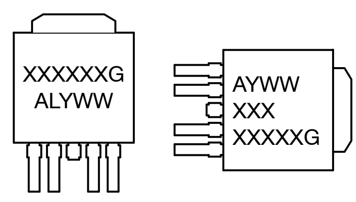
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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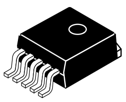
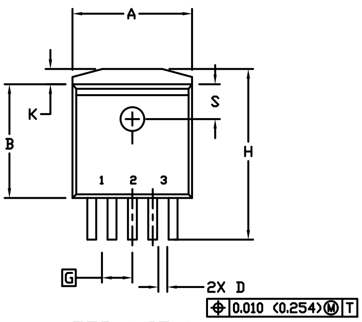


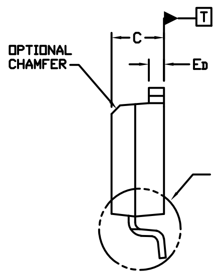
SCALE 1:1

D²PAK 5−LEAD
CASE 936A−02
ISSUE E

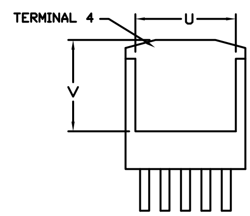
DATE 28 JUL 2021



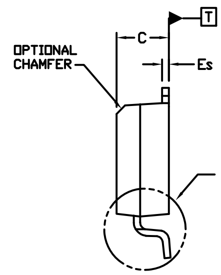
TOP VIEW



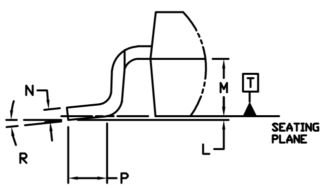
SIDE VIEW
DUAL GUAGE CONSTRUCTION



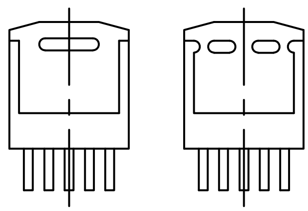
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW

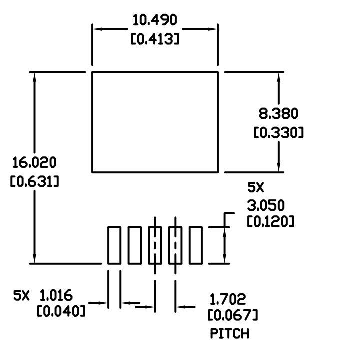


BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

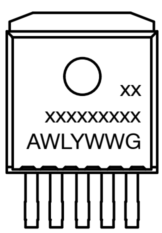
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



xxxxxx	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D2PAK 5−LEAD**	**PAGE 1 OF 1**

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