OPAx192-Q1 36-V, Precision, Rail-to-Rail Input/Output, Low-Offset Voltage, Low-Input Bias Current Op Amp With e-trim™

ADVANCE INFORMATION

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device Human Body Model (HBM) Electrostatic Discharge (ESD) Classification Level 3A
  - Device Charged Device Model (CDM) ESD Classification Level C3
- Low Offset Voltage: ±5 µV
- Low Offset Voltage Drift: ±0.2 µV/°C
- Low Noise: 5.5 nV/√Hz at 1 kHz
- High Common-Mode Rejection: 140 dB
- Low Bias Current: ±5 pA
- Rail-to-Rail Input and Output
- Wide Bandwidth: 10 MHz GBW
- High Slew Rate: 20 V/µs
- Low Quiescent Current: 1 mA per Amplifier
- Wide Supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- EMI/RFI Filtered Inputs
- Differential Input Voltage Range to Supply Rail
- High Capacitive Load Drive Capability: 1 nF
- Industry-Standard Packages:
  - Single Channel in Very Small VSSOP-8
  - Dual Channel in VSSOP-8
  - Quad Channel in SOIC -14

2 Applications

- Motor Control for Automotive
- Traction Inverter
- On Board Charger
- Precision Current Sensing

3 Description

The OPAx192-Q1 family (OPA192-Q1, OPA2192-Q1, and OPA4192-Q1) is a new generation of 36-V, e-trim operational amplifiers. The OPAx192-Q1 family of operational amplifiers use e-trim™, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding.

These devices offer outstanding dc precision and ac performance, including rail-to-rail input/output, low offset (±5 µV, typical), low offset drift (±0.2 µV/°C, typical), and 10-MHz bandwidth.

Unique features such as differential input-voltage range to the supply rail, high output current (±65 mA), high capacitive load drive of up to 1 nF, and high slew rate (20 V/µs) make the OPAx192-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

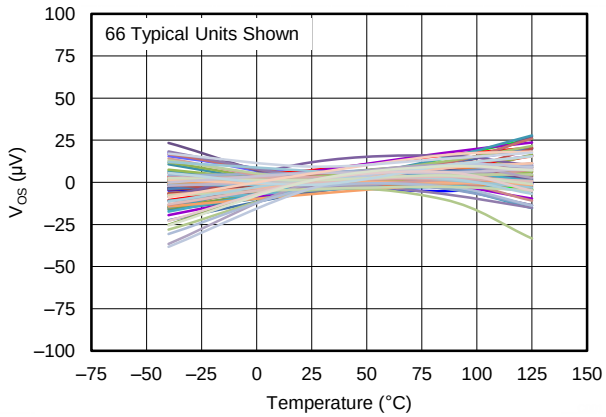
The OPAx192-Q1 family of op amps is available in standard packages and is specified from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA192-Q1	VSSOP (8)	3.00 mm × 3.00 mm
OPA2192-Q1	VSSOP (8)	3.00 mm × 3.00 mm
OPA4192-Q1	SOIC (14)	8.65 mm × 3.90 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

OPAx192-Q1 Maintains Ultra-Low Input Offset Voltage Over Temperature



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information: OPA192-Q1 ... 6
6.5 Thermal Information: OPA2192-Q1 ... 6
6.6 Thermal Information: OPA4192-Q1 ... 6
6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) ... 7
6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) ... 9
6.9 Typical Characteristics ... 11
6.10 Typical Characteristics ... 12
7 Parameter Measurement Information ... 20
7.1 Input Offset Voltage Drift ... 20
8 Detailed Description ... 23
8.1 Overview ... 23
8.2 Functional Block Diagram ... 23
8.3 Feature Description ... 24
8.4 Device Functional Modes ... 30
9 Application and Implementation ... 31
9.1 Application Information ... 31
9.2 Typical Applications ... 31
10 Power-Supply Recommendations ... 35
11 Layout ... 35
11.1 Layout Guidelines ... 35
11.2 Layout Example ... 36
12 Device and Documentation Support ... 37
12.1 Device Support ... 37
12.2 Related Links ... 37
12.3 Receiving Notification of Documentation Updates 37
12.4 Community Resources ... 37
12.5 Trademarks ... 37
12.6 Electrostatic Discharge Caution ... 38
12.7 Glossary ... 38
13 Mechanical, Packaging, and Orderable Information ... 38

ADVANCE INFORMATION

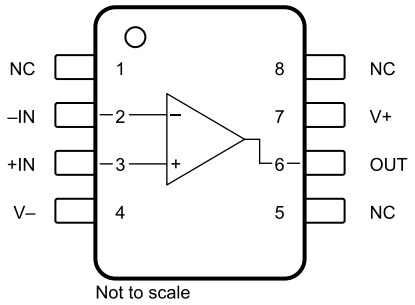
4 Revision History

DATE	REVISION	NOTES
May 2017	*	Initial release.

Copyright © 2017, Texas Instruments Incorporated

5 Pin Configuration and Functions

OPA192-Q1 DGK Package
8-Pin VSSOP
Top View



NC – No internal connection.

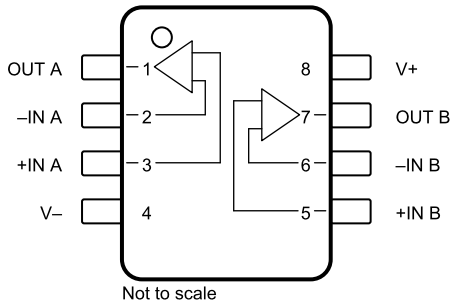
Pin Functions: OPA192-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	2	I	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	O	Output
V+	7	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

ADVANCE INFORMATION

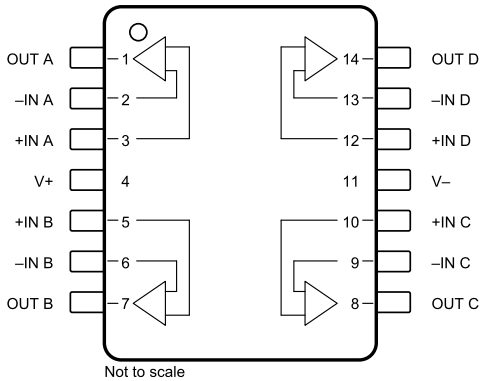
Copyright © 2017, Texas Instruments Incorporated

OPA2192-Q1 DGK Package
8-Pin VSSOP
Top View



Not to scale

OPA4192-Q1 D Package
14-Pin SOIC
Top View



Not to scale

Pin Functions: OPA2192-Q1 and OPA4192-Q1

PIN			I/O	DESCRIPTION
NAME	OPA2192-Q1	OPA4192-Q1		
	DGK (VSSOP)	D (SOIC)		
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	—	10	I	Noninverting input, channel C
+IN D	—	12	I	Noninverting input, channel D
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	—	9	I	Inverting input,,channel C
–IN D	—	13	I	Inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	—	8	O	Output, channel C
OUT D	—	14	O	Output, channel D
V+	8	4	—	Positive (highest) power supply
V–	4	11	—	Negative (lowest) power supply

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				±20 (40, single-supply)	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit[2]				Continuous	
Latch-up per JESD78D				Class 1	
Temperature	Operating range		–55	150	°C
	Junction			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
OPA192-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	
OPA2192-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	
OPA4192-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		+125	°C

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

6.4 Thermal Information: OPA192-Q1

THERMAL METRIC(1)		OPA192-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2192-Q1

THERMAL METRIC(1)		OPA2192-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4192-Q1

THERMAL METRIC(1)		OPA4192-Q1 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

6.7 Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±5	±25	µV
		T_A = 0°C to 85°C			±8	±50	
		T_A = –40°C to 125°C			±10	±75	
		V_{CM} = (V+) – 1.5 V			±10	±40	
			T_A = 0°C to 85°C		±25	±150	
			T_A = –40°C to 125°C		±50	±250	
dV_{OS}/dT	Input offset voltage drift	D packages only	T_A = 0°C to 85°C		±0.1	±0.5	µV/°C
			T_A = –40°C to 125°C		±0.15	±0.8	
		DBV, DGK, and PW packages only	T_A = 0°C to 85°C		±0.1	±0.8	
			T_A = –40°C to 125°C		±0.2	±1.0	
PSRR	Power-supply rejection ratio	T_A = –40°C to 125°C			±0.3	±1.0	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to 125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to 125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 0.1 Hz to 10 Hz		1.30		$µV_{PP}$
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 0.1 Hz to 10 Hz		4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		$nV/\sqrt{Hz}$
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
NOISE (continued)							
i_n	Input current noise density	f = 1 kHz			1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		120	140		dB
			T_A = –40°C to 125°C	114	126		
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to 125°C	86	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		120	134		dB
			T_A = –40°C to 125°C	114	126		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		126	140		
			T_A = –40°C to 125°C	120	134		

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±18 V, G = 1, 10-V step		1.4		µs
			V_S = ±18 V, G = 1, 5-V step		0.9		
		To 0.001%	V_S = ±18 V, G = 1, 10-V step		2.1		
			V_S = ±18 V, G = 1, 5-V step		1.8		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			200		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00008%		
	Crosstalk	OPA2192-Q1 and OPA4192-Q1, at dc			150		dB
		OPA2192-Q1 and OPA4192-Q1, f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive			See *Typical Characteristics*			
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A; see Figure 31			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
		T_A = –40°C to 125°C, I_O = 0 A				1.5	
TEMPERATURE							
	Thermal protection(1)				140		°C

(1) For a detailed description of thermal protection, see *Thermal Protection* .

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

6.8 Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = (V+) – 3 V			±5	±25	µV
			T_A = 0°C to 85°C		±8	±50	
			T_A = –40°C to 125°C		±10	±75	
		(V+) – 3.5 V < V_{CM} < (V+) – 1.5 V			See *Common-Mode Voltage Range*		
		V_{CM} = (V+) – 1.5 V			±10	±40	µV
			T_A = 0°C to 85°C		±25	±150	
			T_A = –40°C to 125°C		±50	±250	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = (V+) – 3 V D packages only	T_A = 0°C to 85°C		±0.1	±0.5	µV/°C
			T_A = –40°C to 125°C		±0.15	±0.8	
		V_{CM} = (V+) – 3 V DBV, DGK, and PW packages only	T_A = 0°C to 85°C		±0.1	±0.8	
			T_A = –40°C to 125°C		±0.2	±1.1	
		V_{CM} = (V+) – 1.5 V, T_A = –40°C to 125°C			±0.5	±3	
PSRR	Power-supply rejection ratio	T_A = –40°C to 125°C, V_{CM} = V_S / 2 – 0.75 V			±1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±5	±20	pA
		T_A = –40°C to 125°C				±5	nA
I_{OS}	Input offset current				±2	±20	pA
		T_A = –40°C to 125°C				±2	nA
NOISE							
E_n	Input voltage noise	(V–) – 0.1 V < V_{CM} < (V+) – 3 V, f = 0.1 Hz to 10 Hz			1.30		μV_{PP}
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V, f = 0.1 Hz to 10 Hz			4		
e_n	Input voltage noise density	(V–) – 0.1 V < V_{CM} < (V+) – 3 V	f = 100 Hz		10.5		$nV/\sqrt{Hz}$
			f = 1 kHz		5.5		
		(V+) – 1.5 V < V_{CM} < (V+) + 0.1 V	f = 100 Hz		32		
			f = 1 kHz		12.5		
i_n	Input current noise density		f = 1 kHz		1.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) – 3 V		94	110		dB
			T_A = –40°C to 125°C	90	104		
		(V+) – 1.5 V < V_{CM} < (V+)		100	120		
			T_A = –40°C to 125°C	84	100		
		(V+) – 3 V < V_{CM} < (V+) – 1.5 V		See *Typical Characteristics*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 1.6		MΩ || pF
Z_{IC}	Common-mode				1 || 6.4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, R_{LOAD} = 2 kΩ		110	120		dB
			T_A = –40°C to 125°C	100	114		
		(V–) + 0.3 V < V_O < (V+) – 0.3 V, R_{LOAD} = 10 kΩ		110	126		
			T_A = –40°C to 125°C	110	120		

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V) (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				10		MHz
SR	Slew rate	G = 1, 10-V step			20		V/µs
t_s	Settling time	To 0.01%	V_S = ±3 V, G = 1, 5-V step		1		µs
t_{OR}	Overload recovery time	V_{IN}× G = V_S			200		ns
	Crosstalk	OPA2192-Q1 and OPA4192-Q1, at dc			150		dB
		OPA2192-Q1 and OPA4192-Q1, f = 100 kHz			130		
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		5	15	mV
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		95	110	
			R_{LOAD} = 2 kΩ		430	500	
I_{SC}	Short-circuit current				±65		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A; see Figure 31			375		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			1	1.2	mA
			T_A = –40°C to 125°C			1.5	
TEMPERATURE							
	Thermal protection(1)				140		°C

(1) For a detailed description of thermal protection, see *Thermal Protection* .

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

6.9 Typical Characteristics

Table 1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1 to Figure 6
Offset Voltage Drift Distribution	Figure 7 to Figure 10
Offset Voltage vs Temperature	Figure 11
Offset Voltage vs Common-Mode Voltage	Figure 12 to Figure 14
Offset Voltage vs Power Supply	Figure 15
Open-Loop Gain and Phase vs Frequency	Figure 16
Closed-Loop Gain and Phase vs Frequency	Figure 17
Input Bias Current vs Common-Mode Voltage	Figure 18
Input Bias Current vs Temperature	Figure 19
Output Voltage Swing vs Output Current (maximum supply)	Figure 20
CMRR and PSRR vs Frequency	Figure 21
CMRR vs Temperature	Figure 22
PSRR vs Temperature	Figure 23
0.1-Hz to 10-Hz Noise	Figure 24
Input Voltage Noise Spectral Density vs Frequency	Figure 25
THD+N Ratio vs Frequency	Figure 26
THD+N vs Output Amplitude	Figure 27
Quiescent Current vs Supply Voltage	Figure 28
Quiescent Current vs Temperature	Figure 29
Open Loop Gain vs Temperature	Figure 30
Open Loop Output Impedance vs Frequency	Figure 31
Small Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 32, Figure 33
No Phase Reversal	Figure 34
Positive Overload Recovery	Figure 35
Negative Overload Recovery	Figure 36
Small-Signal Step Response (100 mV)	Figure 37, Figure 38
Large-Signal Step Response	Figure 39
Settling Time	Figure 40 to Figure 43
Short-Circuit Current vs Temperature	Figure 44
Maximum Output Voltage vs Frequency	Figure 45
Propagation Delay Rising Edge	Figure 46
Propagation Delay Falling Edge	Figure 47
Crosstalk vs Frequency	Figure 48

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

6.10 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

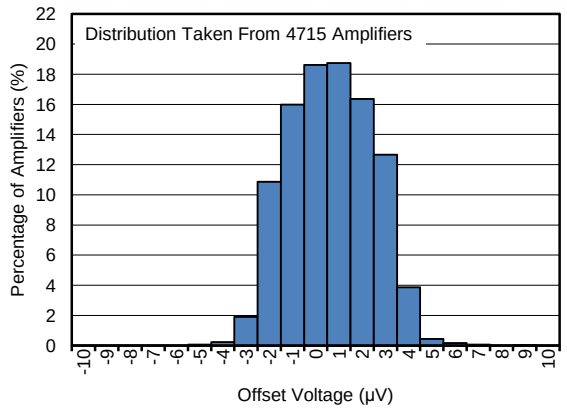
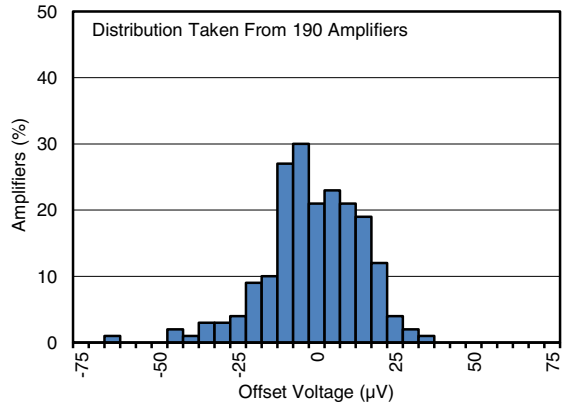
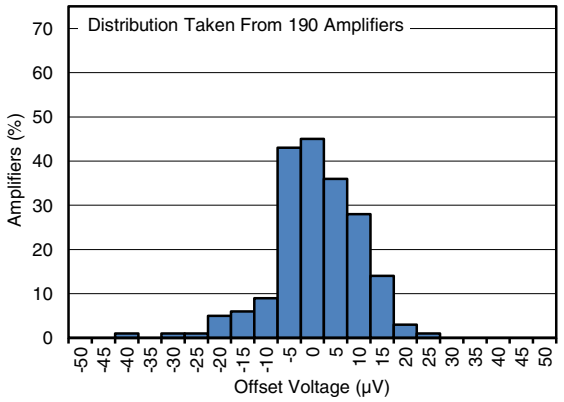


Figure 1. Offset Voltage Production Distribution at 25°C



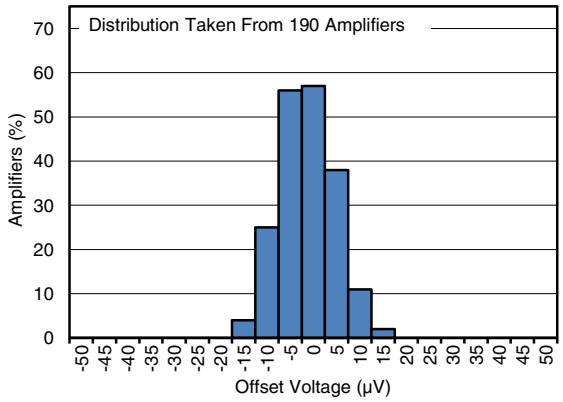
T_A = 125°C

Figure 2. Offset Voltage Production Distribution at 125°C



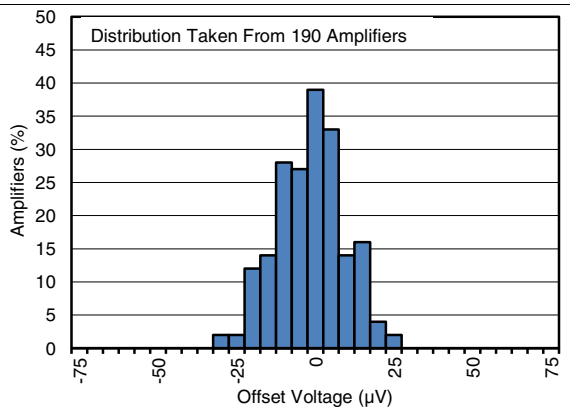
T_A = 85°C

Figure 3. Offset Voltage Production Distribution at 85°C



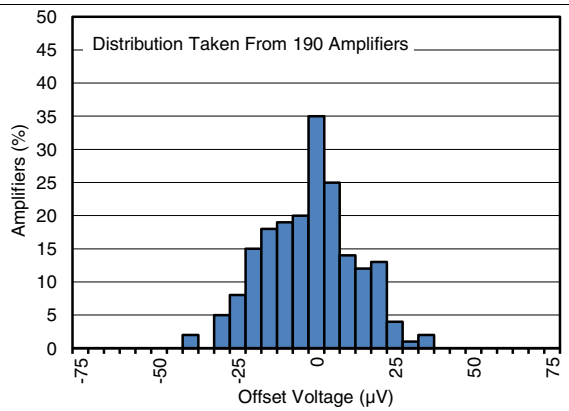
T_A = 0°C

Figure 4. Offset Voltage Production Distribution at 0°C



T_A = –25°C

Figure 5. Offset Voltage Production Distribution at –25°C



T_A = –40° C

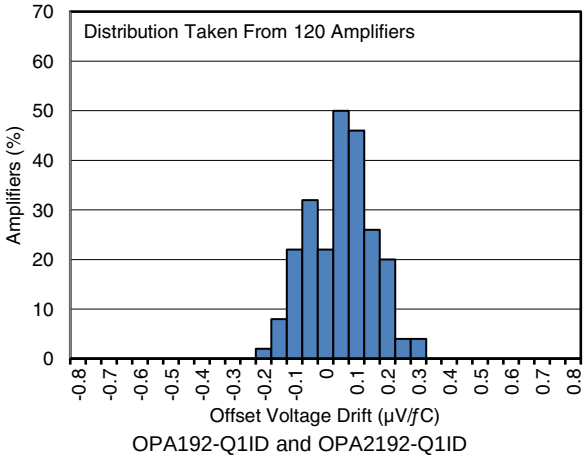
Figure 6. Offset Voltage Production Distribution at –40°C

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

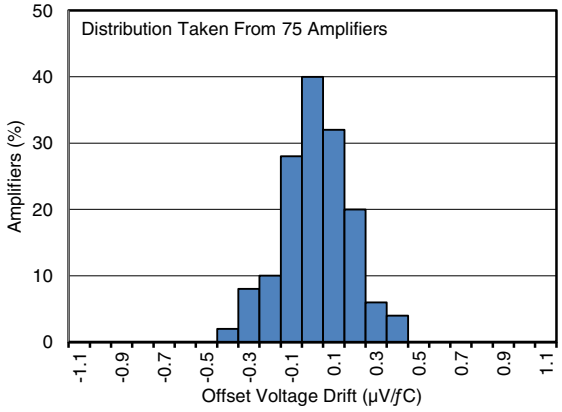
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)



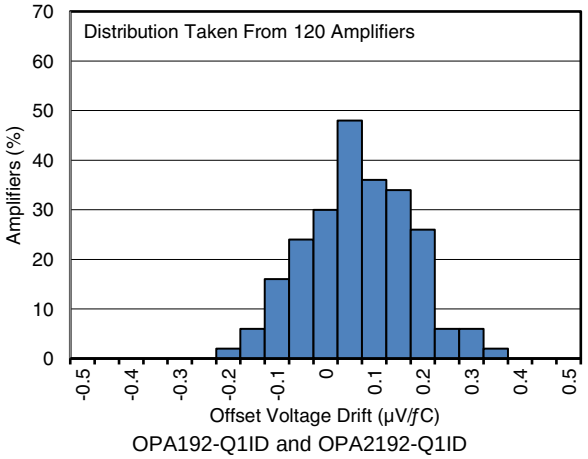
OPA192-Q1ID and OPA2192-Q1ID
SOIC, T_A = –40°C to +125°C

Figure 7. Offset Voltage Drift Distribution from –40°C to +125°C



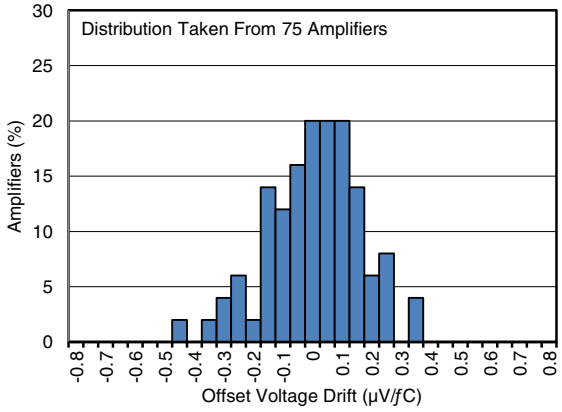
OPA192-Q1IDBV, OPA192-Q1IDGK, OPA2192-Q1IDGK, OPA4192-Q1IPW
SOT and VSSOP, T_A = –40°C to +125°C

Figure 8. Offset Voltage Drift Distribution from –40°C to +125°C



OPA192-Q1ID and OPA2192-Q1ID
SOIC, T_A = 0°C to 85°C

Figure 9. Offset Voltage Drift Distribution from 0°C to 85°C



OPA192-Q1IDBV, OPA192-Q1IDGK, OPA2192-Q1IDGK, OPA4192-Q1IPW
SOT and VSSOP, T_A = 0°C to 85°C

Figure 10. Offset Voltage Drift Distribution from 0°C to 85°C

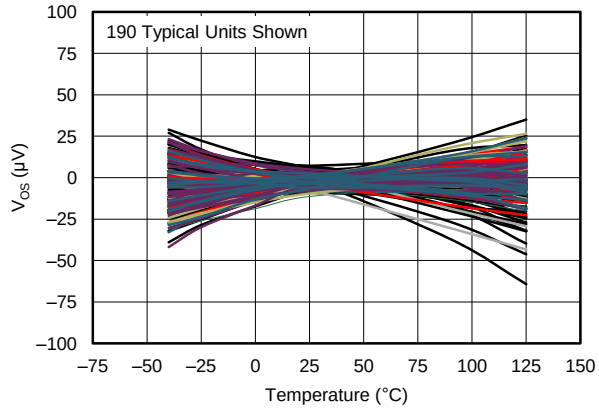


Figure 11. Offset Voltage vs Temperature

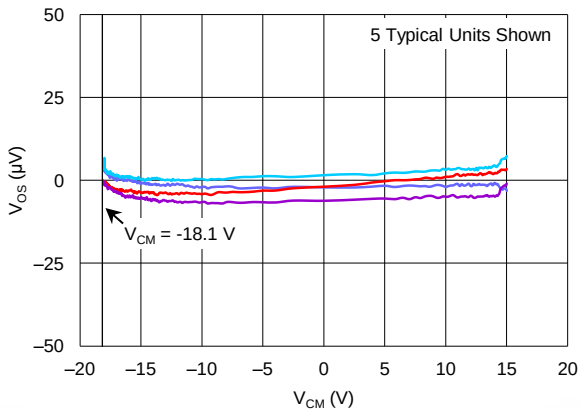


Figure 12. Offset Voltage vs Common-Mode Voltage

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

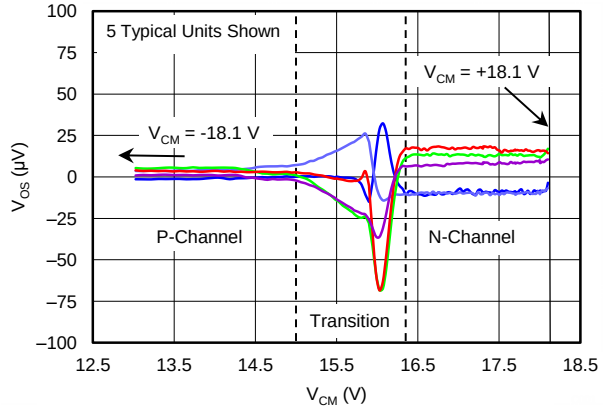


Figure 13. Offset Voltage vs Common-Mode Voltage

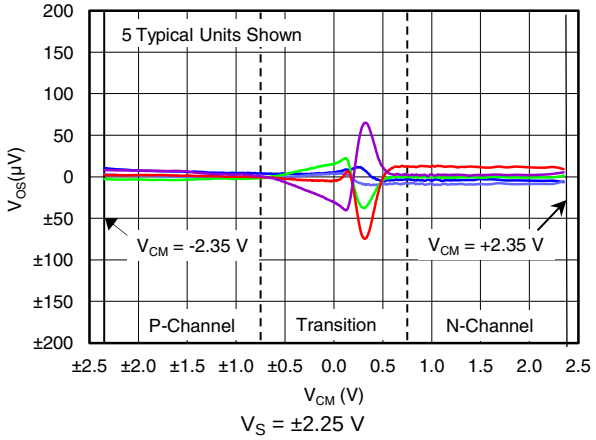


Figure 14. Offset Voltage vs Common-Mode Voltage

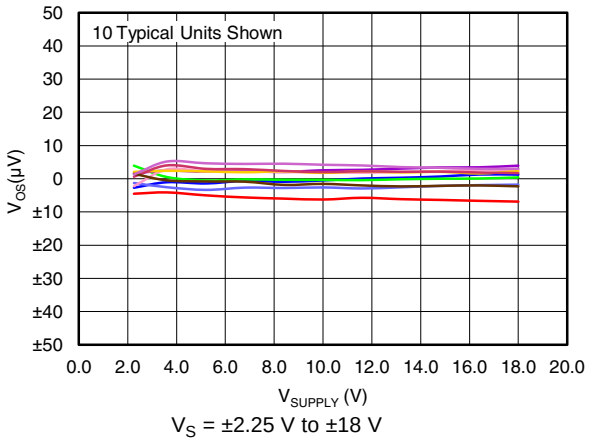


Figure 15. Offset Voltage vs Power Supply

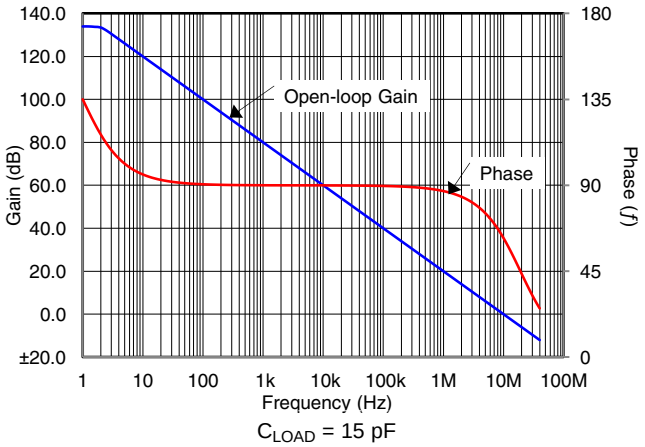


Figure 16. Open-Loop Gain and Phase vs Frequency

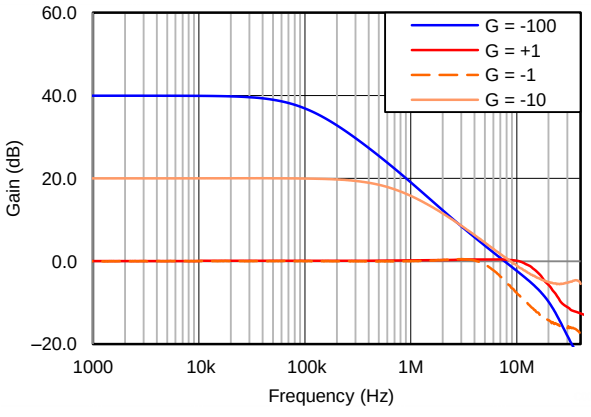


Figure 17. Closed-Loop Gain and Phase vs Frequency

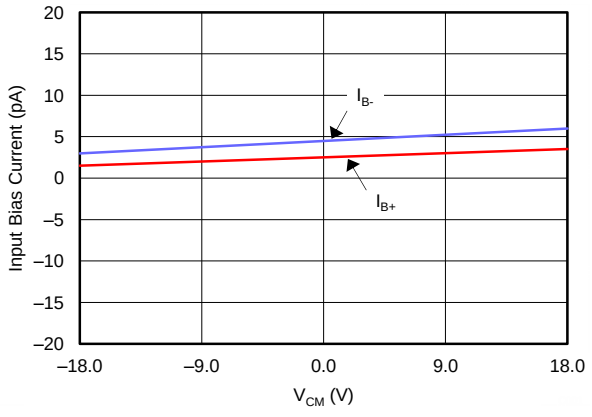


Figure 18. Input Bias Current vs Common-Mode Voltage

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

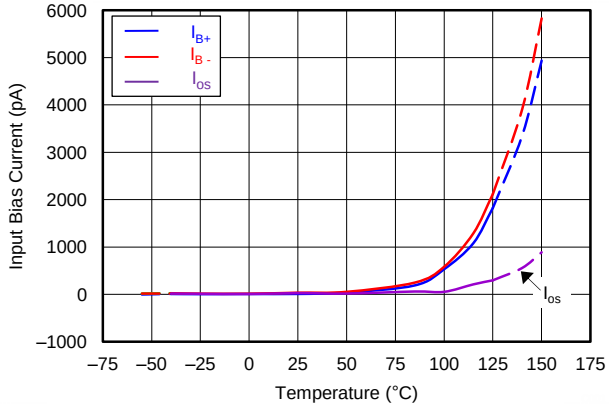


Figure 19. Input Bias Current vs Temperature

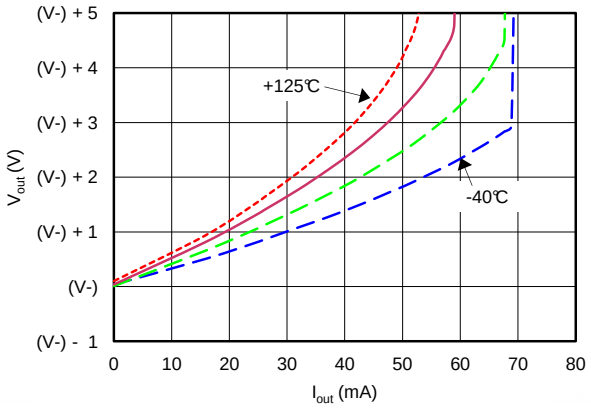


Figure 20. Output Voltage Swing vs Output Current (Maximum Supply)

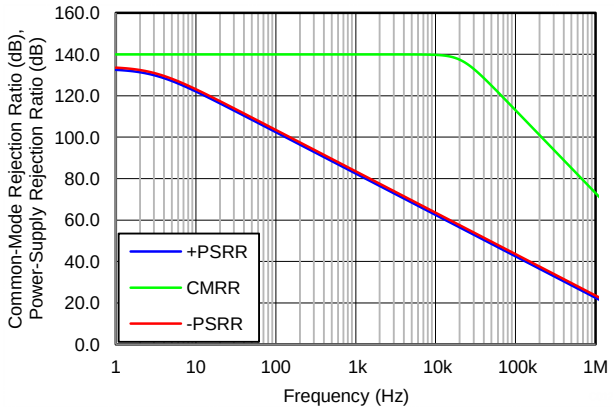


Figure 21. CMRR and PSRR vs Frequency

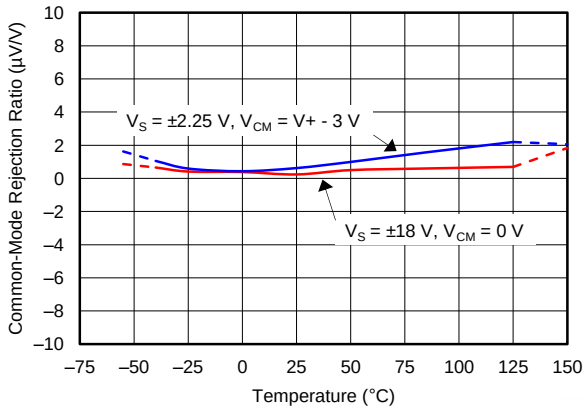


Figure 22. CMRR vs Temperature

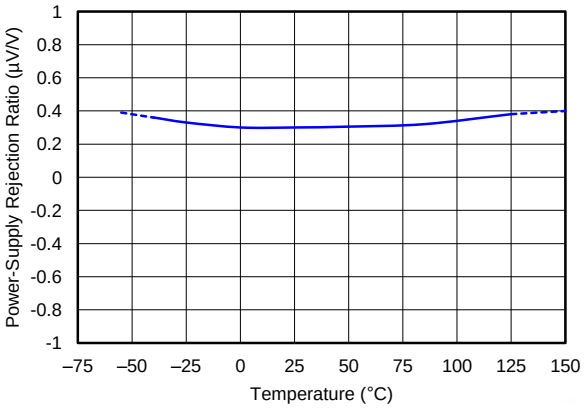


Figure 23. PSRR vs Temperature

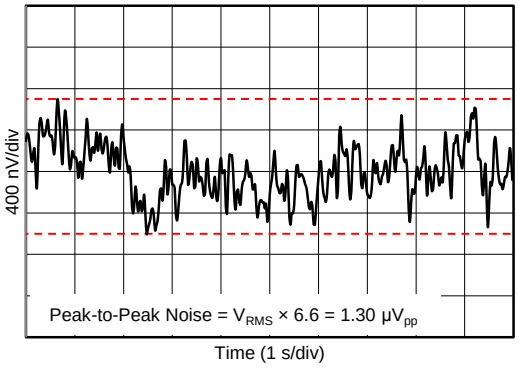


Figure 24. 0.1-Hz to 10-Hz Noise

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

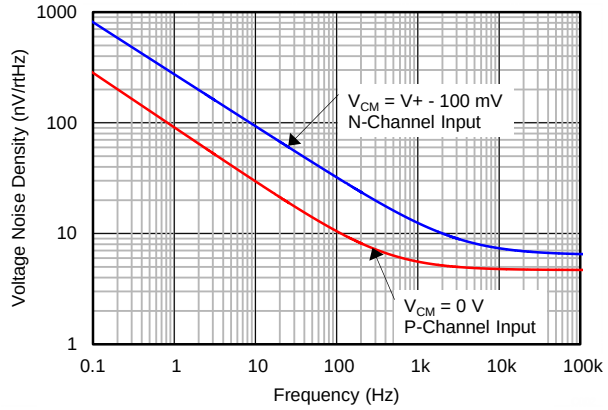


Figure 25. Input Voltage Noise Spectral Density vs Frequency

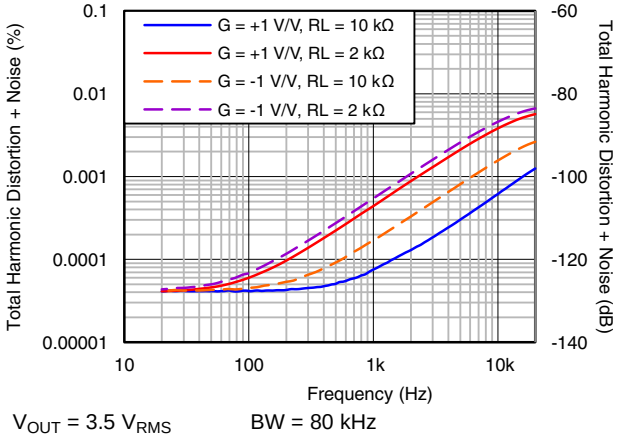


Figure 26. THD+N Ratio vs Frequency

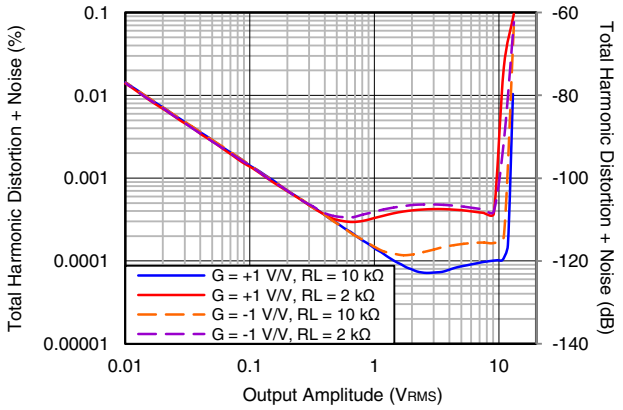


Figure 27. THD+N vs Output Amplitude

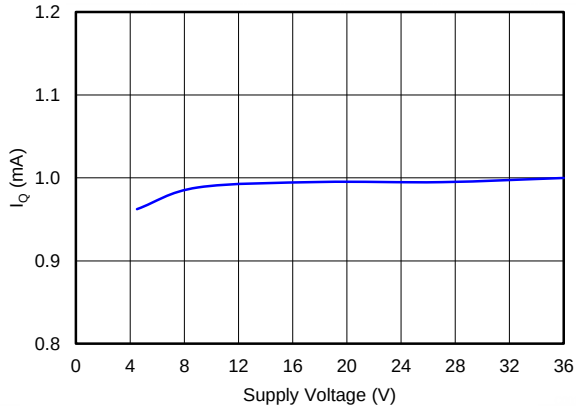


Figure 28. Quiescent Current vs Supply Voltage

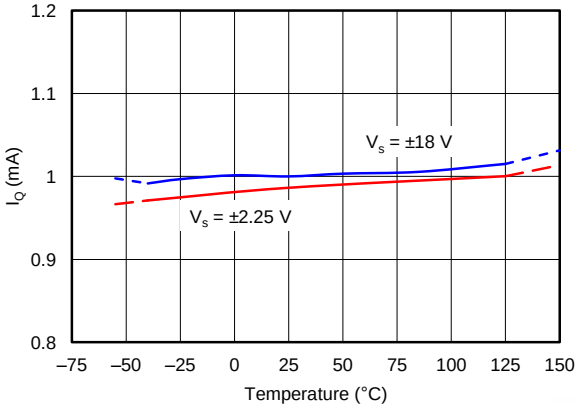


Figure 29. Quiescent Current vs Temperature

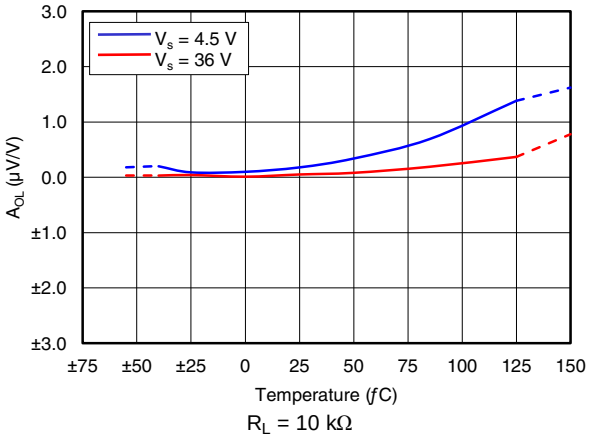


Figure 30. Open-Loop Gain vs Temperature

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

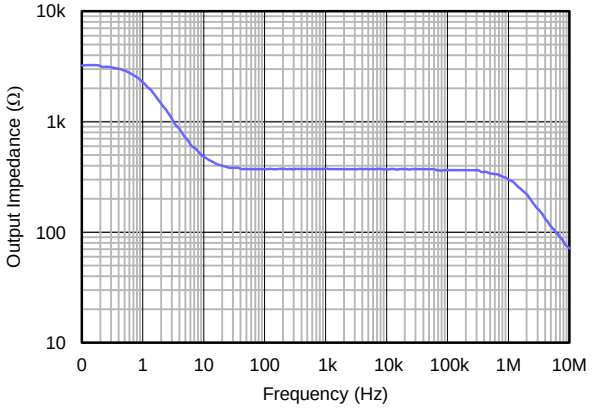
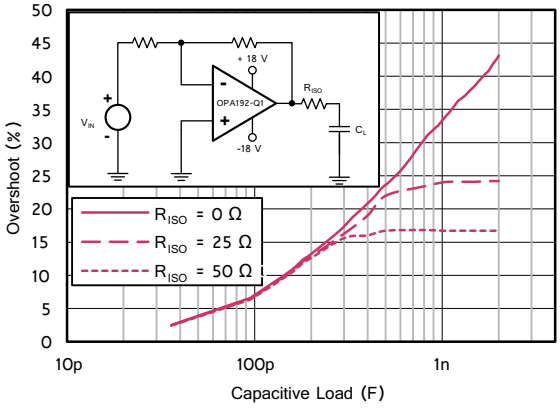
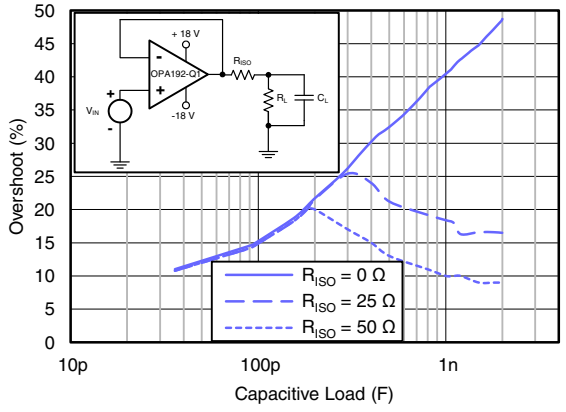


Figure 31. Open-Loop Output Impedance vs Frequency



R_I = 1 kΩ R_F = 1 kΩ G = –1

Figure 32. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)



G = 1

Figure 33. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

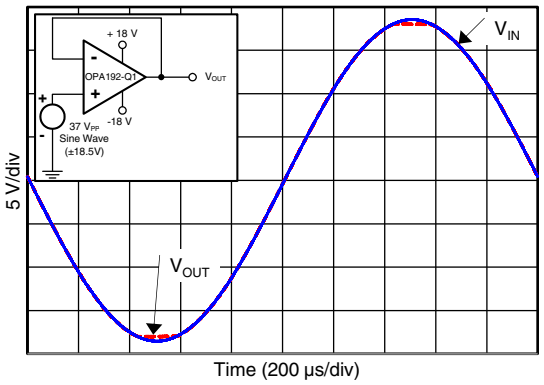
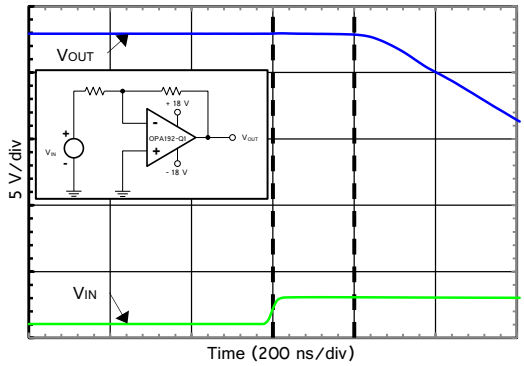
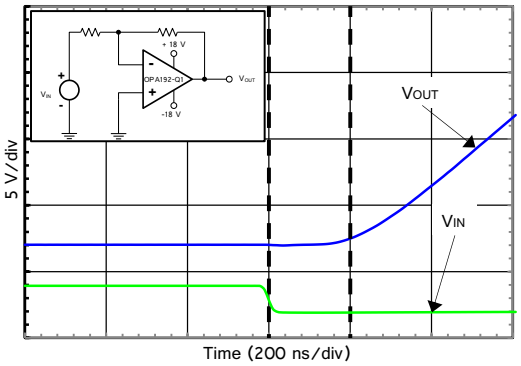


Figure 34. No Phase Reversal



R_I = 1 kΩ R_F = 10 kΩ G = –10

Figure 35. Positive Overload Recovery



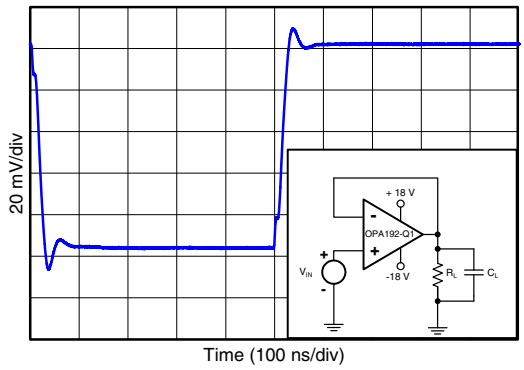
R_I = 1 kΩ G = –10 R_F = 10 kΩ

Figure 36. Negative Overload Recovery

ADVANCE INFORMATION

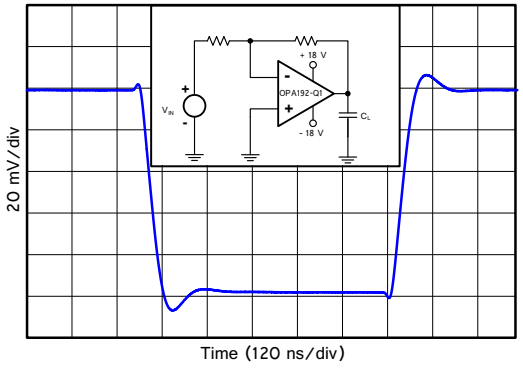
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)



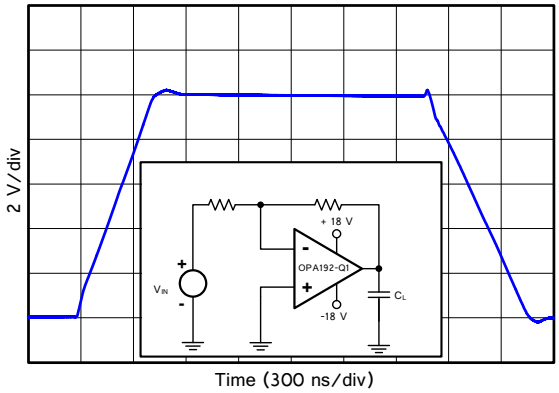
C_L = 10 pF G = 1

Figure 37. Small-Signal Step Response (100 mV)



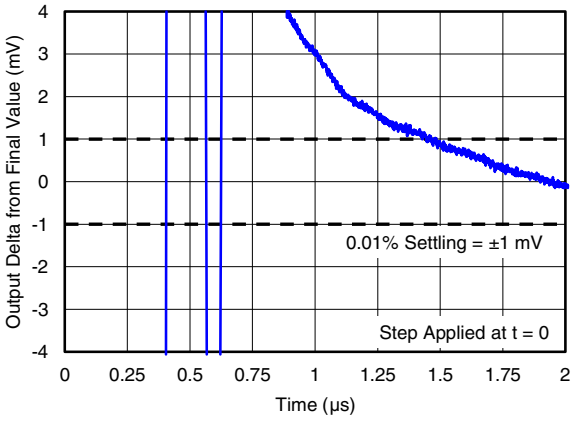
R_L = 1 kΩ C_L = 10 pF G = –1

Figure 38. Small-Signal Step Response (100 mV)



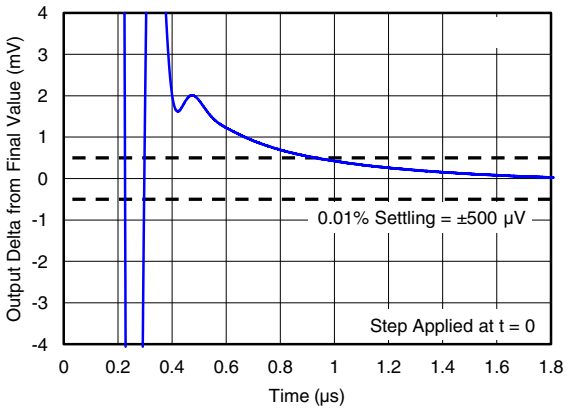
R_L = 1 kΩ C_L = 10 pF G = –1

Figure 39. Large-Signal Step Response



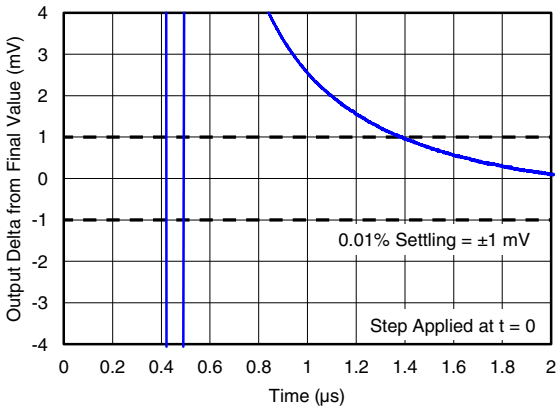
G = 1

Figure 40. Settling Time (10-V Positive Step)



G = 1

Figure 41. Settling Time (5-V Positive Step)



G = 1

Figure 42. Settling Time (10-V Negative Step)

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, (unless otherwise noted)

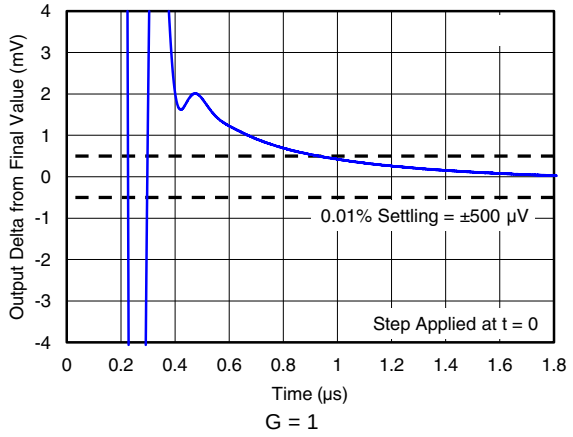


Figure 43. Settling Time (5-V Negative Step)

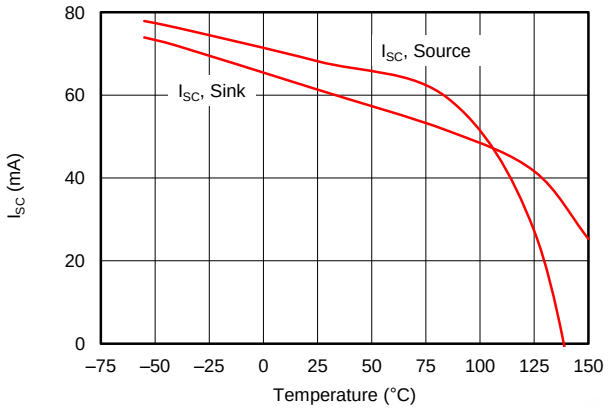


Figure 44. Short-Circuit Current vs Temperature

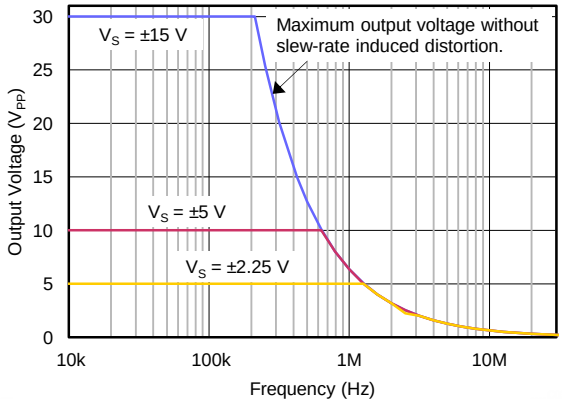


Figure 45. Maximum Output Voltage vs Frequency

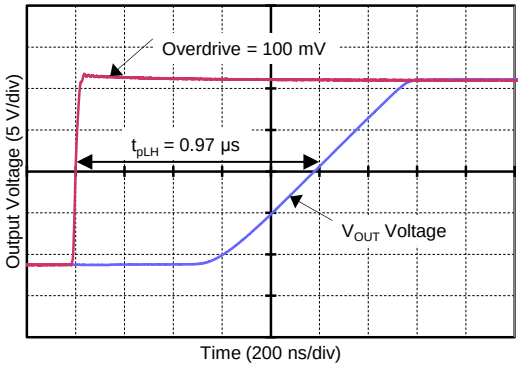


Figure 46. Propagation Delay Rising Edge

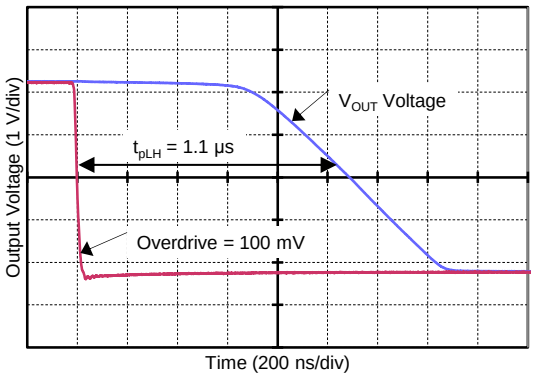


Figure 47. Propagation Delay Falling Edge

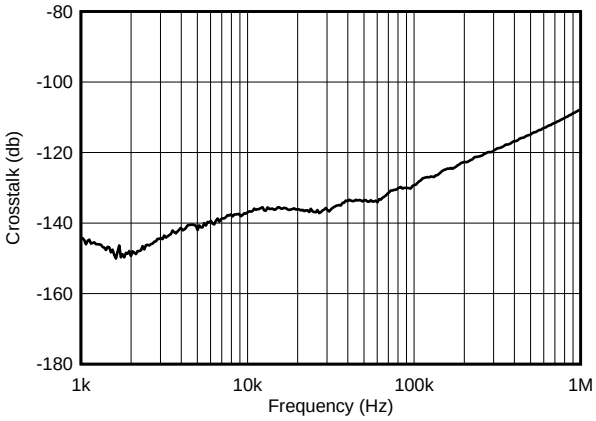


Figure 48. Crosstalk vs Frequency

ADVANCE INFORMATION

7 Parameter Measurement Information

7.1 Input Offset Voltage Drift

The OPAx192-Q1 family of operational amplifiers is manufactured using TI's e-trim technology. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing. When trimming input offset voltage drift the systematic or linear drift error on each device is trimmed to zero. This results in the remaining errors associated with input offset drift are minimal and are the result from only nonlinear error sources. Figure 49 illustrates this concept.

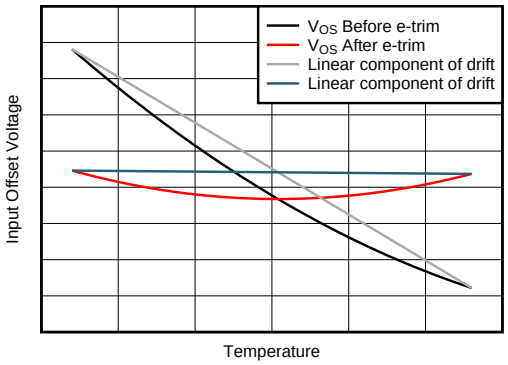


Figure 49. Input Offset Before and After Drift Trim

A common method of specifying input offset voltage drift is the *box method*. The box method estimates a maximum input offset drift by bounding the offset voltage versus temperature curve with a box and using the corners of this bounding box to determine the drift. The slope of the line connecting the diagonal corners of the box corresponds to the input offset voltage drift. Figure 50 shows the box method concept. The box method works particularly well when the input offset drift is dominated by the linear component of drift, but because the OPAx192-Q1 family uses TI's e-trim technology to remove the linear component input offset voltage drift, the box method is not a particularly useful method of accurately performing an error analysis. Figure 50 shows 30 typical units of the OPAx192-Q1 with the box method superimposed for illustrative purposes. The boundaries of the box are determined by the specified temperature range along the x-axis and the maximum specified input offset voltage across that same temperature range along the y-axis. Using the box method predicts an input offset voltage drift of 0.9 µV/°C. As shown in Figure 50, the slopes of the actual input offset voltage versus temperature are much less than that predicted by the box method. The box method predicts a negative value for the maximum input offset voltage drift and is not recommended when performing an error analysis.

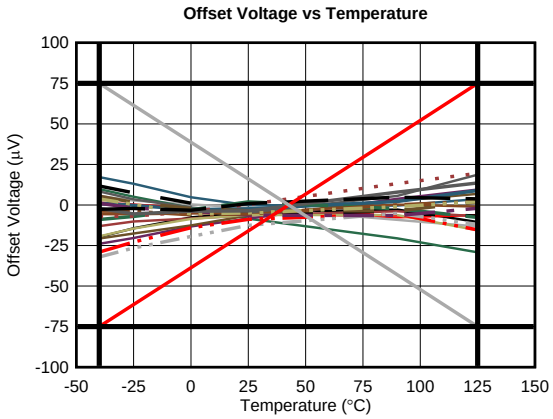


Figure 50. The Box Method

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

Input Offset Voltage Drift (continued)

Instead of the box method, a convenient way to illustrate input offset drift is to compute the slopes of the input offset voltage versus temperature curve. This is the same as computing the input offset drift at each point along the input offset voltage versus temperature curve. The results for the OPAx192-Q1 family are shown in Figure 51 and Figure 52.

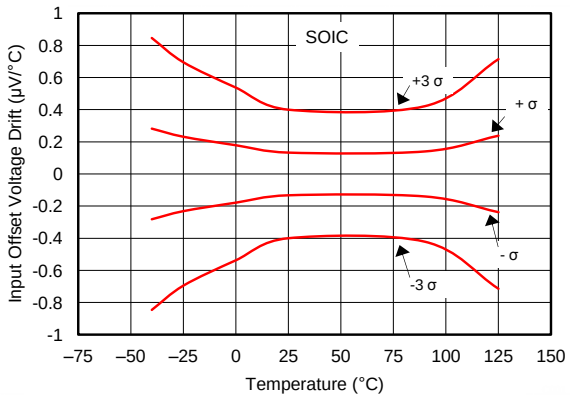


Figure 51. Input Offset Voltage Drift vs Temperature (OPA192-Q1ID and OPA2192-Q1ID)

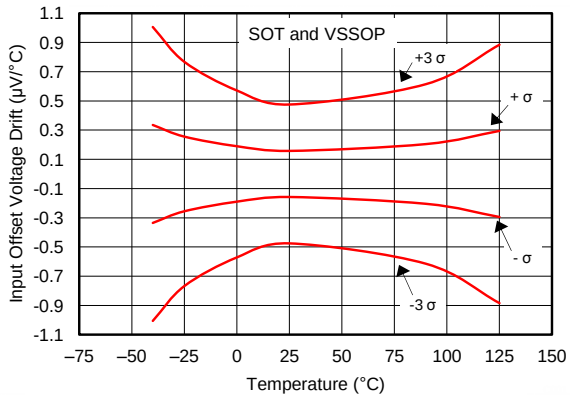


Figure 52. Input Offset Voltage Drift vs Temperature (OPA192-Q1IDBV, OPA192-Q1IDGK, OPA2192-Q1IDGK, and OPA4192-Q1IPW)

As shown in Figure 51, the input offset drift is typically less than ±0.3 µV/°C over the range from –40°C to +125°C. When performing an error analysis over the full specified temperature range, use the typical and maximum values for input offset voltage drift as described in the *Electrical Characteristics: V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)* and *Electrical Characteristics: V_S = ±2.25 V to ±4 V (V_S = 4.5 V to 8 V)* tables. If a reduced temperature range is applicable, use the information shown in Figure 51 or Figure 52 when performing an error analysis. To determine the change in input offset voltage, use Equation 1:

$$\Delta V_{OS} = \Delta T \times dV_{OS} / dT \quad (1)$$

where

- ΔV_{OS} = Change in input offset voltage
- ΔT = Change in temperature
- dV_{OS} / dT = Input offset voltage drift

For example, determine the amount of OPA192-Q1ID input offset voltage change over the temperature range of 25°C to 75°C for 1 σ (68%) of the units. As shown in Figure 51, the input offset drift is typically 0.15 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.15 µV/°C = 7.5 µV .

For 3 σ (99.7%) of the units, Figure 51 shows a typical input offset drift of 0.4 µV/°C. This input offset drift results in a typical input offset voltage change of (75°C – 25°C) × 0.4 µV/°C = 20 µV.

Figure 53 shows six typical units.

ADVANCE INFORMATION

Input Offset Voltage Drift (continued)

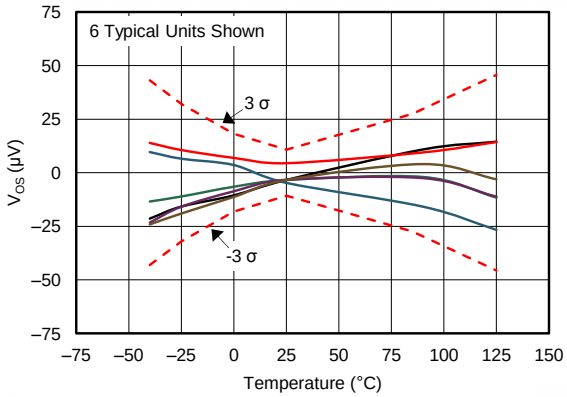


Figure 53. Input Offset Voltage Drift vs Temperature for Six Typical Units

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

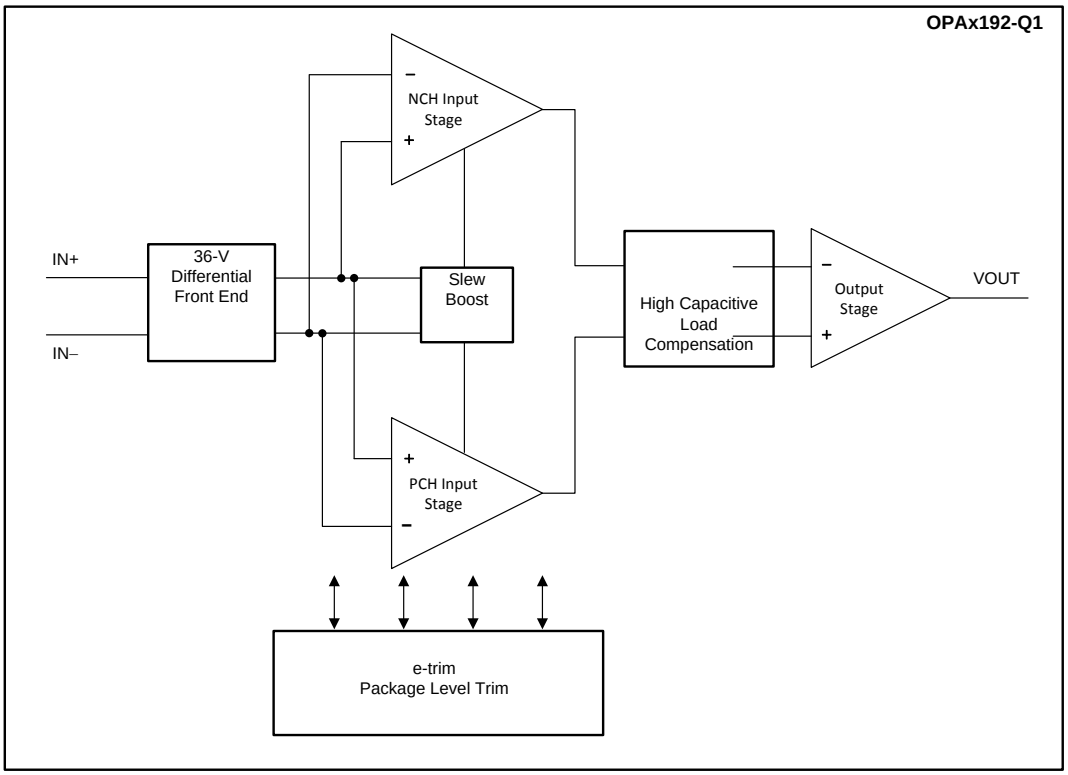
8 Detailed Description

8.1 Overview

The OPAx192-Q1 family of operational amplifiers use *e-trim*, a method of package-level trim for offset and offset temperature drift implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent input transistor mismatch, as well as errors induced during package molding. The trim communication occurs on the output pin of the standard pinout, and after the trim points are set, further communication to the trim structure is permanently disabled. The *Functional Block Diagram* shows the simplified diagram of the OPAx192-Q1 with e-trim.

Unlike previous e-trim op amps, the OPAx192-Q1 uses a patented two-temperature trim architecture to achieve a very low offset voltage of 25 µV (maximum) and low voltage offset drift of 0.5 µV/°C (maximum) over the full specified temperature range. This level of precision performance at wide supply voltages makes these amplifiers useful for high-impedance industrial sensors, filters, and high-voltage data acquisition.

8.2 Functional Block Diagram



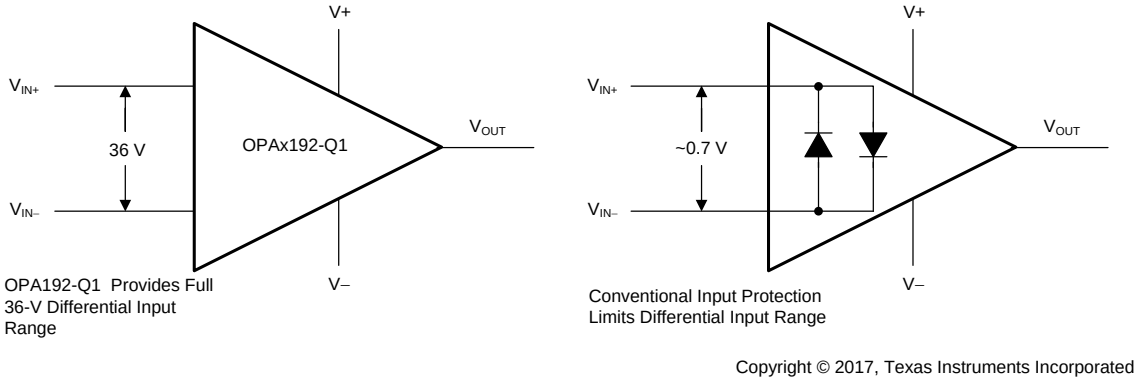
Copyright © 2017, Texas Instruments Incorporated

ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Input Protection Circuitry

The OPAx192-Q1 uses a unique input architecture to eliminate the need for input protection diodes but still provides robust input protection under transient conditions. Conventional input diode protection schemes shown in Figure 54 can be activated by fast transient step responses and can introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 55. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current, and resulting in extended settling time, as shown in Figure 56.



Copyright © 2017, Texas Instruments Incorporated

Figure 54. OPAx192-Q1 Input Protection Does Not Limit Differential Input Capability

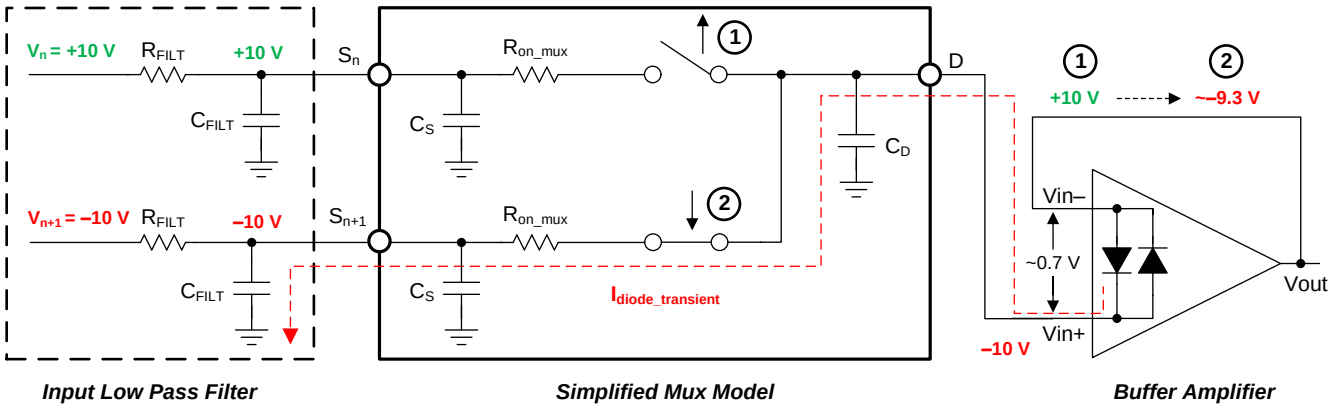


Figure 55. Back-to-Back Diodes Create Settling Issues

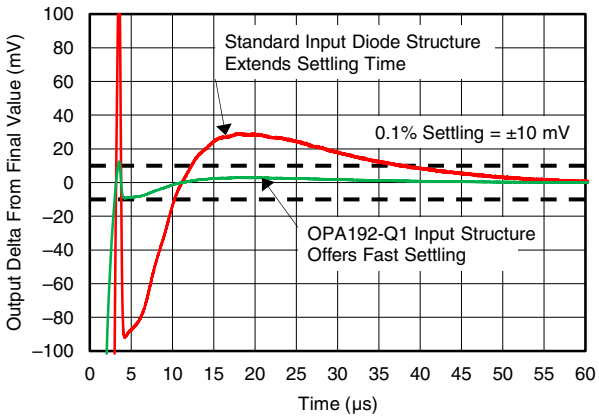


Figure 56. OPAx192-Q1 Protection Circuit Maintains Fast-Settling Transient Response

Copyright © 2017, Texas Instruments Incorporated

ADVANCE INFORMATION

Feature Description (continued)

The OPAx192-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx192-Q1 can tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 36 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as multiplexed data-acquisition systems; see Figure 66.

8.3.2 EMI Rejection

The OPAx192-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx192-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 57 shows the results of this testing on the OPAx192-Q1. Table 2 shows the EMIRR IN+ values for the OPAx192-Q1 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 may be centered on or operated near the particular frequency shown. Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers*, SBOA128, available for download from www.ti.com.

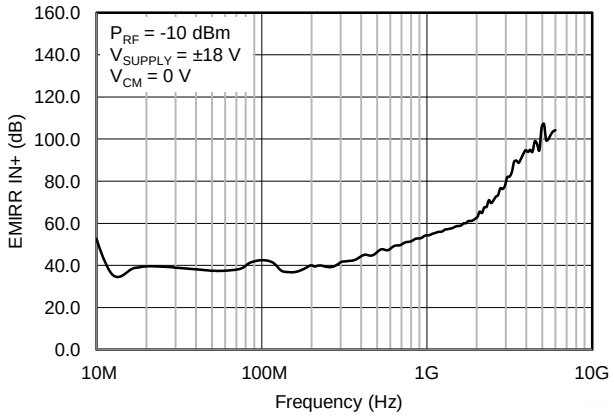


Figure 57. EMIRR Testing

Table 2. OPAx192-Q1 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	44.1 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	61.0 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.5 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.7 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	105.5 dB

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

8.3.3 Phase Reversal Protection

The OPAx192-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx192-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 58.

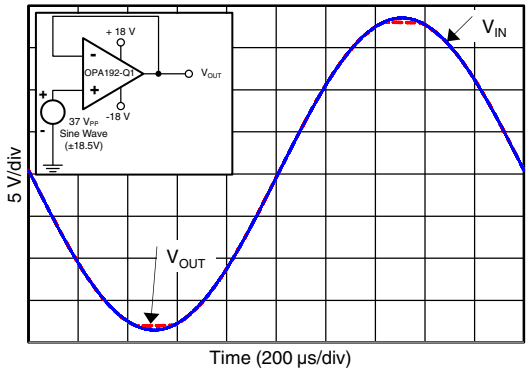
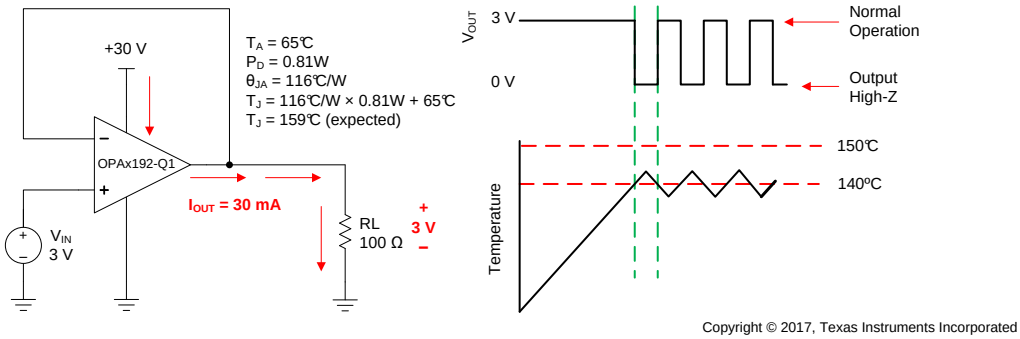


Figure 58. No Phase Reversal

8.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx192-Q1 is 150°C. Exceeding this temperature causes damage to the device. The OPAx192-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 59 shows an application example for the OPAx192-Q1 that has significant self heating (159°C) because of the power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature must reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 59 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.



Copyright © 2017, Texas Instruments Incorporated

Figure 59. Thermal Protection

8.3.5 Capacitive Load and Stability

The OPAx192-Q1 features a patented output stage capable of driving large capacitive loads, and in a unity-gain configuration, directly drives up to 1 nF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 60 and Figure 61. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

Copyright © 2017, Texas Instruments Incorporated

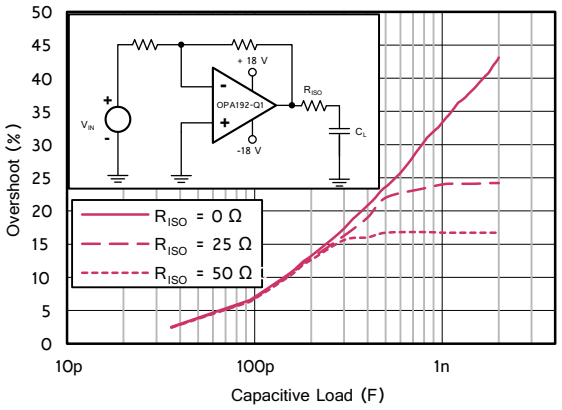


Figure 60. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

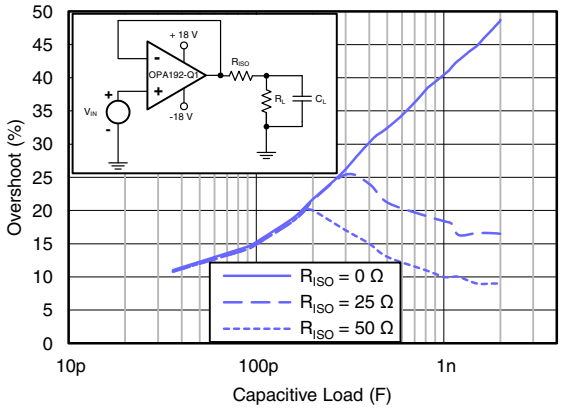


Figure 61. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 62. This resistor significantly reduces ringing and maintains dc performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx192-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 62 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin, and results using the OPAx192-Q1 are summarized in Table 3. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

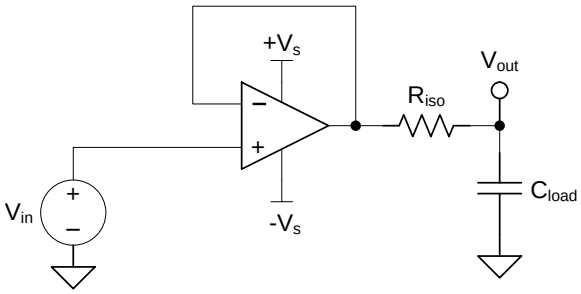


Figure 62. Extending Capacitive Load Drive with the OPAx192-Q1

Table 3. OPAx192-Q1 Capacitive Load Drive Solution Using Isolation Resistor Comparison of Calculated and Measured Results

PARAMETER	VALUE									
Capacitive Load	100 pF		1000 pF		0.01 µF		0.1 µF		1 µF	
Phase Margin	45°	60°	45°	60°	45°	60°	45°	60°	45°	60°
R_{ISO} (Ω)	47	360	24	100	20	51	6.2	15.8	2	4.7
Measured Overshoot (%)	23.2 8.6	10.4	22.5	9.0	22.1	8.7	23.1	8.6	21	8.6
Calculated PM	45.1°	58.1°	45.8°	59.7°	46.1°	60.1°	45.2°	60.2°	47.2°	60.2°

For step-by-step design procedure, circuit schematics, bill of materials, printed circuit board (PCB) files, simulation results, and test results, refer to TI Precision Design TIDU032, *Capacitive Load Drive Solution using an Isolation Resistor* .

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

8.3.6 Common-Mode Voltage Range

The OPAx192-Q1 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 63. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 3 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.5 V. There is a small transition region, typically (V+) –3 V to (V+) – 1.5 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation outside this region.

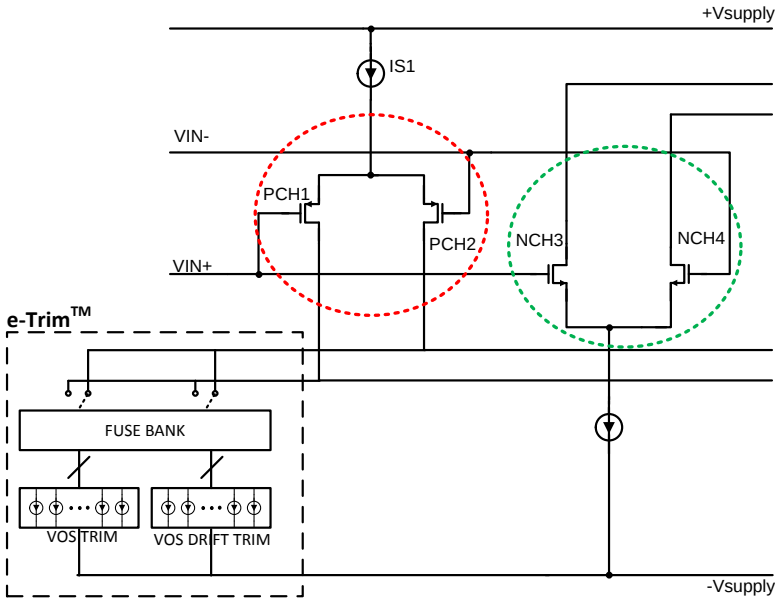


Figure 63. Rail-to-Rail Input Stage

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPAx192-Q1 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range, as shown in Figure 64.

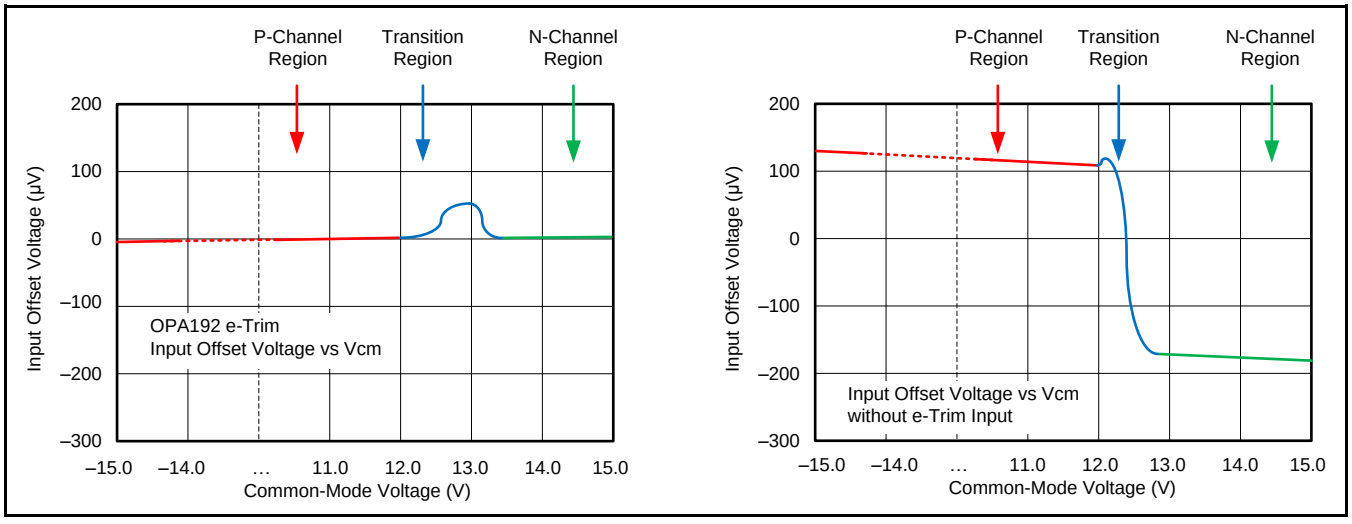


Figure 64. Common-Mode Transition vs Standard Rail-to-Rail Amplifiers

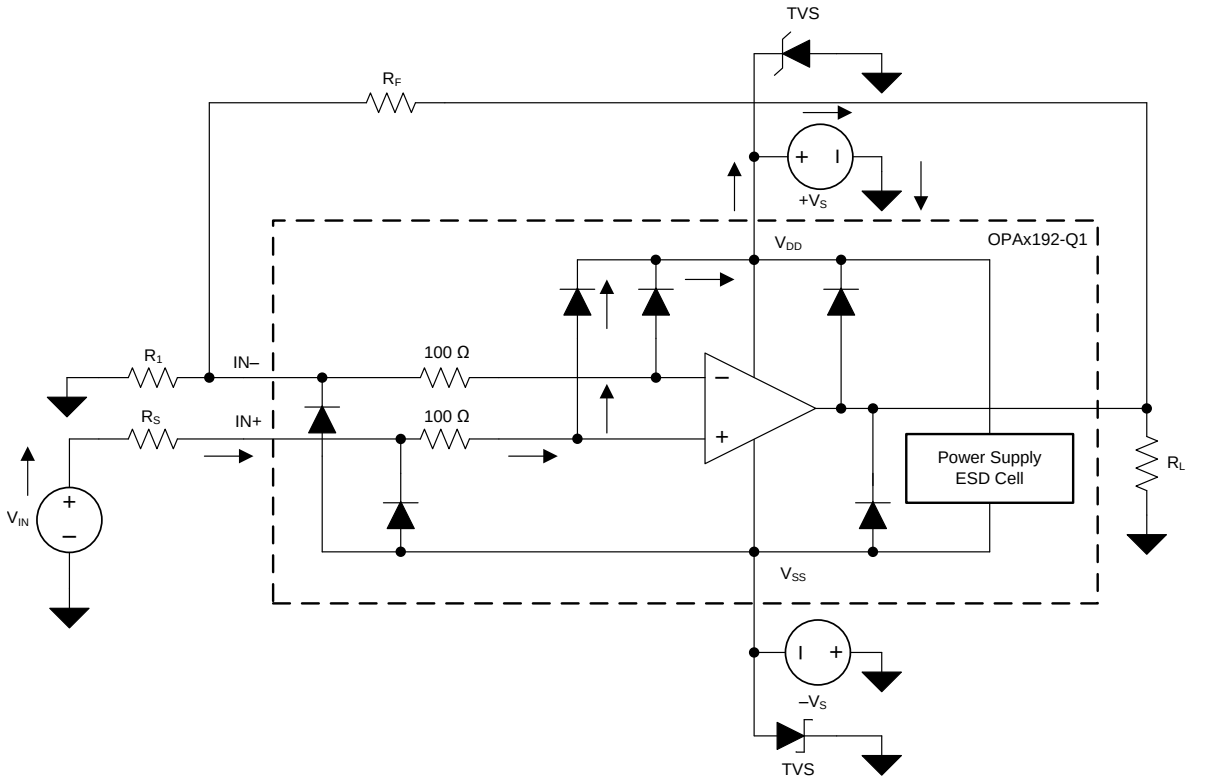
ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 65 shows an illustration of the ESD circuits contained in the OPAx192-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



Copyright © 2017, Texas Instruments Incorporated

Figure 65. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

ADVANCE INFORMATION

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

8.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx192-Q1 is approximately 200 ns.

8.4 Device Functional Modes

The OPAx192-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx192-Q1 is 36 V (±18 V).

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx192-Q1 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer true rail-to-rail input and output, ultra-low offset voltage and offset voltage drift, as well as 10-MHz bandwidth and high capacitive load drive. These features make the OPAx192-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

9.2 Typical Applications

9.2.1 16-Bit Precision Multiplexed Data-Acquisition System

Figure 66 shows a 16-bit, differential, 4-channel, multiplexed data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage differential input. The circuit uses the ADS8864, a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel differential multiplexer (mux). This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the OPAx192-Q1 and OPA140 to achieve excellent dynamic performance and linearity with the ADS8864.

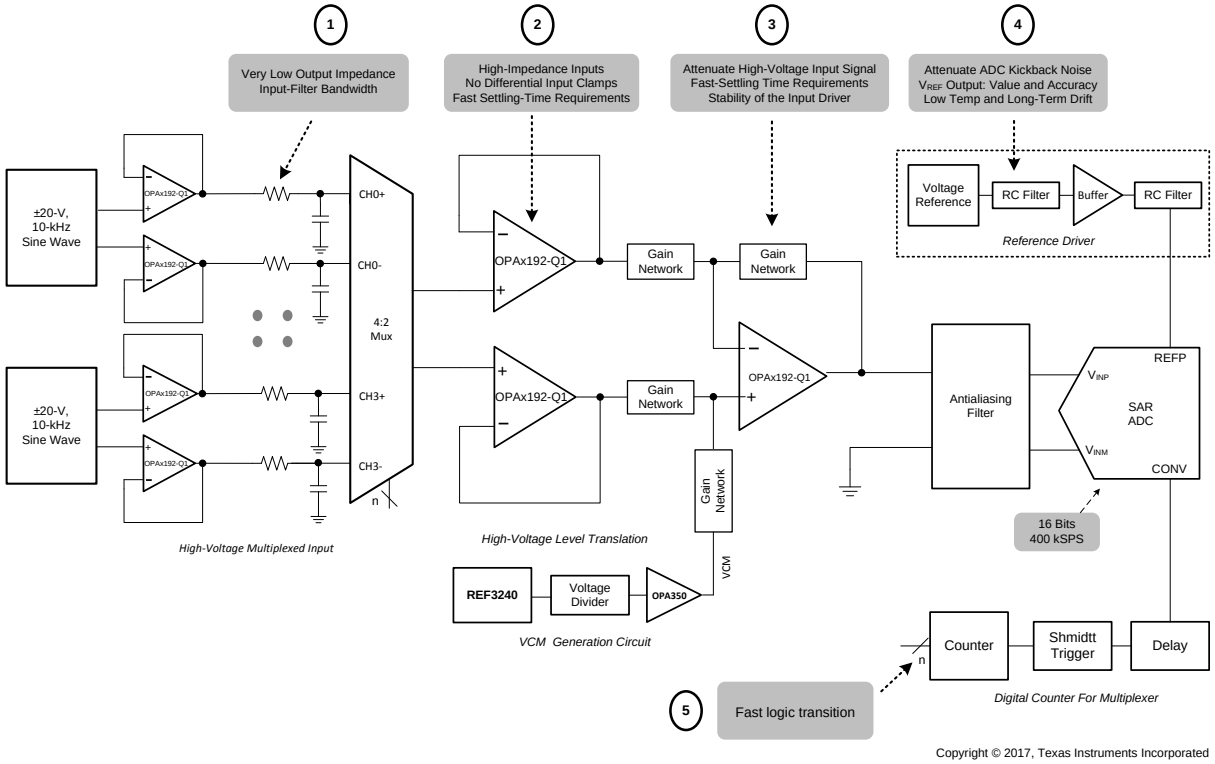


Figure 66. OPAx192-Q1 in 16-Bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High-Voltage Inputs With Lowest Distortion

ADVANCE INFORMATION

Typical Applications (continued)

9.2.1.1 Design Requirements

The primary objective is to design a ±20 V, differential 4-channel multiplexed data acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10 kHz full-scale pure sine-wave input. The design requirements for this block design are:

- System Supply Voltage: ±15 V
- ADC Supply Voltage: 3.3 V
- ADC Sampling Rate: 400 kSPS
- ADC Reference Voltage (REFP): 4.096 V
- System Input Signal: A high-voltage differential input signal with a peak amplitude of 10 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

9.2.1.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal high voltage multiplexed data acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in Figure 66. The circuit is a multichannel data acquisition signal chain consisting of an input low-pass filter, multiplexer (mux), mux output buffer, attenuating SAR ADC driver, digital counter for mux and the reference driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. The two primary design considerations to maximize the performance of a precision multiplexed data acquisition system are the mux input analog front-end and the high-voltage level translation SAR ADC driver design. However, carefully design each analog circuit block based on the ADC performance specifications in order to achieve the fastest settling at 16-bit resolution and lowest distortion system. The diagram includes the most important specifications for each individual analog block.

This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel. The first step in the design is to understand the requirement for extremely low impedance input-filter design for the mux. This understanding helps in the decision of an appropriate input filter and selection of a mux to meet the system settling requirements. The next important step is the design of the attenuating analog front-end (AFE) used to level translate the high-voltage input signal to a low-voltage ADC input when maintaining amplifier stability. The next step is to design a digital interface to switch the mux input channels with minimum delay. The final design challenge is to design a high-precision, reference-driver circuit that provides the required REFP reference voltage with low offset, drift, and noise contributions.

9.2.1.3 Application Curve

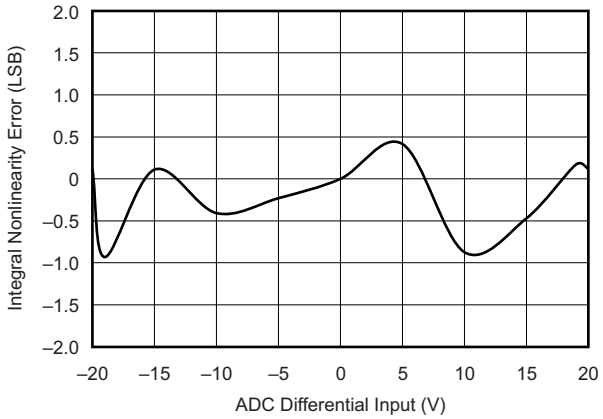


Figure 67. ADC 16-Bit Linearity Error for the Multiplexed Data Acquisition Block

TI Precision Designs

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU181, *16-bit, 400-kSPS, 4-Channel, Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion*.

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

9.2.2 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPAx192-Q1 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems.Figure 68 shows the OPAx192-Q1 in a slew-rate limit design.

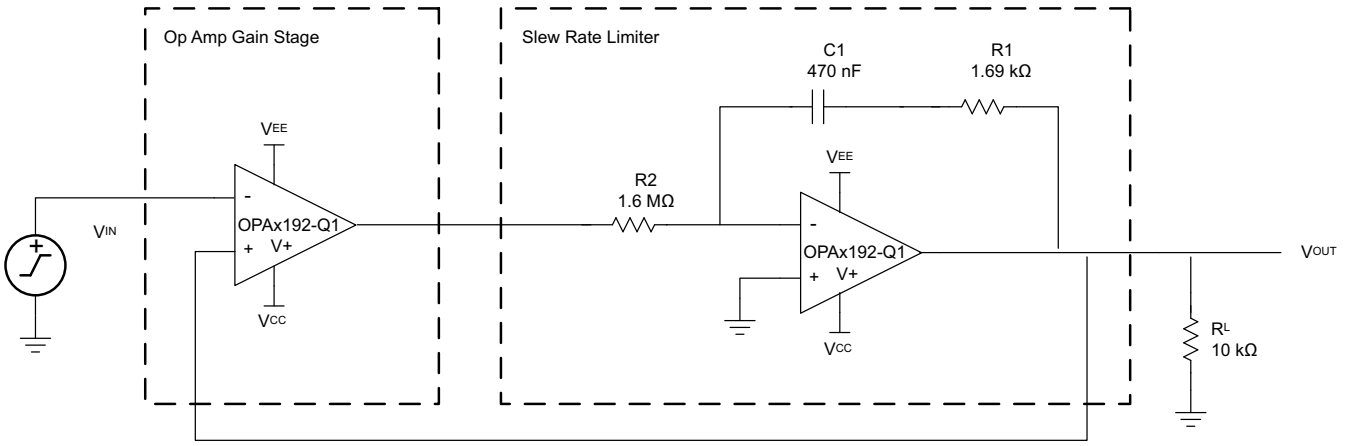


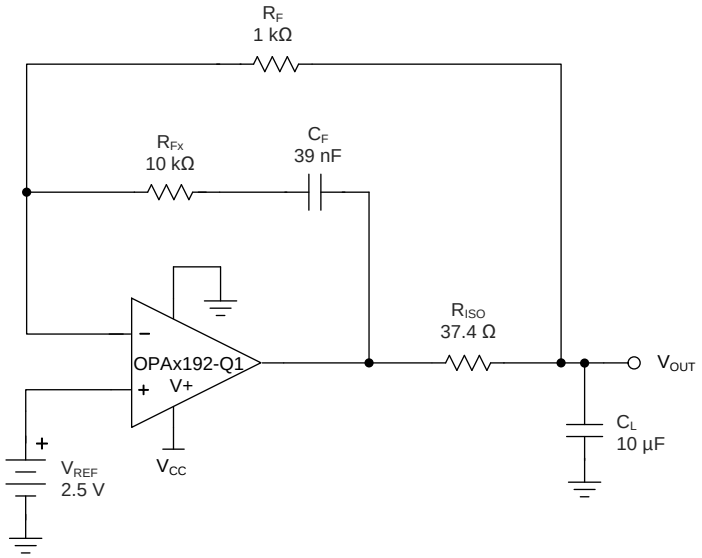
Figure 68. Slew Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, see TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

ADVANCE INFORMATION

9.2.3 Precision Reference Buffer

The OPAx192-Q1 features high output current drive capability and low input offset voltage, making the device an excellent reference buffer to provide an accurate buffered output with ample drive current for transients. For the 10-µF ceramic capacitor shown in Figure 69, R_{ISO}, a 37.4-Ω isolation resistor, provides separation of two feedback paths for optimal stability. Feedback path number one is through R_F and is directly at the output (V_{OUT}). Feedback path number two is through R_{Fx} and C_F and is connected at the output of the op amp. The optimized stability components shown for the 10-µF load give a closed-loop signal bandwidth at V_{OUT} of 4 kHz and still provides a loop gain phase margin of 89°. Any other load capacitances require recalculation of the stability components: R_F, R_{Fx} , C_F , and R_{ISO}.



Copyright © 2017, Texas Instruments Incorporated

Figure 69. Precision Reference Buffer

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

10 Power-Supply Recommendations

The OPAx192-Q1 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. .
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 71, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

ADVANCE INFORMATION

11.2 Layout Example

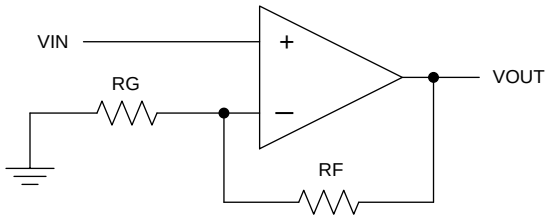
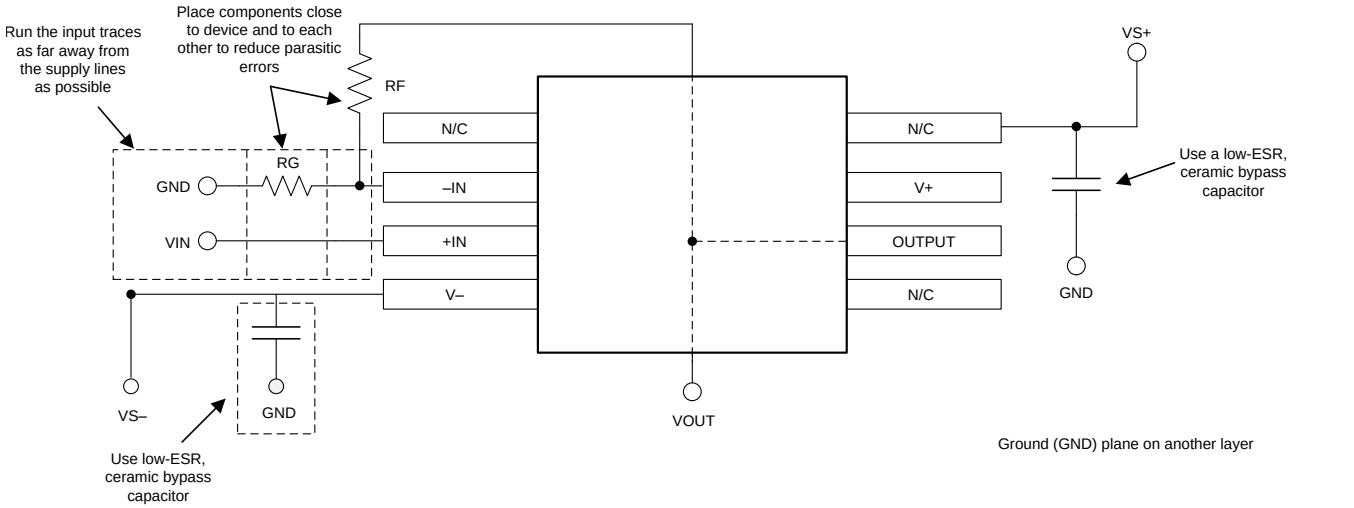


Figure 70. Schematic Representation



Copyright © 2017, Texas Instruments Incorporated

Figure 71. Operational Amplifier Board Layout for Noninverting Configuration

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 TI Precision Designs

The OPA192 is featured in several Texas Instruments (TI) Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Related Links

Table 4 below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA192-Q1	Click here	Click here	Click here	Click here	Click here
OPA2192-Q1	Click here	Click here	Click here	Click here	Click here
OPA4192-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

ADVANCE INFORMATION

12.5 Trademarks (continued)

e-trim, E2E are trademarks of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
e-trim, are trademarks of ~ Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

Copyright © 2017, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA192QDGKRQ1	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
OPA2192QDGKRQ1	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

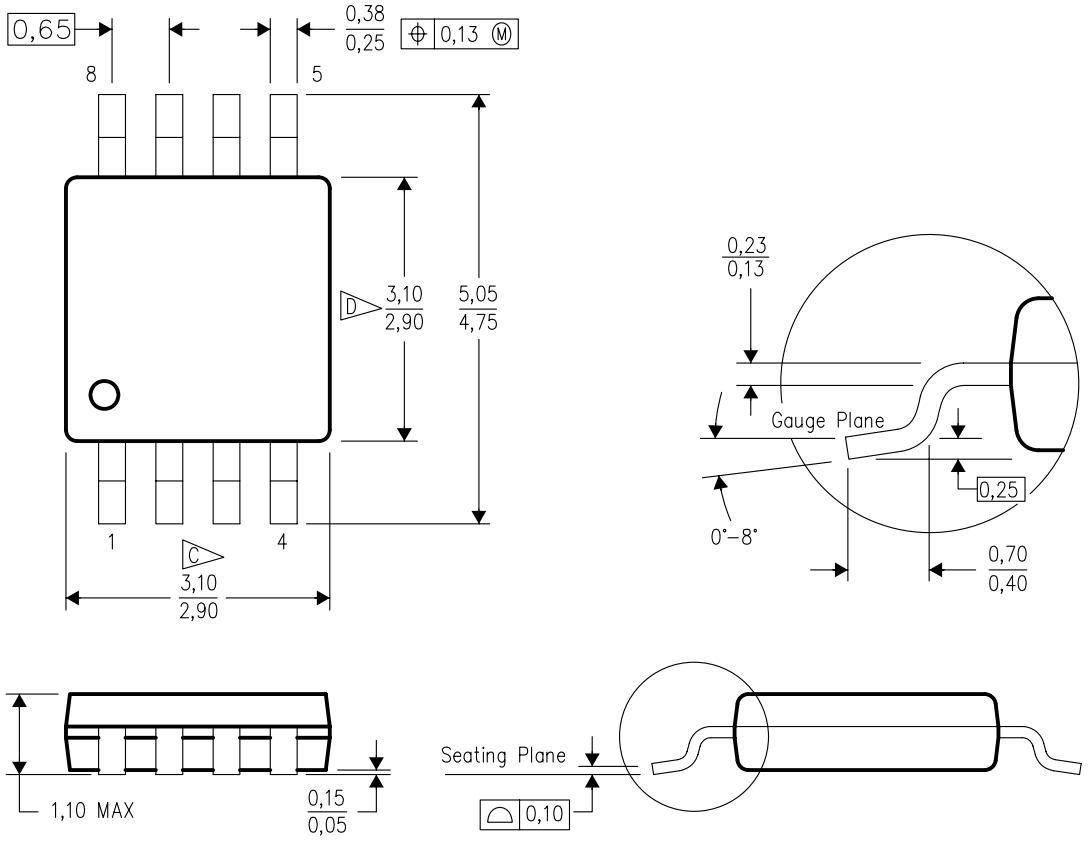
OTHER QUALIFIED VERSIONS OF OPA192-Q1, OPA2192-Q1 :

- Catalog: OPA192, OPA2192

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated