Features

- Pin and Software Compatibility with Standard 80C51 Products and 80C51Fx/Rx/Rx+
- Plug-In Replacement of Intel's 8xC251Sx
- C251 Core: Intel's MCS®251 D-step Compliance
- 40-byte Register File
- Registers Accessible as Bytes, Words or Dwords
- Three-stage Instruction Pipeline
- 16-bit Internal Code Fetch
- Enriched C51 Instruction Set
- 16-bit and 32-bit ALU
- Compare and Conditional Jump Instructions
- Expanded Set of Move Instructions
- Linear Addressing
- 1 Kbyte of On-Chip RAM
- External Memory Space (Code/Data) Programmable from 64 kilobytes to 256 kilobytes
- TSC87251G2D: 32 kilobytes of On-Chip EPROM/OTPROM
  - SINGLE PULSE Programming Algorithm
- TSC83251G2D: 32 kilobytes of On-Chip Masked ROM
- TSC80251G2D: ROMless Version
- Four 8-bit Parallel I/O Ports (Ports 0, 1, 2 and 3 of the Standard 80C51)
- Serial I/O Port: Full Duplex UART (80C51 Compatible) With Independent Baud Rate Generator
- SSLC: Synchronous Serial Link Controller
- TWI Multi-master Protocol
- µWire and SPI Master and Slave Protocols
- Three 16-bit Timers/Counters (Timers 0, 1 and 2 of the Standard 80C51)
- EWC: Event and Waveform Controller
- Compatible with Intel's Programmable Counter Array (PCA)
- Common 16-bit Timer/Counter Reference with Four Possible Clock Sources (Fosc/4, Fosc/12, Timer 1 and External Input)
- Five Modules, Each with Four Programmable Modes:
  - 16-bit Software Timer/Counter
  - 16-bit Timer/Counter Capture Input and Software Pulse Measurement
  - High-speed Output and 16-bit Software Pulse Width Modulation (PWM)
  - 8-bit Hardware PWM Without Overhead
- 16-bit Watchdog Timer/Counter Capability
- Secure 14-bit Hardware Watchdog Timer
- Power Management
- Power-On Reset (Integrated on the Chip)
- Power-Off Flag (Cold and Warm Resets)
- Software Programmable System Clock
- Idle Mode
- Power-down Mode
- Keyboard Interrupt Interface on Port 1
- Non Maskable Interrupt Input (NMI)
- Real-Time Wait States Inputs (WAIT#/AWAIT#)
- ONCE Mode and Full Speed Real-time In-circuit Emulation Support (Third Party Vendors)
- High Speed Versions:
  - 4.5V to 5.5V
  - 16 MHz and 24 MHz
- Typical Operating Current: 35 mA at 24 MHz
  24 mA at 16 MHz
- Typical Power-down Current: 2 µA
- Low Voltage Version:
  - 2.7V to 5.5V
  - 16 MHz

8/16-bit Microcontroller with Serial Communication Interfaces

TSC80251G2D
TSC83251G2D
TSC87251G2D
AT80251G2D
AT83251G2D
AT87251G2D

Rev. 4135F–8051–11/06

- **Typical Operating Current:11 mA at 3V**
- **Typical Power-down Current: 1 µA**
- **Temperature Ranges: Commercial (0°C to +70°C), Industrial (-40°C to +85°C), Automotive ((-40°C to +85°C) ROM only)**
- **Option: Extended Range (-55°C to +125°C)**
- **Packages: PDIL 40, PLCC 44 and VQFP 44**
- **Options: Known Good Dice and Ceramic Packages**

Description

The TSC80251G2D products are derivatives of the Atmel Microcontroller family based on the 8/16-bit C251 Architecture. This family of products is tailored to 8/16-bit microcontroller applications requiring an increased instruction throughput, a reduced operating frequency or a larger addressable memory space. The architecture can provide a significant code size reduction when compiling C programs while fully preserving the legacy of C51 assembly routines.

The TSC80251G2D derivatives are pin and software compatible with standard 80C51/Fx/Rx/Rx+ with extended on-chip data memory (1 Kbyte RAM) and up to 256 kilobytes of external code and data. Additionally, the TSC83251G2D and TSC87251G2D provide on-chip code memory: 32 kilobytes ROM and 32 kilobytes EPROM/OTPROM respectively.

They provide transparent enhancements to Intel's 8xC251Sx family with an additional Synchronous Serial Link Controller (SSLC supporting TWI, µWire and SPI protocols), a Keyboard interrupt interface, a dedicated Baud Rate Generator for UART, and Power Management features.

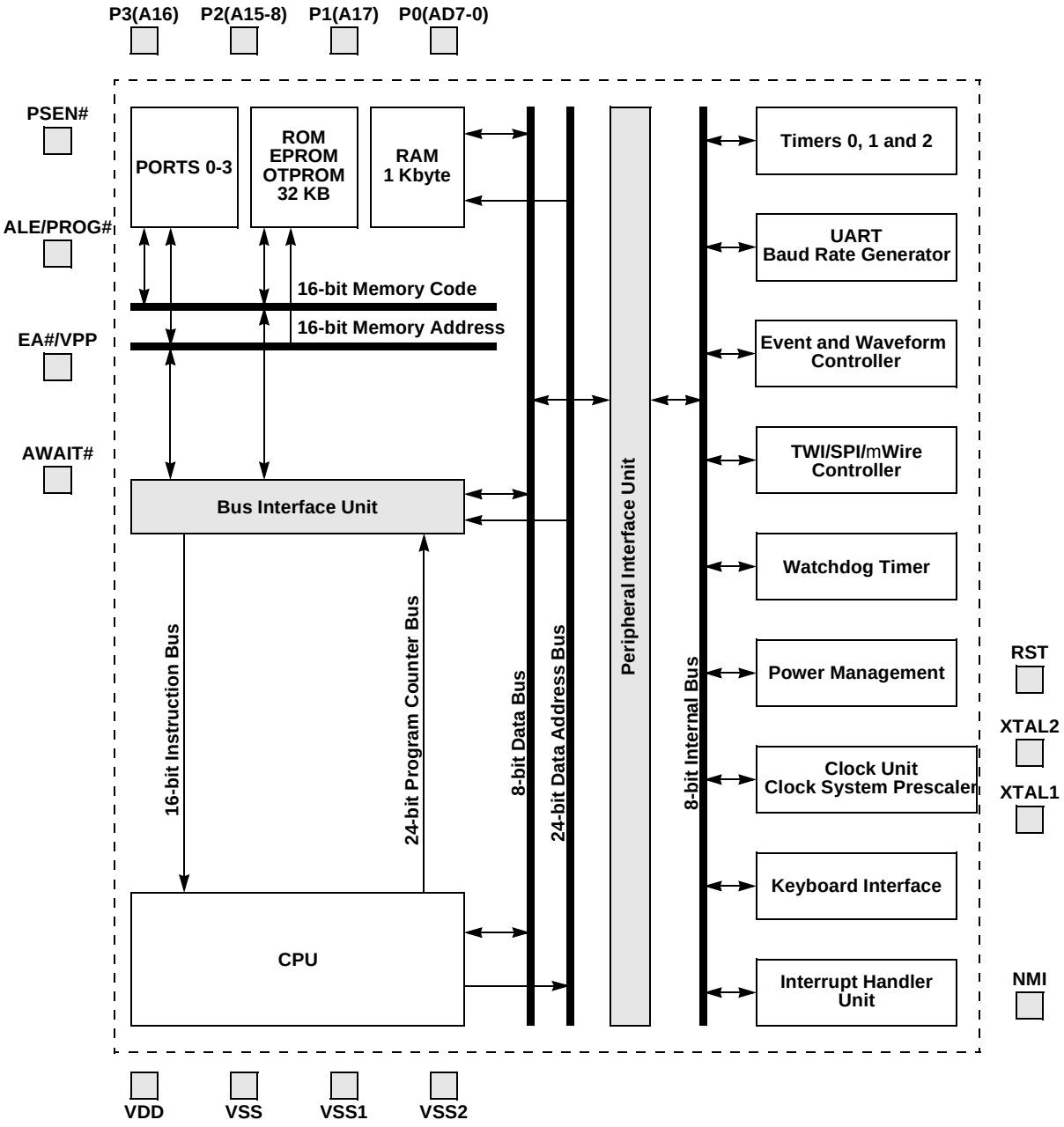
TSC80251G2D derivatives are optimized for speed and for low power consumption on a wide voltage range.

Note: 1. This Datasheet provides the technical description of the TSC80251G2D derivatives. For further information on the device usage, please request the TSC80251 Programmer's Guide and the TSC80251G1D Design Guide and errata sheet.

Typical Applications

- ISDN Terminals
- High-Speed Modems
- PABX (SOHO)
- Line Cards
- DVD ROM and Players
- Printers
- Plotters
- Scanners
- Banking Machines
- Barcode Readers
- Smart Cards Readers
- High-End Digital Monitors
- High-End Joysticks
- High-end TV's

Block Diagram



Pin Description

Pinout

Figure 1. TSC80251G2D 40-pin DIP package

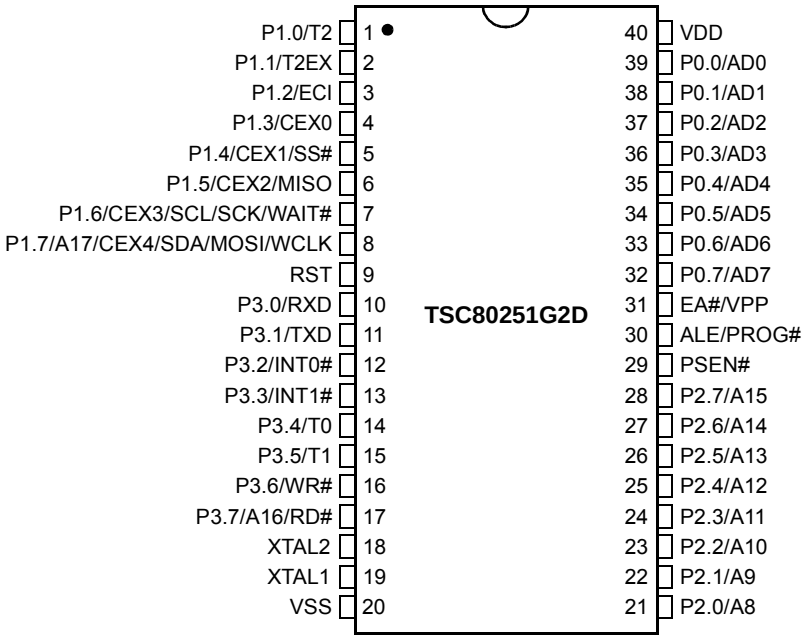


Figure 2. TSC80251G2D 44-pin PLCC Package

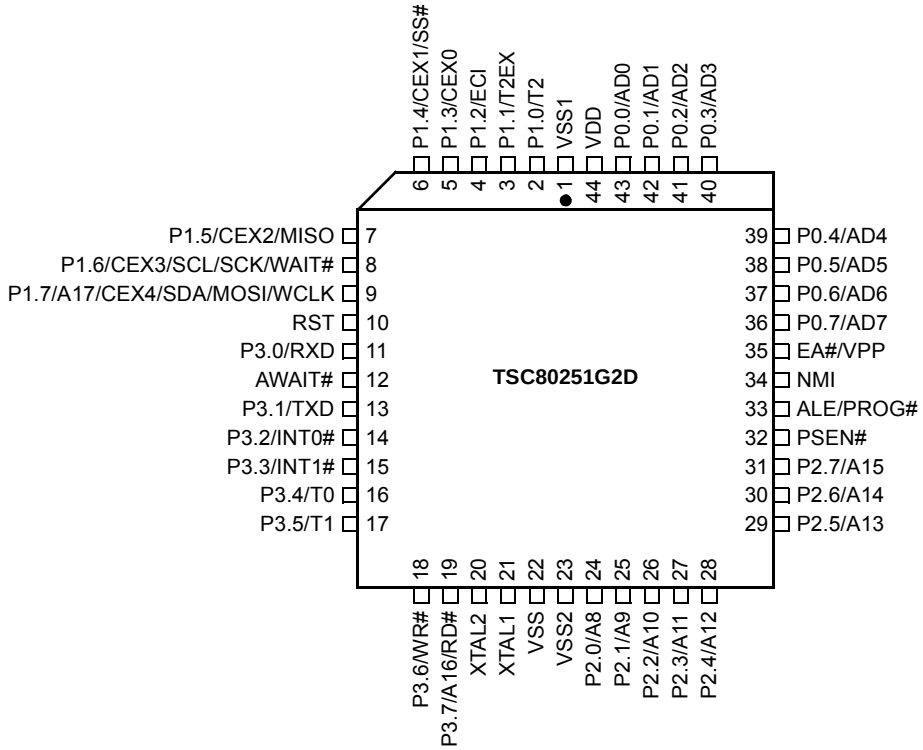


Figure 3. TSC80251G2D 44-pin VQFP Package

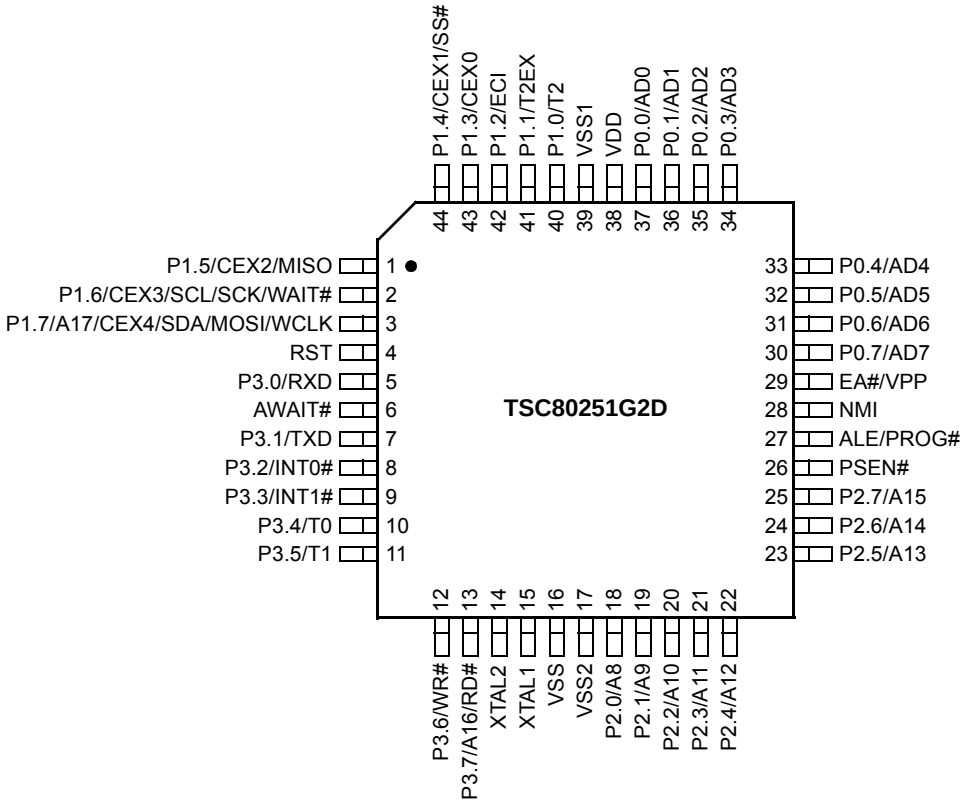


Table 1. TSC80251G2D Pin Assignment

DIP	PLCC	VQFP	Name	DIP	PLCC	VQFP	Name
	1	39	VSS1		23	17	VSS2
1	2	40	P1.0/T2	21	24	18	P2.0/A8
2	3	41	P1.1/T2EX	22	25	19	P2.1/A9
3	4	42	P1.2/ECI	23	26	20	P2.2/A10
4	5	43	P1.3/CEX0	24	27	21	P2.3/A11
5	6	44	P1.4/CEX1/SS#	25	28	22	P2.4/A12
6	7	1	P1.5/CEX2/MISO	26	29	23	P2.5/A13
7	8	2	P1.6/CEX3/SCL/SCK/WAIT#	27	30	24	P2.6/A14
8	9	3	P1.7/A17/CEX4/SDA/MOSI/WCLK	28	31	25	P2.7/A15
9	10	4	RST	29	32	26	PSEN#
10	11	5	P3.0/RXD	30	33	27	ALE/PROG#
	12	6	AWAIT#		34	28	NMI
11	13	7	P3.1/TXD	31	35	29	EA#/VPP
12	14	8	P3.2/INT0#	32	36	30	P0.7/AD7
13	15	9	P3.3/INT1#	33	37	31	P0.6/AD6
14	16	10	P3.4/T0	34	38	32	P0.5/AD5
15	17	11	P3.5/T1	35	39	33	P0.4/AD4
16	18	12	P3.6/WR#	36	40	34	P0.3/AD3
17	19	13	P3.7/A16/RD#	37	41	35	P0.2/AD2
18	20	14	XTAL2	38	42	36	P0.1/AD1
19	21	15	XTAL1	39	43	37	P0.0/AD0
20	22	16	VSS	40	44	38	VDD

Signals

Table 2. Product Name Signal Description

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P1.7
A16	O	**17th Address Bit** Output to memory as 17th external address bit (A16) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
A15:8(1)	O	**Address Lines** Upper address lines for the external bus.	P2.7:0
AD7:0(1)	I/O	**Address/Data Lines** Multiplexed lower address lines and data for the external memory.	P0.7:0
ALE	O	**Address Latch Enable** ALE signals the start of an external bus cycle and indicates that valid address information are available on lines A16/A17 and A7:0. An external latch can use ALE to demultiplex the address from address/data bus.	–
AWAIT#	I	**Real-time Asynchronous Wait States Input** When this pin is active (low level), the memory cycle is stretched until it becomes high. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, AWAIT# can be unconnected without loss of compatibility or power consumption increase (on-chip pull-up). Not available on DIP package.	–
CEX4:0	I/O	**PCA Input/Output pins** CEXx are input signals for the PCA capture mode and output signals for the PCA compare and PWM modes.	P1.7:3
EA#	I	**External Access Enable** EA# directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is on-chip ROM if the address is within the range of the on-chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground.	–
ECI	O	**PCA External Clock input** ECI is the external clock input to the 16-bit PCA timer.	P1.2
MISO	I/O	**SPI Master Input Slave Output line** When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.	P1.5
MOSI	I/O	**SPI Master Output Slave Input line** When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller.	P1.7
INT1:0#	I	**External Interrupts 0 and 1** INT1#/INT0# inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits IT1:0 are cleared, bits IE1:0 are set by a low level on INT1#/INT0#.	P3.3:2

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
NMI	I	**Non Maskable Interrupt** Holding this pin high for 24 oscillator periods triggers an interrupt. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, NMI can be unconnected without loss of compatibility or power consumption increase (on-chip pull-down). Not available on DIP package.	–
P0.0:7	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any paraitic current consumption, Floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.0:7	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups. P1 provides interrupt capability for a keyboard interface.	–
P2.0:7	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.0:7	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	–
PROG#	I	**Programming Pulse input** The programming pulse is applied to this input for programming the on-chip EPROM/OTPROM.	–
PSEN#	O	**Program Store Enable/Read signal output** PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see).	–
RD#	O	**Read or 17th Address Bit (A16)** Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	–
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SCK	I/O	**SPI Serial Clock** When SPI is in master mode, SCK outputs clock to the slave peripheral. When SPI is in slave mode, SCK receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional TWI data line.	P1.7
SS#	I	**SPI Slave Select Input** When in Slave mode, SS# enables the slave mode.	P1.4

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
T1:0	I/O	**Timer 1:0 External Clock Inputs** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	–
T2	I/O	**Timer 2 Clock Input/Output** For the timer 2 capture mode, T2 is the external clock input. For the Timer 2 clock-out mode, T2 is the clock output.	P1.0
T2EX	I	**Timer 2 External Input** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 register to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1
VDD	PWR	**Digital Supply Voltage** Connect this pin to +5V or +3V supply voltage.	–
VPP	I	**Programming Supply Voltage** The programming supply voltage is applied to this input for programming the on-chip EPROM/OTPROM.	–
VSS	GND	**Circuit Ground** Connect this pin to ground.	–
VSS1	GND	**Secondary Ground 1** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC80251G2D as a pin-for-pin replacement for a 8xC51 product, VSS1 can be unconnected without loss of compatibility. Not available on DIP package.	–
VSS2	GND	**Secondary Ground 2** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC80251G2D as a pin-for-pin replacement for a 8xC51 product, VSS2 can be unconnected without loss of compatibility. Not available on DIP package.	–
WAIT#	I	**Real-time Synchronous Wait States Input** The real-time WAIT# input is enabled by setting RTWE bit in WCON (S:A7h). During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal.	P1.6
WCLK	O	**Wait Clock Output** The real-time WCLK output is enabled by setting RTWCE bit in WCON (S:A7h). When enabled, the WCLK output produces a square wave signal with a period of one half the oscillator frequency.	P1.7
WR#	O	**Write** Write signal output to external memory.	P3.6
XTAL1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	–

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
XTAL2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	–

Note: The description of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the Non-Page mode chip configuration. If the chip is configured in Page mode operation, port 0 carries the lower address bits (A7:0) while port 2 carries the upper address bits (A15:8) and the data (D7:0).

Address Spaces

The TSC80251G2D derivatives implement four different address spaces:

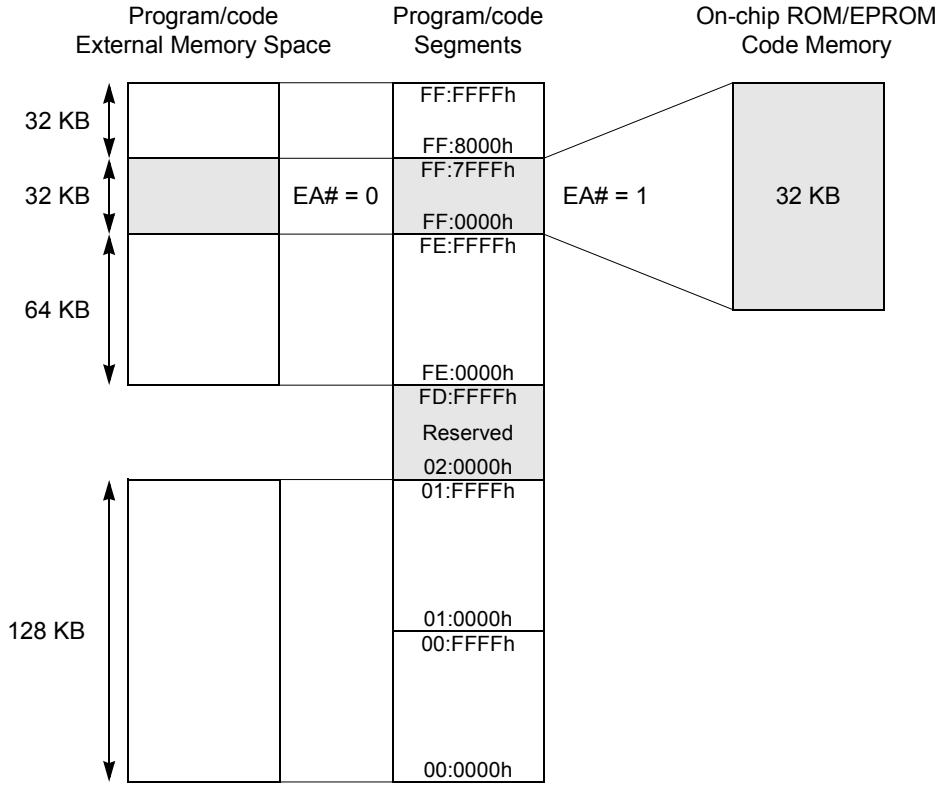
- On-chip ROM program/code memory (not present in ROMless devices)
- On-chip RAM data memory
- Special Function Registers (SFRs)
- Configuration array

Program/Code Memory

The TSC83251G2D and TSC87251G2D implement 32 KB of on-chip program/code memory. Figure 4 shows the split of the internal and external program/code memory spaces. If EA# is tied to a high level, the 32-Kbyte on-chip program memory is mapped in the lower part of segment FF: where the C251 core jumps after reset. The rest of the program/code memory space is mapped to the external memory. If EA# is tied to a low level, the internal program/code memory is not used and all the accesses are directed to the external memory.

The TSC83251G2D products provide the internal program/code memory in a masked ROM memory while the TSC87251G2D products provide it in an EPROM memory. For the TSC80251G2D products, there is no internal program/code memory and EA# must be tied to a low level.

Figure 4. Program/Code Memory Mapping



Note: Special care should be taken when the Program Counter (PC) increments:
If the program executes exclusively from on-chip code memory (not from external memory), beware of executing code from the upper eight bytes of the on-chip ROM (FF:7FF8h-FF:7FFFh). Because of its pipeline capability, the TSC80251G2D derivative may attempt to prefetch code from external memory (at an address above FF:7FFFh) and thereby disrupt I/O Ports 0 and 2. Fetching code constants from these 8 bytes does not affect Ports 0 and 2.
When PC reaches the end of segment FF:, it loops to the reset address FF:0000h (for

compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

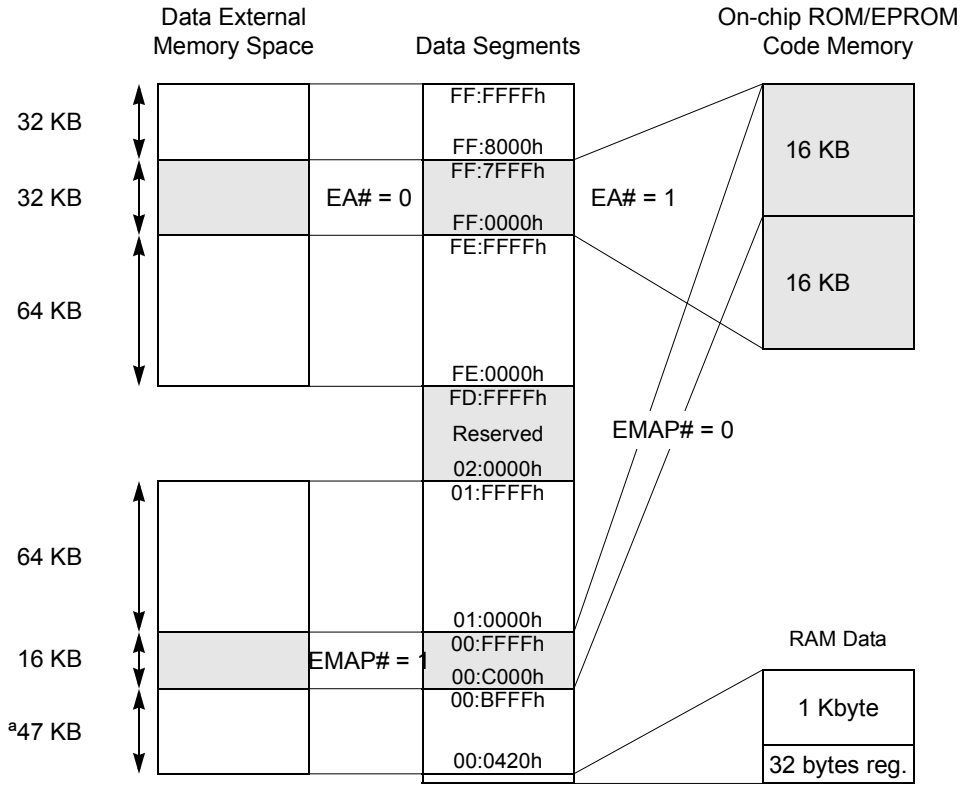
Data Memory

The TSC80251G2D derivatives implement 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip ROM/EPROM code of the TSC83251G2D/TSC87251G2D, its upper 16 KB are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure). However, if EA# is tied to a low level, the TSC80251G2D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 16 KB of the lower 32 KB of the segment FF:). If EMAP# bit is set, the on-chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

Figure 5. Data Memory Mapping



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Special Function Registers

The Special Function Registers (SFRs) of the TSC80251G2D derivatives fall into the categories detailed in Table 1 to Table 9.

SFRs are placed in a reserved on-chip memory region S: which is not represented in the data memory mapping (Figure 5). The relative addresses within S: of these SFRs are provided together with their reset values in Table . They are upward compatible with the SFRs of the standard 80C51 and the Intel's 80C251Sx family. In this table, the C251 core registers are identified by Note 1 and are described in the TSC80251 Programmer's Guide. The other SFRs are described in the TSC80251G1D Design Guide. All the SFRs are bit-addressable using the C251 instruction set.

Table 1. C251 Core SFRs

Mnemonic	Name
ACC(1)	Accumulator
B(1)	B Register
PSW	Program Status Word
PSW1	Program Status Word 1
SP(1)	Stack Pointer - LSB of SPX

Mnemonic	Name
SPH(1)	Stack Pointer High - MSB of SPX
DPL(1)	Data Pointer Low byte - LSB of DPTR
DPH(1)	Data Pointer High byte - MSB of DPTR
DPXL(1)	Data Pointer Extended Low byte of DPX - Region number

Note: 1. These SFRs can also be accessed by their corresponding registers in the register file.

Table 2. I/O Port SFRs

Mnemonic	Name
P0	Port 0
P1	Port 1

Mnemonic	Name
P2	Port 2
P3	Port 3

Table 3. Timers SFRs

Mnemonic	Name
TL0	Timer/Counter 0 Low Byte
TH0	Timer/Counter 0 High Byte
TL1	Timer/Counter 1 Low Byte
TH1	Timer/Counter 1 High Byte
TL2	Timer/Counter 2 Low Byte
TH2	Timer/Counter 2 High Byte
TCON	Timer/Counter 0 and 1 Control

Mnemonic	Name
TMOD	Timer/Counter 0 and 1 Modes
T2CON	Timer/Counter 2 Control
T2MOD	Timer/Counter 2 Mode
RCAP2L	Timer/Counter 2 Reload/Capture Low Byte
RCAP2H	Timer/Counter 2 Reload/Capture High Byte
WDTRST	WatchDog Timer Reset

Table 4. Serial I/O Port SFRs

Mnemonic	Name
SCON	Serial Control
SBUF	Serial Data Buffer
SADEN	Slave Address Mask

Mnemonic	Name
SADDR	Slave Address
BRL	Baud Rate Reload
BDRCON	Baud Rate Control

Table 5. SSLC SFRs

Mnemonic	Name
SSCON	Synchronous Serial control
SSDAT	Synchronous Serial Data
SSCS	Synchronous Serial Control and Status

Mnemonic	Name
SSADR	Synchronous Serial Address
SSBR	Synchronous Serial Bit Rate

Table 6. Event Waveform Control SFRs

Mnemonic	Name
CCON	EWC-PCA Timer/Counter Control
CMOD	EWC-PCA Timer/Counter Mode
CL	EWC-PCA Timer/Counter Low Register
CH	EWC-PCA Timer/Counter High Register
CCAPM0	EWC-PCA Timer/Counter Mode 0
CCAPM1	EWC-PCA Timer/Counter Mode 1
CCAPM2	EWC-PCA Timer/Counter Mode 2
CCAPM3	EWC-PCA Timer/Counter Mode 3
CCAPM4	EWC-PCA Timer/Counter Mode 4

Mnemonic	Name
CCAP0L	EWC-PCA Compare Capture Module 0 Low Register
CCAP1L	EWC-PCA Compare Capture Module 1 Low Register
CCAP2L	EWC-PCA Compare Capture Module 2 Low Register
CCAP3L	EWC-PCA Compare Capture Module 3 Low Register
CCAP4L	EWC-PCA Compare Capture Module 4 Low Register
CCAP0H	EWC-PCA Compare Capture Module 0 High Register
CCAP1H	EWC-PCA Compare Capture Module 1 High Register
CCAP2H	EWC-PCA Compare Capture Module 2 High Register
CCAP3H	EWC-PCA Compare Capture Module 3 High Register
CCAP4H	EWC-PCA Compare Capture Module 4 High Register

Table 7. System Management SFRs

Mnemonic	Name
PCON	Power Control
POWM	Power Management

Mnemonic	Name
CKRL	Clock Reload
WCON	Synchronous Real-Time Wait State Control

Table 8. Interrupt SFRs

Mnemonic	Name
IE0	Interrupt Enable Control 0
IE1	Interrupt Enable Control 1
IPH0	Interrupt Priority Control High 0

Mnemonic	Name
IPL0	Interrupt Priority Control Low 0
IPH1	Interrupt Priority Control High 1
IPL1	Interrupt Priority Control Low 1

Table 9. Keyboard Interface SFRs

Mnemonic	Name
P1IE	Port 1 Input Interrupt Enable
P1F	Port 1 Flag

Mnemonic	Name
P1LS	Port 1 Level Selection

Table 10. SFR Descriptions

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B(1) 0000 0000								F7h
E8h		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC(1) 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW(1) 0000 0000	PSW1(1) 0000 0000							D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IPL0 X000 0000	SADEN 0000 0000					SPH(1) 0000 0000		BFh
B0h	P3 1111 1111	IE1 XX0X XXX0	IPL1 XX0X XXX0	IPH1 XX0X XXX0				IPH0 X000 0000	B7h
A8h	IE0 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111						WDTRST 1111 1111	WCON XXXX XX00	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	P1LS 0000 0000	P1IE 0000 0000	P1F 0000 0000		9Fh
90h	P1 1111 1111		SSBR 0000 0000	SSCON(2)	SSCS(3)	SSDAT 0000 0000	SSADR 0000 0000		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	CKRL 0000 1000	POWM 0XXX XXXX	8Fh
80h	P0 1111 1111	SP(1) 0000 0111	DPL(1) 0000 0000	DPH(1) 0000 0000	DPXL(1) 0000 0001			PCON 0000 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. These registers are described in the TSC80251 Programmer's Guide (C251 core registers).
2. In TWI and SPI modes, SSCON is splitted in two separate registers. SSCON reset value is 0000 0000 in TWI mode and 0000 0100 in SPI mode.
3. In read and write modes, SSCS is splitted in two separate registers. SSCS reset value is 1111 1000 in read mode and 0000 0000 in write mode.

Configuration Bytes

The TSC80251G2D derivatives provide user design flexibility by configuring certain operating features at device reset. These features fall into the following categories:

- external memory interface (Page mode, address bits, programmed wait states and the address range for RD#, WR#, and PSEN#)
- source mode/binary mode opcodes
- selection of bytes stored on the stack by an interrupt
- mapping of the upper portion of on-chip code memory to region 00:

Two user configuration bytes UCONFIG0 (see Table 11) and UCONFIG1 (see Table 12) provide the information.

When EA# is tied to a low level, the configuration bytes are fetched from the external address space. The TSC80251G2D derivatives reserve the top eight bytes of the memory address space (FF:FFF8h-FF:FFFFh) for an external 8-byte configuration array. Only two bytes are actually used: UCONFIG0 at FF:FFF8h and UCONFIG1 at FF:FFF9h.

For the mask ROM devices, configuration information is stored in on-chip memory (see ROM Verifying). When EA# is tied to a high level, the configuration information is retrieved from the on-chip memory instead of the external address space and there is no restriction in the usage of the external memory.

Table 11. Configuration Byte 0
UCONFIG0

7	6	5	4	3	2	1	0
-	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** Set this bit when writing to UCONFIG0.
6	WSA1#	**Wait State A bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (all regions except 01:). WSA1# WSA0# Number of Wait States 0 0 3 0 1 2 1 0 1 1 1 0
5	WSA0#	
4	XALE#	**Extend ALE bit** Clear to extend the duration of the ALE pulse from T_{OSC} to $3 \cdot T_{OSC}$. Set to minimize the duration of the ALE pulse to $1 \cdot T_{OSC}$.
3	RD1	**Memory Signal Select bits** Specify a 18-bit, 17-bit or 16-bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13).
2	RD0	
1	PAGE#	**Page Mode Select bit**(1) Clear to select the faster Page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0. Set to select the non-Page mode(2) with A15:8 on Port 2 and A7:0/D7:0 on Port 0.
0	SRC	**Source Mode/Binary Mode Select bit** Clear to select the binary mode. Set to select the source mode.

Notes: 1. UCONFIG0 is fetched twice so it can be properly read both in Page or Non-Page modes. If P2.1 is cleared during the first data fetch, a Page mode configuration is used, otherwise the subsequent fetches are performed in Non-Page mode.
2. This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.

Table 12. Configuration Byte 1
UCONFIG1

7	6	5	4	3	2	1	0
CSIZE	**-**	**-**	**INTR**	**WSB**	**WSB1#**	**WSB0#**	**EMAP#**

Bit Number	Bit Mnemonic	Description
7	CSIZE TSC87251G2D	**On-Chip Code Memory Size bit**(1) Clear to select 16 KB of on-chip code memory (TSC87251G1D product). Set to select 32 KB of on-chip code memory (TSC87251G2D product).
	TSC80251G2D TSC83251G2D	**Reserved** Set this bit when writing to UCONFIG1.
6	-	**Reserved** Set this bit when writing to UCONFIG1.
5	-	**Reserved** Set this bit when writing to UCONFIG1.
4	INTR	**Interrupt Mode bit**(2) Clear so that the interrupts push two bytes onto the stack (the two lower bytes of the PC register). Set so that the interrupts push four bytes onto the stack (the three bytes of the PC register and the PSW1 register).
3	WSB	**Wait State B bit**(3) Clear to generate one wait state for memory region 01:. Set for no wait states for memory region 01:.
2	WSB1#	**Wait State B bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (only region 01:). WSB1# WSB0# Number of Wait States 0 0 3 0 1 2 1 0 1 1 1 0
1	WSB0#	
0	EMAP#	**On-Chip Code Memory Map bit** Clear to map the upper 16 KB of on-chip code memory (at FF:4000h-FF:7FFFh) to the data space (at 00:C000h-00:FFFFh). Set not to map the upper 16 KB of on-chip code memory (at FF:4000h-FF:7FFFh) to the data space.

Notes:
1. The CSIZE is only available on EPROM/OTPROM products.
2. Two or four bytes are transparently popped according to INTR when using the RETI instruction. INTR must be set if interrupts are used with code executing outside region FF:.
3. Use only for Step A compatibility; set this bit when WSB1:0# are used.

Configuration Byte 1

Table 13. Address Ranges and Usage of RD#, WR# and PSEN# Signals

RD1	RD0	P1.7	P3.7/RD#	PSEN#	WR#	External Memory
0	0	A17	A16	Read signal for all external memory locations	Write signal for all external memory locations	256 KB
0	1	I/O pin	A16	Read signal for all external memory locations	Write signal for all external memory locations	128 KB
1	0	I/O pin	I/O pin	Read signal for all external memory locations	Write signal for all external memory locations	64 KB
1	1	I/O pin	Read signal for regions 00: and 01:	Read signal for regions FE: and FF:	Write signal for all external memory locations	2×64 KB(1)

Notes: 1. This selection provides compatibility with the standard 80C51 hardware which has separate external memory spaces for data and code.

Instruction Set Summary

This section contains tables that summarize the instruction set. For each instruction there is a short description, its length in bytes, and its execution time in states (one state time is equal to two system clock cycles). There are two concurrent processes limiting the effective instruction throughput:

- Instruction Fetch
- Instruction Execution

Table 20 to Table 32 assume code executing from on-chip memory, then the CPU is fetching 16-bit at a time and this is never limiting the execution speed.

If the code is fetched from external memory, a pre-fetch queue will store instructions ahead of execution to optimize the memory bandwidth usage when slower instructions are executed. However, the effective speed may be limited depending on the average size of instructions (for the considered section of the program flow). The maximum average instruction throughput is provided by Table 14 depending on the external memory configuration (from Page Mode to Non-Page Mode and the maximum number of wait states). If the average size of instructions is not an integer, the maximum effective throughput is found by pondering the number of states for the neighbor integer values.

Table 14. Minimum Number of States per Instruction for given Average Sizes

Average size of Instructions (bytes)	Page Mode (states)	Non-page Mode (states)				
		0 Wait State	1 Wait State	2 Wait States	3 Wait States	4 Wait States
1	1	2	3	4	5	6
2	2	4	6	8	10	12
3	3	6	9	12	15	18
4	4	8	12	16	20	24
5	5	10	15	20	25	30

If the average execution time of the considered instructions is larger than the number of states given by Table 14, this larger value will prevail as the limiting factor. Otherwise, the value from Table 14 must be taken. This is providing a fair estimation of the execution speed but only the actual code execution can provide the final value.

Notation for Instruction Operands

Table 15 to Table 19 provide notation for Instruction Operands.

Table 15. Notation for Direct Addressing

Direct Address	Description	C251	C51
dir8	A direct 8-bit address. This can be a memory address (00h-7Fh) or a SFR address (80h-FFh). It is a byte (default), word or double word depending on the other operand.	3	3
dir16	A 16-bit memory address (00:0000h-00:FFFFh) used in direct addressing.	3	–

Table 16. Notation for Immediate Addressing

Immediate Address	Description	C251	C51
#data	An 8-bit constant that is immediately addressed in an instruction	3	3
#data16	A 16-bit constant that is immediately addressed in an instruction	3	–
#0data16 #1data16	A 32-bit constant that is immediately addressed in an instruction. The upper word is filled with zeros (#0data16) or ones (#1data16).	3	–
#short	A constant, equal to 1, 2, or 4, that is immediately addressed in an instruction.	3	–

Table 17. Notation for Bit Addressing

Direct Address	Description	C251	C51
bit51	A directly addressed bit (bit number = 00h-FFh) in memory or an SFR. Bits 00h-7Fh are the 128 bits in byte locations 20h-2Fh in the on-chip RAM. Bits 80h-FFh are the 128 bits in the 16 SFRs with addresses that end in 0h or 8h, S:80h, S:88h, S:90h,..., S:F0h, S:F8h.	–	3
bit	A directly addressed bit in memory locations 00:0020h-00:007Fh or in any defined SFR.	3	

Table 18. Notation for Destination in Control Instructions

Direct Address	Description	C251	C51
rel	A signed (two's complement) 8-bit relative address. The destination is -128 to +127 bytes relative to the next instruction's first byte.	3	3
addr11	An 11-bit target address. The target is in the same 2-Kbyte block of memory as the next instruction's first byte.	–	3
addr16	A 16-bit target address. The target can be anywhere within the same 64-Kbyte region as the next instruction's first byte.	–	3
addr24	A 24-bit target address. The target can be anywhere within the 16-Mbyte address space.	3	–

Table 19. Notation for Register Operands

Register	Description	C251	C51
at Ri	A memory location (00h-FFh) addressed indirectly via byte registers R0 or R1	–	3
Rn n	Byte register R0-R7 of the currently selected register bank Byte register index: n = 0-7	–	3
Rm Rmd Rms m, md, ms	Byte register R0-R15 of the currently selected register file Destination register Source register Byte register index: m, md, ms = 0-15	3	–
WRj WRjd WRjs at WRj at WRj +dis16 j, jd, js	Word register WR0, WR2, ..., WR30 of the currently selected register file Destination register Source register A memory location (00:0000h-00:FFFFh) addressed indirectly through word register WR0-WR30, is the target address for jump instructions. A memory location (00:0000h-00:FFFFh) addressed indirectly through word register (WR0-WR30) + 16-bit signed (two's complement) displacement value Word register index: j, jd, js = 0-30	3	–
DRk DRkd DRks at DRk at DRk +dis16 k, kd, ks	Dword register DR0, DR4, ..., DR28, DR56, DR60 of the currently selected register file Destination register Source register A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register DR0-DR28, DR56 and DR60, is the target address for jump instruction A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register (DR0-DR28, DR56, DR60) + 16-bit (two's complement) signed displacement value Dword register index: k, kd, ks = 0, 4, 8..., 28, 56, 60	3	–

Size and Execution Time for Instruction Families

Table 20. Summary of Add and Subtract Instructions

AddADD <dest>, <src>dest opnd ← dest opnd + src opnd SubtractSUB <dest>, <src>dest opnd ← dest opnd - src opnd Add with CarryADDC <dest>, <src>(A) ← (A) + src opnd + (CY) Subtract with BorrowSUBB <dest>, <src>(A) ← (A) - src opnd - (CY)						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
ADD	A, Rn	Register to ACC	1	1	2	2
	A, dir8	Direct address to ACC	2	1(2)	2	1(2)
	A, at Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
ADD/SUB	Rmd, Rms	Byte register to/from byte register	3	2	2	1
	WRjd, WRjs	Word register to/from word register	3	3	2	2
	DRkd, DRks	Dword register to/from dword register	3	5	2	4
	Rm, #data	Immediate 8-bit data to/from byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to/from word register	5	4	4	3
	DRk, #0data16	16-bit unsigned immediate data to/from dword register	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) to/from byte register	4	3(2)	3	2(2)
	WRj, dir8	Direct address (on-chip RAM or SFR) to/from word register	4	4	3	3
	Rm, dir16	Direct address (64K) to/from byte register	5	3(3)	4	2(3)
	WRj, dir16	Direct address (64K) to/from word register	5	4(4)	4	3(4)
	Rm, at WRj	Indirect address (64K) to/from byte register	4	3(3)	3	2(3)
	Rm, at DRk	Indirect address (16M) to/from byte register	4	4(3)	3	3(3)
ADDC/SUBB	A, Rn	Register to/from ACC with carry	1	1	2	2
	A, dir8	Direct address (on-chip RAM or SFR) to/from ACC with carry	2	1(2)	2	1(2)
	A, at Ri	Indirect address to/from ACC with carry	1	2	2	3
	A, #data	Immediate data to/from ACC with carry	2	1	2	1

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

4. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 21. Summary of Increment and Decrement Instructions

IncrementINC <dest>dest opnd ← dest opnd + 1 IncrementINC <dest>, <src>dest opnd ← dest opnd + src opnd DecrementDEC <dest>dest opnd ← dest opnd - 1 DecrementDEC <dest>, <src>dest opnd ← dest opnd - src opnd						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
INC DEC	A	ACC by 1	1	1	1	1
	Rn	Register by 1	1	1	2	2
	dir8	Direct address (on-chip RAM or SFR) by 1	2	2(2)	2	2(2)
	at Ri	Indirect address by 1	1	3	2	4
INC DEC	Rm, #short	Byte register by 1, 2, or 4	3	2	2	1
	WRj, #short	Word register by 1, 2, or 4	3	2	2	1
INC	DRk, #short	Double word register by 1, 2, or 4	3	4	2	3
DEC	DRk, #short	Double word register by 1, 2, or 4	3	5	2	4
INC	DPTR	Data pointer by 1	1	1	1	1

Notes: 1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 22. Summary of Compare Instructions

CompareCMP <dest>, <src>dest opnd - src opnd						
			Binary Mode		Source Mode	
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Bytes**	**States**	**Bytes**	**States**
CMP	Rmd, Rms	Register with register	3	2	2	1
	WRjd, WRjs	Word register with word register	3	3	2	2
	DRkd, DRks	Dword register with dword register	3	5	2	4
	Rm, #data	Register with immediate data	4	3	3	2
	WRj, #data16	Word register with immediate 16-bit data	5	4	4	3
	DRk, #0data16	Dword register with zero-extended 16-bit immediate data	5	6	4	5
	DRk, #1data16	Dword register with one-extended 16-bit immediate data	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) with byte register	4	3(1)	3	2(1)
	WRj, dir8	Direct address (on-chip RAM or SFR) with word register	4	4	3	3
	Rm, dir16	Direct address (64K) with byte register	5	3(2)	4	2(2)
	WRj, dir16	Direct address (64K) with word register	5	4(3)	4	3(3)
	Rm, at WRj	Indirect address (64K) with byte register	4	3(2)	3	2(2)
	Rm, at DRk	Indirect address (16M) with byte register	4	4(2)	3	3(2)

Notes:
1. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Logical AND[1]ANL <dest>, <src>dest opnd ← dest opnd Λ src opnd
Logical OR[1]ORL <dest>, <src>dest opnd ← dest opnd ς src opnd
Logical Exclusive OR[1]XRL <dest>, <src>dest opnd ← dest opnd ∀ src opnd
Clear[1]CLR A(A) ← 0
Complement[1]CPL A(A) ← ∅ (A)
Rotate LeftRL $A(A)_{n+1} \leftarrow (A)_n$, n = 0..6
$(A)_0 \leftarrow (A)_7$
Rotate Left CarryRLC $A(A)_{n+1} \leftarrow (A)_n$, n = 0..6
$(CY) \leftarrow (A)_7$
$(A)_0 \leftarrow (CY)$
Rotate RightRR $A(A)_{n-1} \leftarrow (A)_n$, n = 7..1
$(A)_7 \leftarrow (A)_0$
Rotate Right CarryRRC $A(A)_{n-1} \leftarrow (A)_n$, n = 7..1
$(CY) \leftarrow (A)_0$
$(A)_7 \leftarrow (CY)$

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ANL ORL XRL	A, Rn	register to ACC	1	1	2	2
	A, dir8	Direct address (on-chip RAM or SFR) to ACC	2	1[3]	2	1[3]
	A, at Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
	dir8, A	ACC to direct address	2	2[4]	2	2[4]
	dir8, #data	Immediate 8-bit data to direct address	3	3[4]	3	3[4]
	Rmd, Rms	Byte register to byte register	3	2	2	1
	WRjd, WRjs	Word register to word register	3	3	2	2
	Rm, #data	Immediate 8-bit data to byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to word register	5	4	4	3
	Rm, dir8	Direct address (on-chip RAM or SFR) to byte register	4	3[3]	3	2[3]
	WRj, dir8	Direct address (on-chip RAM or SFR) to word register	4	4	3	3
	Rm, dir16	Direct address (64K) to byte register	5	3[5]	4	2[5]
	WRj, dir16	Direct address (64K) to word register	5	4[6]	4	3[6]
	Rm, at WRj	Indirect address (64K) to byte register	4	3[5]	3	2[5]
	Rm, at DRk	Indirect address (16M) to byte register	4	4[5]	3	3[5]
CLR	A	Clear ACC	1	1	1	1
CPL	A	Complement ACC	1	1	1	1
RL	A	Rotate ACC left	1	1	1	1
RLC	A	Rotate ACC left through CY	1	1	1	1
RR	A	Rotate ACC right	1	1	1	1
RRC	A	Rotate ACC right through CY	1	1	1	1

Notes: 1. Logical instructions that affect a bit are in Table 27.
2. A shaded cell denotes an instruction in the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
5. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 23. Summary of Logical Instructions (2/2)

Shift Left LogicalSLL <dest><dest>$_0 \leftarrow 0$
<dest>$_{n+1} \leftarrow$ <dest>$_n$, n = 0..msb-1
(CY) $\leftarrow$ <dest>$_{msb}$
Shift Right ArithmeticSRA <dest><dest>$_{msb} \leftarrow$ <dest>$_{msb}$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
Shift Right LogicalSRL <dest><dest>$_{msb} \leftarrow 0$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
SwapSWAP $AA_{3:0}$ $A_{7:4}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
SLL	Rm	Shift byte register left through the MSB	3	2	2	1
	WRj	Shift word register left through the MSB	3	2	2	1
SRA	Rm	Shift byte register right	3	2	2	1
	WRj	Shift word register right	3	2	2	1
SRL	Rm	Shift byte register left	3	2	2	1
	WRj	Shift word register left	3	2	2	1
SWAP	A	Swap nibbles within ACC	1	2	1	2

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Table 24. Summary of Multiply, Divide and Decimal-adjust Instructions

MultiplyMUL AB(B:A) ← (A)×(B)
MUL <dest>, <src>extended dest opnd ← dest opnd × src opnd

DivideDIV AB(A) ← Quotient ((A)/(B))
(B) ← Remainder ((A)/(B))

DivideDIV <dest>, <src>ext. dest opnd high ← Quotient (dest opnd/src opnd)
ext. dest opnd low ← Remainder (dest opnd/src opnd)

Decimal-adjust ACCDA AIF [[$(A)_{3:0}$ > 9] ∨ [(AC) = 1]]
for Addition (BCD) THEN $(A)_{3:0} \leftarrow (A)_{3:0}$ + 6 !affects CY;
IF [[$(A)_{7:4}$ > 9] ∨ [(CY) = 1]]
THEN $(A)_{7:4} \leftarrow (A)_{7:4}$ + 6

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MUL	AB	Multiply A and B	1	5	1	5
	Rmd, Rms	Multiply byte register and byte register	3	6	2	5
	WRjd, WRjs	Multiply word register and word register	3	12	2	11
DIV	AB	Divide A and B	1	10	1	10
	Rmd, Rms	Divide byte register and byte register	3	11	2	10
	WRjd, WRjs	Divide word register and word register	3	21	2	20
DA	A	Decimal adjust ACC	1	1	1	1

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Table 25. Summary of Move Instructions (1/3)

Move to High wordMOVH <dest>, <src>dest $opnd_{31:16}$ ← src opnd Move with Sign extensionMOVS <dest>, <src>dest opnd ← src opnd with sign extend Move with Zero extensionMOVZ <dest>, <src>dest opnd ← src opnd with zero extend Move CodeMOVC A, <src>(A) ← src opnd Move eXtendedMOVX <dest>, <src>dest opnd ← src opnd						
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
MOVH	DRk, #data16	16-bit immediate data into upper word of dword register	5	3	4	2
MOVS	WRj, Rm	Byte register to word register with sign extension	3	2	2	1
MOVZ	WRj, Rm	Byte register to word register with zeros extension	3	2	2	1
MOVC	A, at A +DPTR	Code byte relative to DPTR to ACC	1	6(3)	1	6(3)
	A, at A +PC	Code byte relative to PC to ACC	1	6(3)	1	6(3)
MOVX	A, at Ri	Extended memory (8-bit address) to ACC(2)	1	4	1	5
	A, at DPTR	Extended memory (16-bit address) to ACC(2)	1	3(4)	1	3(4)
	at Ri, A	ACC to extended memory (8-bit address)(2)	1	4	1	4
	at DPTR, A	ACC to extended memory (16-bit address)(2)	1	4(3)	1	4(3)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. Extended memory addressed is in the region specified by DPXL (reset value = 01h).
3. If this instruction addresses external memory location, add N+1 to the number of states (N: number of wait states).
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

Table 26. Summary of Move Instructions (2/3)

Move[1] MOV <dest>, <src> dest opnd ← src opnd						
			Binary Mode		Source Mode	
Mnemonic	<dest>, <src>[2]	Comments	Bytes	States	Bytes	States
MOV	A, Rn	Register to ACC	1	1	2	2
	A, dir8	Direct address (on-chip RAM or SFR) to ACC	2	1[3]	2	1[3]
	A, at Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
	Rn, A	ACC to register	1	1	2	2
	Rn, dir8	Direct address (on-chip RAM or SFR) to register	2	1[3]	3	2[3]
	Rn, #data	Immediate data to register	2	1	3	2
	dir8, A	ACC to direct address (on-chip RAM or SFR)	2	2[3]	2	2[3]
	dir8, Rn	Register to direct address (on-chip RAM or SFR)	2	2[3]	3	3[3]
	dir8, dir8	Direct address to direct address (on-chip RAM or SFR)	3	3[4]	3	3[4]
	dir8, at Ri	Indirect address to direct address (on-chip RAM or SFR)	2	3[3]	3	4[3]
	dir8, #data	Immediate data to direct address (on-chip RAM or SFR)	3	3[3]	3	3[3]
	at Ri, A	ACC to indirect address	1	3	2	4
	at Ri, dir8	Direct address (on-chip RAM or SFR) to indirect address	2	3[3]	3	4[3]
	at Ri, #data	Immediate data to indirect address	2	3	3	4
	DPTR, #data16	Load Data Pointer with a 16-bit constant	3	2	3	2

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions from the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. Apply note 3 for each dir8 operand.

Move[1] MOV <dest>, <src> dest opnd ← src opnd						
			Binary Mode		Source Mode	
Mnemonic	<dest>, <src>[1]	Comments	Bytes	States	Bytes	States
MOV	Rmd, Rms	Byte register to byte register	3	2	2	1
MOV	WRjd, WRjs	Word register to word register	3	2	2	1
MOV	DRkd, DRks	Dword register to dword register	3	3	2	2
MOV	Rm, #data	Immediate 8-bit data to byte register	4	3	3	2
MOV	WRj, #data16	Immediate 16-bit data to word register	5	3	4	2
MOV	DRk, #0data16	zero-ext 16bit immediate data to dword register	5	5	4	4
MOV	DRk, #1data16	one-ext 16bit immediate data to dword register	5	5	4	4
MOV	Rm, dir8	Direct address (on-chip RAM or SFR) to byte register	4	3[3]	3	2[3]
MOV	WRj, dir8	Direct address (on-chip RAM or SFR) to word register	4	4	3	3
MOV	DRk, dir8	Direct address (on-chip RAM or SFR) to dword register	4	6	3	5
MOV	Rm, dir16	Direct address (64K) to byte register	5	3[4]	4	2[4]
MOV	WRj, dir16	Direct address (64K) to word register	5	4[5]	4	3[5]
MOV	DRk, dir16	Direct address (64K) to dword register	5	6[6]	4	5[6]
MOV	Rm, at WRj	Indirect address (64K) to byte register	4	3[4]	3	2[4]
MOV	Rm, at DRk	Indirect address (16M) to byte register	4	4[4]	3	3[4]
MOV	WRjd, at WRjs	Indirect address (64K) to word register	4	4[5]	3	3[5]
MOV	WRj, at DRk	Indirect address (16M) to word register	4	5[5]	3	4[5]
MOV	dir8, Rm	Byte register to direct address (on-chip RAM or SFR)	4	4[3]	3	3[3]
MOV	dir8, WRj	Word register to direct address (on-chip RAM or SFR)	4	5	3	4
MOV	dir8, DRk	Dword register to direct address (on-chip RAM or SFR)	4	7	3	6
MOV	dir16, Rm	Byte register to direct address (64K)	5	4[4]	4	3[4]
MOV	dir16, WRj	Word register to direct address (64K)	5	5[5]	4	4[5]
MOV	dir16, DRk	Dword register to direct address (64K)	5	7[6]	4	6[6]
MOV	at WRj, Rm	Byte register to indirect address (64K)	4	4[4]	3	3[4]
MOV	at DRk, Rm	Byte register to indirect address (16M)	4	5[4]	3	4[4]
MOV	at WRjd, WRjs	Word register to indirect address (64K)	4	5[5]	3	4[5]
MOV	at DRk, WRj	Word register to indirect address (16M)	4	6[5]	3	5[5]
MOV	Rm, at WRj +dis16	Indirect with 16-bit displacement (64K) to byte register	5	6[4]	4	5[4]
MOV	WRj, at WRj +dis16	Indirect with 16-bit displacement (64K) to word register	5	7[5]	4	6[5]
MOV	Rm, at DRk +dis24	Indirect with 16-bit displacement (16M) to byte register	5	7[4]	4	6[4]

MOV	WRj, at WRj +dis24	Indirect with 16-bit displacement (16M) to word register	5	8[5]	4	7[5]
MOV	at WRj +dis16, Rm	Byte register to indirect with 16-bit displacement (64K)	5	6[4]	4	5[4]
MOV	at WRj +dis16, WRj	Word register to indirect with 16-bit displacement (64K)	5	7[5]	4	6[5]
MOV	at DRk +dis24, Rm	Byte register to indirect with 16-bit displacement (16M)	5	7[4]	4	6[4]
MOV	at DRk +dis24, WRj	Word register to indirect with 16-bit displacement (16M)	5	8[5]	4	7[5]

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

Table 27. Summary of Bit Instructions

Clear BitCLR <dest>dest opnd ← 0						
Set BitSETB <dest>dest opnd ← 1						
Complement BitCPL <dest>dest opnd ← ∅ bit						
AND Carry with BitANL CY, <src>(CY) ← (CY) ∧ src opnd						
AND Carry with Complement of BitANL CY, /<src>(CY) ← (CY) ∧ ∅ src opnd						
OR Carry with BitORL CY, <src>(CY) ← (CY) ∨ src opnd						
OR Carry with Complement of BitORL CY, /<src>(CY) ← (CY) ∨ ∅ src opnd						
Move Bit to CarryMOV CY, <src>(CY) ← src opnd						
Move Bit from CarryMOV <dest>, CYdest opnd ← (CY)						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
CLR	CY	Clear carry	1	1	1	1
	bit51	Clear direct bit	2	2(3)	2	2(3)
	bit	Clear direct bit	4	4(3)	3	3(3)
SETB	CY	Set carry	1	1	1	1
	bit51	Set direct bit	2	2(3)	2	2(3)
	bit	Set direct bit	4	4(3)	3	3(3)
CPL	CY	Complement carry	1	1	1	1
	bit51	Complement direct bit	2	2(3)	2	2(3)
	bit	Complement direct bit	4	4(3)	3	3(3)
ANL	CY, bit51	And direct bit to carry	2	1(2)	2	1(2)
	CY, bit	And direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	And complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	And complemented direct bit to carry	4	3(2)	3	2(2)
ORL	CY, bit51	Or direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Or direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	Or complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	Or complemented direct bit to carry	4	3(2)	3	2(2)
MOV	CY, bit51	Move direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Move direct bit to carry	4	3(2)	3	2(2)
	bit51, CY	Move carry to direct bit	2	2(3)	2	2(3)
	bit, CY	Move carry to direct bit	4	4(3)	3	3(3)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 28. Summary of Exchange, Push and Pop Instructions

Exchange bytesXCH A, <src>(A) ↔ src opnd Exchange DigitXCHD A, <src>$(A)_{3:0}$ ↔ src $opnd_{3:0}$ PushPUSH <src>(SP) ← (SP) +1; ((SP)) ← src opnd; (SP) ← (SP) + size (src opnd) - 1 PopPOP <dest>(SP) ← (SP) - size (dest opnd) + 1; dest opnd ← ((SP)); (SP) ← (SP) -1						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
XCH	A, Rn	ACC and register	1	3	2	4
	A, dir8	ACC and direct address (on-chip RAM or SFR)	2	3(3)	2	3(3)
	A, at Ri	ACC and indirect address	1	4	2	5
XCHD	A, at Ri	ACC low nibble and indirect address (256 bytes)	1	4	2	5
PUSH	dir8	Push direct address onto stack	2	2(2)	2	2(2)
	#data	Push immediate data onto stack	4	4	3	3
	#data16	Push 16-bit immediate data onto stack	5	5	4	5
	Rm	Push byte register onto stack	3	4	2	3
	WRj	Push word register onto stack	3	5	2	4
	DRk	Push double word register onto stack	3	9	2	8
POP	dir8	Pop direct address (on-chip RAM or SFR) from stack	2	3(2)	2	3(2)
	Rm	Pop byte register from stack	3	3	2	2
	WRj	Pop word register from stack	3	5	2	4
	DRk	Pop double word register from stack	3	9	2	8

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 29. Summary of Conditional Jump Instructions (1/2)

Jump conditional on statusJcc rel(PC) ← (PC) + size (instr); IF [cc] THEN (PC) ← (PC) + rel						
			Binary Mode		Source Mode	
Mnemonic	**<dest>, <src>[1]**	**Comments**	**Bytes**	**States**	**Bytes**	**States**
JC	rel	Jump if carry	2	1/4[3]	2	1/4[3]
JNC	rel	Jump if not carry	2	1/4[3]	2	1/4[3]
JE	rel	Jump if equal	3	2/5[3]	2	1/4[3]
JNE	rel	Jump if not equal	3	2/5[3]	2	1/4[3]
JG	rel	Jump if greater than	3	2/5[3]	2	1/4[3]
JLE	rel	Jump if less than, or equal	3	2/5[3]	2	1/4[3]
JSL	rel	Jump if less than (signed)	3	2/5[3]	2	1/4[3]
JSLE	rel	Jump if less than, or equal (signed)	3	2/5[3]	2	1/4[3]
JSG	rel	Jump if greater than (signed)	3	2/5[3]	2	1/4[3]
JSGE	rel	Jump if greater than or equal (signed)	3	2/5[3]	2	1/4[3]

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. In internal execution only, add 1 to the number of states of the ‘jump taken’ if the destination address is internal and odd.

Table 30. Summary of Conditional Jump Instructions (2/2)

Jump if bitJB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 1] THEN (PC) ← (PC) + rel

Jump if not bitJNB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 0] THEN (PC) ← (PC) + rel

Jump if bit and clearJBC <dest>, rel(PC) ← (PC) + size (instr);
IF [dest opnd = 1] THEN
dest opnd ← 0
(PC) ← (PC) + rel

Jump if accumulator is zeroJZ rel(PC) ← (PC) + size (instr);
IF [(A) = 0] THEN (PC) ← (PC) + rel

Jump if accumulator is not zeroJNZ rel(PC) ← (PC) + size (instr);
IF [(A) ≠ 0] THEN (PC) ← (PC) + rel

Compare and jump if not equalCJNE <src1>, <src2>, rel(PC) ← (PC) + size (instr);
IF [src opnd1 < src opnd2] THEN (CY) ← 1
IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0
IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel

Decrement and jump if not zeroDJNZ <dest>, rel(PC) ← (PC) + size (instr); dest opnd ← dest opnd -1;
IF [φ (Z)] THEN (PC) ← (PC) + rel

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode[2]		Source Mode[2]	
			Bytes	States	Bytes	States
JB	bit51, rel	Jump if direct bit is set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is set	5	4/7[3][6]	4	3/6[3][6]
JNB	bit51, rel	Jump if direct bit is not set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is not set	5	4/7[3][6]	4	3/6[3]
JBC	bit51, rel	Jump if direct bit is set & clear bit	3	4/7[5][6]	3	4/7[5][6]
	bit, rel	Jump if direct bit of 8-bit address location is set and clear	5	7/10[5][6]	4	6/9[5][6]
JZ	rel	Jump if ACC is zero	2	2/5[6]	2	2/5[6]
JNZ	rel	Jump if ACC is not zero	2	2/5[6]	2	2/5[6]
CJNE	A, dir8, rel	Compare direct address to ACC and jump if not equal	3	2/5[3][6]	3	2/5[3][6]
	A, #data, rel	Compare immediate to ACC and jump if not equal	3	2/5[6]	3	2/5[6]
	Rn, #data, rel	Compare immediate to register and jump if not equal	3	2/5[6]	4	3/6[6]
	at Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	3/6[6]	4	4/7[6]
DJNZ	Rn, rel	Decrement register and jump if not zero	2	2/5[6]	3	3/6[6]
	dir8, rel	Decrement direct address and jump if not zero	3	3/6[4][6]	3	3/6[4][6]

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states.

Add 3 if it addresses a Peripheral SFR.

5. If this instruction addresses an I/O Port (Px, x = 0-3), add 3 to the number of states. Add 5 if it addresses a Peripheral SFR.
6. In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.

Table 31. Summary of Unconditional Jump Instructions

Absolute jumpAJMP <src>(PC) ← (PC) +2; $(PC)_{10:0}$ ← src opnd						
Extended jumpEJMP <src>(PC) ← (PC) + size (instr); $(PC)_{23:0}$ ← src opnd						
Long jumpLJMP <src>(PC) ← (PC) + size (instr); $(PC)_{15:0}$ ← src opnd						
Short jumpSJMP rel(PC) ← (PC) +2; (PC) ← (PC) +rel						
Jump indirectJMP at A +DPTR$(PC)_{23:16}$ ← FFh; $(PC)_{15:0}$ ← (A) + (DPTR)						
No operationNOP(PC) ← (PC) +1						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
AJMP	addr11	Absolute jump	2	3(2)(3)	2	3(2)(3)
EJMP	addr24	Extended jump	5	6(2)(4)	4	5(2)(4)
	at DRk	Extended jump (indirect)	3	7(2)(4)	2	6(2)(4)
LJMP	at WRj	Long jump (indirect)	3	6(2)(4)	2	5(2)(4)
	addr16	Long jump (direct address)	3	5(2)(4)	3	5(2)(4)
SJMP	rel	Short jump (relative address)	2	4(2)(4)	2	4(2)(4)
JMP	at A +DPTR	Jump indirect relative to the DPTR	1	5(2)(4)	1	5(2)(4)
NOP		No operation (Jump never)	1	1	1	1

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 3 to the number of states if the destination address is external.

Table 32. Summary of Call and Return Instructions

Absolute callACALL <src>(PC) ← (PC) +2; push $(PC)_{15:0}$;
$(PC)_{10:0}$ ← src opnd
Extended callECALL <src>(PC) ← (PC) + size (instr); push $(PC)_{23:0}$;
$(PC)_{23:0}$ ← src opnd
Long callLCALL <src>(PC) ← (PC) + size (instr); push $(PC)_{15:0}$;
$(PC)_{15:0}$ ← src opnd
Return from subroutineRETpop $(PC)_{15:0}$
Extended return from subroutineERETpop $(PC)_{23:0}$
Return from interruptRETIIF [INTR = 0] THEN pop $(PC)_{15:0}$
IF [INTR = 1] THEN pop $(PC)_{23:0}$; pop (PSW1)
Trap interruptTRAP(PC) ← (PC) + size (instr);
IF [INTR = 0] THEN push $(PC)_{15:0}$
IF [INTR = 1] THEN push (PSW1); push $(PC)_{23:0}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ACALL	addr11	Absolute subroutine call	2	9(2)(3)	2	9(2)(3)
ECALL	at DRk	Extended subroutine call (indirect)	3	14(2)(3)	2	13(2)(3)
	addr24	Extended subroutine call	5	14(2)(3)	4	13(2)(3)
LCALL	at WRj	Long subroutine call (indirect)	3	10(2)(3)	2	9(2)(3)
	addr16	Long subroutine call	3	9(2)(3)	3	9(2)(3)
RET		Return from subroutine	1	7(2)	1	7(2)
ERET		Extended subroutine return	3	9(2)	2	8(2)
RETI		Return from interrupt	1	7(2)(4)	1	7(2)(4)
TRAP		Jump to the trap interrupt vector	2	12(4)	1	11(4)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 5 to the number of states if INTR = 1.

Programming and Verifying Non-volatile Memory

Internal Features

The internal non-volatile memory of the TSC80251G2D derivatives contains five different areas:

- Code Memory
- Configuration Bytes
- Lock Bits
- Encryption Array
- Signature Bytes

EPROM/OTPROM Devices

All the internal non-volatile memory but the Signature Bytes of the TSC87251G2D products is made of EPROM cells. The Signature Bytes of the TSC87251G2D products are made of Mask ROM.

The TSC87251G2D products are programmed and verified in the same manner as Atmel's TSC87251G1A, using a SINGLE-PULSE algorithm, which programs at V_{PP} = 12.75V using only one 100µs pulse per byte. This results in a programming time of less than 10 seconds for the 32 kilobytes on-chip code memory.

The EPROM of the TSC87251G2D products in Window package is erasable by Ultra-Violet radiation(1) (UV). UV erasure set all the EPROM memory cells to one and allows reprogramming. The quartz window must be covered with an opaque label(2) when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, as to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die during device operation may cause a logical malfunction.

The TSC87251G2D products in plastic packages are One Time Programmable (OTP). An EPROM cell cannot be reset by UV once programmed to zero.

Notes:
1. The recommended erasure procedure is exposure to ultra-violet light (at 2537 Å) to an integrated dose of at least 20 W-sec/cm^2. Exposing the EPROM to an ultra-violet lamp of 12000 µW/cm^2 rating for 30 minutes should be sufficient.
2. Erasure of the EPROM begins to occur when the chip is exposed to light wavelength shorter than 4000 Å. Since sunlight and fluorescent light have wavelength in this range, exposure to these light sources over an extended time (1 week in sunlight or 3 years in room-level fluorescent lighting) could cause inadvertent erasure.

Mask ROM Devices

All the internal non-volatile memory of TSC83251G2D products is made of Mask ROM cells. They can only be verified by the user, using the same algorithm as the EPROM/OTPROM devices.

ROMless Devices

The TSC80251G2D products do not include on-chip Configuration Bytes, Code Memory and Encryption Array. They only include Signature Bytes made of Mask ROM cells which can be read using the same algorithm as the EPROM/OTPROM devices.

Security Features

In some microcontroller applications, it is desirable that the user's program code be secured from unauthorized access. The TSC83251G2D and TSC87251G2D offer two kinds of protection for program code stored in the on-chip array:

- Program code in the on-chip Code Memory is encrypted when read out for verification if the Encryption Array isprogrammed.
- A three-level lock bit system restricts external access to the on-chip code memory.

Lock Bit System

The TSC87251G2D products implement 3 levels of security for User's program as described in Table 33. The TSC83251G2D products implement only the first level of security.

Level 0 is the level of an erased part and does not enable any security features.

Level 1 locks the programming of the User's internal Code Memory, the Configuration Bytes and the Encryption Array.

Level 2 locks the verifying of the User's internal Code Memory. It is always possible to verify the Configuration Bytes and the Lock Bits. It is not possible to verify the Encryption Array.

Level 3 locks the external execution.

Table 33. Lock Bits Programming

Level	Lock bits LB[2:0]	Internal Execution	External Execution	Verification	Programming	External PROM read (MOVC)
0	000	Enable	Enable	Enable(1)	Enable	Enable(2)
1	001	Enable	Enable	Enable(1)	Disable	Disable
2	01x(3)	Enable	Enable	Disable	Disable	Disable
3	1xx(3)	Enable	Disable	Disable	Disable	Disable

Notes: 1. Returns encrypted data if Encryption Array is programmed.
2. Returns non encrypted data.
3. x means don't care. Level 2 always enables level 1, and level 3 always enables levels 1 and 2.

The security level may be verified according to Table 34.

Table 34. Lock Bits Verifying

Level	Lock bits Data(1)
0	xxxxx000
1	xxxxx001
2	xxxxx01x
3	xxxxx1xx

Note: 1. x means don't care.

Encryption Array

The TSC83251G2D and TSC87251G2D products include a 128-byte Encryption Array located in non-volatile memory outside the memory address space. During verification of the on-chip code memory, the seven low-order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive-NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

To preserve the secrecy of the encryption key byte sequence, the Encryption Array can not be verified.

Notes:
1. When a MOVC instruction is executed, the content of the ROM is not encrypted. In order to fully protect the user program code, the lock bit level 1 (see Table 33) must always be set when encryption is used.
2. If the encryption feature is implemented, the portion of the on-chip code memory that does not contain program code should be filled with “random” byte values to prevent the encryption key sequence from being revealed.

Signature Bytes

The TSC80251G2D derivatives contain factory-programmed Signature Bytes. These bytes are located in non-volatile memory outside the memory address space at 30h, 31h, 60h and 61h. To read the Signature Bytes, perform the procedure described in section Verify Algorithm, using the verify signature mode (see Table 37). Signature byte values are listed in Table 35.

Table 35. Signature Bytes (Electronic ID)

		Signature Address	Signature Data
Vendor	Atmel	30h	58h
Architecture	C251	31h	40h
Memory	32 kilobytes EPROM or OTPROM	60h	F7h
	32 kilobytes MaskROM or ROMless		77h
Revision	TSC80251G2D derivative	61h	FDh

Programming Algorithm

Figure 6 shows the hardware setup needed to program the TSC87251G2D EPROM/OTPROM areas:

- The chip has to be put under reset and maintained in this state until completion of the programming sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be to forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the programming sequence (see below).
- The voltage on the EA# pin must be set to V_{DD}.
- The programming mode is selected according to the code applied on Port 0 (see Table 36). It has to be applied until the completion of this programming operation.
- The programming address is applied on Ports 1 and 3 which are respectively the Most Significant Byte (MSB) and the Least Significant Byte (LSB) of the address.
- The programming data are applied on Port 2.
- The EPROM Programming is done by raising the voltage on the EA# pin to V_{PP}, then by generating a low level pulse on ALE/PROG# pin.
- The voltage on the EA# pin must be lowered to V_{DD} before completing the programming operation.
- It is possible to alternate programming and verifying operation (See Paragraph Verify Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to V_{DD} before performing the verifying operation.

- PSEN# and the other control signals have to be released to complete a sequence of programming operations or a sequence of programming and verifying operations.

Figure 6. Setup for Programming

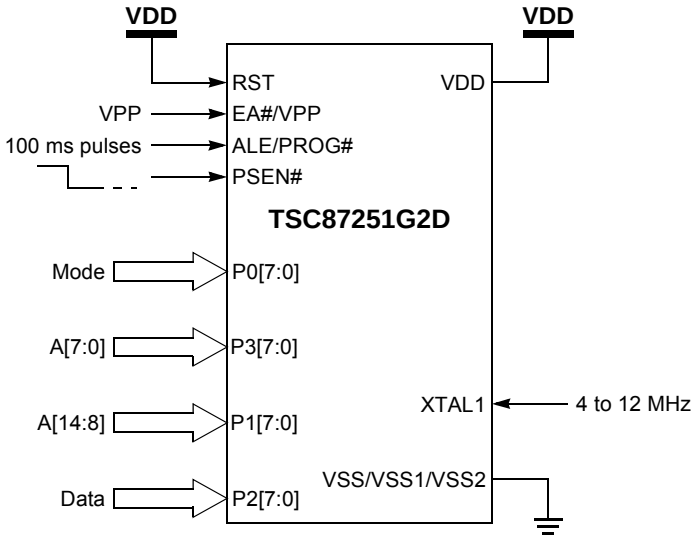


Table 36. Programming Modes

ROM Area[1]	RST	EA#/VPP	PSEN #	ALE/PROG#[2]	P0	P2	P1(MSB) P3(LSB)
On-chip Code Memory	1	V_{PP}	0	1 Pulse	68h	Data	16-bit Address 0000h-7FFFh (32 kilobytes)
Configuration Bytes	1	V_{PP}	0	1 Pulse	69h	Data	CONFIG0: FFF8h CONFIG1: FFF9h
Lock Bits	1	V_{PP}	0	1 Pulse	6Bh	X	LB0: 0001h LB1: 0002h LB2: 0003h
Encryption Array	1	V_{PP}	0	1 Pulse	6Ch	Data	0000h-007Fh

Notes: 1. Signature Bytes are not user-programmable.
2. The ALE/PROG# pulse waveform is shown in Figure 23 page 59.

Verify Algorithm

Figure 7 shows the hardware setup needed to verify the TSC87251G2D EPROM/OTPROM or TSC83251G2D ROM areas:

- The chip has to be put under reset and maintained in this state until the completion of the verifying sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be to forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the verifying sequence (see below).
- The voltage on the EA# pin must be set to V_{DD} and ALE must be set to a high level.
- The Verifying Mode is selected according to the code applied on Port 0. It has to be applied until the completion of this verifying operation.
- The verifying address is applied on Ports 1 and 3 which are respectively the MSB and the LSB of the address.

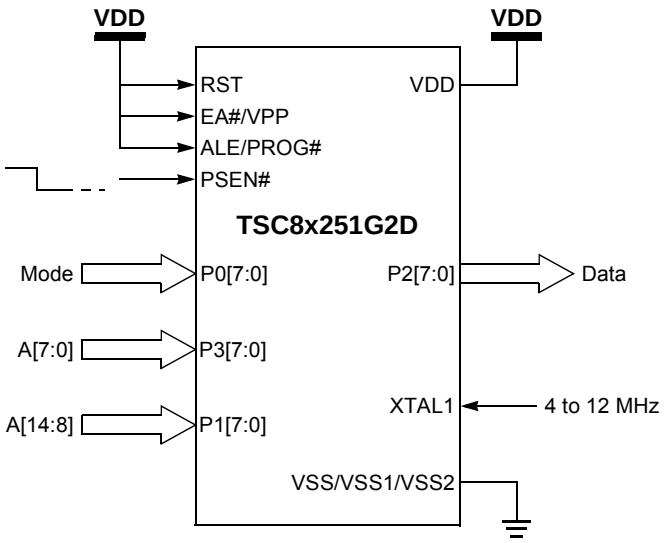
- Then device is driving the data on Port 2.
- It is possible to alternate programming and verification operation (see Paragraph Programming Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to V_{DD} before performing the verifying operation.
- PSEN# and the other control signals have to be released to complete a sequence of verifying operations or a sequence of programming and verifying operations.

Table 37. Verifying Modes

ROM Area[1]	RST	EA#/VPP	PSEN#	ALE/PROG#	P0	P2	P1(MSB) P3(LSB)
On-chip code memory	1	1	0	1	28h	Data	16-bit Address 0000h-7FFFh (32 kilobytes)
Configuration Bytes	1	1	0	1	29h	Data	CONFIG0: FFF8h CONFIG1: FFF9h
Lock Bits	1	1	0	1	2Bh	Data	0000h
Signature Bytes	1	1	0	1	29h	Data	0030h, 0031h, 0060h, 0061h

Notes: 1. To preserve the secrecy of on-chip code memory when encrypted, the Encryption Array can not be verified.

Figure 7. Setup for Verifying



AC Characteristics - Commercial & Industrial

AC Characteristics - External Bus Cycles

Definition of Symbols

Table 38. External Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 39 and Table 40 list the AC timing parameters for the TSC80251G2D derivatives with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by PSEN#/RD#/WR# wait states.

Figure 8 to Figure 13 show the bus cycles with the timing parameters.

Table 39. Bus Cycles AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		24 MHz		Unit
		Min	Max	Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		41		ns
T_{LHLL}	ALE Pulse Width	78		58		38		ns(2)
T_{AVLL}	Address Valid to ALE Low	78		58		37		ns(2)
T_{LLAX}	Address hold after ALE Low	19		11		3		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	162		121		78		ns(3)
T_{WLWH}	WR# Pulse Width	165		124		81		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	22		14		6		ns
T_{LHAX}	ALE High to Address Hold	99		70		40		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		146		104		61	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		0		0		0	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		45		40		30	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		215		165		115	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	49		43		31		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	215		169		115		ns
T_{WHLH}	WR# High to ALE High	215		169		115		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		250		175		105	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		306		223		140	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		150		109		68	ns(3)
T_{AXDX}	Data Hold after Address Hold	0		0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	100		70		40		ns(2)
T_{AVWL1}	Address (P0) Valid to WR# Low	100		70		40		ns(2)
T_{AVWL2}	Address (P2) Valid to WR# Low	158		115		74		ns(2)
T_{WHQX}	Data Hold after WR# High	90		69		32		ns
T_{QVWH}	Data Valid to WR# High	133		102		72		ns(3)
T_{WHAX}	WR# High to Address Hold	167		125		84		ns

Notes:
1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

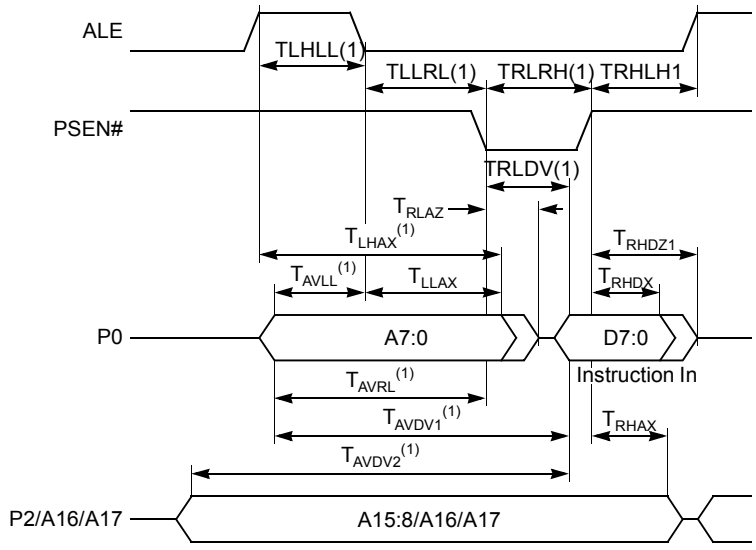
Table 40. Bus Cycles AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		Unit
		Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		ns
T_{LHLL}	ALE Pulse Width	72		52		ns(2)
T_{AVLL}	Address Valid to ALE Low	71		51		ns(2)
T_{LLAX}	Address hold after ALE Low	14		6		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	163		121		ns(3)
T_{WLWH}	WR# Pulse Width	165		124		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	17		11		ns
T_{LHAX}	ALE High to Address Hold	90		57		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		133		92	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		0		0	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		59		48	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		225		175	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	60		47		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	226		172		ns
T_{WHLH}	WR# High to ALE High	226		172		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		289		160	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		296		211	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		144		98	ns(3)
T_{AXDX}	Data Hold after Address Hold	0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	111		64		ns(2)
T_{AVWL1}	Address (P0) Valid to WR# Low	111		64		ns(2)
T_{AVWL2}	Address (P2) Valid to WR# Low	158		116		ns(2)
T_{WHQX}	Data Hold after WR# High	82		66		ns
T_{QVWH}	Data Valid to WR# High	135		103		ns(3)
T_{WHAX}	WR# High to Address Hold	168		125		ns

Notes: 1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

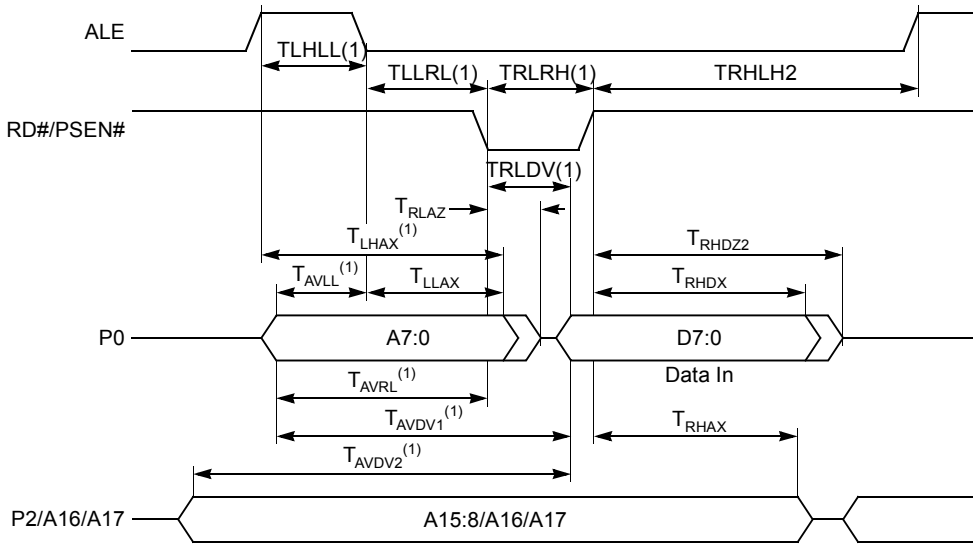
Waveforms in Non-Page Mode

Figure 8. External Bus Cycle: Code Fetch (Non-Page Mode)



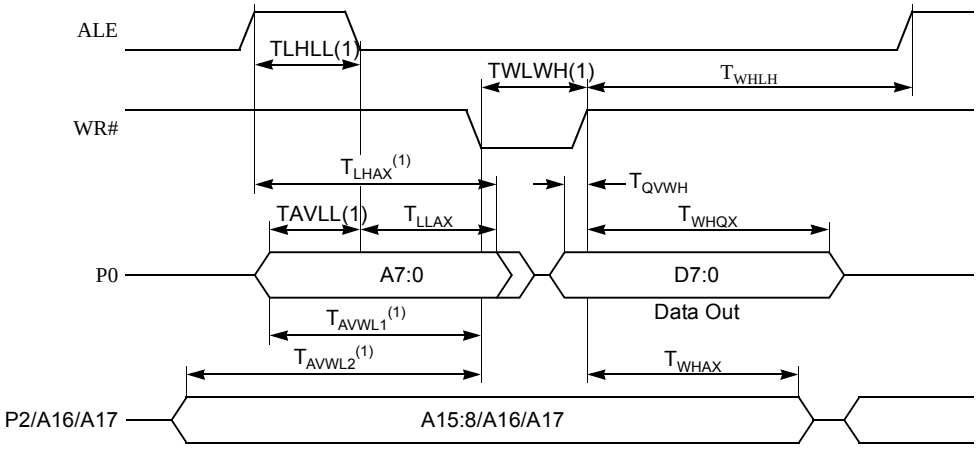
Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Figure 9. External Bus Cycle: Data Read (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

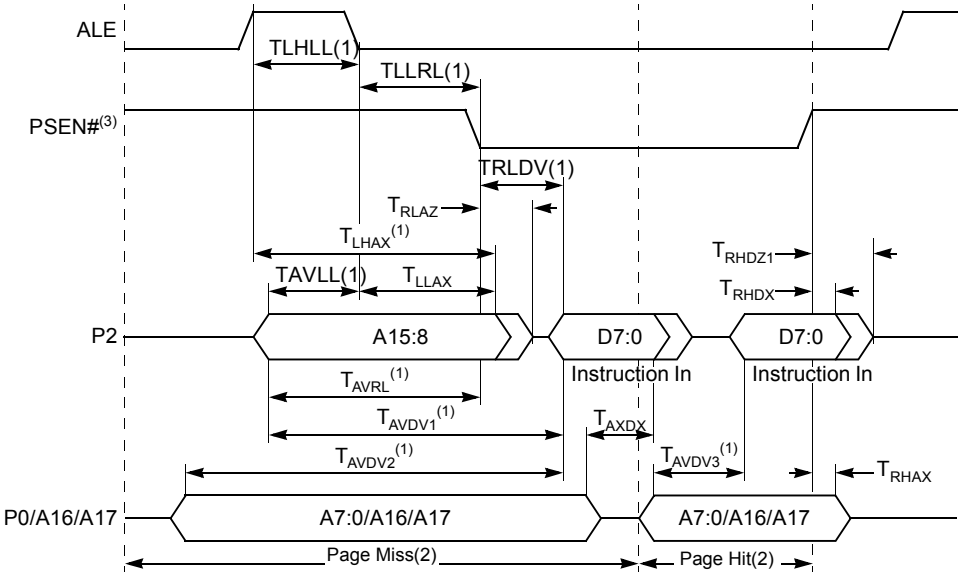
Figure 10. External Bus Cycle: Data Write (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

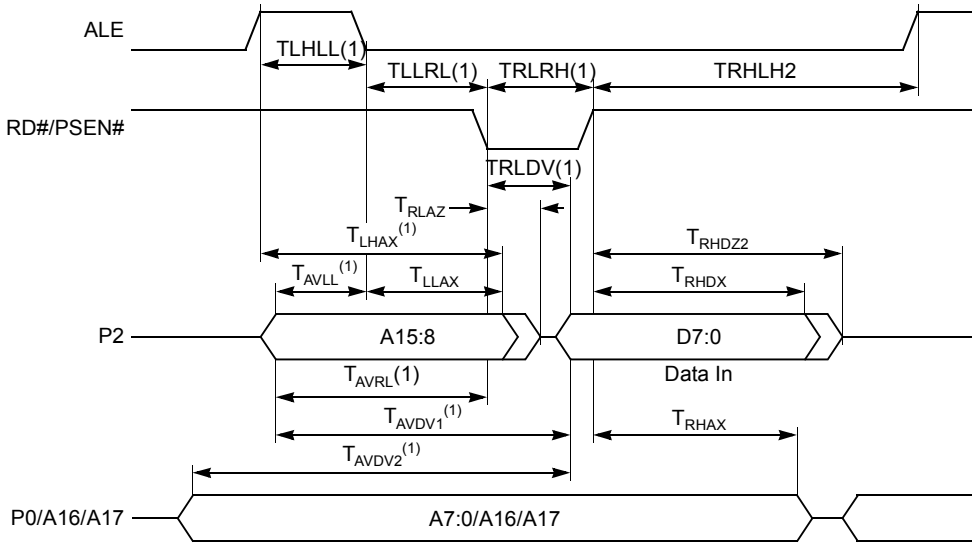
Waveforms in Page Mode

Figure 11. External Bus Cycle: Code Fetch (Page Mode)



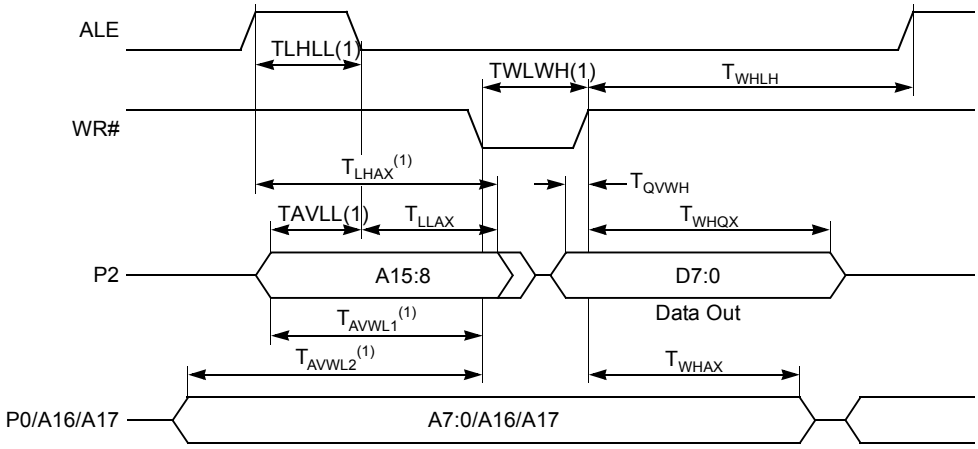
Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.
2. A page hit (i.e., a code fetch to the same 256-byte “page” as the previous code fetch) requires one state ($2 \cdot T_{OSC}$);
a page miss requires two states ($4 \cdot T_{OSC}$).
3. During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

Figure 12. External Bus Cycle: Data Read (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Figure 13. External Bus Cycle: Data Write (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

AC Characteristics - Real-Time Synchronous Wait State

Definition of Symbols

Table 41. Real-Time Synchronous Wait Timing Symbol Definitions

Signals	
C	WCLK
R	RD#/PSEN#
W	WR#
Y	WAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

Table 42. Real-Time Synchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{CLYV}	Wait Clock Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{CLYX}	Wait Hold after Wait Clock Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns
T_{RLYV}	PSEN#/RD# Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{RLYX}	Wait Hold after PSEN#/RD# Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns
T_{WLYV}	WR# Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{WLYX}	Wait Hold after WR# Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns

Waveforms

Figure 14. Real-time Synchronous Wait State: Code Fetch/Data Read

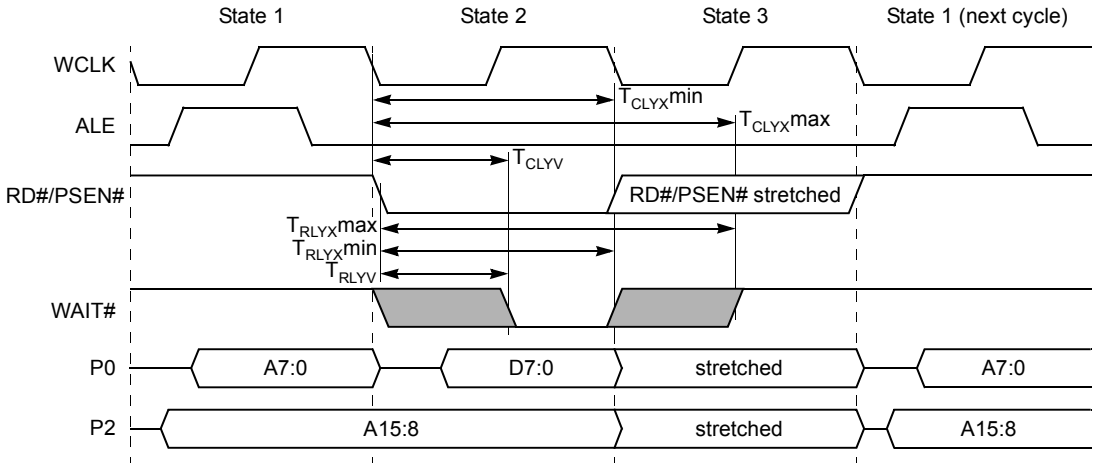
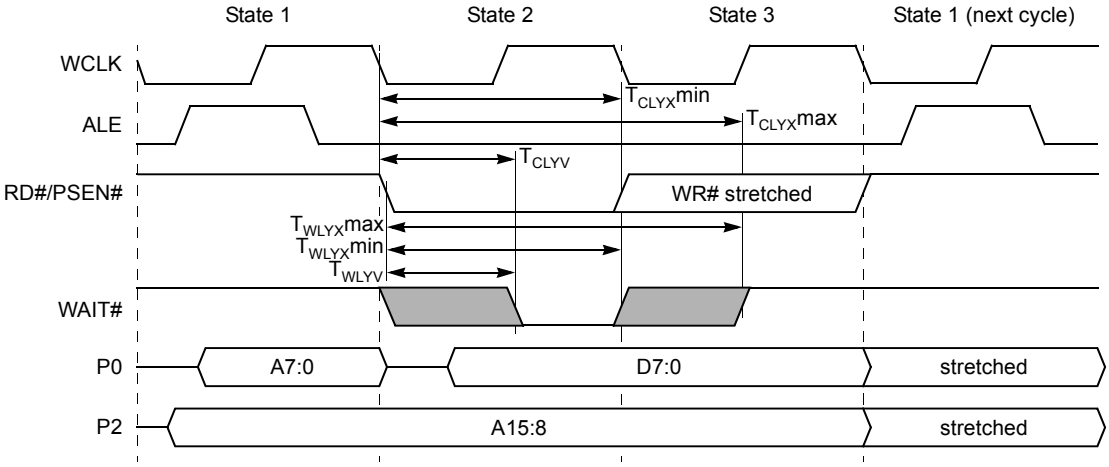


Figure 15. Real-time Synchronous Wait State: Data Write



AC Characteristics - Real-Time Asynchronous Wait State

Definition of Symbols

Table 43. Real-Time Asynchronous Wait Timing Symbol Definitions

Signals	
S	PSEN#/RD#/WR#
Y	AWAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

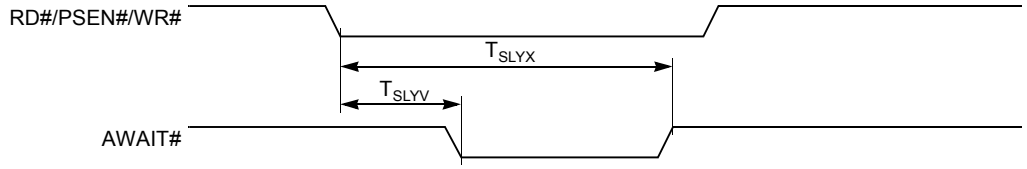
Table 44. Real-Time Asynchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{SLYV}	PSEN#/RD#/WR# Low to Wait Set-up		T_{OSC} - 10	ns
T_{SLYX}	Wait Hold after PSEN#/RD#/WR# Low	$(2N-1)\cdot T_{OSC}$ + 10		ns(1)

Note: 1. N is the number of wait states added (N≥ 1).

Waveforms

Figure 16. Real-time Asynchronous Wait State Timings



AC Characteristics - Serial Port in Shift Register Mode

Definition of Symbols

Table 45. Serial Port Timing Symbol Definitions

Signals	
D	Data In
Q	Data Out
X	Clock

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

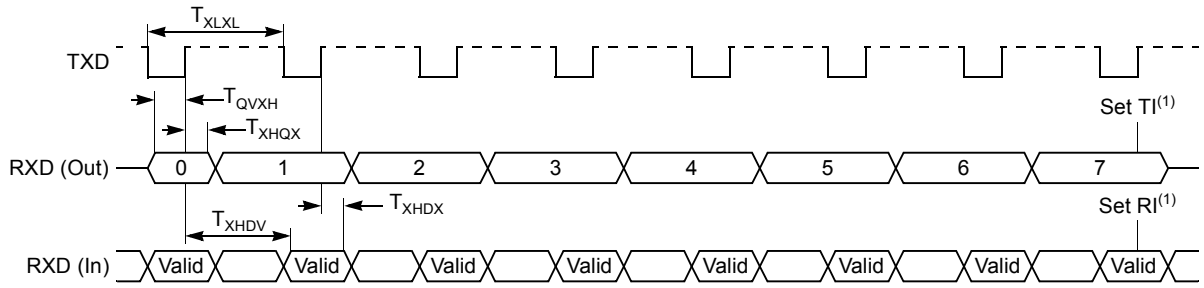
Table 46. Serial Port AC Timing -Shift Register Mode; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		24 MHz(1)		Unit
		Min	Max	Min	Max	Min	Max	
T_{XLXL}	Serial Port Clock Cycle Time	998		749		500		ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	833		625		417		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	165		124		82		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		974		732		482	ns

Note: 1. For high speed versions only.

Waveforms

Figure 17. Serial Port Waveforms - Shift Register Mode



Note: 1. TI and RI are set during S1P1 of the peripheral cycle following the shift of the eight bit.

AC Characteristics - SSLC: TWI Interface

Timings

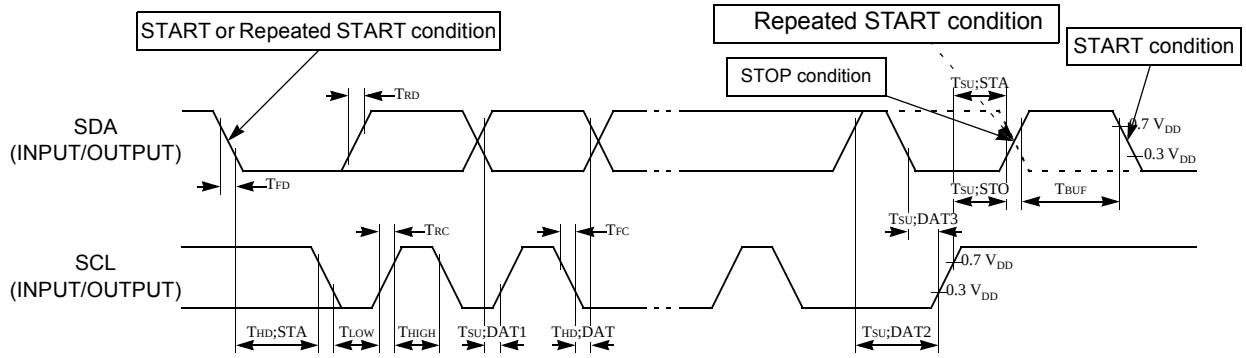
Table 47. TWI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	INPUT Min	INPUT Max	OUTPUT Min	OUTPUT Max
T_{HD}; STA	Start condition hold time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{LOW}	SCL low time	16·T_{CLCL}(4)		4.7 µs(1)	
T_{HIGH}	SCL high time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{RC}	SCL rise time	1 µs		-(2)	
T_{FC}	SCL fall time	0.3 µs		0.3 µs(3)	
T_{SU}; DAT1	Data set-up time	250 ns		20·T_{CLCL}(4)- T_{RD}	
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns		1 µs(1)	
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns		8·T_{CLCL}(4)	
T_{HD}; DAT	Data hold time	0 ns		8·T_{CLCL}(4) - T_{FC}	
T_{SU}; STA	Repeated START set-up time	14·T_{CLCL}(4)		4.7 µs(1)	
T_{SU}; STO	STOP condition set-up time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{BUF}	Bus free time	14·T_{CLCL}(4)		4.7 µs(1)	
T_{RD}	SDA rise time	1 µs		-(2)	
T_{FD}	SDA fall time	0.3 µs		0.3 µs(3)	

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3·T_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
4. T_{CLCL} = T_{OSC} = one oscillator clock period.

Waveforms

Figure 18. TWI Waveforms



AC Characteristics - SSLC: SPI Interface

Definition of Symbols

Table 48. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out
S	SS#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

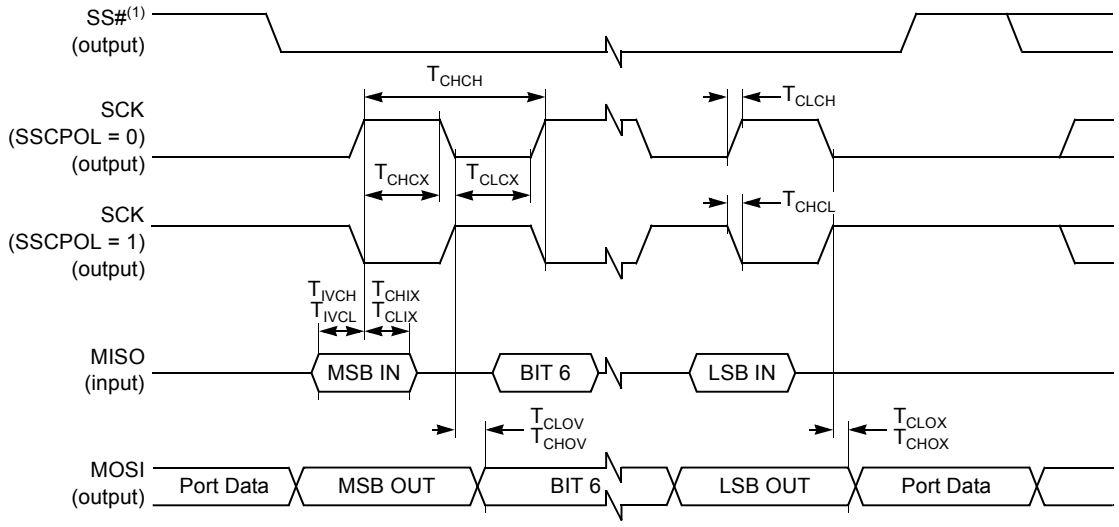
Table 49. SPI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode(1)				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode(3)				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

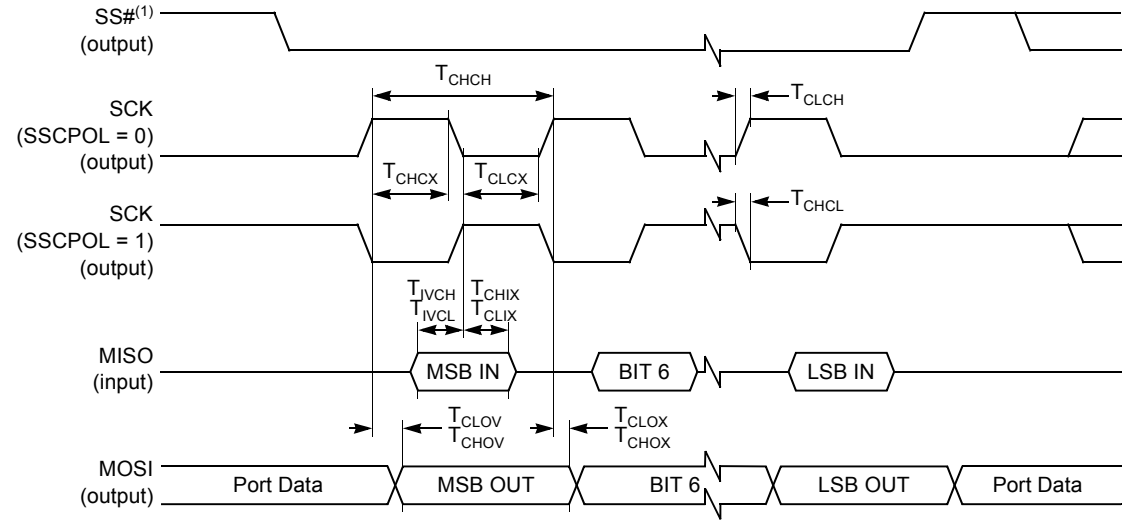
Waveforms

Figure 19. SPI Master Waveforms (SSCPHA = 0)



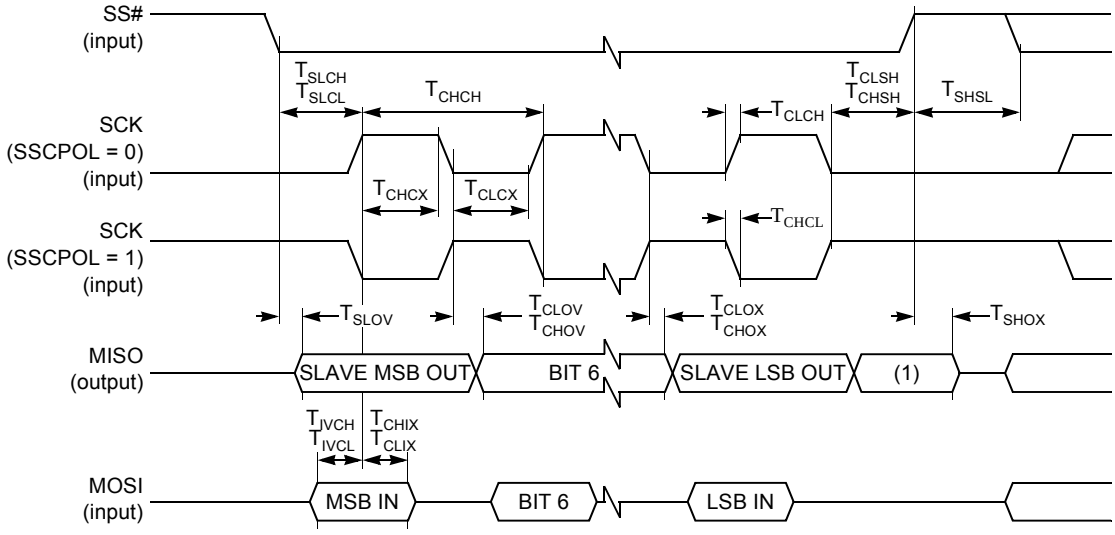
Note: 1. SS# handled by software.

Figure 20. SPI Master Waveforms (SSCPHA = 1)



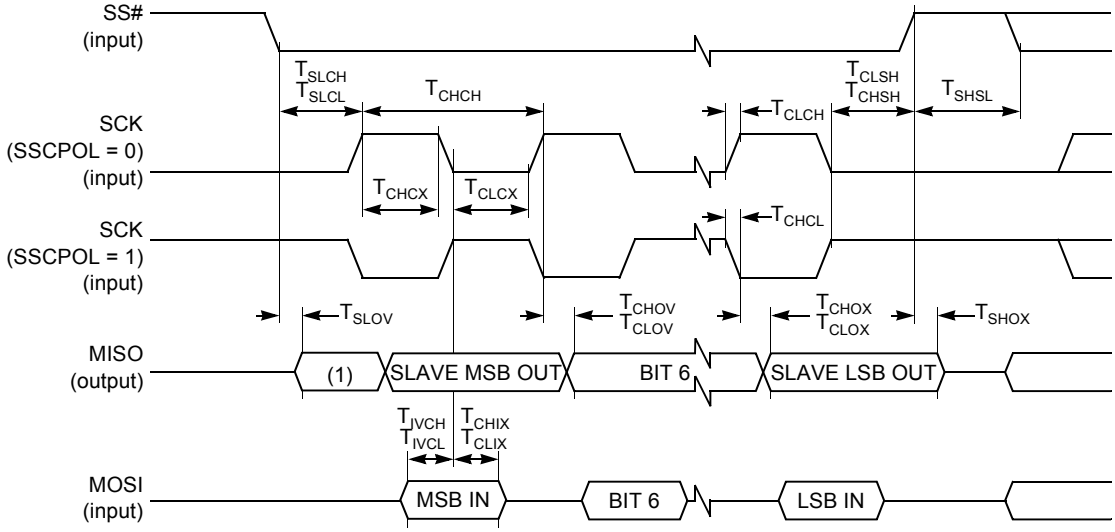
Note: 1. Not Defined but normally MSB of character just received.

Figure 21. SPI Slave Waveforms (SSCPHA = 0)



Note: 1. Not Defined but generally the LSB of the character which has just been received.

Figure 22. SPI Slave Waveforms (SSCPHA = 1)



AC Characteristics - EPROM Programming and Verifying

Definition of Symbols

Table 50. EPROM Programming and Verifying Timing Symbol Definitions

Signals	
A	Address
E	Enable: mode set on Port 0
G	Program
Q	Data Out
S	Supply (V_{PP})

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Table 51. EPROM Programming AC timings; V_{DD} = 4.5 to 5.5 V, T_A = 0 to 40°C

Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Period	83.5	250	ns
T_{AVGL}	Address Setup to PROG# low	48		T_{OSC}
T_{GHAX}	Address Hold after PROG# low	48		T_{OSC}
T_{DVGL}	Data Setup to PROG# low	48		T_{OSC}
T_{GHDX}	Data Hold after PROG#	48		T_{OSC}
T_{ELSH}	ENABLE High to V_{PP}	48		T_{OSC}
T_{SHGL}	V_{PP} Setup to PROG# low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{SLEH}	ENABLE Hold after V_{PP}	0		ns
T_{GLGH}	PROG# Width	90	110	µs

Table 52. EPROM Verifying AC timings; V_{DD} = 4.5 to 5.5 V, V_{DD} = 2.7 to 5.5 V, T_A = 0 to 40°C

Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Period	83.5	250	ns
T_{AVQV}	Address to Data Valid		48	T_{OSC}
T_{AXQX}	Address to Data Invalid	0		ns
T_{ELQV}	ENABLE low to Data Valid	0	48	T_{OSC}
T_{EHQZ}	Data Float after ENABLE	0	48	T_{OSC}

Waveforms

Figure 23. EPROM Programming Waveforms

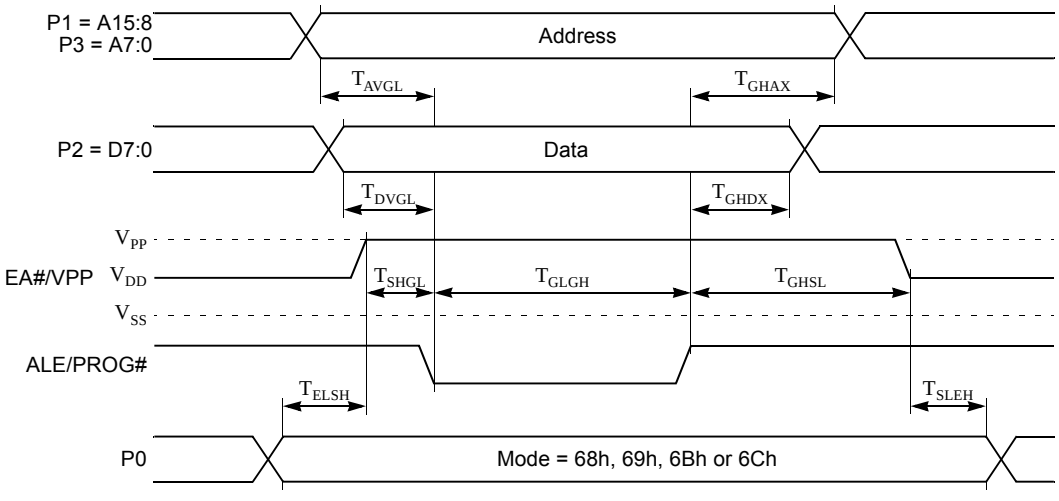
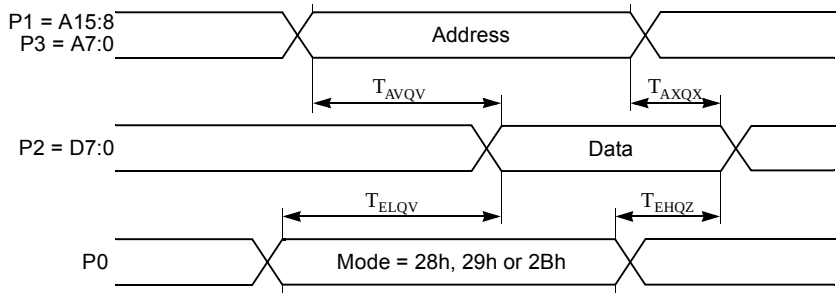


Figure 24. EPROM Verifying Waveforms



AC Characteristics - External Clock Drive and Logic Level References

Definition of Symbols

Table 53. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

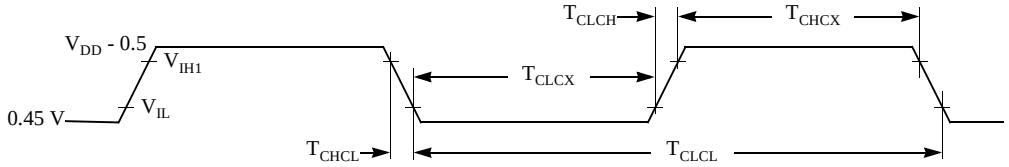
Timings

Table 54. External Clock AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
F_{OSC}	Oscillator Frequency		24	MHz
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns

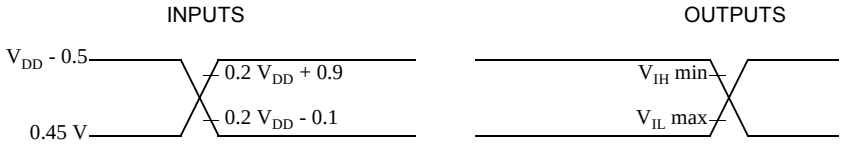
Waveforms

Figure 25. External Clock Waveform



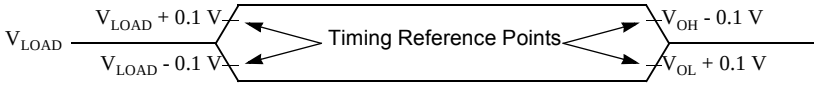
Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 26. AC Testing Input/Output Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ±20 mA.

Figure 27. Float Waveforms



Absolute Maximum Rating and Operating Conditions

Absolute Maximum Ratings

Storage Temperature ..... -65 to +150°C Voltage on any other Pin to VSS ..... -0.5 to +6.5 V I_{OL} per I/O Pin ..... 15 mA Power Dissipation ..... 1.5 W Ambient Temperature Under Bias Commercial.....0 to +70°C Industrial ..... -40 to +85°C Automotive..... -40 to +85°C V_{DD} High Speed versions..... 4.5 to 5.5 V Low Voltage versions..... 2.7 to 5.5 V	*NOTICE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

DC Characteristics

High Speed Versions - Commercial, Industrial, and Automotive

Table 55. DC Characteristics; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA[1][2] I_{OL} = 1.6 mA[1][2] I_{OL} = 3.5 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.3 0.45 1.0	V	I_{OL} = 200 µA[1][2] I_{OL} = 3.2 mA[1][2] I_{OL} = 7.0 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -10 µA[3] I_{OH} = -30 µA[3] I_{OH} = -60 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	V_{IN} = V_{DD}
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3 - AWAIT#)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		20 25 35	25 30 40	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{DL}	Idle Mode Current		5 6.5 9.5	8 10 14	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{PD}	Power-Down Current		2	20	µA	V_{RET} < V_{DD} < 5.5 V
V_{PP}	Programming supply voltage	12.5		13	V	T_A = 0 to +40°C
I_{PP}	Programming supply current			75	mA	T_A = 0 to +40°C

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

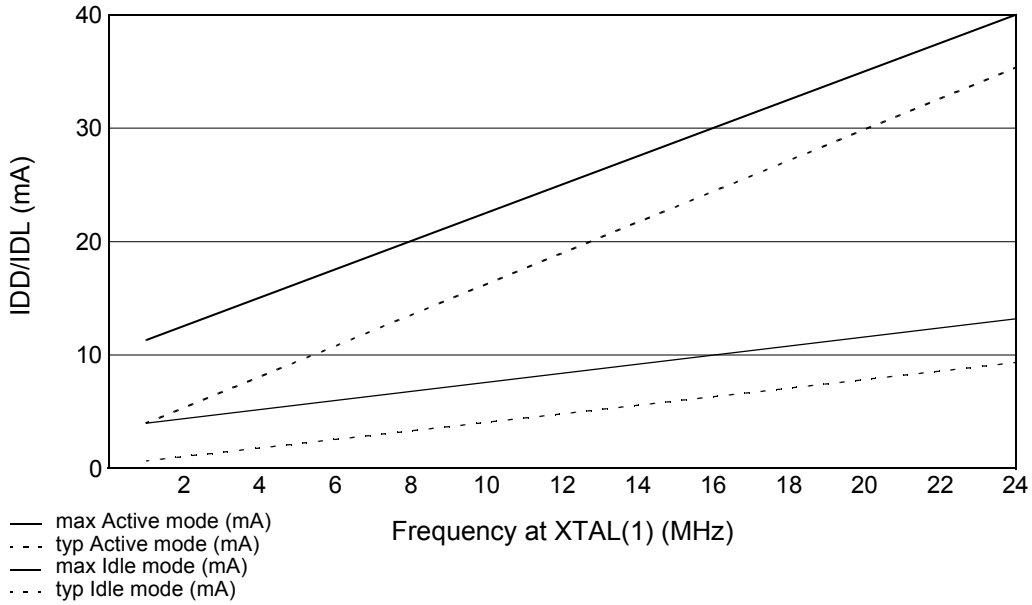
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 5 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

Figure 28. I_{DD}/I_{DL} Versus Frequency; V_{DD} = 4.5 to 5.5 V



Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

Low Voltage Versions - Commercial & Industrial

Table 56. DC Characteristics; V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL} = 0.8 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.45	V	I_{OL} = 1.6 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	$0.9 \cdot V_{DD}$			V	I_{OH} = -10 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	$0.9 \cdot V_{DD}$			V	I_{OH} = -40 µA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3 - AWAIT#)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	$V_{IN} = V_{DD}$
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		4 8 9 11	8 11 12 14	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{DL}	Idle Mode Current		0.5 1.5 2 3	1 4 5 7	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{PD}	Power-Down Current		1	10	µA	V_{RET} < V_{DD} < 3.6 V

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port: Port 0 26 mA

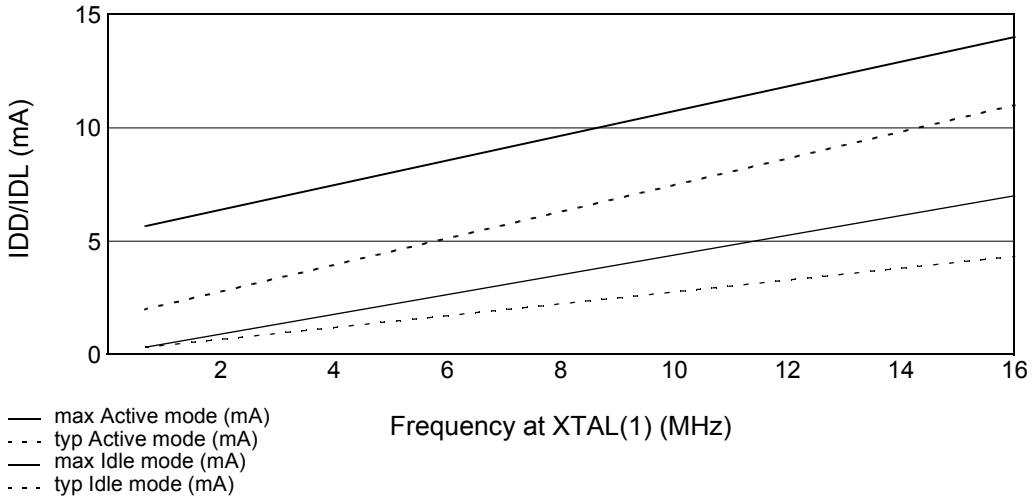
Ports 1-315 mA

Maximum Total IOL for all:Output Pins71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 3 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

Figure 29. I_{DD}/I_{DL} Versus X_{TAL} Frequency; V_{DD} = 2.7 to 3.6 V



Note: 1.The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 30. I_{DD} Test Condition, Active Mode

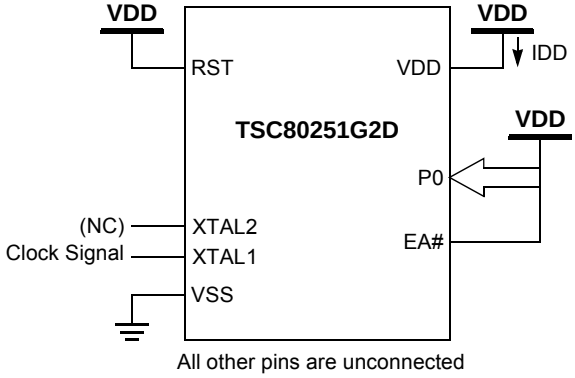


Figure 31. I_{DL} Test Condition, Idle Mode

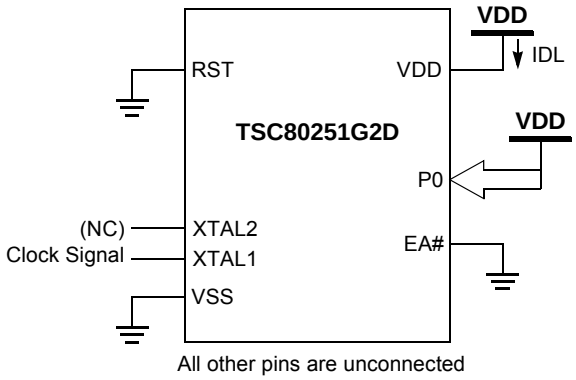
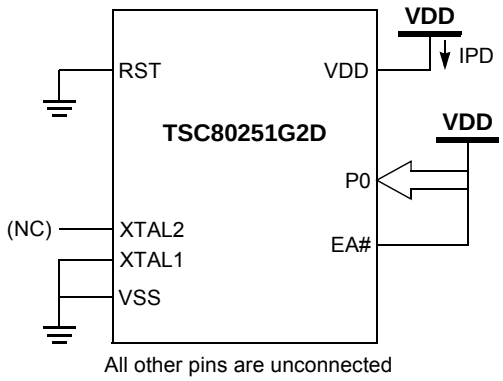


Figure 32. I_{PD} Test Condition, Power-Down Mode



Packages

List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

PDIL 40 - Mechanical Outline

Figure 33. Plastic Dual In Line

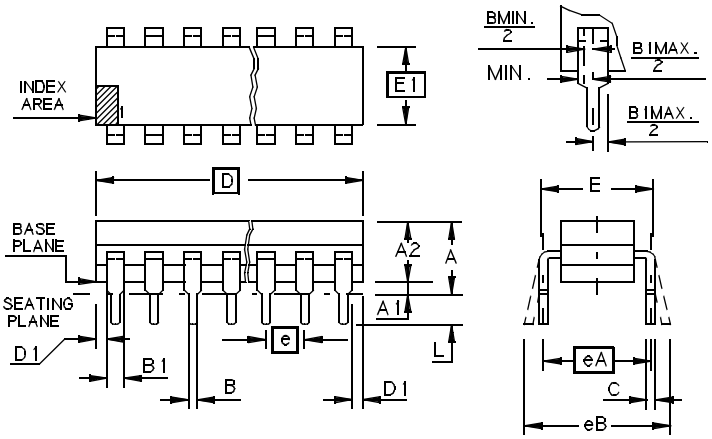


Table 57. PDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-

CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

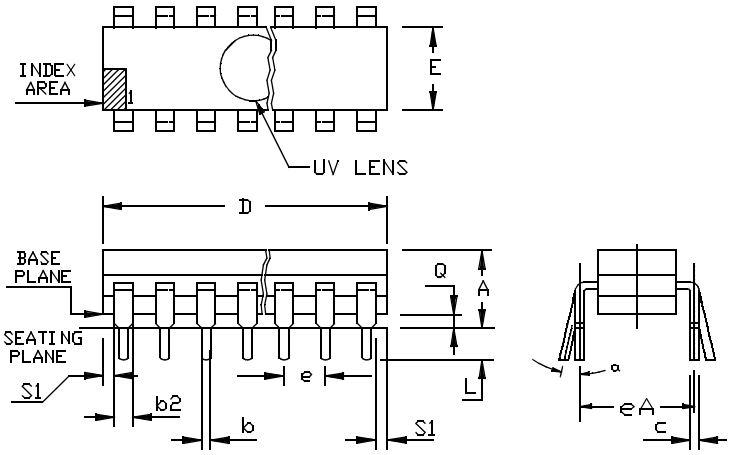


Table 58. CDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

PLCC 44 - Mechanical Outline

Figure 35. Plastic Lead Chip Carrier

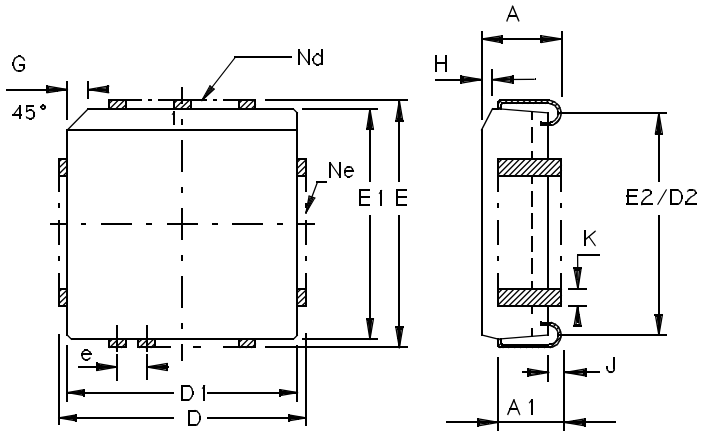


Table 59. PLCC Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

CQPJ 44 with Window - Mechanical Outline

Figure 36. Ceramic Quad Pack J

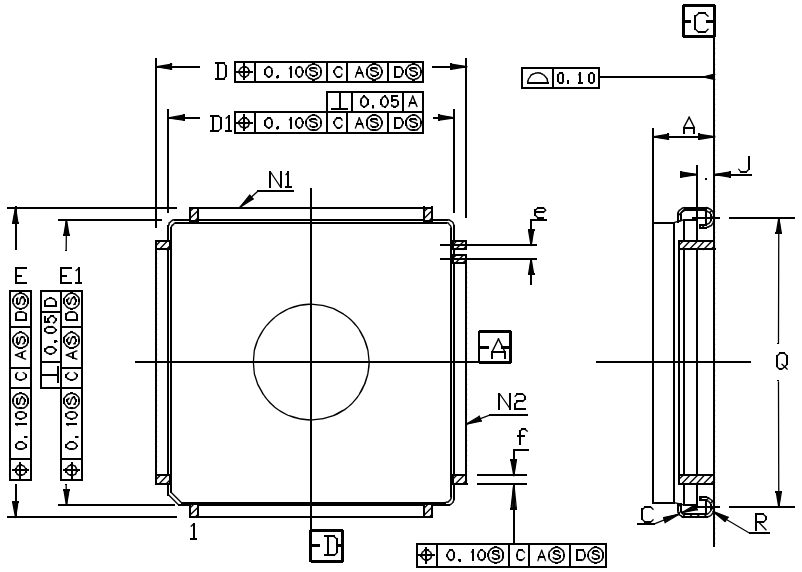


Table 60. CQPJ Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	4.90	-	.193
C	0.15	0.25	.006	.010
D - E	17.40	17.55	.685	.691
D1 - E1	16.36	16.66	.644	.656
e	1.27 TYP		.050 TYP	
f	0.43	0.53	.017	.021
J	0.86	1.12	.034	.044
Q	15.49	16.00	.610	.630
R	0.86 TYP		.034 TYP	
N1	11		11	
N2	11		11	

VQFP 44 (10x10) - Mechanical Outline

Figure 37. Shrink Quad Flat Pack (Plastic)

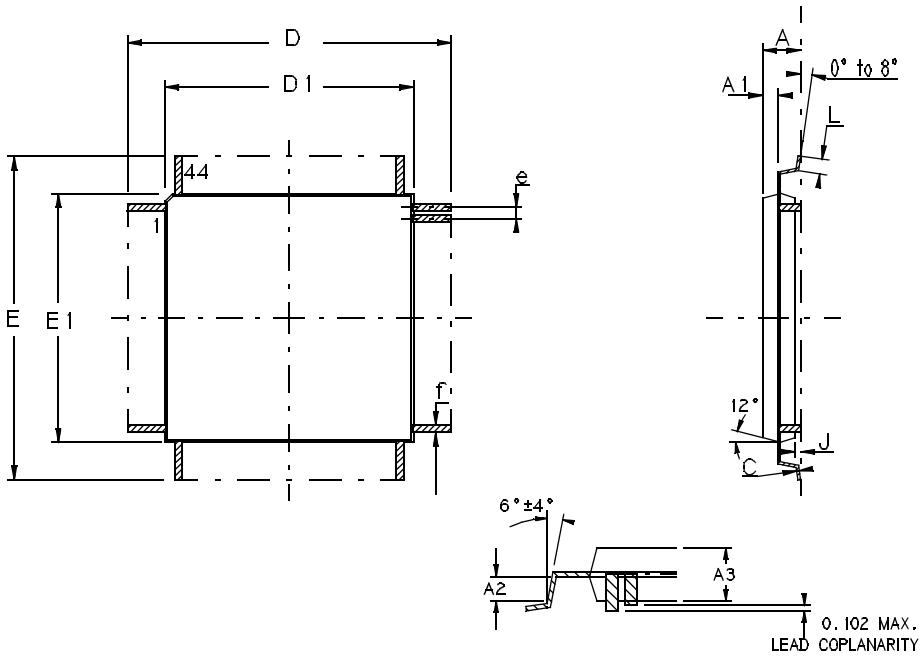


Table 61. VQFP Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	6
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

Ordering Information

AT/TSC80251G2D ROMless

Part Number	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC80251G2D-16CB	ROMless	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G2D-24CB	ROMless	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G2D-24CE	ROMless	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC80251G2D-24IA	ROMless	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC80251G2D-24IB	ROMless	24 MHz, Industrial -40° to 85°C, PLCC 44
AT80251G2D-SLSUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT80251G2D-3CSUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT80251G2D-RLTUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
Low Voltage Versions 2.7 to 5.5 V		
TSC80251G2D-L16CB	ROMless	16 MHz, Commercial, PLCC 44
TSC80251G2D-L16CE	ROMless	16 MHz, Commercial, VQFP 44
AT80251G2D-SLSUL	ROMless	16 MHz, Industrial & Green, PLCC 44
AT80251G2D-RLTUL	ROMless	16 MHz, Industrial & Green, VQFP 44

AT/TSC83251G2D 32 kilobytes MaskROM

Part Number[1]	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC251G2Dxxx-16CB	32K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-24CB	32K MaskROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-24CE	32K MaskROM	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC251G2Dxxx-24IA	32K MaskROM	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC251G2Dxxx-24IB	32K MaskROM	24 MHz, Industrial -40° to 85°C, PLCC 44
AT251G2Dxxx-SLSUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT251G2Dxxx-3CSUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT251G2Dxxx-RLTUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
AT251G2Dxxx-SLSTM	32K MaskROM	24 MHz, Automotive & Green -40° to 85°C, PLCC 44

Part Number[1]	ROM	Description
Low Voltage Versions 2.7 to 5.5 V		
TSC251G2Dxxx-L16CB	32K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-L16CE	32K MaskROM	16 MHz, Commercial 0° to 70°C, VQFP 44
AT251G2Dxxx-SLSUL	32K MaskROM	16 MHz, Industrial & Green, PLCC 44
AT251G2Dxxx-RLTUL	32K MaskROM	16 MHz, Industrial & Green, VQFP 44

Note: 1. xxx: means ROM code, is Cxxx in case of encrypted code.

AT/TSC87251G2D OTPROM

Part Number	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC87251G2D-16CB	32K OTPROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-24CB	32K OTPROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-24CED	32K OTPROM	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC87251G2D-24IA	32K OTPROM	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC87251G2D-24IB	32K OTPROM	24 MHz, Industrial -40° to 85°C, PLCC 44
AT87251G2D-SLSUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT87251G2D-3CSUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT87251G2D-RLTUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
Low Voltage Versions 2.7 to 5.5 V		
TSC87251G2D-L16CB	32K OTPROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-L16CED	32K OTPROM	16 MHz, Commercial 0° to 70°C, VQFP 44
AT87251G2D-SLSUL	32K OTPROM	16 MHz, Industrial & Green, 0° to 70°C, PLCC 44
AT87251G2D-RLTUL	32K OTPROM	16 MHz, Industrial & Green, 0° to 70°C, VQFP 44

Document Revision History

Changes from 4135D to 4135E

1. Added automotive qualification, and ordering information for ROM product version.

Changes from 4135E to 4135F

1. Absolute Maximum Ratings added for automotive product version.

Options (Please consult Atmel sales)

- ROM code encryption
- Tape & Reel or Dry Pack
- Known good dice
- Extended temperature range: -55°C to +125°C

Product Markings

ROMless versions

ATMEL
Part number

YYWW . Lot Number

Mask ROM versions

ATMEL
Customer Part number

Part Number
YYWW . Lot Number

OTP versions

ATMEL
Part number

YYWW . Lot Number

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
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