Product Preview

128 Segment LCD Drivers

CMOS

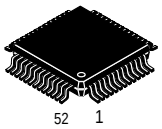
MC145003
MC145004

The MC145003/5004 are 128–segment, multiplexed–by–four LCD Drivers. The two devices are functionally the same except for their data input protocols. The MC145003 uses an SPI data input protocol which is directly compatible with that of the MC6805 family of microcomputers. Using a minimal amount of software (see example), the device may be interfaced to the MC68HCXX product families. The MC145004 has a IIC interface and has essentially the same protocol, except that the device sends an acknowledge bit back to the transmitter after each eight–bit byte is received. MC145004 also has a "read mode", whereby data sent to the device may be retrieved via the IIC bus.

The MC145003/MC145004 drives the liquid–crystal displays in a multiplexed–by–four configuration. The device accepts data from a microprocessor or other serial data source to drive one segment per bit. The chip does not have a decoder, allowing for the flexibility of formatting the segment data externally.

Devices are independently addressable via a two–wire (or three–wire) communication link which can be common with other MC145003/MC145004 and/or other peripheral devices.

- Drives 128 Segments Per Package
- Devices May Be Cascaded for Larger LCD Applications
- May Be Used with the Following LCDs: Segmented Alphanumeric, Bar Graph, Dot Matrix, Custom
- Quiscent Supply Current: 85 μA @ 2.8 V V_{DD}
- Operating Voltage Range: 2.8 to 5.5 V
- Operating Temperature Range: – 40 to 85°C
- Separate Access to LCD Drive Section's Supply Voltage to Allow for Temperature Compensation
- See Application Notes AN1066 and AN442

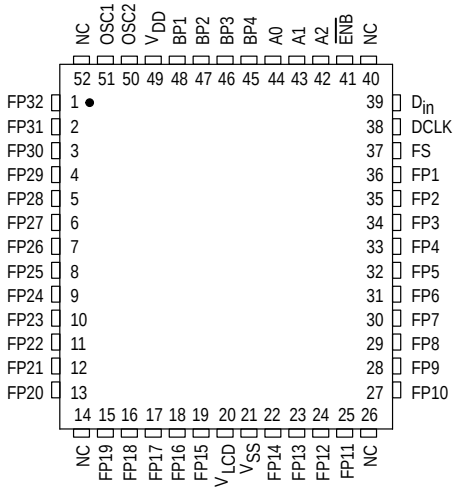


QFP
FU SUFFIX
CASE 848B

ORDERING INFORMATION

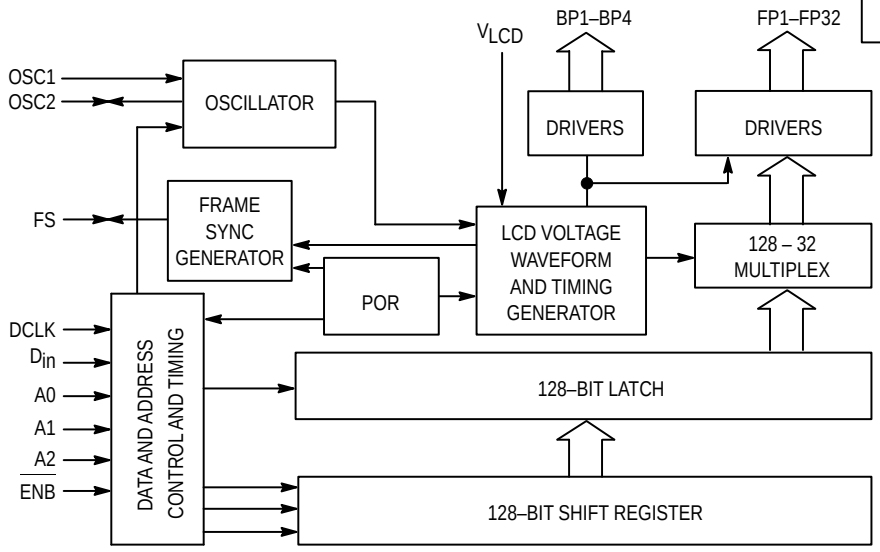
MC145003FU	QFP
MC145004FU	QFP

PIN ASSIGNMENT



NC = NO CONNECTION

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

© Motorola, Inc. 1994

MOTOROLA

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 6.5	V
V_{in}	Input Voltage, D_{in}, and Data Clock	– 0.5 to 15	V
$V_{in\ osc}$	Input Voltage, OSC_{in} of Master	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	V_{LCD} V	–40°C Min	–40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Output Drive Current — Frontplanes										µA
V_O = 0.15 V	I_{FH}	5	2.8	360	—	260	—	240	—	
	I_{FL}	5	2.8	360	—	260	—	240	—	
V_O = 2.65 V	I_{FH}	5	2.8	–320	—	–240	—	–240	—	
	I_{FL}	5	2.8	–320	—	–240	—	–240	—	
V_O = 1.72 V	I_{FH}	5	2.8	–95	—	–40	—	–60	—	
	I_{FL}	5	2.8	—	–1.5	—	–1.5	—	–1	
V_O = 1.08 V	I_{FH}	5	2.8	90	—	40	—	55	—	
	I_{FL}	5	2.8	—	2	—	2	—	1	
V_O = 0.15 V	I_{FH}	5	5.5	600	—	600	—	580	—	
	I_{FL}	5	5.5	600	—	600	—	580	—	
V_O = 5.35 V	I_{FH}	5	5.5	–490	—	–520	—	–520	—	
	I_{FL}	5	5.5	–490	—	–520	—	–520	—	
V_O = 3.52 V	I_{FH}	5	5.5	–100	—	–35	—	–50	—	
	I_{FL}	5	5.5	—	–1.5	—	–1.5	—	–1	
V_O = 1.98 V	I_{FH}	5	5.5	100	—	55	—	70	—	
	I_{FL}	5	5.5	—	1.5	—	1	—	1	
Supply Currents (f_{OSC}) = 110 kHz										µA
I_{DD} = Quiescent @ I_{out} = 0 µA	I_{DDQ}	2.8	—	—	65	—	140	—	85	
I_{LCD} = Quiescent @ I_{out} = 0 µA	I_{LCDQ}	—	2.8	—	30	—	45	—	20	
I_{DD} = Quiescent @ I_{out} = 0 µA	I_{DDQ}	5.5	—	—	350	—	1050	—	350	
I_{LCD} = Quiescent @ I_{out} = 0 µA	I_{LCDQ}	—	5.5	—	60	—	90	—	35	
Input Current	I_{in}	—	—	—	—	–0.1	0.1	—	—	µA
Input Capacitance	C_{in}	—	—	—	—	—	7.5	—	—	pF
Frequencies										
OSC2 Frequency @ R1; R1 = 200 kΩ	f_{OSC2}	5	5	103	111	100	150	123	136	kHz
FS Frequency @ R1	f_{FS}	5	5	100	110	100	140	120	133	Hz
FS Pulse @ R1	f_{FS}	5	5	4.7	5	3.6	5.6	3.5	3.9	µs
BP Frequency @ R1	f_{BP}	5	5	100	110	100	140	120	133	Hz
OSC2 Frequency @ R2; R2 = 996 kΩ	f_{OSC2}	5	5	22.5	24.5	23	33	28	31	kHz
Average DC Offset Voltage (BP Relative to FP)	V_{OO}	5	2.8	–50	+50	–50	+50	–50	+50	mV
Input Voltage “0” Level	V_{IL}	2.8	5	—	—	—	0.85	—	—	V
	V_{IL}	5.5	5	—	—	—	1.65	—	—	
“1” Level	V_{IH}	2.8	5	—	—	2	—	—	—	
	V_{IH}	5.5	5	—	—	3.85	—	—	—	

(continued)

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	V_{DD} V	V_{LCD} V	40°C Min	40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Output Drive Current — Backplanes	V_O = 2.65 V	I_{BH}*	5	2.8	–290	—	–240	—	–240	—	µA
		I_{BL}	5	2.8	–290	—	–240	—	–240	—	
	V_O = 0.15 V	I_{BH}	5	2.8	310	—	260	—	230	—	
		I_{BL}	5	2.8	310	—	260	—	230	—	
	V_O = 1.08V	I_{BH}	5	2.8	90	—	40	—	55	—	
		I_{BL}	5	2.8	—	1	—	2	—	1	
	V_O = 1.72 V	I_{BH}	5	2.8	–90	—	–40	—	–60	—	
		I_{BL}	5	2.8	—	–1.5	—	–1	—	–1	
	V_O = 5.35 V	I_{BH}	5	5.5	–490	—	–520	—	–520	—	
		I_{BL}	5	5.5	–490	—	–520	—	–520	—	
	V_O = 0.15 V	I_{BH}	5	5.5	600	—	600	—	580	—	
		I_{BL}	5	5.5	600	—	600	—	580	—	
	V_O = 1.98 V	I_{BH}	5	5.5	100	—	55	—	70	—	
		I_{BL}	5	5.5	—	1.5	—	1	—	1	
	V_O = 3.52 V	I_{BH}	5	5.5	–100	—	–35	—	–50	—	
		I_{BL}	5	5.5	—	–1	—	–1	—	–1	
Pulse Width, Data Clock	(Figure 1)	t_w	5				50	—			ns
			3				100	—			
DCLK Rise/Fall Time	(Figure 1)	t_r, t_f	5				—	20			µs
			3				—	120			
Setup Time, D_{in} to DCLK	(Figure 2)	t_{su}	5				0	—			ns
			3				0	—			
Hold Time, D_{in} to DCLK	(Figure 2)	t_h	5				30	—			ns
			3				60	—			
DCLK Low to $\overline{ENB}$ High	(Figure 3)	t_h	5				10	—			ns
			3				20	—			
ENB High to DCLK High	(Figure 3)	t_{rec}	5				10	—			ns
			3				20	—			
ENB High Pulse Width	(Figure 3)	t_w	5				50	—			ns
			3				100	—			
$\overline{ENB}$ Low to DCLK High	(Figure 3)	t_{su}	5				10	—			ns
			3				20	—			

NOTE: Timing for Figures 1, 2, and 3 are design estimates only.

* For a time (t = 4/OSC FREQ.) after the backplane waveform changes to a new voltage level, the circuit is maintained in the high–current state to allow the load capacitances to charge quickly. The circuit is then returned to the low–current state until the next voltage change.

SWITCHING WAVEFORMS

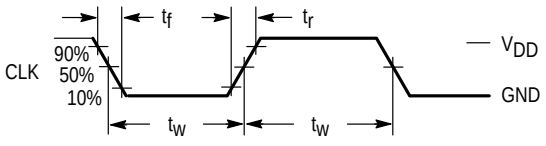


Figure 1.

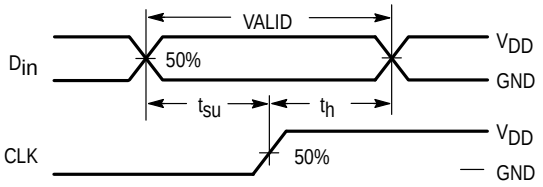


Figure 2.

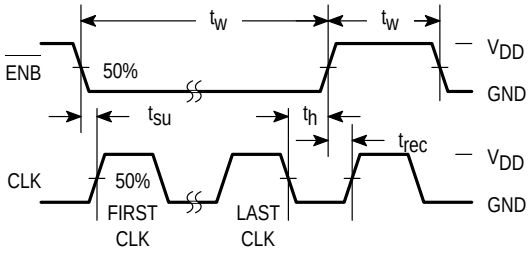


Figure 3.

FUNCTIONAL DESCRIPTION

The MC145003/MC145004 has essentially two sections which operate asynchronously from each other; the data input and storage section and the LCD drive section. The LCD drive and timing is derived from the oscillator, while the data input and storage is controlled by the Data In (D_{in}), Data Clock (DCLK), Address (A0, A1, A2), and Enable (ENB) pins.

Data is shifted serially into the 128–bit shift register and arranged into four consecutive blocks of 32 parallel data bits. A time–multiplex of the four backplane drivers is made (each backplane driver becoming active then inactive one after another) and, at the start of each backplane active period, the corresponding block of 32 bits is made available at the frontplane drivers. A high input to a plane driver turns the driver on, and a low input turns the driver off.

Figure 4 shows the sequence of backplanes. Figure 5 shows the possible configurations of the frontplanes relative to the backplanes. When a backplane driver is on, its output switches from V_{LCD} to 0 V, and when it is off, it switches from 1/3 V_{LCD} to 2/3 V_{LCD}. When a frontplane driver is on, its output switches from 0 V to V_{LCD}, and when it is off, it switches from 2/3 V_{LCD} to 1/3 V_{LCD}.

The LCD drive and timing section provides the multiplex signals and backplane driver input signals and formats the frontplane and backplane waveforms. It also provides a “frame sync” pulse which may be used in a system where many LCD drivers are cascaded, to synchronize the backplanes/frontplanes of all participating LCD drivers.

The address pins are used in cascaded systems to uniquely distinguish one LCD driver from another (and from any other chips on the same bus) and to define one LCD driver as the “master” in the system. There must be one master in any system.

The enable pin may be used as a third control line in the communication bus. It may be used to define the moment when the data is latched. If not used, then the data is latched after 128 bits of data have been received.

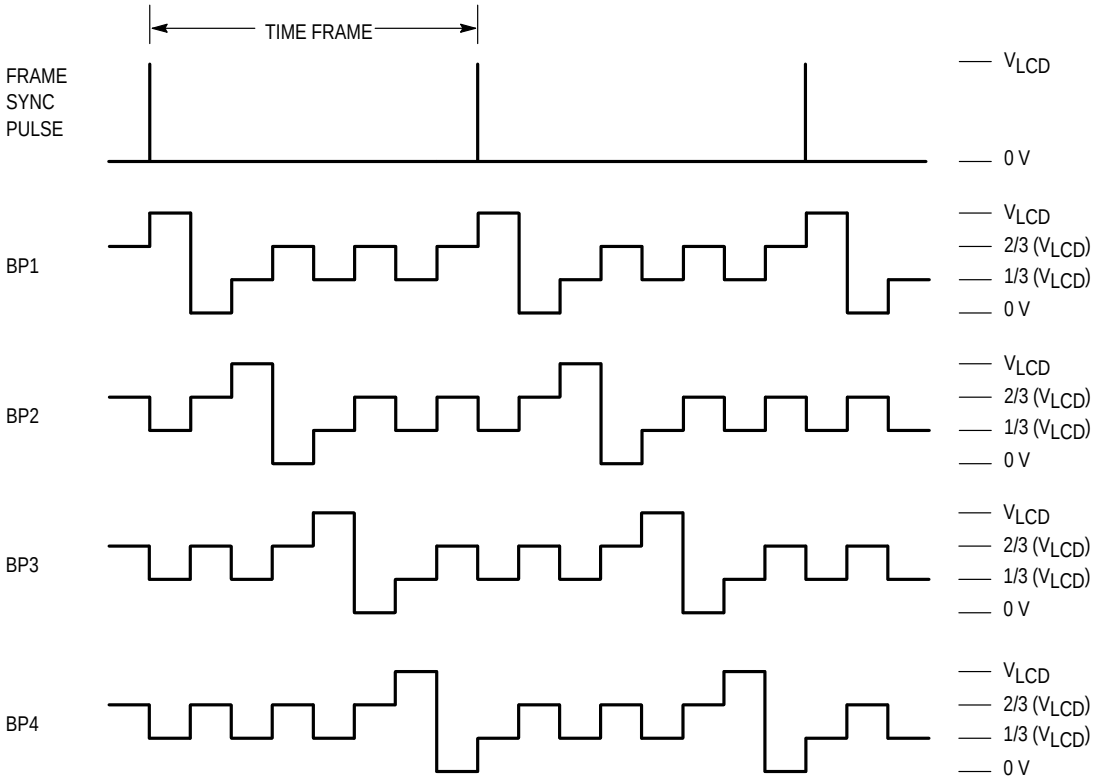


Figure 4. Backplane Sequence

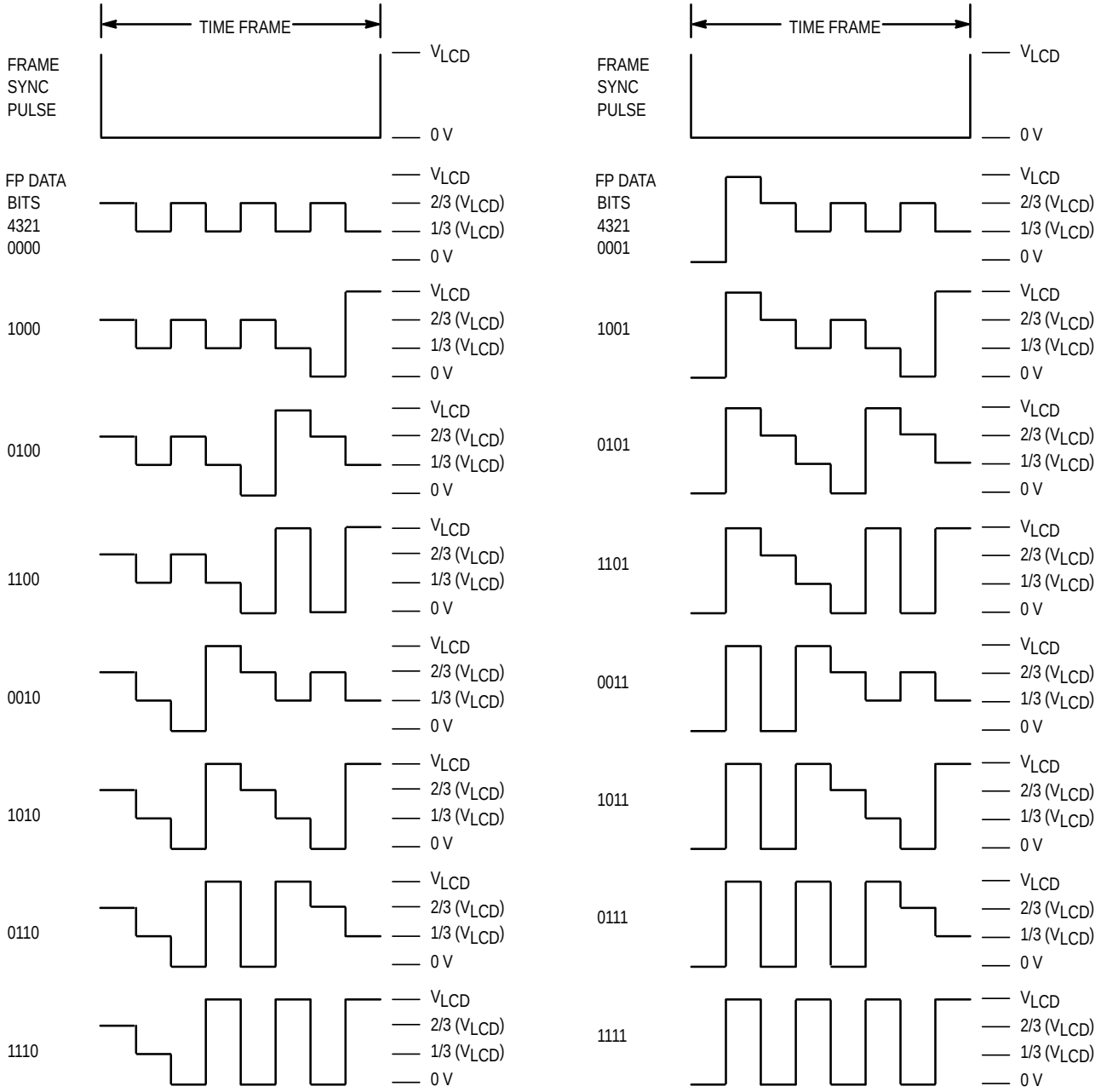


Figure 5. Frontplane Combinations

PIN DESCRIPTIONS

A0–A2
Address Inputs (Pins 42–44)

The devices have to receive a correct address before they will accept data. Three address pins (A2, A1, A0) are used to define the states of the three programmable bits of MC145003/MC145004's 8–bit address.

The address is 0111vwxy where v, w, x represent A2, A1, and A0 respectively. Where v, w, x = 0, then A2, A1, and A0 should be tied to 0 V. Where v, w, x = 1, then A2, A1, and A0 should be tied to V_{DD}.

For systems where only one MC145003/MC145004 is used, the address pins must be tied to V_{DD}. This defines the device as a master. Other configurations of the address pins (except 000*) defines a device to be a slave. For systems with more than one MC145003/MC145004 (cascaded application) one of the MC145003/MC145004 must have all of its address pins tied to V_{DD} (this defines it as the master). The master is responsible for:

1. Supplying the oscillator input to all slaves.
2. Sending one frame sync pulse at the beginning of every BP1 (backplane 1) period to keep the MC145003/MC145004 synchronized.
3. Supplying a common set of backplane signals to be shared by all participating devices in the cascaded system (if desired).

NOTE

Note: In applications where the circuit will be isolated from external manual interference the system designer may take advantage of the self–programming feature. Upon power–on, address pins which are left open–circuit will be charged to V_{DD}. However, care must be taken not to inadvertently discharge the pins after power–on since the address may then be lost. A similar feature is also available on the ENB pin.

CAUTION

The configuration A0, A1, A2 = 000 should not be used. This does not give a valid address and is reserved for Motorola's use only. All three address pins should never be tied to 0 V simultaneously. Any other combination of Master (111) plus six Slaves (110, 101, 100, 011, 010, 001) is allowed.

$\overline{ENB}$
Enable Input (Pin 41)

If the ENB pin is tied to V_{DD}, the MC145003/MC145004 will always latch the data after 128 bits have been received. The latched data is multiplexed and fed to the frontplane drivers for display. If external control of this latching function is required (for example, in a cascaded application where multiplexing of new data may require a delay until all participating MC145003/MC145004 data is updated), then the ENB pin should be held low, followed by one high pulse on ENB when data display is required. (This may also be useful in a system where one MC145003/MC145004 is permanently addressed and only the last 128 bits of data sent are required to be latched for display). The pulse on the ENB pin must occur while DCLK is high.

DCLK, D_{in}
Data Clock and Data Input (Pins 38, 39)

Address input and data input controls. See **Data Input Protocol** sections for relevant option.

OSC1, OSC2
Oscillator Pins (Pins 51, 50)

To use the on–board oscillator, an external resistor should be connected between OSC1 and OSC2 of the master device. Optionally, the OSC1 pin of the master device may be driven by an externally generated clock signal. The oscillator signal for any slave(s) in the system is provided by the master device by connecting the master's OSC2 pin to the slaves'(s) OSC2 pin(s). The slaves'(s) OSC1 pin(s) should be connected to ground.

A resistor of 680 kΩ connected between the master's OSC1 and OSC2 pins gives an oscillator frequency of about 30 kHz, giving approximately 30 Hz as seen at the LCD driver outputs. A resistor of 200 kΩ gives about 100 kHz, which results in 100 Hz at the driver outputs. LCD manufacturers recommend an LCD drive frequency of between 30 Hz and 100 Hz. See Figure 6.

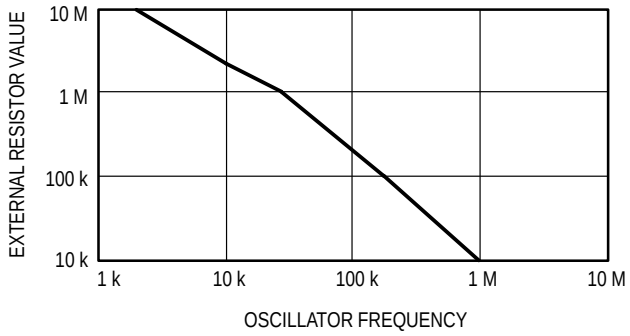


Figure 6. Oscillator Frequency vs Load Resistance (Approximate)

FS
Frame Sync (Pin 37)

The frame sync pin (FS) is configured as an output on the master device and as an input on the slave device(s). The master device outputs a pulse on the FS pin once at the beginning of each BP1 (backplane 1) active period to keep all MC145003/MC145004s synchronized.

FP1–FP32
Frontplane Drivers (Pins 36–27, 25–22, 19–15, 13–1)

Frontplane driver outputs.

BP1–BP4
Backplane Drivers (Pins 48–45)

Backplane driver outputs.

V_{LCD}
LCD Driver Supply (Pin 20)

Power supply input for LCD drive outputs. May be used to supply a temperature–compensated voltage to the LCD drive section, which can be separate from the logic voltage supply, V_{DD}.

V_{DD}
Positive Power Supply (Pin 49)

This pin supplies power to the main processor interface and logic portions of the device. The voltage range is 2.8 to 5.5 V with respect to the V_{SS} pin.

For optimum performance, V_{DD} should be bypassed to V_{SS} using a low inductance capacitor mounted very closely to these pins. Lead length on this capacitor should be minimized.

V_{SS}
Ground (Pin 21)

Common ground.

DATA INPUT PROTOCOL

Two–wire communication bus DCLK, D_{in}; three–wire communication bus DCLK, D_{in}, ENB.

MC145003 — SPI DEVICE (FIGURE 7)

Before communication with an MC145003 can begin, a start condition must be set up on the bus by the transmitter. To establish a start condition, the transmitter must pull the data line low while the clock line is high. The "idle" state for the clock line and data line is the high state.

After the start condition has been established, an eight–bit address should be sent by the transmitter. If the address sent corresponds to the address of (one of) the MC145003(s) then on each successive clock pulse, the addressed device will accept a data bit.

If the ENB pin is permanently high, then the addressed MC145003's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise, the control of this latch function may be overridden by holding the ENB line low until the new data is required to be displayed, then a high pulse should be sent on the ENB line. The high pulse must be sent during DCLK high (clock idle).

To end communication with an MC145003, a stop condition should be set up on the bus (or another start condition may be set up if another communication is desired). Note that the communication channel to an addressed device may be left open after the 128 data bits have been sent by not setting up a stop or a start condition. In such a case, the 129th rising DCLK edge, which normally would be used to set up the stop or start condition, is ignored by the MC145003 and data continues to be received on the 130th rising DCLK. The latch function continues to work as normal (i.e., data is be latched either after each block of 128 data bits has been received or under external control as required).

At any time during data transmission, the transfer may be interrupted with a stop condition. Data transmission may be resumed with a start condition and resending the address.

Interfacing the MC145003 with the MC6805 family

The MC145003 performs as a slave receiver in an SPI environment if the clock idle state has been defined to be "high" (SPICR5 = 1). In three–wire or four–wire SPI environments, the slave select wire (SPISS) can be used for the ENB pin on the MC145003 as described above. Note that in full duplex SPI environments, MC145003 only receives data, it does not re–transmit data.

MC145004 — IIC DEVICE (FIGURE 8)

Before communication with an MC145004 can begin, a start condition must be set up on the bus by the controller. To establish a start condition, the controller must pull the data line low while the clock line is high.

After the start condition has been established, an eight–bit address should be sent by the controller followed by an extra clock pulse while the data line is left high. In this option, only the seven most significant bits of the address are used to uniquely define devices on the bus, the least significant bit is used as a read/write control: if the least significant bit is 0, then the controller writes to the LCD driver; if it is 1, then the controller reads from the LCD driver's 128–bit shift register on a first–in first–out basis. If the seven most significant address bits sent correspond to the address of (one of) the LCD driver(s) then the addressed LCD driver responds by sending an "acknowledge" bit back to the controller (i.e., the LCD driver pulls the data line low during the extra clock pulse supplied by the controller). If the least significant address bit was 0, then the controller should continue to send data to the LCD driver in blocks of eight bits followed by an extra ninth clock pulse to allow the LCD driver to pull the data line D_{in} low as an acknowledgement. If the least significant address bit was 1, then the LCD driver sends data back to the controller (the clock is supplied by the controller). After each successive group of eight bits sent, the LCD driver leaves the data line high for one pulse.

If the $\overline{ENB}$ pin is permanently high, then the addressed MC145004's internal counter latches the data to be displayed after 128 data bits have been received. Otherwise the control of this latch function may be overridden by holding the ENB line low until the new data is required to be displayed, then a high pulse should be sent on the ENB line. The high pulse must be sent during DCLK high (clock idle).

To end communication with an MC145004, a stop condition should be set up on the bus (or another start condition may be set up if another communication is desired). Note that the communication channel to an addressed device may be left open after the 128 data bits have been sent by not setting up a stop or a start condition. In such a case the rising DCLK edge which comes after all 128 data bits have been sent and after the last acknowledge–related clock pulse has been made is ignored; data continues to be received on the following DCLK high. The latch function continues to work as normal (i.e., data is latched either after each block of 128 data bits has been received or under external control as required).

At any time during data transmission, the transfer may be interrupted with a stop condition. Data transmission may be resumed with a start condition and resending the address.

CASCADED OPERATION

The master device supplies the oscillator input via its OSC2 pin to the slave devices via their OSC2 pin(s). It sends a frame sync pulse via its FS pin to the slaves via their FS pins at the beginning of every BP1 valid time. In Figure 9, the ENB pins are tied together and used as a chip enable to latch the new data — the ENB pins could have been tied to V_{DD} if it were desirable to use the internal data bit counter to latch the new data.

The four backplane inputs may come from the master only, with the slave backplanes being left open, as shown in Figure 6, or if more drive is required, then the slaves' backplanes may be connected to the corresponding backplanes of the master. Example: at room temperature, with a drive frequency of 30 Hz, around four to five MC145003/MC145004s may be used in a system where only the master's backplanes are connected to the LCD. For applications with heavier loads (e.g., large liquid crystals) or high drive frequencies or at high temperatures, the dc voltage component seen by the LCD may be kept to a minimum by connecting the corresponding backplanes of all participating MC145003/MC145004s together.

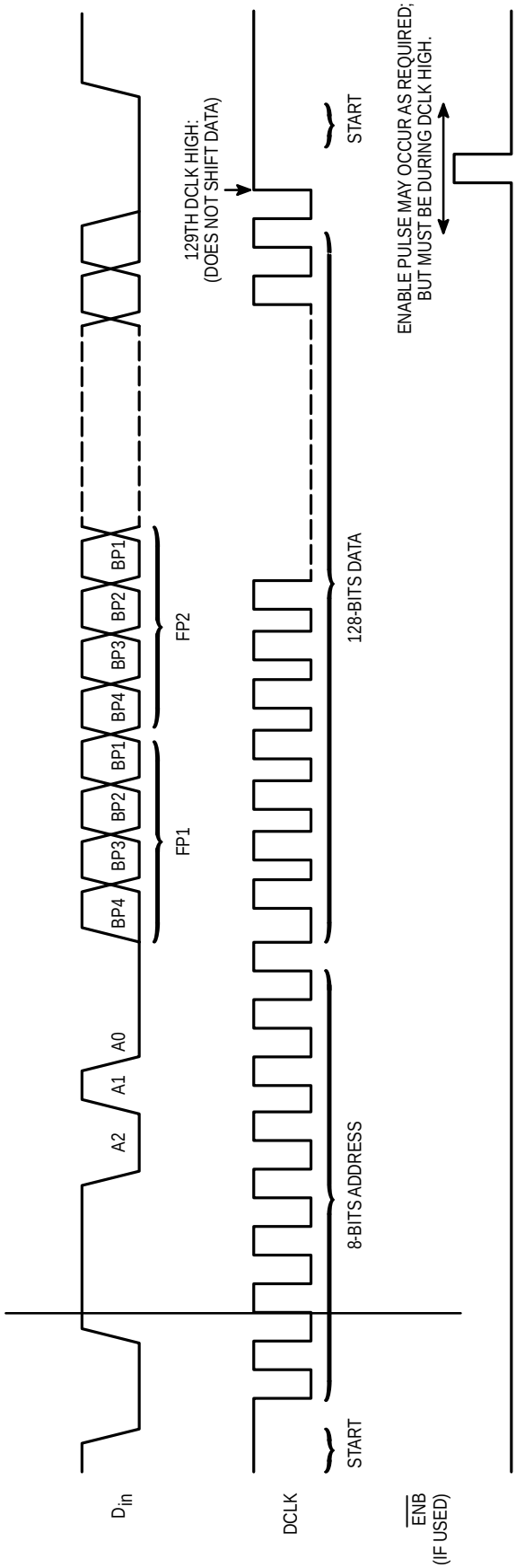


Figure 7a. Data Input — MC145003

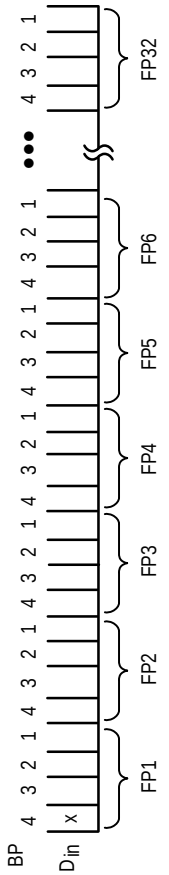


Figure 7b. Serial 128 Bits Data

Figure 7. MC145003 (SPI DEVICE)

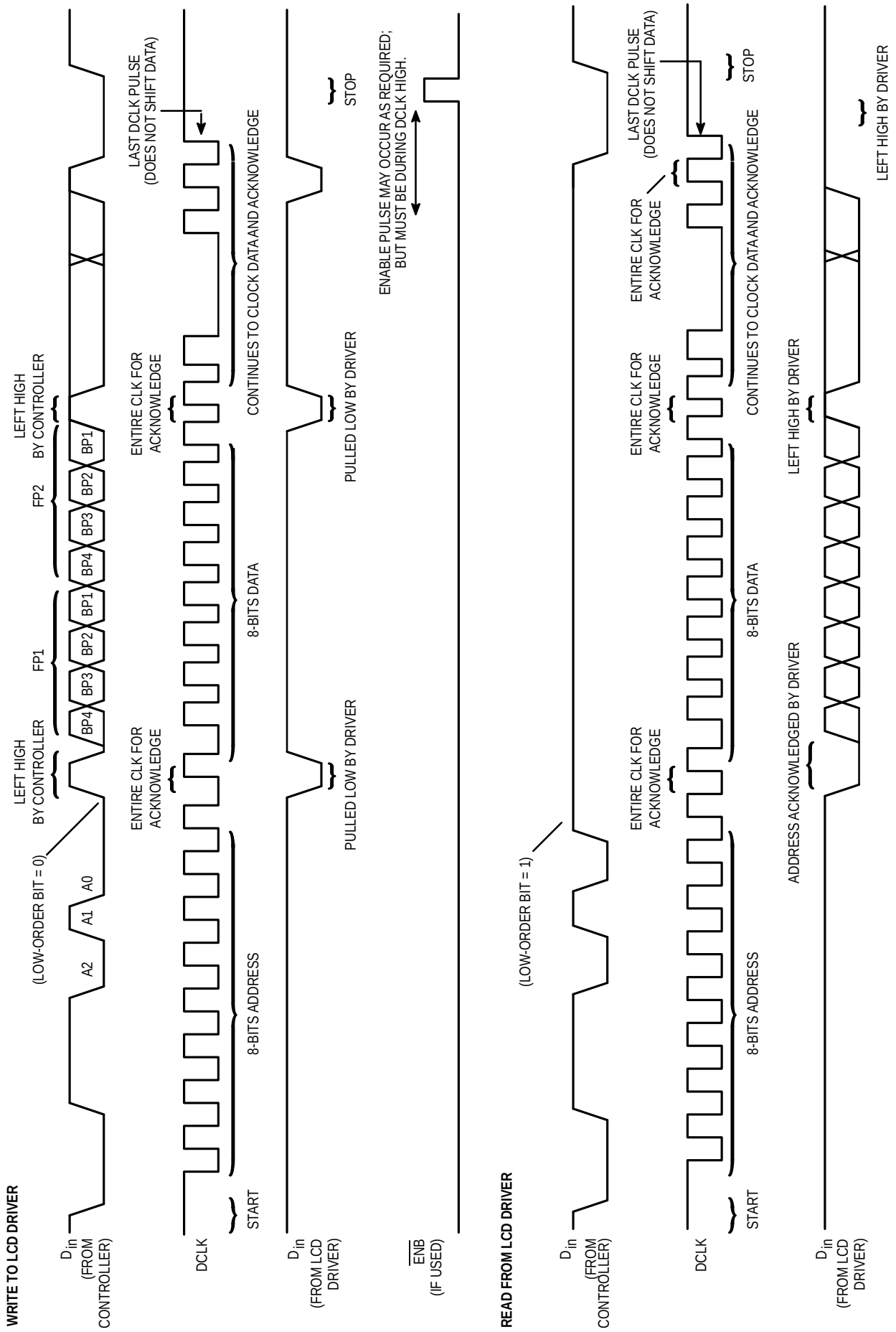


Figure 8. Data Input MC145004 (IIC Device)

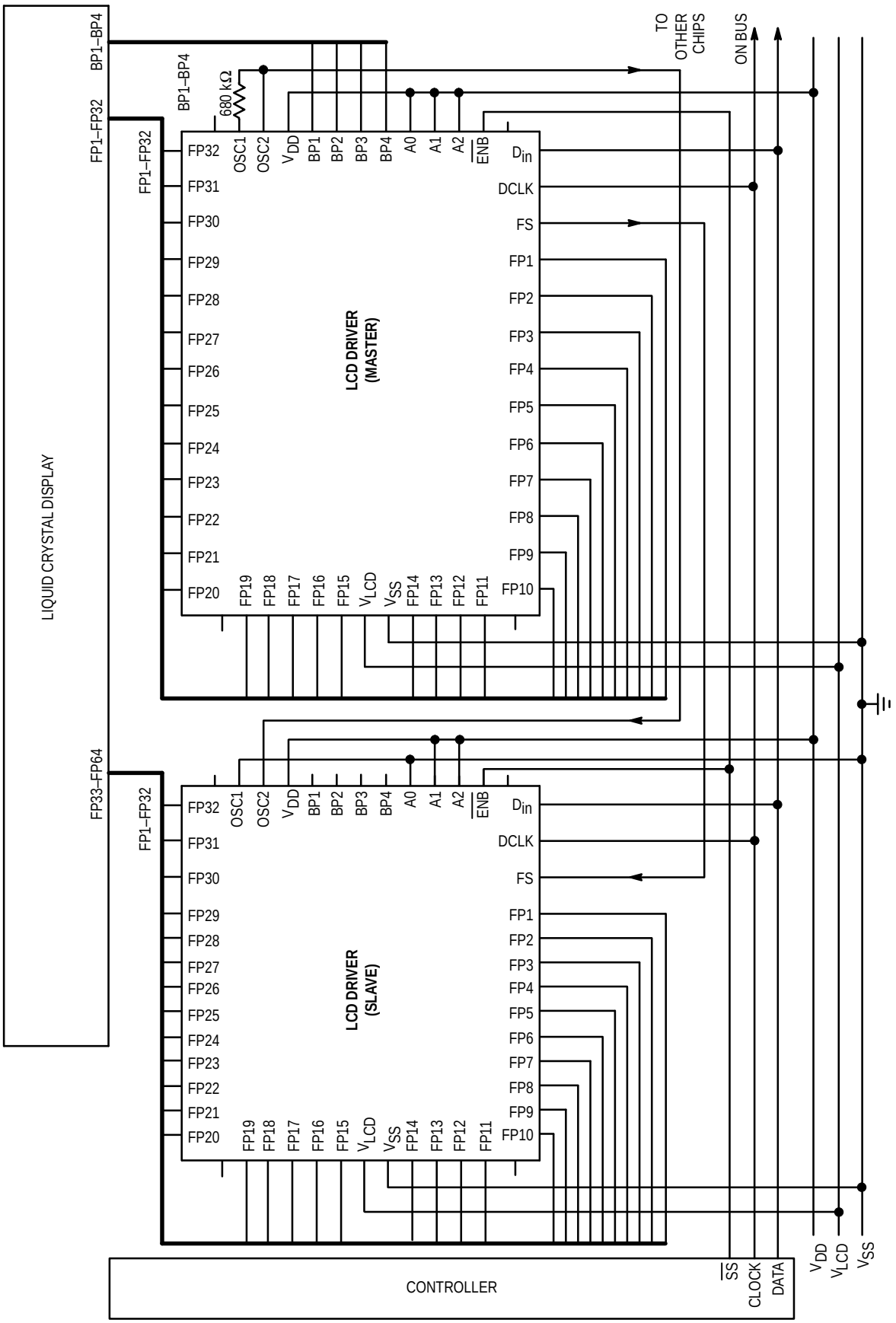


Figure 9. Cascading Example

APPLICATION INFORMATION

Figure 10 shows an interface example.

Example 1 shows a semi–automatic SPI Mode (only start and stop conditions are done in non–SPI Mode). Example 2 contains the software to use HC11 with MC145003 in manual SPI Mode. Both examples use the same hardware connection.

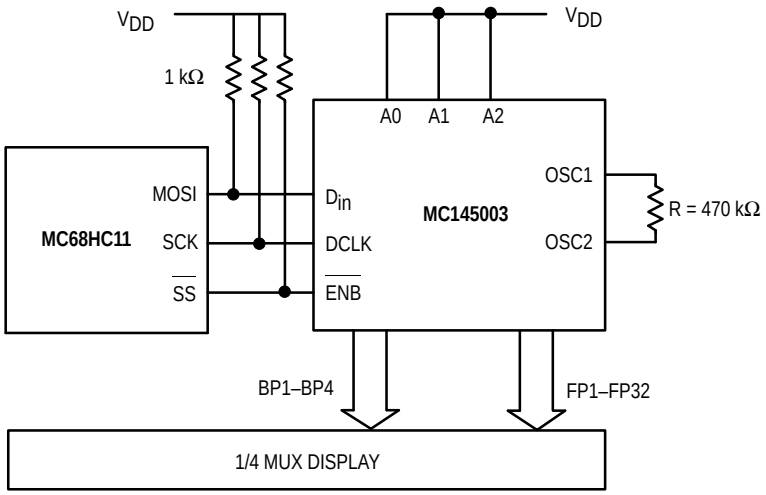


Figure 10. Interface Example Between MC68HC11 and MC145003

```
    CPOL = 0
    CPHA = 0
SPI Off
    EW = 0
    Setup Start Condition with SPI off (Write Data Port to 0)
    SPI On                    < ldaa $73, staa $1028
    Send Address Byte         $7E
    Send 16 bytes of Data
    SPI Off                   < ldaa $33, staa $1028
    DATA = 0                  SPI Off
    ENB = 1   }
    CLK = 1   }  Allows the latch of data to the FP outputs
    DATA = 1                  Stop Condition
```

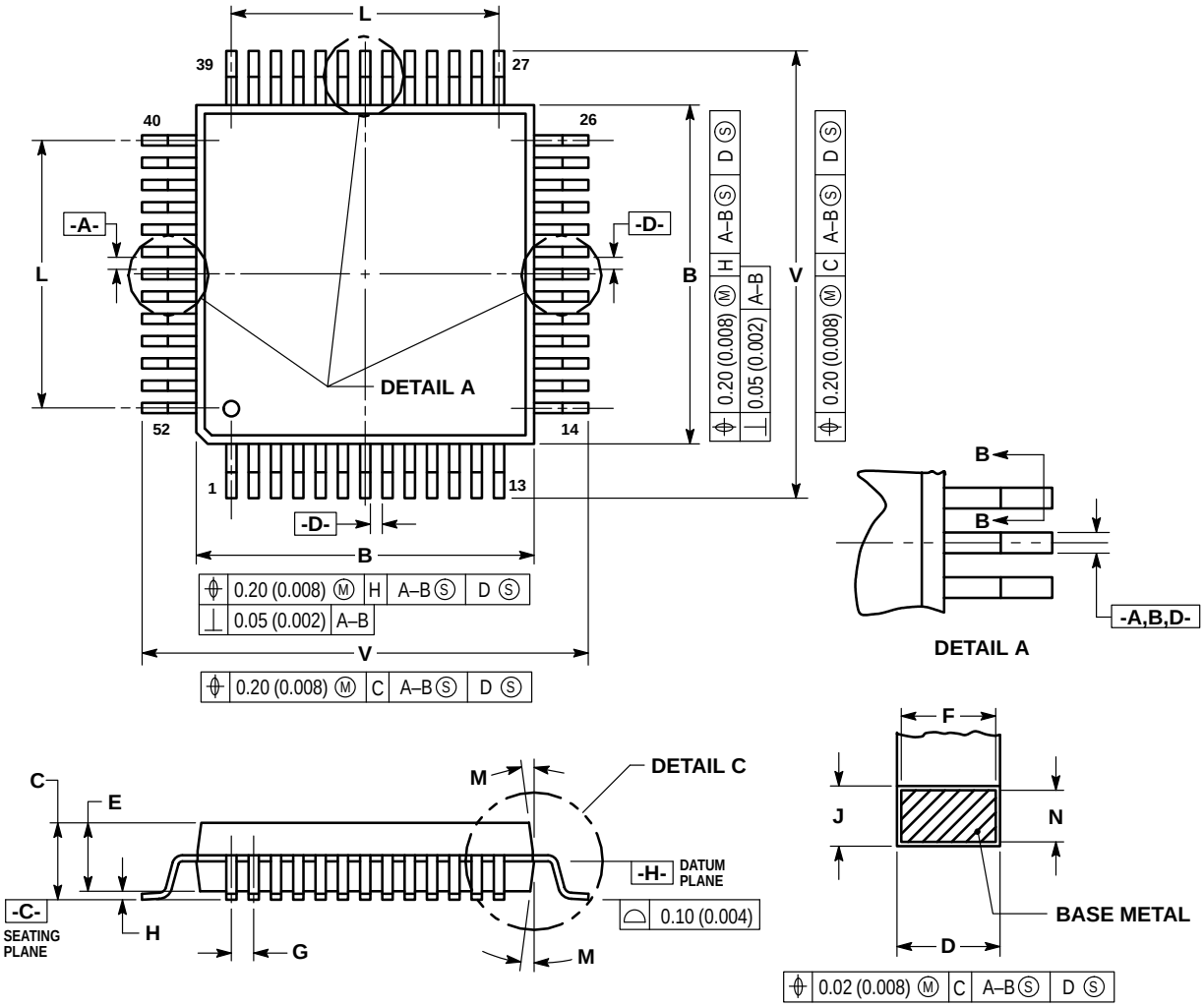
Example 1. Semi–Automatic SPI Method

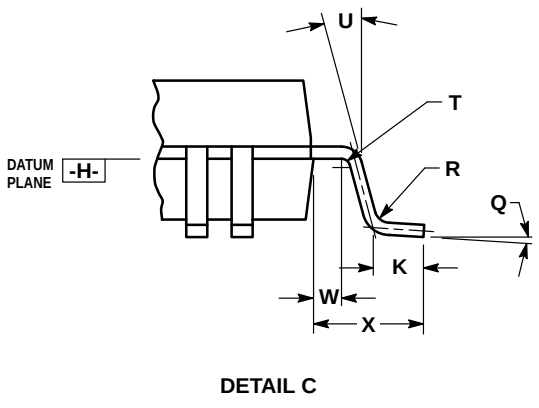
```
 1
 2                          ;=======CONSTANTS================================================
 3  0000  T                 extram     equ         $A000                ;$A000 for 8K RAM
 4  0000  T                 stack      equ         $00FF                ;last RAM byte
 5  0000  T                 intofs     equ         $1000                ;Internal Registers
 6  0000  T                 data       equ         $08
 7  0000  T                 clock      equ         $10
 8  0000  T                 enable     equ         $20
 9  0000  T                 portd      equ         8
10
11
12                          ;=======PROGRAM BEGIN============================================
13  A000  T                            org         extram               ;Program into RAM
14  A000  N  8E00FF         cold       lds         #stack               ;set stack pointer
15  A003  M  8638                      ldaa        #$38                 ;set of MOSI,SS,SCK
16  A005  T  B71009                    staa        $1009                ;DDRD
17  A008  M  C611                      ldab        #17
18  A00A  N  CEA05E                    ldx         #send
19  A00D  T  BDA010                    jsr         spi
20  A010  T                            end         cold
21
22  A010  U  18CE1000       spi        ldy         #intofs
23  A014  J  181D0820                  bclr        portd,y #enable      ;EN = 0
24  A018  T  BDA031                    jsr         start                ;start condition
25  A01B  X  A600           again      ldaa        0 , x                ;SPI Mode Use
26  A01D  T  B7102A                    staa        $102A                ;SPDR
27  A020  L  181F2980FB                brclr       $29,y,#$80,*
28  A025  H  08                        inx                              ;next DATA
29  A026  H  5A                        decb
30  A027  R  26F2                      bne         again
31  A029  J  181C0820                  bset        portd,y #enable
32  A02D  T  BDA04C                    jsr         stop                 ;stop condition
33  A030  H  39                        rts
34
35  A031  M  8633           start      ldaa        #$33                 ;Normal Mode
36  A033  T  B71028                    staa        $1028                ;SPCR
37  A036  J  181C0808                  bset        portd,y #data        ;DATA = 1
38  A03A  J  181C0810                  bset        portd,y #clock       ;CLK = 1
39  A03E  J  181D0808                  bclr        portd,y #data        ;DATA = 0
40  A042  J  181D0810                  bclr        portd,y #clock       ;CLK = 0
41  A046  M  8673                      ldaa        #$73                 ;SPI Mode
42  A048  T  B71028                    staa        $1028                ;SPCR
43  A04B  H  39                        rts
44  A04C  M  8633           stop       ldaa        #$33                 ;Normal Mode
45  A04E  T  B71028                    staa        $1028                ;SPCR
46  A051  J  181D0808                  bclr        portd,y #data        ;DATA = 0
47  A055  J  181C0810                  bset        portd,y #clock       ;CLK = 1
48  A059  J  181C0808                  bset        portd,y #data        ;DATA = 0
49  A05D  H  39                        rts
50
51  A05E  T  7E             send       fcb         $007E                ;LCD Driver Address
52  A05F  T  F0                        fcb         $00f0                ;Data to sent
53  A060  T  F0                        fcb         $00f0
54  A061  T  F0                        fcb         $00f0
55  A062  T  F0                        fcb         $00f0
56  A063  T  F0                        fcb         $00f0
57  A064  T  F0                        fcb         $00f0
58  A065  T  F0                        fcb         $00f0
59  A066  T  F0                        fcb         $00f0
60  A067  T  F0                        fcb         $00f0
61  A068  T  F0                        fcb         $00f0
62  A069  T  F0                        fcb         $00f0
63  A06A  T  F0                        fcb         $00f0
64  A06B  T  F0                        fcb         $00f0
65  A06C  T  F0                        fcb         $00f0
66  A06D  T  F0                        fcb         $00f0
67  A06E  T  F0                        fcb         $00f0
68  A06F  H  39                        rts
69
70                          ;=======PROGRAM END==============================================
```

Example 2. Manual Method

PACKAGE DIMENSIONS

QFP
FU SUFFIX
CASE 848B–02





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0. 38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters can and do vary in different applications. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4–32–1, Nishi–Gotanda, Shinagawa–ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MOTOROLA

◊ CODELINE TO BE PLACED HERE

MC145003/D