GENERAL DESCRIPTION

The XRT94L31 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L31 interfaces directly to the optical transceiver.

The XRT94L31 processes the section, line and path overhead in the SONET/SDH data stream. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L31 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L31 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L31 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L31 provides 3 mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

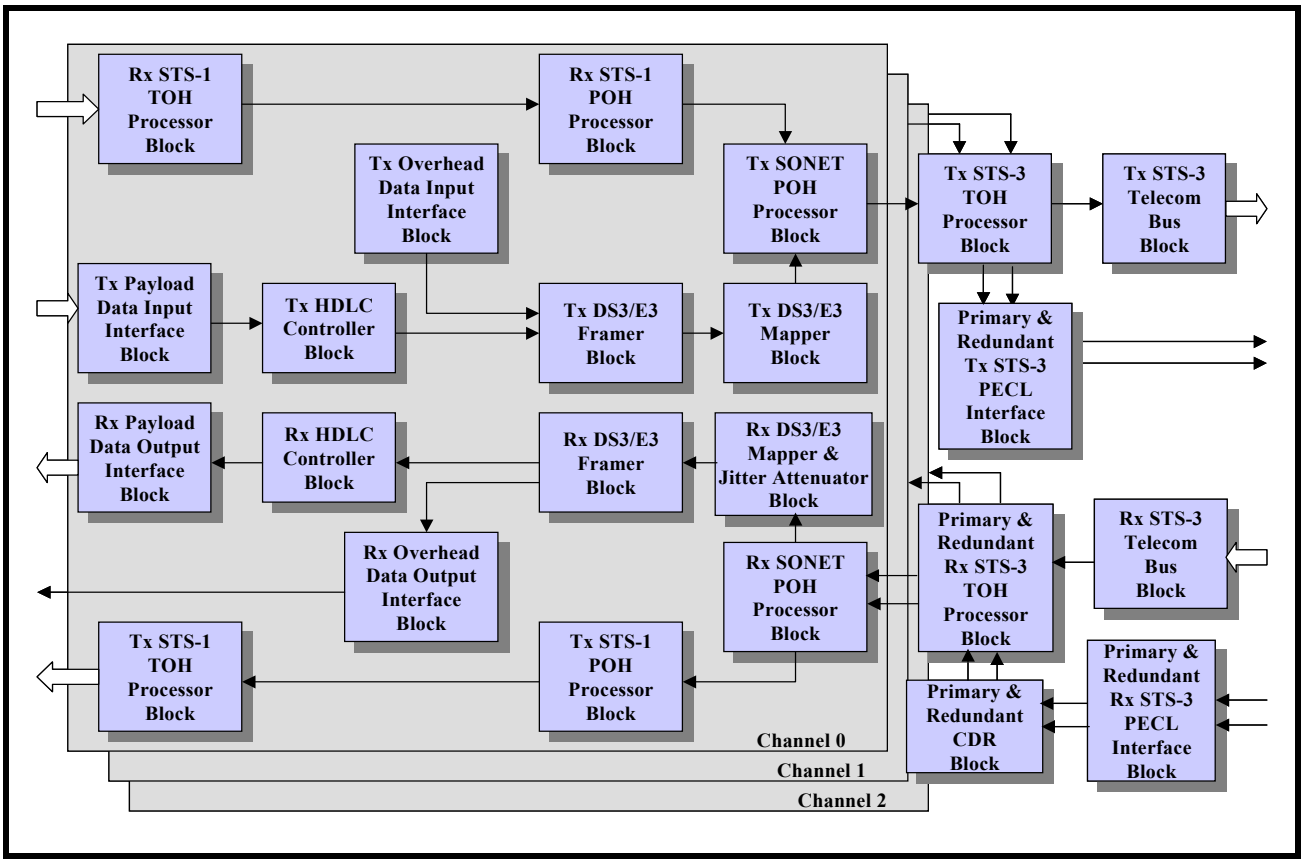
APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/ 19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149·8-bit microprocessor interface·
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 504 Ball TBGA package

FIGURE 1. BLOCK DIAGRAM OF THE XRT94L31



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L31IB	27 x 27 504 Lead TBGA	-40°C to +85°C

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
				MICROPROCESSOR INTERFACE
Y22	PCLK	I	TTL	**Microprocessor Interface Clock Input:** This clock input signal is only used if the Microprocessor Interface has been configured to operate in one of the Synchronous Modes (e.g., Power PC 403 Mode). If the Microprocessor Interface is configured to operate in one of these modes, then it will use this clock signal to do the following.· • To sample the CS*, WR*/R/W*, A[14:0], D[7:0], RD*/DS* and DBEN input pins, and· To update the state of D[7:0] and the RDY/DTACK output signals. ***NOTES:*** *1. The Microprocessor Interface can work with mPCLK frequencies ranging up to 33MHz.* *2. This pin is inactive if the Microprocessor Interface has been configured to operate in either the Intel-Asynchronous or the Motorola-Asynchronousl Modes. In this case, tie this pin to GND.*
AD25 AD23 AC21	PTYPE_0PTYPE_1P TYPE_2	I	TTL	**Microprocessor Type Select input:** These three input pins are used to configure the Microprocessor Interface block to readily support a wide variety of Microprocessor Interfaces. The relationship between the settings of these input pins and the corresponding Microprocessor Interface configuration is presented below. PTYPE[2:0] Microprocessor Interface Mode 000 Intel-Asynchronous Mode 001 Motorola - Asynchronous Mode 010 Intel X86 011 Intel I960 100 IDT3051/52 (MIPS) 101 Power PC 403 Mode 111 Motorola 860
AD27 AB25 W23 Y24 AD26 AC25 AA24 Y23 AE24 AB20 AD22 AC20 AD21 AE23 AF24	PADDR_0 PADDR_1 PADDR_2 PADDR_3 PADDR_4 PADDR_5 PADDR_6 PADDR_7 PADDR_8 PADDR_9 PADDR_10 PADDR_11 PADDR_12 PADDR_13 PADDR_14	I	TTL	**Address Bus Input pins (Microprocessor Interface):** These pins permit the Microprocessor to identify on-chip registers and Buffer/Memory locations (within the XRT94L31) whenever it performs READ and WRITE operations with the XRT94L31.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD20 AC19 AE22 AG24 AE21 AD19 AF23 AE20	PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	I/O	TTL	**Bi-Directional Data Bus pins (Microprocessor Interface):** These pins are used to drive and receive data over the bi-directional data bus, whenever the Microprocessor performs READ and WRITE operations with the Microprocessor Interface of the XRT94L31.
AF22	PWR_L/R/W*	I	TTL	**Write Strobe/Read-Write Operation Identifier:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - WR* - Write Strobe Input:** If the Microprocessor Interface is configured to operate in the Intel-Asynchronous Mode, then this input pin functions as the WR* (Active-Low WRITE Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the input buffers (associated with the Bi-Directional Data Bus pins, D[7:0]) will be enabled. The Microprocessor Interface will latch the contents on the Bi-Directional Data Bus (into the target register or address location, within the XRT94L31) upon the rising of this input. **Motorola-Asynchronous Mode - R/W* - Read/Write Operation Identification Input Pin:** If the Microprocessor Interface is operating in the Motorola-Asynchronous Mode, then this pin is functionally equivalent to the R/W* input pin. In the Motorola Mode, a READ operation occurs if this pin is held at a logic 1, coincident to a falling edge of the RD/DS* (Data Strobe) input pin. **PowerPC 403 Mode - R/W* - Read/Write Operation Identification Input:** If the Microprocessor Interface is configured to operate in the PowerPC 403 Mode, then this input pin will function as the Read/Write Operation Identification input pin. Anytime the Microprocessor Interface samples this input signal at a logic "Low" (while also sampling the CS* input pin "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A]14:0]) into the Microprocessor Interface circuitry, in preparation for this forthcoming READ operation. At some point (later in this READ operation) the Microprocessor will also assert the DBEN*/OE* input pin, and the Microprocessor Interface will then place the contents of the target register (or address location within the XRT94L31) upon the Bi-Directional Dat Bus pins (D[7:0]), where it can be read by the Microprocessor. Anytime the Microprocessor Interface samples this input signal at a logic "High" (while also sampling the CS* input pin at a logic "Low") upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents of the Address Bus (A[14:0]) into the Microprocessor Interface circuitry, in preparation for the forthcoming WRITE operation. At some point (later in this WRITE operation) the Microprocessor will also assert the RD*/DS*/WE* input pin, and the Microprocessor Interface will then latch the contents of the Bi-Directional Data Bus (D[7:0]) into the contents of the target register or buffer location (within the XRT94L31).

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AC18	PRD_L/DS*/WE*	I	TTL	**READ Strobe /Data Strobe:** The function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - RD* - READ Strobe Input:** If the Microprocessor Interface is operating in the Intel-Asynchronous Mode, then this input pin will function as the RD* (Active "Low" READ Strobe) input signal from the Microprocessor. Once this active-low signal is asserted, then the XRT94L31 will place the contents of the addressed register (or buffer location) on the Microprocessor Bi-directional Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Motorola-Asynchronous (68K) Mode - DS* - Data Strobe Input:** If the Microprocessor Interface is operating in the Motorola Asynchronous Mode, then this input will function as the DS* (Data Strobe) input signal. **PowerPC 403 Mode - WE* - Write Enable Input:** If the Microprocessor Interface is operating in the PowerPC 403 Mode, then this input pin will function as the WE* (Write Enable) input pin. Anytime the Microprocessor Interface samples this active-low input signal (along with CS* and WR*/R/W*) also being asserted (at a logic level) upon the rising edge of PCLK, then the Microprocessor Interface will (upon the very same rising edge of PCLK) latch the contents on the Bi-Directional Data Bus (D[7:0]) into the target on-chip register or buffer location within the XRT94L31.
AG23	ALE/AS_L	I	TTL	**Address Latch Enable/Address Strobe:T** he function of this input pin depends upon which mode the Microprocessor Interface has been configured to operate in, as described below. **Intel-Asynchronous Mode - ALE** If the Microprocessor Interface (of the XRT94L31) has been configured to operate in the Intel-Asynchronous Mode, then this active-high input pin is used to latch the address (present at the Microprocessor Interface Address Bus input pins (A[14:0]) into the XRT94L31 Microprocessor Interface block and to indicate the start of a READ or WRITE cycle. Pulling this input pin "High" enables the input bus drivers for the Address Bus input pins (A[14:0]). The contents of the Address Bus will be latched into the XRT94L31 Microprocessor Interface circuitry, upon the falling edge of this input signal. **Motorola-Asynchronous (68K) Mode - AS*** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this active-low input pin is used to latch the data (residing on the Address Bus, A[14:0]) into the Microprocessor Interface circuitry of the XRT94L31. Pulling this input pin "Low" enables the input bus drivers for the Address Bus input pins. The contents of the Address Bus will be latched into the Microprocessor Interface circuitry, upon the rising edge of this signal. **PowerPC 403 Mode - No Function - Tie to GND:** If the MIcroprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this input pin has no role nor function and should be tied to GND.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AE19	PCS_L	I	TTL	**Chip Select Input:** This active-low signal must be asserted in order to select the Microprocessor Interface for READ and WRITE operations between the Microprocessor and the XRT94L31 on-chip registers, LAPD and Trace Buffer locations.
AD18	PRDY_L/ DTACK*RDY	O	CMOS	**READY or DTACK Output:** The function of this input pin depends upon wich mode the Microprocessor Interface has been configured to operate in, as described below. **Intel Asynchronous Mode - RDY* - READY output:** If the Microprocessor Interface has been configured to operate in the Intel-Asyncrhronous Mode, then this output pin will function as the active-low READY output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "Low" level ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" level, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detect this output pin being toggled to the logic "Low" level. **Motorola Mode - DTACK* - Data Transfer Acknowledge Output:** If the Microprocessor Interface has been configured to operate in the Motorola-Asynchronous Mode, then this output pin will function as the active-low DTACK* ouytput. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "Low" level, ONLY when it (the Microprocessor Interface) is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has determined that this input pin has toggled to the logic "Low" leve, then it is now safe for it to move on and execute the next READ or WRITE cycle. If (during a READ or WRITE cycle) the Microprocessor Interface block is holding this output pin at a logic "High" level, then the MIcroprocessor is expected to extend this READ or WRITE cycle, until it detects this output pin being toggled to the logic "Low" level. **PowerPC 403 Mode - RDY - Ready Output:** If the Microprocessor Interface has been configured to operate in the PowerPC 403 Mode, then this output pin will function as the active-high READY output. During a READ or WRITE cycle, the Microprocessor Interface block will toggle this output pin to the logic "High" level, ONLY when the Microprocessor Interface is ready to complete or terminate the current READ or WRITE cycle. Once the Microprocessor has sampled this signal being at a logic "High" level (upon the rising edge of PCLK) then it is now safe for it to move on and execute the next READ or WRITE cycle. The Microprocessor Interface will update the state of this output pin upon the rising edge of PCLK.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AF21	PDBEN_L	I	TTL	**Bi-directional Data Bus Enable Input pin:** This input pin is used to either enable or tri-state the Bi-Directional Data Bus pins (D[7:0]), as described below. Setting this input pin "Low" enables the Bi-directional Data bus. Setting this input "High" tri-states the Bi-directional Data Bus.
AF20	PBLAST_L	I	TTL	**Last Burst Transfer Indicator input pin:** If the Microprocessor Interface is operating in the Intel-I960 Mode, then this input pin is used to indicate (to the Microprocessor Interface block) that the current data transfer is the last data transfer within the current burst operation. The Microprocessor should assert this input pin (by toggling it "Low") in order to denote that the current READ or WRITE operation (within a BURST operation) is the last operation of this BURST operation. ***NOTE:*** *Connect this input pin to GND whenever the Microprocessor Interface has been configured to operate in the Intel-Async, Motorola 68K and IBM PowerPC 403 modes.*
AG22	PINT_L	O	CMOS	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the Mapper/Framer device is requesting interrupt service from the Microprocessor. This output pin should typically be connected to the Interrupt Request input of the Microprocessor.
AB24	RESET_L	I	TTL	**Reset Input:** When this active-low signal is asserted, the XRT94L31 will be asynchronously reset. When this occurs, all outputs will be tri-stated and all on-chip registers will be reset to their default values.
AE18	DIRECT_ADD_SEL	I	TTL	**Address Location Select input pin:** This input pin must be pulled "High" in order to permit normal operation of the Microprocessor Interface.
SONET/SDH SERIAL LINE INTERFACE PINS				
T3	RXLDAT_P	I	LVPECL	**Receive STS-3/STM-1 Data - Positive Polarity PECL Input:** This input pin, along with RXLDAT_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_N functions as the Primary STS-3/STM-1 Receive Data Input Port.*
T2	RXLDAT_N	I	LVPECL	**Receive STS-3/STM-1 Data - Negative Polarity PECL Input:** This input pin, along with RXLDAT_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_P functions as the Primary Receive STS-3/STM-1 Data Input Port*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
U2	RXLDAT_R_P	I	LVPECL	**Receive STS-3/STM-1 Data - Positive Polarity PECL Input - Redundant Port:** This input pin, along with RXLDAT_R_N functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_R_N functions as the Redundant Receive STS-3/STM-1 Data Input Port.*
U1	RXLDAT_R_N	I	LVPECL	**Receive STS-3/STM-1 Data - Negative Polarity PECL Input - Redundant Port:** This input pin, along with RXLDAT_R_P functions as the Recovered Data Input, from the Optical Transceiver or as the Receive Data Input from the system back-plane. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this input pin, along with RXLDAT_R_N functions as the Redundant Receive STS-3/STM-1 Data Input Port.*
AE27	RXCLK_19MHZ	O	CMOS	**19.44MHz Recovered Output Clock:** This pin outputs a 19.44MHz clock signal that has been derived from the incoming STS-3/STM-1 LVPECL line signal (via the Receive STS-3/STM-1 PECL Interface block) and has been extracted out and derived by Clock and Data Recovery PLL (within the Receive STS-3/STM-1 PECL Interface block). To operate the STS-3/STM-1 Interface of the XRT94L31 in the loop-timing mode, route this particular output signal through a narrow-band PLL (in order to attenuate any jitter within this signal) prior to routing it to the REFTTL input pin.
P3	REFCLK_P	I	LVPECL	**Transmit Reference Clock - Positive Polarity PECL Input:** This input pin, along with REFCLK_N and REFTTL can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If these two input pins are configured to function as the timing source, a 155.52MHz clock signal must be applied to these input pins in the form of a PECL signal. Configure these two inputs to function as the timing source by writing the appropriate data into the Transmit Line Interface Control Register (Address Location = 0x0383) ***NOTE:*** *If REFTTL clock input is used, set this pin to a logic "High"*
P2	REFCLK_N	I	LVPECL	**Transmit Reference Clock - Negative Polarity PECL Input:** This input pin, along with REFCLK_P and REFTTL can be configured to function as the timing source for the STS-3/STM-1 Transmit Interface Block. If these two input pins are configured to function as the timing source, then the user must apply a 155.52MHz clock signal, in the form of a PECL signal to these input pins. These two inputscan be configured to function as the timing source by writing the appropriate data into the Transmit Line Interface Control Register (Address Location = 0x0383). ***NOTE:*** *Set this pin to a logic "Low" if REFTTL clock input is used*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
P5	TXLDATO_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity LVPECL Output:** This output pin, along with TXLDATO_N functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System-Board). For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_P/TXLCLKO_N. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_N functions as the Primary Transmit STS-3/STM-1 Data Output Port.*
P6	TXLDATO_N	O	LVPECL	**Transmit STS-3/STM-1 Data - Negative Polarity LVPECL Output:** This output pin, along with TXLDATO_P functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System board). For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_P/TXLCLKO_N. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_P functions as the Primary Transmit STS-3/STM-1 Data Output Port.*
M4	TXLDATO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Data - Positive Polarity LVPECL Output - Redundant Port:** This output pin, along with TXLDATO_R_N functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver or to the system back-plane. For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_R_P/ TXLCLKO_R_N). ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_N functions as the Redundant Transmit STS-3/STM-4 Data Output Port.*
M3	TXLDATO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Data - Negative Polarity LVPECL Output - Redundant Port:** This output pin, along with TXLDATO_R_P functions as the Transmit Data Output (from the Transmit STS-3/STM-1 PECL Interface block), to the Optical Transceiver (for transmission to remote terminal equipment) or to the system back-plane (for transmission to some other System board). For High-Speed Back-Plane Applications, data is output from these output pins upon the rising/falling edge of TXLCLKO_R_P/ TXLCLKO_R_N).Note: ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLDATO_R_P functions as the Redundant Transmit STS-3/STM-1 Data Output Port.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
N6	TXLCLKO_P	O	LVPECL	**Transmit STS-3/STM-1 Clock - Positive Polarity PECL Output:** This output pin, along with TXLCLKO_N functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_P/TXLDATO_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_N functions as the Primary Transmit Output Clock signal.*
N5	TXLCLKO_N	O	LVPECL	**Transmit STS-3/STM-1 Clock - Negative Polarity PECL Output:** This output pin, along with TXLCLKO_P functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_P/TXLDATO_N output pins upon the falling edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_N functions as the Primary Transmit Output Clock signal.*
M1	TXLCLKO_R_P	O	LVPECL	**Transmit STS-3/STM-1 Clock - Positive Polarity PECL Output - Redundant Port:** This output pin, along with TXLCLKO_R_N functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_R_P/TXLDATO_R_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_R_N functions as the Redundant Transmit Output Clock signal.*
M2	TXLCLKO_R_N	O	LVPECL	**Transmit STS-3/STM-1 Clock - Negative Polarity PECL Output - Redundant Port:** This output pin, along with TXLCLKO_R_P functions as the Transmit Clock Output signal. These output pins are typically used in High-Speed Back-Plane Applications. In this case, outbound STS-3/STM-1 data is output via the TXLDATO_R_P/TXLDATO_R_N output pins upon the rising edge of this clock signal. ***NOTE:*** *For APS (Automatic Protection Switching) purposes, this output pin, along with TXLCLKO_R_P functions as the Redundant Transmit Output Clock signal.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
P1	REFTTL	I	TTL	**19.44MHz or 77.76MHz Clock Synthesizer Reference Clock Input Pin:** The function of this input pin depends upon whether or not the Clock Synthesizer block is enabled. **If Clock Synthesizer is Enabled.** If the Clock Synthesizer block is enabled, then it will be used to generate the 155.52MHz, 19.44MHz and/or 77.76MHz clock signal for the Transmit STS-3/STM-1 circuitry. In this mode, the user should apply a clock signal of any of the following frequencies to this input pin. • 19.44 MHz • 38.88 MHz • 51.84 MHz • 77.76 MHz Afterwards, the user needs to write the appropriate data into the Transmit Line Interface Control Register (Address Location = 0x0383) in order to (1) configure the Clock Synthesizer Block to accept any of the above-mentioned signals and generate a 155.52MHz, 19.44MHz or 77.76MHz clock signal, (2) to configure the Clock Synthesizer to function as the Clock Source for the STS-3/STM-1 block. **If Clock Synthesizer is NOT Enabled:** If the Clock Synthesizer block is NOT enabled, then it will NOT be used to generate the 19.44MHz and/or 77.76MHz clock signal, for the STS-3/STM-1 block. In this configuration seting, the user MUST apply a 19.44MHz clock signal to this input pin. ***NOTE:*** *The user must place a clock signal to this input pin in order to perform READ and WRITE operations to much of the SONET/SDH-related registers via the Microprocessor Interface.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>AG3</td><td>LOSTTL</td><td>I</td><td>TTL</td><td>
Loss of Optical Carrier Input - Primary Receive STS-3/STM-1 PECL Interface - TTL Input:
If the user is using an Optical Transceiver that contains an LOS (or Signal Detect) output that is of the CMOS/TTL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSTTL input pin to be either an active-low or an active-high signal, by pulling the LOSPECL input pin to the appropriate level as described below.
<table>
<tr><th>LOSPECL</th><th>LOSTTL Active-Low/ Active-High</th><th>Description of LOSTTL</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>
If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
• The Primary Receive STS-3 TOH Processor block will declare the Loss of Optical Carrier condition.
• The Primary Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Primary Receive STS-3 TOH Processor block to declare the LOS defect condition.
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>AG25</td><td>LOSTTL_R</td><td>I</td><td>TTL</td><td>
Loss of Optical Carrier Input - Redundant Receive STS-3/STM-1 PECL Interface - TTL Input:
If the user is using the Optical Transceiver that contains an LOS (or Signal Detect) output that is of the CMOS/TTL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSTTL_R input pin to either an active-low or an active-high signal, by pulling the LOSPECL_R input pin to the appropriate level as described below.
<table>
<tr><th>LOSPECL_R</th><th>LOSTTL_R Active-Low/ Active-High</th><th>Description of LOSTTL_R</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>
If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
The Redundant Receive STS-3 TOH Processor block wil declare the Loss of Optical Carrier condition
The Redundant Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Redundant Receive STS-3 TOH Processor block to declare the LOS defect condition.
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>L4</td><td>LOSPECL_P</td><td>I</td><td>LVPECL</td><td>
Loss of Optical Carrier/Signal Input - Single-Ended PECL Interface Input - Primary Receive STS-3/STM-1 PECL Interface:
If the user is using an Optical Transceiver that contains an LOS (or Signal Detect) output pin that is of the LVPECL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSPECL_P input pin to function as either an active-low or active-low signal by pulling the LOSTTL input pin to the appropriate level as described below.

<table>
<tr><th>LOSTTL</th><th>LOSPECL_P Active-Low/ Active-High</th><th>Description of LOSPECL_P</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>

If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
• The Primary Receive STS-3 TOH Processor block will declare the Loss of Optical Carrier condition.
• The Primary Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Primary Receive STS-3 TOH Processor block to declare the LOS defect condition.
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>I/O</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>L3</td><td>LOSPECL_R</td><td>I</td><td>LVPECL</td><td>
Loss of Optical Carrier/Signal Input - Single-Ended PECL Interface Input - Redundant Receive STS-3/STM-1 PECL Interface:
If the user is using an Optical Transceiver that contains an LOS (or Signal Detect) output pin that is of the LVPECL format, then connect this LOS output signal to this input pin of the XRT94L31.
Configure the LOSPECL_R input pin to function as either an active-low or active-low signal by pulling the LOSTTL input pin to the appropriate level as described below.

<table>
<tr><th>LOSTTL</th><th>LOSPECL_R Active-Low/ Active-High</th><th>Description of LOSPECL_R</th></tr>
<tr><td>GND</td><td>Active-Low</td><td>Setting this input pin "low" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
<tr><td>VDD</td><td>Active-High</td><td>Setting this input pin "high" configures the Redundant Receive Line Interface block to declare the "LOS_Detect" condition.</td></tr>
</table>

If this input pin is pulled to the appropriate state such that LOS is TRUE, then all of the following events will happen.
• The Redundant Receive STS-3 TOH Processor block will declare the Loss of Optical Carrier condition.
• The Redundant Receive STS-3/STM-1 Line Interface block will declare the LOS_Detect condition.Note:
NOTE: If this input pin is pulled to the appropriate state such that LOS is TRUE, this (by itself) will NOT cause the Redundant Receive STS-3 TOH Processor block to declare the LOS defect condition..
</td></tr>
</table>

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
V1	LOCKDET	O	CMOS	**Lock Detect Output Pin - Clock and Data Recovery PLL Block** This output pin indicates whether or not the Clock and data recovery PLL block has obtained lock to incoming STS-3/STM-1 signal. As the Receive STS-3/STM-1 PECL Interface block receives this STS-3/STM-1 signal, the CDR (Clock and Data Recovery) PLL will attempt to lock onto this STS-3/STM-1 PECL signal. The Receive STS-3/STM-1 PECL Interface block will (internally) derive a 19.44MHz clock signal from this incoming STS-3/STM-1 PECL signal. The CDR PLL will then continuously compare the frequency of this 19.44MHz clock signal, with that derived from either the Clock Synthesizer block (or from the 19.44MHz clock signal applied to the REFTTL input pin). If the CDR PLL determines that the frequency difference between these two signals is less than 0.05%, then it will declare that the CDR PLL is in Lock. If the CDR PLL determines that the frequency difference between these two signals is greater than 0.05%, then it will declare the the CDR PLL is Out of Lock. 0 - Indicates that the CDR PLL (within the Receive STS-3/STM-1 PECL Interface Block) is declaring the Lock Condition. 1 - Indicates that the CDR PLL is declaring the Out of Lock Condition.
STS-3/STM-1 TELECOM BUS INTERFACE - TRANSMIT DIRECTION				
E1	TXA_CLK	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Clock Output Signal:** This output clock signal functions as the clock source for the Transmit STS-3/STM-1 Telecom Bus Interface. All signals, that are output via the Transmit STS-3/STM-1 Telecom Bus Interface (e.g., TXA_C1J1, TXA_ALARM, TXA_DP, TXA_PL and TXA_D[7:0]) are updated upon the rising edge of this clock signal. This clock signal operates at 19.44MHz and is derived from the Clock Synthesizer block.
F2	TXA_C1J1whether or not the	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Output Signal:** This output pin pulses "High" under the following two conditions; • Coincident to whenever the C1/J0 byte (of the outbound STS-3/STM-1 signal) is being output via the TxA_D[7:0] output, and • Coincident to whenever the J1 byte(s) (of the outbound STS-3/STS-3c/STM-1 signal) is being output via the TxA_D[7:0] output. ***NOTES:*** *1. The Transmit STS-3/STM-1 Telecom Bus Interface will indicate that it is currently transmitting the C1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "High" (for one period of TXA_CLK) and keeping the TXA_PL output pin pulled "Low".* *2. The Transmit STS-3/STM-1 Telecom Bus will indicate that it is currently transmitting the J1 byte (via the TXA_D[7:0] output pins), by pulsing this output pin "High" (for one period of TXA_CLK) while the TXA_PL output pin is pulled "High".* *3. This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface block is enabled and is configured to operate in the Re-Phase OFF Mode.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E2	TXA_ALARM	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus - Alarm Indicator Output signal:** This output pin pulses "High", coincdent to the instant that the Transmit STS-3/STM-1 Telecom Bus outputs a byte (via the TxA_D[7:0] output pins) that pertains to any that STS-1 or STS-3c signal is carrying the AIS-P indicator. This output pin is "Low" for all other conditions. ***NOTE:*** *This output pin is only active if the Transmit STS-3/STM-1 Telecom Bus Interface is enabled and has been configured to operate in the Re-Phase OFF Mode.*
H3	TXA_DP	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus - Parity Output pin:** This output pin can be configured to function as one of the following.To reflect either the EVEN or ODD parity value of the bits which are currently being output via the TXA_D[7:0] output pins. To reflect either the EVEN or ODD parity value of the bits which are currently being output via the TXA_D[7:0] output pins and the states of the TXA_PL and TXA_C1J1 output pins. ***NOTE:*** *Any one of these configuration selections can be made by writing the appropriate value into the Telecom Bus Control Register (Address Location = 0x0137).*
G4	TxSBFP	I	TTL	**Transmit STS-3/STM-1 Frame Alignment Sync Input:** The Transmit STS-3 TOH Processor Block can be configured to initiate its generation of a new outbound STS-3/STM-1 frame based upon an externally supplied 8kHz clock signal to this input pin. If this feature is used, the Transmit STS-3/STM-1 Telecom Bus Interface will begin transmitting the very first byte of given STS-3 or STM-1 frame, upon sensing a rising edge (of the 8kHz signal) at this input pin. ***NOTES:*** 1. *If this input pin is connected to GND, then the Transmit STS-3 TOH Processor block will generate its outbound STS-3/STM-1 frames asynchronously, with respect to any input signal.* 2. *This input signal must be synchronized with the signal that is supplied to the REFTTL input pin. Failure to insure this will result in bit errors being generated within the outbound STS-3/STM-1 signal.* 3. *The user must supply an 8kHz pulse (to this input pin) that has a width of approximately 51.4412.8ns (one 19.44MHz clock period). The user must not apply a 50% duty cycle 8kHz signal to this input pin.* 4. *Register HRSYNC_DLY (Address Location: 0x0135) defines the timing for TxSBFP input pin.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
K5	TxA_PL	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Payload Data Indicator Output Signal:** This output pin indicates whether or not the Transmit STS-3/STM-1 Telecom Bus Interface is currently placing a Transport Overhead byte or a non-Transport Overhead Byte (e.g., STS-1 SPE, STS-3c SPE, VC-3 or VC-4 data) via the TXA_D[7:0] output pins. This output pin is pulled "Low" for the duration that the Transmit STS-3/STM-1 Telecom Bus Interface is transmitting a Transport Overhead byte via the TXA_D[7:0] output pins. Conversely, this output pin is pulled "High" for the duration that the Transmit STS-3/STM-1 Telecom Bus Interface is transmitting something other than a Transport Overhead byte via the TXA_D[7:0] output pins.
J4 G3 D1 F3 J5 H4 D2 E3	TxA_D0 TxA_D1 TxA_D2 TxA_D3 TxA_D4 TxA_D5 TxA_D6 TxA_D7	O	CMOS	**Transmit STS-3/STM-1 Telecom Bus Interface - Transmit Output Data Bus pins:** These 8 output pins function as the Transmit STS-3/STM-1 Telecom Bus Interface - Output data bus. If the STS-3/STM-1 Telecom Bus Interface is enabled, then all outbound STS-3/STM-1 data is output via these pins (in a byte-wide manner), upon the rising edge of the TXA_CLK output pin.
STS-3/STM-1 TELECOM BUS INTERFACE - RECEIVE DIRECTION				
W2	RxD_CLK	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Clock Input Signal:** This input clock signal functions as the clock source for the Receive STS-3/STM-1 Telecom Bus Interface. All input signals are sampled upon the falling edge of this input clock signal. This clock signal should operate at 19.44MHz.Note: ***NOTE:*** *This input pin is only used if the STS-3/STM-1 Telecom Bus has been enabled. It should be connected to GND otherwise.*
AA3	RxD_PL	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Payload Data Indicator Output Signal:** This input pin indicates whether or not the Receive STS-3/STM-1 Telecom Bus Interface is currently receiving Transport Overhead bytes or non-Transport Overhead bytes (e.g., STS-1 SPE, STS-3c SPE,VC-3 or VC-4 data) via the RXD_D[7:0] input pins. This input pin should be pulled "Low" for the duration that the Receive STS-3/STM-1 Telecom Bus Interface is receiving a Transport Overhead byte via the RXD_D[7:0] input pins. Conversely, this input pin should be pulled "High" for the duration that the Receive STS-3/STM-1 Telecom Bus Interface is receiving something other than a Transport Overhead byte via the RXD_D[7:0] input pins. ***NOTE:*** *Connect this pin to GND if the STS-3/STM-1 Telecom Bus is NOT enabled*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD1	RxD_C1J1	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal:** This input pin should be pulsed "High" during both of the following conditions. a. Coincident to whenever the C1/J0 byte (within the incoming STS-3/STM-1 signal) is being applied to the Receive STS-3/STM-1 Telecom Bus - Data Input pins (RXD_D[7:0]). b. Coincident to whenever the J1 byte(s) (within the incoming STS-3/STM-1 signal) is being applied to the Receive STS-3/STM-1 Telecom Bus - Data Input pins (RXD_D[7:0]) input. ***NOTE:*** *This input pin should be pulled "Low" during all other times.*
AB3	RxD_DP	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Parity Input pin:** This input pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits (within the incoming STS-3/STM-1 signal) which are currently being input via the RXD_D[7:0] input pins. The EVEN or ODD parity value of the bits (within the incoming STS-3/STM-1 signal) which are being input via the RXD_D[7:0] input and the states of the RXD_PL and RXD_C1J1 input pins. The Receive STS-3/STM-1 Telecom Bus Interface block will use this input signal to compute and verify the Parity of each byte within the incoming STS-3/STM-1 data-stream. ***NOTES:*** 1. *Any one of these configuration selections can be made by writing the appropriate value into the Telecom Bus Control register (Address Location = 0x0137).* 2. *Tie this input pin to GND if the STS-3/STM-1 Telecom Bus Interface is disabled.*
W1	RxD_ALARM	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Alarm Indicator Input:** This input pin should be pulsed "High" for one RxD_CLK period coincident to whenever the Receive STS-3/STM-1 Telecom Bus Interface is accepting a byte from an incoming STS-1 or STS-3c signal (via the RxD_D[7:0] input pins) that is carrying the AIS-P indicator. This input pin should be held at a logic "Low" at all other times. ***NOTES:*** 1. *If the RxD_ALARM input signal pulses "High" for any given STS-1 signal (within the incoming STS-3), the XRT94L31 will automatically declare the AIS-P defect condition for that STS-1 or STS-3c channel.* 2. *Tie this input pin to GND, if the STS-3/STM-1 Telecom Bus Interface is disabled.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
Y2 AD2 AC3 AA4A B4 Y1 AD3 AA5	RxD_D0 RxD_D1 RxD_D2 RxD_D3 RxD_D4 RxD_D5 RxD_D6 RxD_D7	I	TTL	**Receive STS-3/STM-1 Telecom Bus Interface - Receive Input Data Bus pins:** These 8 input pins function as the Receive STS-3/STM-1 Telecom Bus Interface Receive Input data bus. All STS-3/STM-1 data is sampled and latched (into the XRT94L31, via these input pins) upon the falling edge of the RXA_CLK input pin. ***NOTE:*** *These input pins are only active if the Receive STS-3/STM-1 Telecom Bus Interface has been enabled. If the XRT94L31 is configured to exchange STS-3/STM-1 data via the PECL Interface (instead), tie these pins to GND.*
SONET/SDH OVERHEAD INTERFACE - TRANSMIT DIRECTION				
H6	TxTOHClk	O	CMOS	**Transmit TOH Input Port - Clock Output:** This output pin, along with the TxTOHEnable, TxTOHFrame output pins and the TxTOH and TxTOHIns input pins function as the Transmit TOH Input Port.The Transmit TOH Input Port is usedr to insert the users own value for the TOH bytes (in the outbound STS-3/STM-1 signal). This output pin provides the user with a clock signal. If the TxTOHEnable output pin is "High" and if the TxTOHIns input pin is pulled "High", then the user is expected to provide a given bit (within the TOH) to the TxTOH input pin, upon the falling edge of this clock signal. The data, residing on the TxTOH input pin will be latched into the XRT94L31 upon the rising edge of this clock signal. The XRT94L31 will then insert this particular TOH bit value into the appropriate TOH bit positions within the outbound STS-3 data-stream. ***NOTE:*** *The Transmit TOH Input Port only supports the insertion of the TOH within the first STS-1, within the outbound STS-3 signal.*
G5	TxTOHEnable	O	CMOS	**Transmit TOH Input Port - TOH Enable (or READY) indicator:** This output pin, along with the TxTOHClk, TxTOHFrame output pins and the TxTOH and TxTOHIns input pins function as the Transmit TOH Input Port. This output pin will toggle and remain "High" anytime the Transmit TOH Input Port is ready to externally accept TOH data. To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHFrame and this output pin upon the rising edge of TxTOHClk. • Whenever this output pin pulses "High", then the user's external circuitry should drive the TxTOHIns input pin "High". • Next, output the next TOH bit, onto the TxTOH input pin, upon the rising edge of TxTOHClk

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
F8	TxTOH	I	TTL	**Transmit TOH Input Port - Input pin:** This input pin, along with the TxTOHIns input pin, the TxTOHEnable and TxTOHFrame and TxTOHClk output pins function as the Transmit TOH Input Port.To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHFrame and TxTOHEnable upon the rising edge of TxTOHClk • Whenever TxTOHEnable pulses "High", then the user's external circuitry should drive the TxTOHIns input pin "High" • Next, output the next TOH bit, onto this input pin, upon the rising edge of TxTOHClk. The Transmit TOH Input Port will sample the data (on this input pin) upon the falling edge of TxTOHClk. ***NOTE:*** *Data at this input pin will be ignored (e.g., not sampled) unless the TxTOHEnable output pin is "High" and the TxTOHIns input pin is pulled "High".*
E8	TxTOHFrame	O	CMOS	**Transmit TOH Input Port - STS-3/STM-1 Frame Indicator:** This output pin, along with TxTOHClk, TxTOHEnable output pins, and the TxTOH and TxTOHIns input pins function as the Transmit TOH Input Port.This output pin will pulse "High" (for one period of TxTOHClk), one TxTOHClk clock period prior to the first TOH bit of a given STS-3 frame, being expected via the TxTOH input pin.To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHEnable and this output pin upon the rising edge of TxTOHClk. • Whenever the TxTOHEnable output pin pulse "High", then the user's external circuitry should drive the TxTOHIns input pin "High". • Next, output the next TOH bit, onto the TxTOH input pin, upon the rising edge of TxTOHClk. ***NOTE:*** *The external circuitry (which is being interfaced to the Transmit TOH Input Port can use this particular output pin to denote the boundary of STS-3 frames.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D6	TxTOHIns	I	TTL	**Transmit TOH Input Port - Insert Enable Input pin:** This input pin, along with the TxTOH input pin, and the TxTOHEnable, TxTOHFrame and TxTOHClk output pins function as the Transmit TOH Input Port. This input pin is used to either enable or disable the Transmit TOH Input Port. If this input pin is "Low", then the Transmit TOH Input Port will be disabled and will not sample and insert (into the outbound STS-3 data stream) any data residing on the TxTOH input, upon the rising edge of TxTOHClk. If this input pin is "High", then the Transmit TOH Input Port will be enabled. In this mode, whenever the TxTOHEnable output pin is also "High", the Transmit TOH Input Port will sample and latch any data that is presented on the TxTOH input pin, upon the rising edge of TxTOHClk. To externally insert user values of TOH into the outbound STS-3 data stream via the Transmit TOH Input Port, do the following. • Continuously sample the state of TxTOHFrame and TxTOHEnable upon the rising edge of TxTOHClk. • Whenever the TxTOHEnable output pin is sampled "High" then the user's external circuitry should drive this input pin "High". • Next, output the next TOH bit, onto the TxTOH input pin, upon the falling edge of TxTOHClk. The Transmit TOH Input Port will sample the data (on this input pin) upon the falling edge of TxTOHClk.] ***NOTES:*** *1. Data applied to the TxTOH input pin will be sampled according to the following insertion priority scheme:* *2. For DCC, E1, F1, E2 bytes, TxTOH input pin will be sampled if both TxTOHEnable and TxTOHIns are "High".* *3. For other TOH bytes, TxTOH input pin will be sampled if both TxTOHEnable and TxTOHIns are "High" or if both TxTOHIns and Software Insertion Enabled are "Low".*
B4	TxLDCCEnable	O	CMOS	**Transmit - Line DCC Input Port - Enable Output pin:** This output pin, along with the TxTOHClk output pin and the TxLDCC input pin are used to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the outbound STS-3 data-stream. The Line DCC HDLC Controller circuitry (which is connected to the TxTOHClk, the TxSDCC and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "High", then the Line DCC HDLC Controller circuitry should place the next Line DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxLDCC input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxLDCC input pin, will be sampled upon the falling edge of TxOHClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D7	TxSDCCEnable	O	CMOS	**Transmit - Section DCC Input Port - Enable Output pin:** This output pin, along with the TxTOHClk output pin and the TxSDCC input pin is used to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the D1, D2 and D3 byte-fields, within the outbound STS-3 data-stream. The Section DCC HDLC Controller circuitry (which is connected to the TxTOHClk, the TxSDCC and this output pin, is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "High", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxSDCC input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxSDCC input pin, will be sampled upon the falling edge of TxOHClk.
C5	TxSDCC	I	TTL	**Transmit - Section DCC Input Port - Input pin:** This input pin, along with the TxSDCCEnable and the TxTOHClk output pins is used to insert their value for the D1, D2 and D3 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the D1, D2 and D3 byte fields, within the outbound STS-3 data-stream. The Section DCC HDLC Circuitry that is interfaced to this input pin, the TxSDCCEnable and the TxTOHClk pins is suppose to do the following. It should continuously monitor the state of the TxSDCCEnable input pin. Whenever the TxSDCCEnable input pin pulses "High", then the Section DCC HDLC Controller circuitry should place the next Section DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto this input pin upon the rising edge of TxTOHClk. Any data that is placed on the TxSDCC input pin, will be sampled upon the falling edge of TxTOHClk.Note: ***NOTE:*** *This pin should be connected to GND if it is not used.*
D8	TxLDCC	I	TTL	**Transmit - Line DCC Input Port:** This input pin, along with the TxLDCCEnable and the TxTOHClk pins is used to insert their value for the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the D4, D5, D6, D7, D8, D9, D10, D11 and D12 byte-fields, within the outbound STS-3 data-stream. Whatever Line DCC HDLC Controller Circuitry is interface to the this input pin, the TxLDCCEnable and the TxTOHClk is suppose to do the following. It should continuously monitor the state of the TxLDCCEnable input pin. Whenever the TxLDCCEnable input pin pulses "High", then the Section DCC Interface circuitry should place the next Line DCC bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxLDCC input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxLDCC input pin, will be sampled upon the falling edge of TxTOHClk.Note: ***NOTE:*** *This pin should be connected to GND if it is not used.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E9	TxE1F1E2Enable	O	CMOS	**Transmit E1-F1-E2 Byte Input Port - Enable (or Ready) Indicator Output pin:** This output pin, along with the TxTOHClk output pin and the TxE1F1E2 input pin is used to insert their value for the E1, F1 and E2 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and will insert into the E1, F1 and E2 byte-fields, within the outbound STS-3 data-stream. Whatever external circuitry (which is connected to the TxTOHClk, the TxE1F1E2 and this output pin), is suppose to do the following. It should continuously monitor the state of this output pin. Whenever this output pin pulses "High", then the external circuitry should place the next orderwire bit (to be inserted into the Transmit STS-3 TOH Processor block) onto the TxE1F1E2 input pin, upon the rising edge of TxTOHClk. Any data that is placed on the TxE1F1E2 input pin, will be sampled upon the falling edge of TxOHClk.
C6	TxE1F1E2Frame	O	CMOS	**Transmit E1-F1-E2 Byte Input Port - Framing Output Pin.** This output pin pulses "High" for one period of TxTOHClk, one TxTOHClk bit-period prior to the Transmit E1-F1-E2 Byte Input Port expecting the very first byte of the E1 byte, within a given outbound STS-3 frame.
A4	TxE1F1E2	I	TTL	**Transmit E1-F1-E2 Byte Input Port - Input Pin:** This input pin, along with the TxE1F1E2Enable and the TxTOHClk output pins are used to insert their value for the E1, F1 and E2 bytes, into the Transmit STS-3 TOH Processor Block. The Transmit STS-3 TOH Processor block will accept this data and insert it into the E1, F1 and E2 byte fields, within the outbound STS-3 data-stream. Whatever external circuitry that is interfaced to this input pin, the TxE1F1E2Enable and the TxTOHClk pins is suppose to do the following. It should continuously monitor the state of the TxE1F1E2Enable input pin. Whenever the TxE1F1E2Enable input pin pulses "High", then the external circuitry should place the next orderwire bit (to be inserted into the Transmit STS-3 TOH Processor block) onto this input pin upon the rising edge of TxTOHClk. Any data that is placed on the TxE1F1E2 input pin, will be sampled upon the falling edge of TxTOHClk.Note: ***NOTE:*** *This pin should be connected to GND if it is not used.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C7	TXPOH	I	TTL	**Transmit Path Overhead Input Port - Input pin.** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used.This input pin is used to insert the POH data into the Transmit AU-4/VC-4 Mapper POH Processor blocks for insertion and transmission via the outbound STS-3 signal.In this mode, the external circuitry (which is being interfaced to the Transmit Path Overhead Input Port is suppose to monitor the following output pins; • TxPOHFrame_n • TxPOHEnable_n • TxPOHClk_n The TxPOHFrame_n output pin will toggle "High" upon the rising edge of TxPOHClk_n approximately one TxPOHClk_n period prior to the TxPOH port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The TxPOHFrame_n output pin will remain "High" for eight consecutive TxPOHClk_n periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The TxPOHEnable_n output pin will toggle "High" upon the rising edge of TxPOHClk_n approximately one TxPOHClk_n period prior to the TxPOH port being ready to accept and process the first bit within a given POH byte. To externally insert a given POH byte: a. assert the TxPOHIns_n input pin by toggling it "High", and b. place the value of the first bit (within this particular POH byte) on this input pin upon the very next rising edge of TxPOHClk_n. This data bit will be sampled upon the very next falling edge of TxPOHClk_n. The external circuitry should continue to keep the TxPOHIns_n input pin "High" and advancing the next bits (within the POH bytes) upon each rising edge of TxPOHClk_n.
D9	TXPOHCLK	O	TTL	**Transmit Path Overhead Input Port - Clock Output pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This output pin, along with TxPOH, TxPOHEnable, TxPOHIns and TxPOHFrame function as the Transmit Path Overhead (TxPOH) Input Port. The TxPOHFrame and TxPOHEnable output pins are updated upon the falling edge this clock output signal. The TxPOHIns input pins and the data residing on the TxPOH input pins are sampled upon the next falling edge of this clock signal.
B5	TXPOHFRAME	O	TTL	Transmit Path Overhead Input Port - Frame Output pin: This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. This output pin, along with the TxPOH, TxPOHEnable, TxPOHIns and TxPOHClk function as the Transmit Path Overhead Input Port.If the user is only inserting POH data via these input pins: ***NOTE:*** *In this mode, the TxPOH port will pulse these output pins "High" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C8	TXPOHINS	I	TTL	**Transmit Path Overhead Input Port - Insert Enable Input pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. These input pins, along with TxPOH, TxPOHEnable, TxPOHFrame and TxPOHClk function as the Transmit Path Overhead (TxPOH) Input Port.These input pins are used to enable or disable the TxPOH input port. If these input pins are pulled "High", then the TxPOH port will sample and latch data via the corresponding TxPOH input pins, upon the falling edge of TxPOHClk. ***NOTE:*** *Conversely, if these input pins are pulled "Low", then the TxPOH port will NOT sample and latch data via the corresponding TxPOH input pins.*
B6	TXPOHENABLE	O	TTL	**Transmit Path Overhead Input Port - POH Indicator Output pin:** This pin is used for the Transmit AU-4/VC-4 Mapper POH Processor Block when TUG-3 mapping is used. Th[s output pins, along with TxPOH, TxPOHIns, TxPOHFrame and TxPOHClk function as the Transmit Path Overhead (TxPOH) Input Port. These output pins will pulse "High" anytime the TxPOH port is ready to accept and process POH bytes. These output pins will be "Low" at all other times.
E10 B8 D11	TxPOH_0 TxPOH_1 TxPOH_2	I	TTL	**Transmit Path Overhead Input Port - Input pin.** These input pins are used to insert the POH data into each of the 3 Transmit SONET POH Processor blocks (for insertion and transmission via the outbound STS-3 signal.If the user is only inserting POH data via these input pins: In this mode, the external circuitry (which is being interfaced to the Transmit Path Overhead Input Port is suppose to monitor the following output pins; TxPOHFrame_n TxPOHEnable_n TxPOHClk_n The TxPOHFrame_n output pin will toggle "High" upon the rising edge of TxPOHClk_n approximately one TxPOHClk_n period prior to the TxPOH port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The TxPOHFrame_n output pin will remain "High" for eight consecutive TxPOHClk_n periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The TxPOHEnable_n output pin will toggle "High" upon the rising edge of TxPOHClk_n approximately one TxPOHClk_n period prior to the TxPOH port being ready to accept and process the first bit within a given POH byte. To externally insert a given POH byte: a. assert the TxPOHIns_n input pin by toggling it "High", and b. place the value of the first bit (within this particular POH byte) on this input pin upon the very next rising edge of TxPOHClk_n. This data bit will be sampled upon the very next falling edge of TxPOHClk_n. The external circuitry should continue to keep the TxPOHIns_n input pin "High" and advancing the next bits (within the POH bytes) upon each rising edge of TxPOHClk_n.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A5 A6 A7	TxPOHClk_0 TxPOHClk_1 TxPOHClk_2	O	CMOS	**Transmit Path Overhead Input Port - Clock Output pin:** These output pins, along with TxPOH_n, TxPOHEnable_n, TxPOHIns_n and TxPOHFrame function as the Transmit Path Overhead (TxPOH) Input Port. The TxPOHFrame and TxPOHEnable output pins are updated upon the falling edge this clock output signal. The TxPOHIns_n input pins and the data residing on the TxPOH_n input pins are sampled upon the next falling edge of this clock signal.
C9 C10 A8	TxPOHFrame_0 TxPOHFrame_1 TxPOHFrame_2	O	CMOS	**Transmit Path Overhead Input Port - Frame Output pin:** These output pins, along with the TxPOH_n, TxPOHEnable_n, TxPOHIns_n and TxPOHClk_n function as the Transmit Path Overhead Input Port.The function of these output pins depends upon whether or not the user inserting POH or TOH data via the TxPOH_n input pins.If the user is only inserting POH data via these input pins:The TxPOH port will pulse these output pins "High" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port. ***NOTES:*** *1. The externally circuitry can determine whether or not the TxPOH port is expecting the A1 byte or the J1 byte, by checking the state of the corresponding TxPOHEnable output pin. If the TxPOHEnable_n output pin is "Low" while the TxPOHFrame_n output pin is "High", then the TxPOH port is ready to process the A1 (TOH) bytes.* *2. If the TxPOHEnable_n output pin is "High" while the TxPOHFrame_n output pin is "High", then the TxPOH port is ready to process the J1 (POH) bytes.*
D10 E11 C11	TxPOHIns_0 TxPOHIns_1 TxPOHIns_2	I	TTL	**Transmit Path Overhead Input Port - Insert Enable Input pin:** These input pins, along with TxPOH_n, TxPOHEnable_n, TxPOHFrame_n and TxPOHClk_n function as the Transmit Path Overhead (TxPOH) Input Port. These input pins are used to enable or disable the TxPOH input port. If these input pins are pulled "High", then the TxPOH port will sample and latch data via the corresponding TxPOH input pins, upon the falling edge of TxPOHClk_n. Conversely, if these input pins are pulled "Low", then the TxPOH port will NOT sample and latch data via the corresponding TxPOH input pins.Note: ***NOTE:*** *If the TxPOHIns_n input pin is pulled "Low", this setting will be overridden if the user has configured the Transmit SONET/STS-1 POH Processor or Transmit STS-1 TOH Processor blocks to accept certain POH or TOH overhead bytes via the external port.*
B7 B9 B10	TxPOHEnable_0 TxPOHEnable_1 TxPOHEnable_2	O	CMOS	**Transmit Path Overhead Input Port - POH Indicator Output pin:** These output pins, along with TxPOH_n, TxPOHIns_n, TxPOHFrame_n and TxPOHClk_n function as the Transmit Path Overhead (TxPOH) Input Port. These output pins will pulse "High" anytime the TxPOH port is ready to accept and process POH bytes. These output pins will be "Low" at all other times.
TRANSMIT LINE/ SYSTEM SIDE INTERFACE PINS				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C12 B20 AF17	TXDS3CLK_0 TXE3CLK_0 TXDS3CLK_1 TXE3CLK_1 TXDS3CLK_2 TXE3CLK_2	I	TTL	**Transmit DS3/E3 Reference Clock Input - Channel_n (Not used for Mapper Applications):n=[0:2]** The manner in which the user should handle this input pin depends upon whether Channe_n has been configured to operate in the Mapper Mode or in the ATM UNI/PPP Mode. **If Channel_n is configured to operate in the Mapper Mode:** If Channel_n has been configured to operate in the Mapper Mode, then this input pin supports no function, and should, therefore, be connected to GND. **If Channel_n is configured to operate in the ATM UNI/PPP/Clear Channel Mode:** If Channel_n (within the XRT94L31) has been configured to operate in the ATM UNI/PPP Mode, then this input pin will function as the timing reference clock signal for the Transmit STS-1/DS3/E3 Framer block circuitry, provided that Channel_n has been configured to operate in the Local Timing Mode. If Channel_h has been configured to operate in the DS3 Mode, then the user is expected to apply a 44.736MHz clock signal to this input pin. Likewise, if Channel_n has been configured to operate in the E3 Mode, then the user is expected to apply a 34.368MHz clock signal to this input pin. ***NOTE:*** *For more information on using the XRT94L31 for ATM UNI/PPP applications, the user should consult the XRT94L31 1-Channel STS-3c/3-Channel DS3/E3/STS-1 ATM UNI/PPP Data Sheet.*
B11 A22 AD16	TxOHClk_0 TxOHClk_1 TxOHClk_2	O	CMOS	**Transmit Overhead Clock Output:** This output pin functions as the Transmit Overhead Clock output for the transmit system side interface when the XRT94L31 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the Transmit STS-1 Overhead clock output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This output pin functions as the Transmit Overhead Data Input Interface clock signal. If the user enables the Transmit Overhead Data Input Interface block by asserting the TxOHIns input pin, then the Transmit Overhead Data Input Interface block will sample and latch the data (residing on the TxOH_n input pin) upon the falling edge of this signal. **When configured to operate in STS-1 mode:** These output pins, along with TxOH_n, TxOHEnable_n, TxOHIns_n and TxOHFrame function as the Transmit Path Overhead (TxOH) Input Port. The TxOHFrame and TxOHEnable output pins are updated upon the falling edge this clock output signal. The TxOHIns_n input pins and the data residing on the TxOH_n input pins are sampled upon the falling edge of this clock signal.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D12 C18 AC16	TxOHENABLE_0 TxOHENABLE_1 TxOHENABLE_2	O	CMOS	**Transmit Overhead Enable Output indicator** This output pin functions as the Transmit Overhead Enable output indicator for the transmit system side interface when the XRT94L31 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the Transmit STS-1 Overhead Enable output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The Channel will assert this output pin, for one TxInClk period, just prior to the instant that the Transmit Overhead Data Input Interface will be sampling and processing an overhead bit. If the local terminal equipment intends to insert its own value for an overhead bit, into the outbound DS3 or E3 data stream, then it is expected to sample the state of this signal, upon the falling edge of TxInClk. Upon sampling the TxOHEnable_n signal "High", the local terminal equipment should (1) place the desired value of the overhead bit, onto the TxOH_n input pin and (2) assert the TxOHIns_n input pin. The Transmit Overhead Data Input Interface block will sample and latch the data on the TxOH_n signal, upon the rising edge of the very next TxInClk_n input signal. **When configured to operate in STS-1 mode:** These output pins, along with TxOH_n, TxOHIns_n, TxOHFrame_n and TxOHClk_n function as the Transmit Path Overhead (TxOH) Input Port. These output pins will pulse "High" anytime the TxOH port is ready to accept and process POH bytes. These output pins will be "Low" at all other times.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E12 E17 AB16	TxOH_0 TxOH_1 TxOH_2	I	TTL	**Transmit Overhead Data Input:** This input pin functions as the Transmit Overhead Data output indicator for the transmit system side interface when the XRT94L31 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the Transmit STS-1 Overhead Enable output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The Transmit Overhead Data Input Interface accepts overhead via these input pins, and insert this data into the overhead bit positions within the outbound DS3 or E3 frames. If the TxOHIns_n input pin is pulled "High", then the Transmit Overhead Data Input Interface will sample the overhead data, via this input pin, upon the falling edge of the TxOHClk_n output signal. Conversely, if the TxOHIns_n input pin is NOT pulled "High", then the Transmit Overhead Data Input Interface block will be inactive and will not accept any overhead data via the TxOH_n input pin. **When configured to operate in STS-1 mode:** These input pins are used to do the following. a. To insert the POH data into each of the 3 Transmit STS-1 POH Processor blocks (for insertion and transmission via each of the outbound STS-1 signals).2. b. To insert the TOH data into each of the 3 Transmit STS-1 TOH Processor blocks (for insertion and transmission via each of the outbound STS-1 signals). The function of these input pins, depend upon whether or not the user has opted to insert the TOH data into the 3 Transmit STS-1 TOH Processor blocks. **If the user is only inserting POH data via these input pins:** In this mode, the external circuitry (which is being interfaced to the Transmit Path Overhead Input Port is suppose to monitor the following output pins. • TxOHFrame_n • TxOHEnable_n • TxOHClk_n The TxOHFrame_n output pin will toggle "High" upon the falling edge of TxOHClk_n approximately one TxOHClk_n period prior to the TxOH port being ready to accept and process the first bit within J1 byte (e.g., the first POH byte). The TxOHFrame_n output pin will remain "High" for eight consecutive TxOHClk_n periods. The external circuitry should use this pin to note STS-1 SPE frame boundaries. The TxOHEnable_n output pin will toggle "High" upon the falling edge of TxOHClk_n approximately one TxOHClk_n period prior to the TxOH port being ready to accept and process the first bit within a given POH byte. If the user wishes to externally insert a given POH byte; a. assert the TxOHIns_n input pin by toggling it "High", and b. place the value of the first bit (within this particular POH byte) on this input pin upon the very next falling edge of TxOHClk_n. This data bit will be sampled upon the very next falling edge of TxOHClk_n. The external circuitry should continue to keep the TxOHIns_n input pin "High" and advancing the next bits (within the POH bytes) upon each rising edge of TxOHClk_n.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E12 E17 AB16	TxOH_0 TxOH_1 TxOH_2	I	TTL	**Continued** **If the user is inserting both POH and TOH data via these input pins:** In this mode, the external circuitry (which is being interfaced to the Transmit Path Overhead Input Port is suppose to monitor the following output pins. • TxOHFrame_n • TxOHEnable_n • TxOHClk_n The TxOHFrame_n output pin will toggle "High" twice during a given STS-1 frame period. First, this output pin will toggle "High" coincident with the TxOH port being ready to accept and process the A1 byte (e.g., the very first TOH byte). Second, this output pin will toggle "High" coincident with the TxOH port being ready to accept and process the J1 byte (e.g., the very first POH byte). If the externally circuitry samples the TxOHFrame_n output pin "High", and the TxOHEnable_n output pin "Low", then the TxOH port is now ready to accept and process the very first TOH byte. If the externally circuitry samples the TxOHFrame_n output pin "High" and the TxOHEnable_n output pin "High", then the TxOH port is now ready to accept and process the very first POH byte. To externally insert a given POH or TOH byte; a. assert the TxOHIns_n input pin by toggling it "High", and b. place the value of the first bit (within this particular POH or TOH byte) on this input upon the very next falling edge of TxOHClk_n This data bit will be sampled upon the very next falling edge of TxOHClk_n. The external circuitry should continue to keep the TxOHIns_n input pin "High" and advancing the next bits (within the POH bytes) upon each rising edge of TxOHClk_n.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
F12 B19 AG19	TxOHINS_0 TxOHINS_1 TxOHINS_2	I	TTL	**Transmit Overhead Data Insert Input:** This input pin functions as the Transmit Overhead Data Insert input indicator for the transmit system side interface when the XRT94L31 is configured to operate in STS-1/DS3/E3 mode, however, it functions as the Transmit STS-1 Overhead Enable output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This input pin is used to either enable or disable the Transmit Overhead Data Input Interface block within the DS3/E3 Frame Generator block. If the Transmit Overhead Data Input Interface block is enabled, then the DS3/E3 Frame Generator block will accept overhead data (from the local terminal equipment) via the TxOH_n input pin; and insert this data into the overhead bit positions within the outbound DS3 or E3 data stream. Conversely, if the Transmit Overhead Data Input Interface block is disabled, then the DS3/E3 Frame Generator block it will NOT accept overhead data from the local terminal equipment.Pulling this input pin "High" enables the Transmit Overhead Data Input Interface block. Pulling this input pin "Low" disables the Transmit Overhead Data Input Interface block. **When configured to operate in STS-1 mode:** These input pins, along with TxOH_n, TxOHEnable_n, TxOHFrame_n and TxOHClk_n function as the Transmit Overhead (TxOH) Input Port. These input pins are used to enable or disable the TxOH input port. If these input pins are pulled "High", then the TxOH port will sample and latch data via the corresponding TxOH input pins, upon the falling edge of TxOHClk_n. Conversely, if these input pins are pulled "Low", then the TxOH port will NOT sample and latch data via the corresponding TxOH input pins ***NOTE:*** *If the TxOHIns_n input pin is pulled "Low", this setting will be overridden if the user has configured the Transmit SONET/STS-1 POH Processor or Transmit STS-1 TOH Processor blocks to accept certain POH or TOH overhead bytes via the external port.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A9 D17 AF18	TxOHFRAME_0 TxOHFRAME_1 TxOHFRAME_2	O	CMOS	**Transmit Overhead Framing Pulse:** This input pin functions as the Transmit Overhead Framing Pulse for the transmit system side interface when the XRT94L31 is configured to operate in DS3/E3 mode, however, it functions as the Transmit STS-1 Overhead Enable output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This output pin pulses "High" (for one TxOHClk_n period) coincident with the instant that the DS3/E3 Frame Generator block will be accepting the very first overhead bit within an outbound DS3 or E3 frame (via Transmit Overhead Data Input Interface). **When configured to operate in STS-1 mode:** These output pins, along with the TxOH_n, TxOHEnable_n, TxOHIns_n and TxOHClk_n function as the Transmit Overhead Input Port.The function of these output pins depends upon whether or not the user inserting POH or TOH data via the TxOH_n input pins. **If the user is only inserting POH data via these input pins:** In this mode, the TxOH port will pulse these output pins "High" whenever it is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port. **If the user is inserting both POH and TOH data via these input pins:** In this mode, the TxOH port will pulse these output pins "High" coincident with the following. Whenever the TxOH port is ready to accept and process the A1 byte (e.g., the very first TOH byte) via this port. Whenever the TxOH port is ready to accept and process the J1 byte (e.g., the very first POH byte) via this port. ***NOTES:*** *1. The externally circuitry can determine whether or not the TxOH port is expecting the A1 byte or the J1 byte, by checking the state of the corresponding TxOHEnable output pin. If the TxOHEnable_n output pin is "Low" while the TxOHFrame_n output pin is "High", then the TxOH port is ready to process the A1 (TOH) bytes.* *2. If the TxOHEnable_n output pin is "High" while the TxOHFrame_n output pin is "High", then the TxOH port is ready to process the J1 (POH) bytes.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AF19 AG21 AE17	STUFFCNTL_0/ TXHDLC_CLK_0 STUFFCNTL_1/ TXHDLC_CLK_1 STUFFCNTL_2/ TXHDLC_CLK_2	I/O	TTL/ CMOS	**STUFFCNTL_n/TxHDLC_CLK_n:** The function of this input pin depends upon (1) whether or not the XRT94L31 has been configured to operate in the ATM UNI/PLCP Mode and (2) whether a given DS3/E3 Framer block/Channel has been configured to operate in the High-Speed HDLC Controller Mode, as described below. **STUFFCNT_n:Transmit PLCP Processor block Nibble-Stuff Control Input pin - ATM UNI Mode Only:** This pin only functions in this particular role if the XRT94L31 has been configured to operate in the ATM UNI Mode. **TxHDLC_CLK[2:0]:Transmit HDLC Controller block Clock output signal - High-Speed HDLC Controller Mode Only:** This output signal functions as the demand clock for the Transmit HDLC Controller, associated with the DS3/E3 Framer blocks. Whenever the user pulls the Snd_Msg input pin "High" then the Transmit HDLC Controller block begins to sample and latch the contents of the TxHDLCDat[7:0] input pins upon the falling edge of this clock signal. The user is advised to configure their terminal equipment circuitry to output (or place) data onto the TxHDLCDat[7:0] bus upon the rising edge of this clock signal. Since the Transmit HDLC Controller block is sampling and latching 8-bits of data at a given time, it may be assumed that the frequency of the TxHDLC_CLK_n output signal is either 34.368MHz/8 or 44.736MHz/8. In general, this presumption is true. However, because the Transmit HDLC Controller block is also performing Zero-Stuffing of the user data that it accepts from the Terminal Equipment, the frequency of this signal may be slower. ***NOTE:*** *If the DS3/E3 Framer block has NOT been configured to operate in the High-Speed HDLC Controller Mode, tie this pin to GND.*
AC17 AD17 AG20	EIGHTKHZSYNC_0/ RXHDLC_CLK_0 EIGHTKHZSYNC_1/ RXHDLC_CLK_1 EIGHTKHZSYNC_2/ RXHDLC_CLK_2	I/O	TTL/ CMOS	EIGHTKHZSYNC_n/RXHDLC_CLK_n: The function of this input pin depends upon (1) whether or not the XRT94L31 has been configured to operate in the ATM UNI/PLCP Mode and (2) whether a given DS3/E3 Framer Block/Channel has been configured to operate in the High-Speed HDLC Controller Mode, as described below. **EIGHTKHZSYNC_n: Transmit PLCP Processor Block 8kHz Framing Alignment Input - ATM UNI Mode Only:** This pin only functions in this particular role if the XRT94L31 has been configured to operate in the ATM UNI Mode. **RxHDLC_CLK_n: Receive High-Speed HDLC Controller Output Interface block - Clock output signal - High-Speed HDLC Controller over DS3/STS-3 Mode Only:** The Receive High-Speed HDLC Controller Output Interface block outputs data via the RxHDLCDat_n[7:0] output pins upon the rising edge of this clock signal. The user is advised to configure the terminal equipment to sample the contents of the RxHDLCDat_n[7:0] output pins upon the falling edge of this clock signal. ***NOTE:*** *If the DS3/E3 Framer block has NOT been configured to operate in the High-Speed HDLC Controller Mode, tie this pin to GND.*
D27	TXPERR	I	TTL	**For Mapper applications, please connect this pin to GND.**
G25	TxPEOP	I	TTL	**For Mapper applications, please connect this pin to GND.**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
F25	TxMOD_0	I	TTL	**For Mapper applications, please connect this pin to GND.**
J24	TxUPRTY/TxPPRTY	I	TTL	**For Mapper applications, please connect this pin to GND.**
H27 G27 L24 J26 L23 K25 F27 H26 G26 K24 J25 E27 K23 F26 H25 E26	TxUDATA_0/ TxPDATA_0 TxUDATA_1/ TxPDATA_1 TxUDATA_2/ TxPDATA_2 TxUDATA_3/ TxPDATA_3 TxUDATA_4/ TxPDATA_4 TxUDATA_5/ TxPDATA_5 TxUDATA_6/ TxPDATA_6 TxUDATA_7/ TxPDATA_7 TxUDATA_8/ TxPDATA_8 TxUDATA_9/ TxPDATA_9 TxUDATA_10/ TxPDATA_10 TxUDATA_11/ TxPDATA_11 TxUDATA_12/ TxPDATA_12 TxUDATA_13/ TxPDATA_13 TxUDATA_14/ TxPDATA_14 TxUDATA_15/ TxPDATA_15	I	TTL	**For Mapper applications, please connect this pin to GND.**
M24 M23J 27K2 6L25	TxUADDR_0TxUADDR_1TxUADDR_2TxUADDR_3TxUADDR_4	I	TTL	**For Mapper applications, please connect this pin to GND.**
L26	TxUClav/TxPPA	O	CMOS	**For Mapper applications, please leave this pin open.**
M25	TxUSOC/TXPSOP/ TXPSOC	I	TTL	**For Mapper applications, please connect this pin to GND.**
K27	TxTSX /TXPSOF	I	TTL	**For Mapper applications, please connect this pin to GND.**
M26	TXUENB_L/ TXPENB_L	I	TTL	**For Mapper applications, please connect this pin to VDD.**
L27	TXUCLKO/TXPCLKO	O	CMOS	**For Mapper applications, please leave this pin open.**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
M27	TXUCLK/TXPCLK	I	TTL	**For Mapper applications, please connect this pin to GND.**
STS-1 TELECOM BUS INTERFACE - TRANSMIT DIRECTION				
C14 E19 AC14	STS1TXA_CK_0 TXSENDFCS_0 TXGFCCLK_0 STS1TXA_CK_1 TXSENDFCS_1 TXGFCCLK_1 STS1TXA_CK_2 TXSENDFCS_2 TXGFCCLK_2	I I O	TTL TTL CMOS	**STS-1 Transmit Telecom Bus Clock Input pin/Transmit High-Speed HDLC Controller Input Interface Block - Send FCS Command Input pin - Channel n (n=0,1,2):** The function of this input pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled - STS1TXA_CLK_[0:3] - Transmit STS-1 Telecom Bus Interface Block Transmit Clock Input - Channel n:** This input clock signal functions as the clock source for the Transmit STS-1 Telecom Bus, associated with Channel n. All input signals (e.g., STS1TXA_ALARM_n, STS1TXA_D_n[7:0], STS1TXA_DP_n, STS1TXA_PL_n, STS1TXA_C1J1_n) are sampled upon the falling edge of this input clock signal.This clock signal should operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (for STS-1 mode). If STS-1 Telecom Bus (Channel n) has NOT been enabled: If STS-1 Telecom Bus (Channel n) has not been enabled, then this particular pin can be configured to function in either of the following roles. **TXSENDFCS_n (Transmit High-Speed HDLC Controller Input Interface block Send FCS Command Input - Channel n - High-Speed HDLC Controller Mode Only)** The user's terminal equipment is expected to control both this input pin and the TXSENDMSG_0 input pin during the construction and transmission of each outbound HDLC frame. This input pin is used to command the Transmit HDLC Controller block to compute and insert the computed FCS value into the back-end of the outbound HDLC frame as a trailer. If the user has configured the Transmit HDLC Controller to compute and insert a CRC-16 value into the outbound HDLC frame, then the terminal equipment is expected to pull this input pin "High" for two periods of TxHDLCClk_n. Likewise, if the user has configured the Transmit HDLC Controller to compute and insert a CRC-32 value into the outbound HDLC frame, then the terminal equipment is expected to pull this input pin "High" for four periods of TxHDLCClk_n. **TXGFCCLK_n (Transmit GFC Nibble-Field Input Port clock signal Input) - ATM Applications ONLY.** This pin only functions in this particular role if the XRT94L31 has been configured to operate in the ATM UNI Mode. ***NOTE:*** *The user should tie this pin to GND if the DS3/E3 Framer block has NOT been configured to operate in the High-Speed HDLC Controller Mode.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E14 c22 AD14	STS1TXA_PL_0 TXSENDMSG_0 STS1TXA_PL_n TXSENDMSG_n STS1TXA_PL_n TXSENDMSG_n	I	TTL	**STS-1 Transmit Telecom Bus - Payload Indicator Signal input/ Transmit High-Speed HDLC Controller Input Interface block - Send Message Command Input pin - Channel n (n=0, 1, 2):** The function of this input depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled - STS1TXA_PL_n - Transmit STS-1 Telecom Bus Interface - Payload Indicator Input Signal - Channel n:** This input pin indicates whether or not Transport Overhead (TOH) bytes are being input via the TXA_D_n[7:0] input pins. This input pin should be pulled "Low" for the duration that the Transmit STS-1 Telecom Bus Interface is accepting a TOH byte, via the TXA_D_n[7:0] input pins. Conversely, this input pin should be pulled "High" at all other times. ***NOTE:*** *This input signal is sampled upon the falling edge of STS1TXA_CK_n.* **If STS-1 Telecom Bus (Channel n) has NOT been enabled:** If STS-1 Telecom Bus (Channel n) has not been enabled, then this particular pin can either be configured to function as the TxSENDMSG_n input pin (if the DS3/E3 Framer block within Channel n has been configured to operate in the High-Speed HDLC Controller Mode), or the user should simply tie this input pin to GND. The details of this pin's role as the TxSENDMSG_n input pin is described below. **If STS-1 Telecom Bus (Channel n) is disabled: TXSENDMSG_n (:Transmit High-Speed HDLC Controller Input Interface block - Send Message Command Input - Channel n - High-Speed HDLC Controller Mode Only)** This input pin is used to command the Transmit High-Speed HDLC Controller Input Interface block (associated with Channel n) to begin sampling and latching the data which is being applied to the TxHDLCDat_n[7:0] input pins. If the user pulls this input pin "High", then the Transmit High-Speed HDLC Controller block samples and latches the data which is applied to the TxHDLCDat_n[7:0] input pins upon the rising edge of TxHDLCClk_n. Each byte of this sampled data will ultimately be encapsulated into an outbound HDLC frame and will be mapped into the payload bits within the outbound DS3/E3 frames via the DS3/E3 Framer block. If the user pulls this input pin "Low" then the Transmit High-Speed HDLC Controller block will NOT sample and latch the contents on the TxHDLCDat_n[7:0] input pins, and the Transmit High-Speed HDLC Controller block will simply generate a continuous stream of flag sequence octets (0x7E). ***NOTE:*** *If the DS3/E3 Framer block has NOT been configured to operate in the High-Speed HDLC Controller Mode, tie this pin to GND.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D14 A24 AF14	STS1TXA_C1J1_0RXDS3LINECLK_0 STS1TXA_C1J1_nRXDS3LINECLK_n STS1TXA_C1J1_nRXDS3LINECLK_n	I	TTL	**STS-1 Transmit Telecom Bus C1/J1 Byte Phase Indicator Input Signal/Receive DS3/E3/STS-1 Clock Input from LIU (Channel n) (n=0, 1, 2):** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled - Transmit STS-1 Telecom Bus Interface - C1/J1 Byte Phase Indicator Input Signal (Channel n):** This input pin should be pulsed "High" during both of the following conditions. Coincident to whenever the C1/J0 byte (within the incoming STS-1/STS-3/STM-1 signal) is being input to the Transmit STS-1 Telecom Bus Interface - Data Bus Input pins (TXA_D_n[7:0]). Coincident to whenever the J1 byte(s) (within the incoming STS-1/STS-3/STM-1 signal) is being input to the Transmit STS-1 Telecom Bus Interface - Data Bus Input pins (TXA_D_n[7:0]). This input pin should be held "Low" at all other times. **If STS-1 Telecom Bus (Channel n) has NOT been enabled - RXDS3LINECLK_n (Receive DS3/E3/STS-1 clock input from LIU)** The DS3/E3 Framer block and/or the Receive STS-1 TOH Processor block (associated with Channel n) use this input pin to sample and latch the data that is present on the RxDS3POS_n and RxDS3NEG_n (for Dual-Rail Operation only) inputs. This input clock signal also functions as the timing source for the Ingress Direction signal and circuitry within the DS3/E3 Framer block of Channel n. The user is expected to connect this input to the Recovered Clock Output of an off-chip DS3/E3/STS-1 LIU IC.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B14 C21 AG15	STS1TXA_DP_n RXDS3POS_n STS1TXA_DP_n RXDS3POS_n STS1TXA_DP_n RXDS3POS_n	I	TTL	**STS-1 Transmit Telecom Bus - Parity Input pin/Receive DS3/E3/ STS-1 Positive-Polarity Data Input from LIU - Channel n:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled - STS1TXA_DP_n - Transmit STS-1 Telecom Bus Interface # n - Parity Input Pin:** This input pin can be configured to function as one of the following. To refect either the EVEN or ODD parity value of the bits (within the incoming STS-1/STS-3/STM-1 data-stream) which are currently being input via the STS1TXA_D_n[7:0] input pins. To reflect either the EVEN or ODD parity value of the bits (within the incoming STS-1/STS-3/STM-1 data-stream) which are being input via the STS1TXA_D_n[7:0] input, and the states of the STS1TXA_PL_n and STS1TXA_C1J1_n input pins. ***NOTE:*** *The user can make any one of these configuration selections by writing the appropriate value into the Interface Control Register - Byte 0 register (Address Location = 0x013B).* **If STS-1 Telecom Bus (Channel n) has NOT been enabled - RXDS3POS_n (Receive DS3/E3/STS-1 Positive-Polarity data input from LIU)** The DS3/E3 Framer block and the Receive STS-1 TOH Processor block (associated with Channel n) will sample the data being applied to this input pin upon the user-selected edge of the RXDS3LINECLK_n input signal. If the user has configured Channel n to operate in the STS-1 Mode, or in the Single-Rail Mode (if also configured to operate in the DS3/E3 Mode), then all Recovered DS3, E3 or STS-1 data (from the DS3/E3/STS-1 LIU IC) should be applied to this input pin. If the user has configured Channel n to operate in both the DS3/E3 and the Dual-Rail Mode, then only the positive-polarity portion of the Recovered DS3/E3 data output (from the DS3/E3 LIU IC) should be applied to this input pin.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A13 D19 AF15	STS1TXA_ALARM_n RXDS3NEG_n RxLCV_n STS1TXA_ALARM_n RXDS3NEG_n RxLCV_n STS1TXA_ALARM_n RXDS3NEG_n RxLCV_n	I	TTL	**Transmit STS-1 Telecom Bus - Alarm Indicator Input - Channel n/ Receive DS3/E3 Negative-Polarity Data Input from LIU - Channel n/ Receive DS3/E3 Line Code Violation Input from LIU - Channel n:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus Interface (associated with Channel n) has been enabled - Transmit STS-1 Telecom Bus Interface - Alarm Indicator Input - STS1TxA_ALARM_n:** This input pin should be pulsed "High" for one STS1TxA_CLK_n period coincident to whenever the Transmit STS-1 Telecom Bus Interface (associated with Channel n) is accepting a byte from an incoming STS-1/ STS-3/STM-1 signal (via the STS1TxA_D_n[7:0] input pins) that is carrying the AIS-P indicator.This input pin should be held at a logic "Low" at all other times. ***NOTE:*** *If the STS1TXA_ALARM_n input signal pulses "High" for any given STS-1 signal (within the incoming STS-1), then the XRT94L31 will automatically declare the AIS-P defect condition for that particular STS-1 channel.* **If STS-1 Telecom Bus (Channel n) has NOT been enabled:** If the STS-1 Telecom Bus (Channel n) has NOT been enabled, then the role that this particular input pin plays depends upon whether Channel n is operating in the STS-1 Mode, the DS3/E3 Single-Rail Mode or in the DS3/E3 Dual-Rail Mode, as described below. **If Channel n is operating in the STS-1 Mode - NO FUNCTION:** If Channel n is operating in the STS-1 Mode, then the user should tie this pin to GND. **If Channel n is operating in the DS3/E3 Single-Rail Mode - Receive LCV Input from LIU** If Channel n is operating in both the DS3/E3 and Single-Rail Modes, then this input pin will function as the LCV (Line Code Violation) input signal. In this mode, the user is expected to connect the LCV output pin from the LIU IC to this input pin. The DS3/E3 Framer block will sample this input pin upon the user-configured edge of the RXDS3LINECLK_n clock signal, and the Primary Frame Synchronizer block (corresponding with Channel n) will increment the PMON LCV or EXZ Event Count registers based upon the data sampled at this input pin. **If Channel n is operating in the DS3/E3 Dual-Rail Mode - Receive DS3/E3 Negative-Polarity Data Input from LIU** If the user has configured Channel n to operate in both the DS3/E3 and the Dual-Rail Mode, then only the negative-polarity portion of the Receive DS3/E3 data output (from the DS3/E3 LIU IC) should be applied to this input pin.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B13	STS1TXA_0_D0 TXHDLCDAT_0_0 TXGFCMSB_0	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 0/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 0:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel n is enabled. **If STS-1 Telecom Bus (Channel n) has been enabled -Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 0 - STS1TxA_0_D0:** This input pin along with STS1TXA_D_0[7:1] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. This particular input pin functions as the LSB (Least Significant Bit) input pin on the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. The LSB of any byte (within the incoming STS-1/STS-3 or STM-1 signal), which is being input into the Transmit STS-1 Telecom Bus - Input Data Bus (for Channel 0) should be input via this pin. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled:** This input pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Data Bus Input pin # 0 - TxHDLCDAT_0_0: **If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 0 (the LSB) within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCData_0[7:0] input pins).** The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCData_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode** **- TXGFCMSB_0 (Transmit GFC MSB Indicator - Channel 0)** **- TXGFC_0 (Transmit GFC data - Channel 0)** **- TXCELLTXED_0 (Cell Transmitted - Channel 0)** This input pin will only function in this role if the XRT94L31 has been configured to operate in the ATM UNI Mode.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C13	STS1TXA_0_D1 TXHDLCDAT_0_1 TXGFC_0	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 1/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 1:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 1 - STS1TxA_0_D1:** This input pin along with STS1TXA_0_D[7:2] and STS1TXA_0_D0 function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled:** This input pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Data Bus Input pin # 1 - TxHDLCDAT_0_1:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode - TXGFC_0 (Transmit GFC data - Channel 0)** This input pin will only function in this role if the XRT94L31 has been configured to operate in the ATM UNI Mode.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D13	STS1TXA_0_D2 TXHDLCDAT_0_2 TXCELLTXED_0	I	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 2/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 2:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 2 - STS1TXA_0_D2:** This input pin along with STS1TXA_0_D[7:3] and STS1TXA_0_D[1:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled.** This input pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Data Bus Input pin # 2 - TXHDLCDAT_0_2:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode - TXCELLTXED_0 (Cell Transmitted - Channel 0)** This input pin will only function in this role if the XRT94L31 has been configured to operate in the ATM UNI Mode.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E13	STS1TXA_0_D3 TXHDLCDAT_0_3 SSI_CLK	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 3/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 3/Slow-Speed Interface - Clock Input/Output signal:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. If STS-1 Telecom Bus (Channel 0) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 3 - STS1TXA_0_D3: This input pin along with STS1TXA_0_D[7:4] and STS1TXA_0_D[2:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled.** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Data Bus Input pin # 3 - TxHDLCDAT_0_3:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 3 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins).The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 is configured to operate in the DS3/E3/STS-1 to STS-3/STM-1 Mapper Mode - Slow-Speed Interface for Ingress Path - Clock Input/Output - SSI_CLK:** This pin along with the SSI_POS and SSI_NEG pins function as the Slow-Speed Interface for the Ingress Direction signal Path Input/Output Port. The Slow-Speed Interface can be configured to function as either an Input (ADD) or Output (DROP) port, as described below.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E13	STS1TXA_0_D3 TXHDLCDAT_0_3 SSI_CLK(Continued)	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 3/Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus - Channel 0 - Pin 3/Slow-Speed Interface - Clock Input/Output signal (Continued):** **If the XRT94L31 is configured to operate in the DS3/E3/STS-1 to STS-3/STM-1 Mapper Mode - Slow-Speed Interface for Ingress Path - Clock Input/Output - SSI_CLK - Continued:** ***If configured to operate as an Input Port*** If the Slow-Speed Interface is configured to operate as an Input Port, then this port can be configured to accept a DS3, E3 or STS-1 signal (from external circuitry) and it will ADD this DS3/E3/STS-1 signal into the Selected Ingress Direction Channel within the XRT94L31. In this mode, the SSI_CLK will function as a Clock Input signal that can accept either a 34.368MHz, 44.736MHz or 51.84MHz clock signal (depending upon which type of signal is being ADDed. ***If configured to operate as an Output Port:*** If the Slow-Speed Interface is configured to operate as an Output Port, then this port can be configured to output (or DROP out) the Selected Ingress Direction Channel within the XRT94L31.In this mode, the SSI_CLK will function as a Clock Output signal which will be at either the 34.368MHz, 44.736MHz or 51.84MHz clock frequency (depending upon which type of signal is being DROPed)

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A12	STS1TXA_0_D4 TXHDLCDAT_0_4 TXDS3OHIND_0	IO	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 4/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 4/Transmit DS3/E3 Overhead Indicator Output - Channel 0:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 4 - STS1TXA_0_D4:** This input pin along with STS1TXA_0_D[7:5] and STS1TXA_0_D[3:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Data Bus Input pin # 4 - TxHDLCDATA_0_4:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 4 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3/E3 Overhead Indicator Output - Channel 0 - TxDS3OHInd_0:** If the XRT94L31 has been configured to operate in the Clear-Channel Framer over STS-3/STM-1 Mapper Mode, then this output pin can be configured to functions as the transmit overhead data indicator for the System-Side terminal equipment, or as a Gapped-Clock output for the Transmit Payload Data Input Interface. This output pin is pulsed "High" for one DS3 or E3 bit period in order to indicate (to the System-Side terminal equipment) that the Transmit Section of the Framer is going to be processing an overhead bit, upon the next rising edge of TxInClk_0, and will NOT latch the data that is applied to the TxDS3DATA_0 input pin.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A12	STS1TXA_0_D4 TXHDLCDAT_0_4 TXDS3OHIND_0(Continued)	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus - Channel 0 - Input Data Bus pin number 4/Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus - Pin 4/Transmit DS3/E3 Overhead Indicator Output - Channel 0 - Continued:** **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled - Continued:If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3 Overhead Indicator - Channel 0 - TxDS3OHInd_0 - Continued:** Therefore, whenever the System-Side terminal equipment samples the TxDS3OHInd_0 output pin "High", then it must not apply the next payload bit to TxDS3DATA_0 input pin.This output pin serves as a warning that this particular payload bit is going to be ignored by the Transmit Section of the Framer, and will not be inserted into payload bits, within the outbound DS3 or E3 data stream.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A11	STS1TXA_0_D5TXHDLCDAT_0_5TXDS3FP_0	I/O	TTL/CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Input Data Bus pin number 5/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 5/Transmit DS3/E3 Frame Boundary Indicator Output - Channel 0:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 5 - STS1TXA_0_D5:** This input pin along with STS1TXA_0_D[7:6] and STS1TXA_0_D[4:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Data Bus Input pin # 5 - TxHDLCDAT_0_5: **If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins).** The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3/E3 Frame Boundary Indicator Output - Channel 0 - TxDS3FP_0: This output pin is pulse "High" for one DS3 or E3 clock period, when the Transmit Payload Data Input Interface block of Channel 0 (within the XRT94L31) is processing the last bit of a given DS3 or E3 frame.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B12	STS1TXA_0_D6 TXHDLCDAT_0_6 TXDS3DATA_0 TXSBDATA_6_0	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 0 - Data Bus Input pin number 6/Transmit High-Speed HDLC Controller Input Interface block - Channel 0 - Input Data Bus - Pin 6/Transmit DS3/E3 Serial Data Input - Channel 0:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 6: STS1TXA_0_D6:** This input pin along with STS1TXA_0_D7 and STS1TXA_0_D[5:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. **If the STS-1 Telecom Bus Interface (associated with Channel 0) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode -Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input pin # 6 - Channel 0 - TxHDLCDAT_0_6: If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 6 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit Payload Data Input Interface -Channel 0 - Transmit DS3/E3 Serial Data Input - TxDS3DATA_0:** If the XRT94L31 is configured to operate in the Clear-Channel Framer over STS-3/STM-1 Mapper mode, then this input pin functions as the Transmit Payload Data Serial Input pin for Channel 0. In this case, the System-Side terminal equipment is expected to apply all outbound data (which is intended to be carried via the DS3 or E3 payload bits) to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxDS3DATA_0 input pin, upon the rising edge of TxInClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A10	STS1TXA_D7_0 TXHDLCDAT_7_0 TXAISEN_0 TXSBDATA_7_0	I	TTL	Transmit STS-1 Telecom Bus Interface - Channel 0 - Input Data Bus pin number 7/Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus - Pin 7/Transmit DS3/E3 AIS Input Pin - Channel 0: The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled -Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 7: STS1TXA_0_D7:** This input pin along with STS1TXA_0_D[6:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 0. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_0. ***NOTE:*** *This input pin functions as the MSB (Most Significant Bit) of the Transmit (Add) Telecom Bus, for Channel 0.* **If the STS-1 Telecom Bus (associated with Channel 0) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input Pin # 7 - Channel 0 - TXHDLCDAT_0_7:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_0[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_0). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_0[7:0] input pins) upon the rising edge of the TxHDLCClk_0 clock output signal. **If the XRT94L31 is configured to operate in any other mode that involves the DS3/E3 Framer block - Transmit DS3/E3 AIS Enable Input - Channel 0 - TXAISEN_0:** This input pin is used to command the Frame Generator block (within Channel 0) to generate and transmit the DS3/E3 AIS pattern, as described below. • "Low" - Configures the Frame Generator block to NOT generate and transmit the DS3/E3 AIS Pattern • "High" - Configures the Frame Generator block to generate and transmit the DS3/E3 AIS Pattern ***NOTE:*** *If the user intends to control the transmission of DS3/E3 AIS via Software, then this input pin mudt be tied to GND.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B23	STS1TXA_1_D0 TXHDLCDAT_1_0 TXGFCMSB_1	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Input Data Bus pin number 0/Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Input Data Bus - Pin 0:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 0 - STS1TXA_1_D0:** This input pin along with STS1TXA_1_D[7:1] functions as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. This particular input pin functions as the LSB (Least Significant Bit) input pin on the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus. The Transmit STS-1 Telecom Bus Interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. The LSB of any byte, which is being input into the STS-1 Transmit Telecom Bus Interface - Data Bus (for Channel 1) should be input via this pin. **If the STS-1 Telecom Bus (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - - Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input Pin # 0 - Channel 1 - TxHDLCDAT_1_0:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 0 (the LSB) within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **TXGFCMSB_1 (Transmit GFC MSB Indicator - Channel 1)** This input pin will only function in this role if the XRT94L31 has been configured to operate in the ATM UNI Mode.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C20	STS1TXA_1_D1 TXHDLCDAT_1_1 TXGFC_1	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Data Bus Input pin number 1/Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus - Pin 1:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 1 - STS1TxA_1_D1:** This input pin along with STS1TXA_1_D[7:2] and STS1TXA_1_D0 function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Data Bus Input pin # 1 - TXHDLCDAT_1_1:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode** - TXGFC_1 (Transmit GFC data - Channel 1) **If the XRT94L31 has been configured to operate in the 3-Channel DS3/E3/STS-1 to STS-3/STM-1 Mapper Mode** - NO FUNCTION: The user should tie this input pin to GND.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B22	STS1TXA_1_D2 TXHDLCDAT_1_2 TXCELLTXED_1	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Data Bus Input pin number 2/Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Input Data Bus - Pin 2:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 2 - STS1TXA_1_D2:** This input pin along with STS1TXA_1_D[7:3] and STS1TXA_1_D[1:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled.** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Data Bus Input pin # 2 - TxHDLCDAT_1_2:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode** - TXCELLTXED_1 (Cell Transmitted - Channel 1)

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
E18	STS1TXA_1_D3 TXHDLCDAT_1_3 SSI_POS	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Data Bus Input pin number 3/Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Input Data Bus - Pin 3/Slow-Speed Interface - Positive Polarity Data Input/Output signal:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled -Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 3: STS1TXA_1_D3:** This input pin along with STS1TXA_1_D[7:4] and STS1TXA_1_D[2:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Data Bus Input pin # 3 - TXHDLCDAT_1_3:** In this mode this input pin will function as Bit 3 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 is configured to operate in the DS3/E3/STS-1 to STS-3/STM-1 Mapper Mode - Slow Speed Interface for Ingress Path - Positive-Polarity Data Input/Output - SSI_POS:** This pin along with the SSI_NEG and SSI_CLK pins function as the Slow-Speed Interface for the Ingress Direction Signal Path Input/Output Port and can be configured to function as either an Input (ADD) or Output (DROP) port. ***If the SSI Port is configured to operate as an Input (ADD) Port:*** Then this port can be configured to accept a DS3, E3 or STS-1 signal (from external circuitry) and it will ADD this DS3/E3/STS-1 signal into the Selected Ingress Direction Channel within the XRT94L31. In this mode, the SSI_POS will function as the Positive-Polarity Portion of the DS3/E3/STS-1 signal that is being ADDed. In this mode, the SSI Port will sample the data (being applied to this pin) upon the rising edge of SSI_CLK. ***If the SSI Interface is configured to operate as an Output (DROP) Port:*** Then this port can be configured to output (or DROP out) the Selected Ingress Direction Channel within the XRT94L31.In this mode the SSI_POS will output the Positive Polarity portion of this selected Ingress Direction signal. This output pin will be updated upon the falling edge of the SSI_CLK output pin.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A23	STS1TXA_1_D4 TXHDLCDAT_1_4 TXDS3OHIND_1	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Input Data Bus Input pin number 4/Transmit High-Speed HDLC Controller Input Interface block -Channel 1 - Input Data Bus - Pin 4/Transmit DS3/E3 Overhead Indicator Output - Channel 1:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 4: STS1TXA_1_D4:** This input pin along with STS1TXA_1_D[7:5] and STS1TXA_1_D[3:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Data Bus Input pin # 4 - TxHDLCDAT_1_4:** Then this input pin will function as Bit 4 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3/E3 Overhead Indicator Output - Channel 1 - TXDS3OHIND_1:** This output pin will pulse "High" one bit-period prior to the time that the DS3/E3 Frame Generator block (within Channel 1) will be processing an Overhead bit. The purpose of this outpout pin is to warn the Terminal Equipment that, during the very next bit-period, the DS3/E3 Frame Generator block is going to be processing an Overhead Bit and will be ignoring any data that is applied to to the TxDS3DATA_1 input pin. ***NOTE:*** *This output pin can be ignored providing that either the Primary or Secondary Frame Synchronizer block is always up-stream from the DS3/E3 Frame Generator block.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C19	STS1TXA_1_D5 TXHDLCDAT_1_5 TXDS3FP_1	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Input Data Bus pin number 5/Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Input Data Bus - Pin 5/Transmit DS3/E3 Frame Boundary Indicator Output - Channel 1:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled -Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 5: STS1TXA_1_D5:** This input pin along with STS1TXA_1_D[7:6] and STS1TXA_1_D[4:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Data Bus Input pin # 5 -TXHDLCDAT_1_5:** If the XRT94L31 is configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode, then this input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3/E3 Frame Boundary Indicator Output - Channel 1 - TXDS3FP_1:** This output pin is pulse "High" for one DS3 or E3 clock period, when the Transmit Payload Data Input Interface block of Channel 1 (within the XRT94L31) is processing the last bit of a given DS3 or E3 frame.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D18	STS1TXA_1_D6 TXHDLCDAT_1_6 TXDS3DATA_1	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Data Bus Input pin number 6/Transmit High-Speed HDLC Controller Input Interface block - Channel 1 - Input Data Bus - Pin 6/Transmit DS3/E3 Serial Data Input - Channel 1:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 6 - STS1TXA_1_D6:** This input pin along with STS1TXA_1_D7 and STS1TXA_1_D[5:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input pin # 6 - Channel 1 - TxHDLCDAT_1_6:** This input pin will function as Bit 6 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 is configured to operate in the the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit Payload Data Input Interface - Channel 1 - Transmit DS3/E3 Serial Data Input - TXDS3DATA_1:** This input pin functions as the Transmit Payload Data Serial Input pin for Channel 1. In this case, the System-Side terminal equipment is expected to apply all outbound data (which is intended to be carried via the DS3 or E3 payload bits) to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxDS3DATA_1 input pin, upon the rising edge of TxInClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B21	STS1TXA_1_D7TXHDLCDAT_1_7TXAISEN_1	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 1 - Input Data Bus pin number 7/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 7/Transmit DS3/E3 AIS Input Pin - Channel 1:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled -Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 7: STS1TXA_1_D7:** This input pin along with STS1TXA_1_D[6:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 1. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_1. ***NOTE:*** *This input pin functions as the MSB (Most Significant Bit) of the Transmit (Add) Telecom Bus, for Channel 1.* **If the STS-1 Telecom Bus (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input Pin # 7 - Channel 1 -TXHDLCDAT_1_7:** This input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_1[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_1). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_1[7:0] input pins) upon the rising edge of the TxHDLCClk_1 clock output signal. **If the XRT94L31 is configured to operate in any other mode that involves the DS3/E3 Framer block - Transmit DS3/E3 AIS Enable Input - Channel 1 - TXAISEN_1:T** his input pin is used to command the Frame Generator block (within Channel 1) to generate and transmit the DS3/E3 AIS pattern, as described below. • "Low" - Configures the Frame Generator block to NOT generate and transmit the DS3/E3 AIS Pattern • "High" - Configures the Frame Generator block to generate and transmit the DS3/E3 AIS Pattern ***NOTE:*** *If the transmission of DS3/E3 AIS is controlled via Software, then this input pin MUST be tied to GND*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AE15	STS1TXA_2_D0 TXHDLCDAT_2_0 TXGFCMSB_2	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 2 - Input Data Bus pin number 0/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 0:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 0 - STS1TXA_2_D0:** This input pin along with STS1TXA_D_2[7:1] functions as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. This particular input pin functions as the LSB (Least Significant Bit) input pin on the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. The LSB of any byte, which is being input into the STS-1 Transmit Telecom Bus Interface - Data Bus (for Channel 2) should be input via this pin. **If the STS-1 Telecom Bus (associated with Channel 2) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface Block - Data Bus Input pin # 0 - Channel 2 - TXHDLCDAT_2_0:** In this mode, this input pin will function as Bit 0 (the LSB) within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **TXGFCMSB_2 (Transmit GFC MSB Indicator - Channel 2)** This input pin will only function in this role if the XRT94L31 has been configured to operate in the ATM UNI Mode.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD15	STS1TXA_2_D1 TXHDLCDAT_2_1 TXGFC_2	I	TTL	Transmit STS-1 Telecom Bus Interface - Channel 2 - Data Bus Input pin number 1/Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus - Pin 1: The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 1 - STS1TxA_2_D1:** This input pin along with STS1TXA_2_D[7:2] and STS1TXA_2_D0 functions as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. **If the STS-1 Telecom Bus Interface (associated with Channel 2) has been disabled:** This input pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Data Bus Input pin # 2 - TXHDLCDAT_2_1:** In this mode this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins).The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode** - TXGFC_2 (Transmit GFC data - Channel 2) **If the XRT94L31 has been configured to operate in the 3-Channel DS3/E3/STS-1 to STS-3/STM-1 Mapper Mode** - NO FUNCTION: Tie this input pin to GND.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AC15	STS1TXA_2_D2 TXHDLCDAT_2_2 TXCELLTXED_2	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 2 - Data Bus Input pin number 2/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 2:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 2 - STS1TXA_2_D2:** This input pin along with STS1TXA_2_D[7:3] and STS1TXA_2_D[1:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. **If the STS-1 Telecom Bus Interface (associated with Channel 2) has been disabled.** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in. If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Transmit High-Speed HDLC Controller Input Interface block - Channel 2- Data Bus Input pin # 2 TXHDLCDAT_2_2: In this mode, this input pin will function as Bit 1 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 has been configured to operate in the ATM UNI Mode** - TXCELLTXED_2 (Cell Transmitted - Channel 2)

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG16	STS1TXA_2_D3 TXHDLCDAT_2_3 SSI_NEG	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 2 - Data Bus Input pin number 3/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 3/Slow-Speed Interface - Negative Polarity Data Input/Output signal:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 3 - STS1TXA_2_D3:** This input pin along with STS1TXA_2_D[7:4] and STS1TXA_2_D[2:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Data Bus Input Pin # 3 TXHDLCDAT_2_3:** In this mode, this input pin will function as Bit 3 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins).The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 is configured to operate in the DS3/E3/STS-1 to STS-3/STM-1 Mapper Mode - Slow-Speed Interface for Ingress Path - Negative-Polarity Data Input/Output - SSI_NEG:** This pin along with the SSI_POS and SSI_CLK pins function as the Slow-Speed Interface for the Ingress Direction Signal Path Input/Output Port. which can be configured to function as either an Input (ADD) or Output (DROP) port. ***If the SSI Port is configured to operate as an Input (ADD) Port:*** In this configuration this port can be configured to accept a DS3, E3 or STS-1 signal (from external circuitry) and it will ADD this DS3/E3/STS-1 signal into the Selected Ingress Direction Channel within the XRT94L31. In this mode, the SSI_NEG will function as the Negative-Polarity Portion of the DS3/E3/STS-1 signal that is being ADDed. In this mode, the SSI Port will sample the data (being applied to this pin) upon the rising edge of SSI_CLK. ***If the SSI Port is configured to operate as an Output (DROP) Port:*** If the Slow-Speed Interface is configured to operate as an Output Port, then this port can be configured to output (or DROP out) the Selected Ingress Direction Channel within the XRT94L31. In this mode, the SSI_NEG will output the Negative Polarity portion of this selected Ingress Direction signal. This output pin will be updated upon the falling edge of the SSI_CLK output pin.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG17	STS1TXA_2_D4 TXHDLCDAT_2_4 TXDS3OHIND_2	I/O	TTL/ CMOS	**Transmit STS-1 Telecom Bus Interface - Channel 2 - Data Bus Input pin number 4/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 4/Transmit DS3/E3 Overhead Indicator Output - Channel 2:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 4 - STS1TXA_2_D4:** This input pin along with STS1TXA_2_D[7:5] and STS1TXA_2_D[3:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. **If the STS-1 Telecom Bus Interface (associated with Channel 2) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Data Bus Input Pin # 4 -TXHDLCDAT_2_4:** in this configuration, this input pin will function as Bit 4 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3/E3 Overhead Indicator Output - Channel 2 - TXDS3OHIND_2:** This output pin will pulse "High" one bit-period prior to the time that the DS3/E3 Frame Generator block (within Channel 2) will be processing an Overhead bit. The purpose of this outpout pin is to warn the Terminal Equipment that, during the very next bit-period, the DS3/E3 Frame Generator block is going to be processing an Overhead Bit and will be ignoring any data that is applied to to the TxDS3DATA_2 input pin. ***NOTE:*** *This output pin can be ignored provide that either the Primary or Secondary Frame Synchronizer block is always up-stream from the DS3/E3 Frame Generator block.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AF16	STS1TXA_2_D5 TXHDLCDAT_2_5 TXDS3FP_2	I/O	TTL/ CMOS	Transmit STS-1 Telecom Bus Interface - Channel 2 - Input Data Bus pin number 5/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 5/Transmit DS3/E3 Frame Boundary Indicator Output - Channel 2: The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 5 - STS1TXA_2_D5: This input pin along with STS1TXA_2_D[7:6] and STS1TXA_2_D[4:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. **If the STS-1 Telecom Bus Interface (associated with Channel 1) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Data Bus Input Pin # 5 - TXHDLCDAT_2_5:** In this configuration, this input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins). The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit DS3/E3 Frame Boundary Indicator Output - Channel 1 - TXDS3FP_2:** This output pin is pulse "High" for one DS3 or E3 clock period, when the Transmit Payload Data Input Interface block of Channel 2 (within the XRT94L31) is processing the last bit of a given DS3 or E3 frame.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG18	STS1TXA_2_D6TXHDLCDAT_2_6TXDS3DATA_2	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 2 - Data Input Bus pin number 6/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 6/Transmit DS3/E3 Serial Data Input - Channel 2:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 6 - STS1TXA_2_D6:** This input pin along with STS1TXA_2_D7 and STS1TXA_2_D[5:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. **If the STS-1 Telecom Bus Interface (associated with Channel 2) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input pin # 6 - Channel 2 - TXHDLCDAT_2_6:** In this configuration, this input pin will function as Bit 6 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins).The Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 is configured to operate in the Clear-Channel DS3/E3 Framer over STS-3/STM-1 Mapper Mode - Transmit Payload Data Input Interface - Channel 2 - Transmit DS3/E3 Serial Data Input - TXDS3DATA_2:** In this configuration, this input pin functions as the Transmit Payload Data Serial Input pin for Channel 2. In this case, the System-Side terminal equipment is expected to apply all outbound data (which is intended to be carried via the DS3 or E3 payload bits) to this input pin. The Transmit Payload Data Input Interface will sample the data, residing at the TxDS3DATA_2 input pin, upon the rising edge of TxInClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AE16	STS1TXA_2_D7 TXHDLCDAT_2_7 TXAISEN_2	I	TTL	**Transmit STS-1 Telecom Bus Interface - Channel 2 - Input Data Bus pin number 7/Transmit High-Speed HDLC Controller Input Interface block - Channel 2 - Input Data Bus - Pin 7/Transmit DS3/E3 AIS Input Pin - Channel 2:** The function of this pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled - Transmit STS-1 Telecom Bus Interface - Input Data Bus pin number 7 - STS1TXA_2_D7:** This input pin along with STS1TXA_2_D[6:0] function as the Transmit (Add) STS-1 Telecom Bus Interface - Input Data Bus for Channel 2. The Transmit STS-1 Telecom Bus interface will sample and latch this pin upon the falling edge of STS1TXA_CLK_2. ***NOTE:*** *This input pin functions as the MSB (Most Significant Bit) of the Transmit (Add) Telecom Bus, for Channel 2.* **If the STS-1 Telecom Bus (associated with Channel 2) has been disabled:** This input/output pin can function in either of the following roles, depending upon which mode the XRT94L31 has been configured to operate in, as described below. **If the XRT94L31 has been configured to operate in the High-Speed HDLC Controller over DS3/STS-3 Mode - Transmit High-Speed HDLC Controller Input Interface block - Data Bus Input Pin # 7 - Channel 2 -TXHDLCDAT_2_7:** In this configuration, this input pin will function as Bit 5 within the Transmit High-Speed HDLC Controller Input Interface block - Input Data Bus (e.g., the TxHDLCDat_2[7:0] input pins).T he Transmit High-Speed HDLC Controller Input Interface block will provide the System-Side Terminal equipment with a byte-wide Transmit High-Speed HDLC Controlller clock output signal (TxHDLCClk_2). The Transmit High-Speed HDLC Controller Input Interface block will sample the data residing on this input pin (along with the rest of the TxHDLCDat_2[7:0] input pins) upon the rising edge of the TxHDLCClk_2 clock output signal. **If the XRT94L31 is configured to operate in any other mode that involves the DS3/E3 Framer block** - Transmit DS3/E3 AIS Enable Input - Channel 2 - TXAISEN_2: This input pin is used to command the Frame Generator block (within Channel 1) to generate and transmit the DS3/E3 AIS pattern, as described below. • "Low" - Configures the Frame Generator block to NOT generate and transmit the DS3/E3 AIS Pattern • "High" - Configures the Frame Generator block to generate and transmit the DS3/E3 AIS Pattern **If the XRT94L31 is configured to operate in any other mode that involves the DS3/E3 Framer block - Transmit DS3/E3 AIS Enable Input - Channel 2 - TXAISEN_2:** ***NOTE:*** *To control the transmission of DS3/E3 AIS via Software, this input pin must be tied to GND.*
RECEIVE SYSTEM SIDE INTERFACE PINS				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
B15 C23 AG13	RxOH_0 RxOH_1 RxOH_2	O	CMOS	**Receive Overhead Data Output Interface - output** This output pin functions as the Receive Overhead Data output for the receive system side interface when the XRT94L31 is configured to operate in DS3/E3 mode, however, it functions as the Receive STS-1 Overhead Data output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** All overhead bits, which are received via the Receive Section of the channel, will be output via this output pin, upon the rising edge of RxOHClk_n. **When configured to operate in STS-1 mode:** These output pins, along with RxOHEnable_n, RxOHClk_n and RxOHFrame_n function as the Receive STS-1 TOH and POH Output Port.Each bit, within the TOH and POH bytes (within the incoming STS-1 data stream) is updated upon the falling edge of RxOHClk_n. As a consequence, external circuitry receiving this data, should sample this data upon the rising edge of RxOHClk_n. ***NOTES:*** 1. *The external circuitry can determine whether or not it is receiving POH or TOH data via this output pin. The RxOHEnable_n output pin will be "High" anytime POH data is being output via these output pins. Conversely, the RxOHEnable_n output pin will be "Low" anytime TOH data is being output via these output pins.* 2. *TOH and POH data, associated with Receive STS-1 TOH and POH Processor Block - Channel 0 will be output via the RxOH_0, and so on.*
C15 D21 AF13	RxOHENABLE_0 RxOHENABLE_1 RxOHENABLE_2	O	CMOS	**Receive Overhead Data Output Interface - Enable Output** This output pin functions as the Receive Overhead Enable output for the receive system side interface when the XRT94L31 is configured to operate in DS3/E3 mode, however, it functions as the Receive STS-1 Overhead Data output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The channel will assert this output signal for one RxOHClk_n period when it is safe for the local terminal equipment to sample the data on the RxOH_n output pin. **When configured to operate in STS-1 mode:** These output pins, along with RxOHClk_n, RxOHFrame_n and RxOH_n function as the Receive STS-1 TOH and POH Output Port. These output pins indicate whether POH or TOH data is being output via the RxOH_n output pins. These output pins will toggle "High" coincident with when POH data is being output via the RxOH_n output pins. Conversely, these output pins will toggle "Low" coincident with when TOH data is being output via the RxOH_n output pins. These output pins are updated upon the falling edge of RxOHClk_n. As a consequence, external circuitry, receiving this data, should sample this data upon the rising edge of RxOHClk_n.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D15 E20 AE13	RxOHCLK_0 RxOHCLK_1 RxOHCLK_2	O	CMOS	**Receive Overhead Data Output Interface - clock** This output pin functions as the Receive Overhead Clock output for the receive system side interface when the XRT94L31 is configured to operate in DS3/E3 mode, however, it functions as the Receive STS-1 Overhead Clock output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** The channel will output the overhead bits (within the incoming DS3 or E3 frames) via the RxOH_n output pin, upon the falling edge of this clock signal. As a consequence, the user's local terminal equipment should use the rising edge of this clock signal to sample the data on both the RxOH and RxOHFrame output pins. ***NOTE:*** *This clock signal is always active.* **When configured to operate in STS-1 mode:** These output pins, along with RxOH_n, RxOHFrame_n, and RxOHEnable_n function as the Receive STS-1 TOH and POH Output Port.These output pins function as the Clock Output signals for the Receive STS-1 TOH and POH Output Port. The RxOH_n, RxSTS1Frame_n and RxOHEnable_n output pins are updated upon the falling edge of this clock signal.
E15 D22 AD13	RxOHFRAME_0 RxOHFRAME_1 RxOHFRAME_2	O	CMOS	**Receive Overhead Data Interface - Framing Pulse indicator** This output pin functions as the Receive Overhead Clock output for the receive system side interface when the XRT94L31 is configured to operate in DS3/E3 mode, however, it functions as the Receive STS-1 Overhead Clock output when the device is configured to operate in the STS-1 mode. **When configured to operate in DS3/E3 mode:** This output pin pulses "High" whenever the Receive Overhead Data Output Interface block outputs the first overhead bit of a new DS3 or E3 frame. **When configured to operate in STS-1 mode:** These output pins, along with RxOH_n, RxOHEnable_n and RxOHClk_n function as the Receive STS-1 TOH and POH Output Port. These output pins will pulse "High" coincident with either of the following events. When the very first TOH byte (A1), of a given STS-1 frame, is being output via the corresponding RxOH_n output pin. When the very first POH byte (J1), of a given STS-1 frame, is being output via the corresponding RxOH_n output pin. The external circuitry can determine whether or not these output pins are pulsing "High" for the first TOH or POH byte by checking the state of the corresponding RxOHEnable_n output pin.
Y26	RxPERR	O	CMOS	**For mapper applications, Please let this pin float.**
AB27	RxPEOP	O	CMOS	**For mapper applications, Please let this pin float.**
AA26	RxPDVAL	O	CMOS	**For mapper applications, Please let this pin float.**
V24	RxMOD_0	O	CMOS	**For mapper applications, Please let this pin float.**
V25	RxUPRTY/RxPPRTY	O	CMOS	**For mapper applications, Please let this pin float.**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
U23	RxUDATA_0	O	CMOS	**For mapper applications, Please let these pins float.**
	RxPDATA_0			
W26	RxUDATA_1			
	RxPDATA_1			
U24	RxUDATA_2			
	RxPDATA_2			
AA27	RxUDATA_3			
	RxPDATA_3			
Y27	RxUDATA_4			
	RxPDATA_4			
U25	RxUDATA_5			
	RxPDATA_5			
V26	RxUDATA_6			
	RxPDATA_6			
W27	RxUDATA_7			
	RxPDATA_7			
T23	RxUDATA_8			
	RxPDATA_8			
T24	RxUDATA_9			
	RxPDATA_9			
U26	RxUDATA_10			
	RxPDATA_10			
T25	RxUDATA_11			
	RxPDATA_11			
V27	RxUDATA_12			
	RxPDATA_12			
T26	RxUDATA_13			
	RxPDATA_13			
U27	RxUDATA_14			
	RxPDATA_14			
T27	RxUDATA_15			
	RxPDATA_15			
R23	RxUADDR_0	I	TTL	**For mapper applications, Please connect these pins to GND**
R24	RxUADDR_1			
R25	RxUADDR_2			
R26	RxUADDR_3			
R27	RxUADDR_4			
P27	RxUClav/RxPPA	O	CMOS	**For mapper applications, Please let this pin float.**
P25	RxUSOC/RxPSOP/ RxPSOC	O	CMOS	**For mapper applications, Please let this pin float.**
P23	RxTSX/RXPSOF	O	CMOS	**For mapper applications, Please let this pin float.**
P24	RXUENB_L/ RXPENB_L	I	TTL	**For mapper applications, Please connect this pin to VDD**
P26	RXUCLKO/ RXPCLKO	O	CMOS	**For mapper applications, Please let this pin float.**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
N27	RXUCLK/RXPCLK	I	TTL	**For mapper applications, Please connect this pin to GND**
A16 J23 AC13	EXTLOS_0 EXTLOS_1 EXTLOS_2	I	TTL	**Receive LOS (Loss of Signal) Indicator Input (from an off-chip DS3/E3/STS-1 LIU IC):** These input pins are intended to be connected to a corresponding RLOS (Receive Loss of Signal) output pin of an off-chip DS3/E3/STS-1 LIU IC. Through this connection, if a given LIU Channel declares the LOS defect condition, it will (in-turn) drive the corresponding EXTLOS_n input pin (to the XRT94L31) to the logic "High" level. If the a given channel (within the XRT94L31) is configured to operate in either the DS3 or E3 Mode, and if the off-chip LIU IC asserts the corresponding EXTLOS_n input pin (by driving it to the logic "High" level), then the DS3/E3 Framer block (within this particular channel) will automatically declare the LOS defect condition (for the duration that this input pin is driven to a logic "High". If the LIU Channel toggles this input pin "Low", then the corresponding DS3/E3 Framer block (within the XRT94L31) will MOST LIKELY clear the LOS defect condition. ***NOTES:*** *1. The DS3/E3 Framer block can be configured to declare and clear the LOS defect condition based upon both the state of this input pin and the content within the incoming DS3/E3 data-stream. However, the DS3/E3 Framer block will UNCONDITIONALLY declare the LOS defect condition, if its corresponding EXTLOS_n input pin is driven to the logic "High" level.* *2. These input pins are ignored if their corresponding Channel has been configured to operate in the STS-1 Mode. The Receive STS-1 TOH Processor block will only declare and clear the LOS defect condition based the number of consecutive All Zero bytes that are detected within the incoming STS-1 data-stream.*
A14D20AE14	RxOOF_0RxOOF_1RxOOF_2	O	CMOS	Receive STS-1/DS3/E3 Out of Frame IndicatorThe STS-1/DS3/E3 Receive DS3 Framer will assert this output signal whenever it has declared an Out of Frame (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
A15B24AG14	RxLOS_0RxLOS_1RxLOS_2	O	CMOS	**STS-1/DS3/E3 Framer - Loss of Signal Output Indicator:** This pin is asserted when the Receive Section of the channel encounters 180 consecutive 0's (for DS3 applications) or 32 consecutive 0's (for E3 applications) via the RxPOS_n and RxNEG pins. For STS-1 applications, users can set the LOS threshold value in the Receive LOS Threshold register. (RxSTOH_LOS_TH, Address Location: 0xN02E - 0xN02F) This pin will be negated once the Receive DS3/E3 Framer has detected at least 60 1s out of 180 consecutive bits (for DS3 applications) or has detected at least four consecutive 32 bit strings of data that contain at least 8 1s in the receive path.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
STS-1 TELECOM BUS INTERFACE - RECEIVE DIRECTION				
A21	STS1RXD_CK_0 RXVALIDFCS_0 RXGFCCLK_0	O	CMOS	**Receive STS-1/STS-3 Telecom Bus Clock Output - Channel 0;** The function of this input pin depends upon whether or not the STS-1 Telecom Bus Interface associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled -** STS-1 Receive Telecom Bus Clock Output - Channel 0;STS1RXD_CK_0: All signals, which are output via the Receive Telecom Bus - Channel 0 are clocked out upon the rising edge of this clock signal. This includes the following signals. • STS1RXD_D_0[7:0] • STS1RXD_ALARM_0 • STS1RXD_DP_0 • STS1RXD_PL_0 • STS1RXD_C1J1_0 This clock signal will operate at 19.44MHz (For STS-3 mode) or 6.48MHz (Fro STS-1 mode) **RXVALIDFCS_0 (Receive HDLC block valid FCS Indicator - Channel 0)** **RXGFCCLK_0 (Receive ATM GFC clock signal - Channel 0)**
H24	STS1RXD_CK_1 RXVALIDFCS_1 RXGFCCLK_1 TxP_STPA	O	CMOS	**Receive STS-1 Telecom Bus Clock Output - Channel 1;** The function of this input pin depends upon whether or not the STS-1 Telecom Bus Interface associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled** - STS-1 Receive Telecom Bus Clock Output - Channel 1; STS1RXD_CK_1: All signals, which are output via the Receive Telecom Bus - Channel 1 are clocked out upon the rising edge of this clock signal. This includes the following signals. • STS1RXD_D_1[7:0] • STS1RXD_ALARM_1 • STS1RXD_DP_1 • STS1RXD_PL_1 • STS1RXD_C1J1_1 This clock signal will operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (Fro STS-1 mode) **RXVALIDFCS_1 (Receive HDLC block valid FCS Indicator - Channel 1)** **RXGFCCLK_1 (Receive ATM GFC clock signal - Channel 1)** **TxP_STPA (Transmit PPP Level 2 Selected Channel Packet Available)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG8	STS1RXD_CK_2 RXVALIDFCS_2 RXGFCCLK_2	O	CMOS	Receive STS-1 Telecom Bus Clock Output - Channel 2; The function of this input pin depends upon whether or not the STS-1 Telecom Bus Interface associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus Clock Output - Channel 2; STS1RXD_CK_2: All signals, which are output via the Receive Telecom Bus - Channel 2 are clocked out upon the rising edge of this clock signal. This includes the following signals. • STS1RXD_D_2[7:0] • STS1RXD_ALARM_2 • STS1RXD_DP_2 • STS1RXD_PL_2 • STS1RXD_C1J1_2 This clock signal will operate at 19.44MHz. (For STS-3 mode) or 6.48MHz (Fro STS-1 mode) **RXVALIDFCS_2 (Receive HDLC block valid FCS Indicator - Channel 2)** **RXGFCCLK_2 (Receive ATM GFC clock signal - Channel 2)**
A20 D26 AE11	STS1RXD_PL_0 RXIDLE_0 RXLCD_0 STS1RXD_PL_1 RXIDLE_1 RXLCD_1 STS1RXD_PL_2 RXIDLE_2 RXLCD_2	O	CMOS	**STS-1 Receive (Drop) Telecom Bus - Payload Indicator Output Signal - Channel n:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface block associated with Channel n has been enabled or disabled. **If the STS-1 Telecom Bus Interface (associated with Channel n) is enabled** - STS-1/STS-1 Receive (Drop) Telecom Bus - Payload Indicator Output - STS1RXD_PL_0: This output pin indicates whether or not Transport Overhead bytes are being output via the STS1RXD_D_0[7:0] output pins. This output pin is pulled "Low" for the duration that the STS-1 Receive Telecom Bus is transmitting a Transport Overhead byte via the STS1RXD_D_0[7:0] output pins. Conversely, this output pin is pulled "High" for the duration that the STS-1 Receive Telecom Bus is transmitting something other than a Transport Overhead byte via the STS1RXD_D_0[7:0] output pins. **RXIDLE_0 (Receive HDLC block idle indicator - Channel n)** **RXLCD_0 (Receive Cell Processor Loss of Cell Delineation - Channel n)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C17 E25 AF10	STS1RXD_C1J1_0 TXDS3LINECLK_0 STS1RXD_C1J1_1 TXDS3LINECLK_1 STS1RXD_C1J1_2 TXDS3LINECLK_2	O	CMOS	**STS-1 Receive Telecom Bus - C1/J1 Byte Phase Indicator Output Signal - Channel n:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled - STS-1 Receive Telecom Bus - C1/J1 Byte Phase Indicator Output Signal:** This output pin pulses "High" under the following two conditions.Whenever the C1 byte is being output via the STS1RXD_D_0[7:0] output, and Whenever the J1 byte is being output via the STS1RXD_D_0[7:0] output. ***NOTES:*** *1. The STS-1 Receive (Drop) Telecom Bus (associated with Channel n) will indicate that it is transmitting the C1 byte (via the STS1RXD_D_0[7:0] output pins), by pulsing this output pin "High" (for one period of STS1RXD_CK_0) and keeping the STS1RXD_PL_0 output pin pulled "Low".* *2. The STS-1 Receive (Drop) Telecom Bus (associated with Channel n) will indicate that it is transmitting the J1 byte (via the STS1RXD_D_0[7:0] output pins), by pulsing this output pin "High" (for one period of STS1RXD_CK_0) while the STS1TXD_PL_0 output pin is pulled "High".* **TXDS3LINECLK_0 (Transmit DS3/E3/STS-1 line clock to LIU - Channel n)**
B18 G24 AG9	STS1RXD_DP_0 TXDS3POS_0 STS1RXD_DP_1 TXDS3POS_1 STS1RXD_DP_2 TXDS3POS_2	O	CMOS	**STS-1 Receive (Drop) Telecom Bus - Parity Output pin - Channel n:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled** - STS-1 Receive Telecom Bus - Parity Output pin: This output pin can be configured to function as one of the following. The EVEN or ODD parity value of the bits which are output via the STS1RXD_D_0[7:0] output pins. The EVEN or ODD parity value of the bits which are being output via the STS1RXD_D_0[7:0] output pins and the states of the STS1RXD_PL_0 and STS1RXD_C1J1_0 output pins. This output pin will ultimately be used (by drop-side circuitry) to verify the verify of the data which is output via the STS-1 Telecom Bus Interface associated with Channel n. ***NOTE:*** *The user can make any one of these configuration selections by writing the appropriate value into the Telecom Bus Control Register (Address Location = 0x013B).TXDS3POS_0 (Transmit DS3/E3/STS-1 line data positive to LIU- Channel n)*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A19 H23 AB12	STS1RXD_ALARM_0 TXDS3NEG_0 STS1RXD_ALARM_1 TXDS3NEG_1/ STS1RXD_ALARM_2 TXDS3NEG_2	O	CMOS	**STS-1 Receive (Drop) Telecom Bus - Alarm Indicator Output signal - Channel n:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface for Channel n has been enabled. **If STS-1 Telecom Bus (Channel n) has been enabled** - STS-1 Receive Telecom Bus - Alarm Indicator Output signal: This output pin pulses "High", coincident with any STS-1 signal (that is being output via the STS1RXD_D_n[7:0] output pins) that is carrying an AIS-P indicator. This output pin is "Low" for all other conditions. **TXDS3NEG_n (Transmit DS3/E3 line data negative to LIU - Channel n)**
F16	STS1RXD_D0_0 RXHDLCDAT_0_0 RXGFCMSB_0	O	CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 0:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - STS-1 Receive Telecom Bus** - Output Data bus pin number 0: STS1RXD_D0_0 This output pin along with STS1RXD_D_0[7:1] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0:. ***NOTE:*** *This input pin functions as the LSB (Least Significant Bit) of the Receive (Drop) Telecom Bus for Channel 0.* **RXHDLCDAT_0_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 0)** **RXGFCMSB_0 (Receive GFC MSB Indicator - Channel 0)**
E16	STS1RXD_D1_0 RXHDLCDAT_1_0 RXGFC_0	O	CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 1:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled - STS-1 Receive Telecom Bus** - Output Data bus pin number 1: STS1RXD_D1_0 This output pin along with STS1RXD_D_0[7:2] and STS1RXD_D0_0 function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0. **RXHDLCDAT_1_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 1):** **RXGFC_0 (Receive GFC output data - Channel 0)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
D16	STS1RXD_D2_0 RXHDLCDAT_2_0 RXCELLRXED_0	O	CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 2:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 2: STS1RXD_D2_0 This output pin along with STS1RxD_D_0[7:3] and STS1RxD_D_0[1:0] function as the STS-3/STM-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-3/STM-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RxD_CK_0. **RXHDLCDAT_2_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 2)** **RXCELLRXED_0 (Receive cell received indicator - Channel 0)**
B17	STS1RXD_D3_0 RXHDLCDAT_3_0 SSE_CLK	OO IO O	CMOS CMOS TTL/ CMOS CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 3:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 3: STS1RXD_D3_0 This output pin along with STS1RXD_D_0[7:4] and STS1RXD_D_0[2:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0. **RXHDLCDAT_3_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 3)** **SSE_CLK (Slow Speed Clock Interface for Egress Path)**
C16	STS1RXD_D4_0 RXHDLCDAT_4_0 RXOHIND_0	O	CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 4:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 4: STS1RXD_D4_0 This output pin along with STS1RXD_D_0[7:5] and STS1RXD_D_0[3:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0. **RXHDLCDAT_4_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 4)** **RXOHIND_0 (Receive Overhead Indicator - Channel 0)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
A18	STS1RXD_D5_0 RXHDLCDAT_5_0 RXDS3FP_0	O	CMOS	Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 5: The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 5: STS1RXD_D5_0 This output pin along with STS1RXD_D_0[7:6] and STS1RXD_D_0[4:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0. **RXHDLCDAT_5_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 5)** **RXDS3FP_0 (Receive DS3 frame pulse - Channel 0)**
B16	STS1RXD_D6_0 RXHDLCDAT_6_0 RXDS3DATA_0	O	CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 6:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. If STS-1 Telecom Bus (Channel 0) has been enabled - STS-1 Receive Telecom Bus - Output Data bus pin number 6: STS1RXD_D6_0 This output pin along with STS1RXD_D7_0 and STS1RXD_D_0[5:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0. **RXHDLCDAT_6_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 6)** **RXDS3DATA_0 (Receive DS3 data - Channel 0)**
A17	STS1RXD_D7_0 RXHDLCDAT_7_0 RXDS3CLK_0	O	CMOS	**Receive STS-1 Telecom Bus - Channel 0 - Output Data Bus pin number 7:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 0 is enabled. **If STS-1 Telecom Bus (Channel 0) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 7: STS1RXD_D7_0 This output pin along with STS1RXD_D_0[6:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 0. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_0:. ***NOTE:*** *This output pin functions as the MSB (Most Significant Bit) for the STS-1 Receive (Drop) Telecom Bus Interface - Output Data Bus (Channel 0).* **RXHDLCDAT_7_0 (Receive HDLC block data output - Channel 0 - Output Data Bus pin 7)** **RXDS3CLK_0 (Receive DS3 clock - Channel 0)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
F24	STS1RXD_D0_1 RXHDLCDAT_0_1 RXGFCMSB_1	O	CMOS	**Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 0:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. If STS-1 Telecom Bus (Channel 1) has been enabled - STS-1 Receive Telecom Bus - Output Data bus pin number 0: STS1RXD_D0_1 This output pin along with STS1RXD_D_1[7:1] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. ***NOTE:*** *This input pin functions as the LSB (Least Significant Bit) of the Receive (Drop) Telecom Bus for Channel 1.* **RXHDLCDAT_0_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 0)RXGFCMSB_1 (Receive GFC MSB Indicator - Channel 1)**
H22	STS1RXD_D1_1 RXHDLCDAT_1_1 RXGFC_1	O	CMOS	**Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 1:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 1: STS1RXD_D1_1 This output pin along with STS1RXD_D_1[7:2] and STS1RXD_D0_1 function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. **RXHDLCDAT_1_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 1)** **RXGFC_1 (Receive GFC output data - Channel 1)**
D25	STS1RXD_D2_1 RXHDLCDAT_2_1 RXCELLRXED_1	O	CMOS	Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 2: The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 2: STS1RXD_D2_1This output pin along with STS1RXD_D_1[7:3] and STS1RXD_D_1[1:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. **RXHDLCDAT_2_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 2)** **RXCELLRXED_1 (Receive cell received indicator - Channel 1)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
G23	STS1RXD_D3_1 RXHDLCDAT_3_1 SSE_POS	OO IO O	CMOS CMOS TTL/ CMOS CMOS	Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 3: The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. If STS-1 Telecom Bus (Channel 1) has been enabled - STS-1 Receive Telecom Bus - Output Data bus pin number 3: STS1RXD_D3_1 This output pin along with STS1RXD_D_1[7:4] and STS1RXD_D_1[2:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. **RXHDLCDAT_3_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 3)** **SSE_POS (Slow Speed Interface Data Positive for Egress Path)**
D23	STS1RXD_D4_1RXHDLCDAT_4_1RXOHIND_1	O	CMOS	**Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 4:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 4: STS1RXD_D4_1 This output pin along with STS1RXD_D_1[7:5] and STS1RXD_D_1[3:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. **RXHDLCDAT_4_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 4)** **RXOHIND_1 (Receive Overhead Indicator - Channel 1)**
E21	STS1RXD_D5_1RXHDLCDAT_5_1RXDS3FP_1	O	CMOS	Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 5: The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 5: STS1RXD_D5_1 This output pin along with STS1RXD_D_1[7:6] and STS1RXD_D_1[4:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. **RXHDLCDAT_5_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 5)** **RXDS3FP_1 (Receive DS3 frame pulse - Channel 1)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
C24	STS1RXD_D6_1RXHDLCDAT_6_1RXDS3DATA_1	O	CMOS	**Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 6:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. If STS-1 Telecom Bus (Channel 1) has been enabled - STS-1 Receive Telecom Bus - Output Data bus pin number 6: STS1RXD_D6_1 This output pin along with STS1RXD_D7_1 and STS1RXD_D_1[5:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. **RXHDLCDAT_6_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 6):** **RXDS3DATA_1 (Receive DS3 data - Channel 1):**
F20	STS1RXD_D7_1 RXHDLCDAT_7_1 RXDS3CLK_1	O	CMOS	**Receive STS-1 Telecom Bus - Channel 1 - Output Data Bus pin number 7:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 1 is enabled. **If STS-1 Telecom Bus (Channel 1) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 7: STS1RXD_D7_1 This output pin along with STS1RXD_D_1[6:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 1. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_1. ***NOTE:*** *This output pin functions as the MSB (Most Significant Bit) for the STS-1 Receive (Drop) Telecom Bus Interface - Output Data Bus (Channel 1).* **RXHDLCDAT_7_1 (Receive HDLC block data output - Channel 1 - Output Data Bus pin 7)** **RXDS3CLK_1 (Receive DS3 clock - Channel 1)**
AC12	STS1RXD_D0_2 RXHDLCDAT_0_2 RXGFCMSB_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 0:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 0: STS1RXD_D0_2 This output pin along with STS1RXD_D_2[7:1] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. ***NOTE:*** *This input pin functions as the LSB (Least Significant Bit) of the Receive (Drop) Telecom Bus for Channel 2.* **RXHDLCDAT_0_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 0)** **RXGFCMSB_2 (Receive GFC MSB Indicator - Channel 2)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD12	STS1RXD_D1_2 RXHDLCDAT_1_2 RXGFC_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 1:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 1: STS1RXD_D1_2 This output pin along with STS1RXD_D_2[7:2] and STS1RXD_D0_2 function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. **RXHDLCDAT_1_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 1)** **RXGFC_2 (Receive GFC output data - Channel 2)**
AF11	STS1RXD_D2_2RXHDLCDAT_2_2 RXCELLRXED_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 2:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 2: STS1RXD_D2_2 This output pin along with STS1RXD_D_2[7:3] and STS1RXD_D_2[1:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. **RXHDLCDAT_2_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 2)** **RXCELLRXED_2 (Receive cell received indicator - Channel 2)**
AE12	STS1RXD_D3_2 RXHDLCDAT_3_2 SSE_NEG	OO IO O	CMOS CMOS TTL/ CMOS CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 3:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 3: STS1RXD_D3_2 This output pin along with STS1RXD_D_2[7:4] and STS1RXD_D_2[2:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. **RXHDLCDAT_3_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 3)** **SSE_NEG (Slow Speed Interface Data Negative for Egress Path)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG10	STS1RXD_D4_2RXHDLCDAT_4_2RXOHIND_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 4:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 4: STS1RXD_D4_2 This output pin along with STS1RXD_D_2[7:5] and STS1RXD_D_2[3:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. **RXHDLCDAT_4_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 4)** **RXOHIND_2 (Receive Overhead Indicator - Channel 2)**
AF12	STS1RXD_D5_2RXHDLCDAT_5_2RXDS3FP_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 5:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 5: STS1RXD_D5_2 This output pin along with STS1RXD_D_2[7:6] and STS1RXD_D_2[4:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. **RXHDLCDAT_5_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin5)** **RXDS3FP_2 (Receive DS3 frame pulse - Channel 2)**
AG11	STS1RXD_D6_2RXHDLCDAT_6_2RXDS3DATA_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 6:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 6: STS1RXD_D6_2 This output pin along with STS1RXD_D7_2 and STS1RXD_D_2[5:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. **RXHDLCDAT_6_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 6)** **RXDS3DATA_2 (Receive DS3 data - Channel 2)**

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG12	STS1RXD_D7_2 RXHDLCDAT_7_2 RXDS3CLK_2	O	CMOS	**Receive STS-1 Telecom Bus - Channel 2 - Output Data Bus pin number 7:** The function of this output pin depends upon whether or not the STS-1 Telecom Bus Interface, associated with Channel 2 is enabled. **If STS-1 Telecom Bus (Channel 2) has been enabled** - STS-1 Receive Telecom Bus - Output Data bus pin number 7: STS1RXD_D7_2 This output pin along with STS1RXD_D_2[6:0] function as the STS-1 Receive (Drop) Telecom Bus - Output Data Bus for Channel 2. The STS-1 Telecom Bus Interface will update the data via this output upon the rising edge of STS1RXD_CK_2. ***NOTE:*** *This output pin functions as the MSB (Most Significant Bit) for the STS-1 Receive (Drop) Telecom Bus Interface - Output Data Bus (Channel 2).RXHDLCDAT_7_2 (Receive HDLC block data output - Channel 2 - Output Data Bus pin 7)RXDS3CLK_2 (Receive DS3 clock - Channel 2)*
RECEIVE TRANSPORT OVERHEAD INTERFACE				
AD5	RxTOHClk	O	CMOS	**Receive TOH Output Port - Clock Output:** This output pin, along with RxTOH, RxTOHValid and RxTOHFrame function as the Receive TOH Output Port. The Receive TOH Output Port permits is used to obtain the value of the TOH Bytes, within the incoming STS-3/STM-1 signal. This output pin provides the user with a clock signal. If the RxTOHValid output pin is "High", then the contents of the TOH bytes, within the incoming STS-3 data-stream will be serially output via the RxTOH output. This data will be updated upon the falling edge of this clock signal. Therefore, the user is advised to sample the data (at the RxTOH output pin) upon the rising edge of this clock output signal.
AC7	RxTOHValid	O	CMOS	**Receive TOH Output Port - TOH Valid (or READY) indicator:** This output pin, along with RxTOH and RxTOHFrame function as the Receive TOH Output Port. This output pin will toggle "High" whenever valid TOH data is being output via the RxTOH output pin.
AE4	RxTOH	O	CMOS	**Receive TOH Output port - Output pin:** This output pin, along with RxTOHClk, RxTOHValid and RxTOHFrame function as the Receive TOH Output port. All TOH data that resides within the incoming STS-3 data-stream will be output via this output pin. The RxTOHValid output pin will toggle "High", coincident with anytime a bit (from the Receive STS-3 TOH data) is being output via this output pin. The RxTOHFrame output pin will pulse "High" (for eight periods of RxTOHClk) coincident to when the A1 byte is being output via this output pin. Data, on this output pin, is updated upon the falling edge of RxTOHClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AB8	RxTOHFrame	O	CMOS	**Receive TOH Output Port - STS-3/STM-1 Frame Indicator:** This output pin, along with the RxTOHClk, RxTOHValid and RxTOH output pins function as the Receive TOH Output port. This output pin will pulse "High", for one period of RxTOHClk, one RxTOHClk period prior to the very first TOH bit (of a given STS-3 frame) being output via the RxTOH output pin.
AD7	RxLDCCVAL	O	CMOS	**Receive - Line DCC Output Port - DCC Value Indicator Output pin:** This output pin, along with the RxTOHClk and the RxLDCC output pins function as the Receive Line DCC output port of the XRT94L31. This output pin pulses "High" coincident to when the Receive Line DCC output port outputs a DCC bit via the RxLDCC output pin. This output pin is updated upon the falling edge of RxTOHClk. The Line DCC HDLC Controller circuitry that is interfaced to this output pin, the RxLDCC and the RxTOHClk pins is suppose to do the following. It should continuously sample and monitor the state of this output pin upon the rising edge of RxTOHClk. Anytime the Line DCC HDLC circuitry samples this output pin being "High", it should sample and latch the data on the RxLDCC output pin (as a valid Line DCC bit) into the Line DCC HDLC circuitry.
AE5	RxLDCC	O	CMOS	**Receive - Line DCC Output Port - Output Pin:** This output pin, along with RxLDCCVAL and the RxTOHClk output pins function as the Receive Line DCC output port of the XRT94L31. This pin outputs the contents of the Line DCC (e.g., the D4, D5, D6, D7, D8, D9, D10, D11 and D12 bytes), within the incoming STS-3 datastream. The Receive Line DCC Output port will assert the RxLDCCVAL output pin, in order to indicate that the data, residing on the RxLDCC output pin is a valid Line DCC byte. The Receive Line DCC output port will update the RxLDCCVAL and the RxLDCC output pins upon the falling edge of the RxTOHClk output pin. The Line DCC HDLC circuitry that is interfaced to this output pin, the RxLDCCVAL and the RxTOHClk pins is suppose to do the following. It should continuously sample and monitor the state of the RxLDCCVAL output pin upon the rising edge of RxTOHClk. Anytime the Line DCC HDLC circuitry samples the RxLDCCVAL output pin "High", it should sample and latch the contents of this output pin (as a valid Line DCC bit) into the Line DCC HDLC circuitry.
AD8	RxE1F1E2FP	O	CMOS	**Receive - Order-Wire Output Port - Frame Boundary Indicator:** This output pin, along with RxE1F1E2, RxE1F1E2Val and the RxTOHClk output pins function as the Receive Order-Wire Output port of the XRT94L31. This output pin pulses "High" (for one period of RxTOHClk) coincident to when the very first bit (of the E1 byte) is being output vi the RxE1F1E2 output pin.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AC9	RxE1F1E2	O	CMOS	**Receive - Order-Wire Output Port - Output Pin:** This output pin, along with RxE1F1E2Val, RxE1F1F2FP, and the RxTOHClk output pins function as the Receive Order-Wire Output Port of the XRT94L31. This pin outputs the contents of the Order-Wire bytes (e.g., the E1, F1 and E2 bytes) within the incoming STS-3 data-stream. The Receive Order-Wire Output port will pulse the RxE1F1E2FP output pin "High" (for one period of RxTOHClk) coincident to when the very first bit (of the E1 byte) is being output via the RxE1F1E2 output pin. Additionally, the Receive Order-Wire Output port will also assert the RxE1F1E2Val output pin, in order to indicate that the data, residing on the RxE1F1E2 output pin is valid Order-Wire byte. The Receive Order-Wire output port will update the RxE1F1E2Val, the RxE1F1E2FP and the RxE1F1E2 output pins upon the falling edge of the RxTOHClk output pin. The Receive Order-Wire circuitry that is interfaced to this output pin, and the RxE1F1E2Val, the RxE1F1E2 and the RxTOHClk pins is suppose to do the following. It should continuously sample and monitor the state of the RxE1F1E2Val and RxE1F1E2FP output pins upon the rising edge of RxTOHClk. Anytime the Order-wire circuitry samples the RxE1F1E2Val and RxE1F1E2FP output pins "High", it should begin to sample and latch the contents of this output pin (as a valid Order-Wire bit) into the Order-Wire circuitry. The Order-Wire circuitry should continue to sample and latch the contents of the output pin until the RxE1F2E2Val output pin is sampled "Low".
AC8	RxSDCC	O	CMOS	**Receive - Section DCC Output Port - Output Pin:** This output pin, along with RxSDCCVAL and the RxTOHClk output pins function as the Receive Section DCC output port of the XRT94L31. This pin outputs the contents of the Section DCC (e.g., the D1, D2 and D3 bytes), within the incoming STS-3 data-stream. The Receive Section DCC Output port will assert the RxSDCCVAL output pin, in order to indicate that the data, residing on the RxSDCC output pin is a valid Section DCC byte. The Receive Section DCC output port will update the RxSDCCVAL and the RxSDCC output pins upon the falling edge of the RxTOHClk output pin. The Section DCC HDLC circuitry that is interfaced to this output pin, the RxSDCCVAL and the RxTOHClk pins is suppose to do the following. It should continuously sample and monitor the state of the RxSDCCVAL output pin upon the rising edge of RxTOHClk. Anytime the Section DCC HDLC circuitry samples the RxSDCCVAL output pin "High", it should sample and latch the contents of this output pin (as a valid Section DCC bit) into the Section DCC HDLC circuitry.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AD6	RxSDCCVAL	O	CMOS	**Receive - Section DCC Output Port - DCC Value Indicator Output pin:** This output pin, along with the RxTOHClk and the RxSDCC output pins function as the Receive Section DCC output port of the XRT94L31. This output pin pulses "High" coincident to when the Receive Section DCC output port outputs a DCC bit via the RxSDCC output pin. This output pin is updated upon the falling edge of RxTOHClk. The Section DCC HDLC Controller circuitry that is interfaced to this output pin, the RxSDCC and the RxTOHClk pins is suppose to do the following. It should continuously sample and monitor the state of this output pin upon the rising edge of RxTOHClk. Anytime the Section DCC HDLC circuitry samples this output pin being "High", it should sample and latch the data on the RxSDCC output pin (as a valid Section DCC bit) into the Section DCC HDLC circuitry.
AF4	RxE1F1E2VAL	O	CMOS	**Receive - Order Wire Output Port - E1F1E2 Value Indicator Output Pin:** This output pin, along with the RxTOHClk, RxE1F1E2FP, RxE1F1E2 and RxTOHClk output pins function as the Receive - Order Wire Output Port of the XRT94L31. This output pin pulses "High" coincident to when the Receive - Order Wire output port outputs the contents of an E1, F1 or E2 byte, via the RxE1F1E2 output pin. This output pin is updated upon the falling edge of RxTOHClk.The Receive Order-Wire circuitry, that is interfaced to this output pin, the RxE1F1E2 and the RxTOHClk pins is suppose to do the following. It should continuously sample and monitor the state of this output pin upon the rising edge of RxTOHClk. Anytime the Receive Order-Wire circuitry samples this output pin being "High", it should sample and latch the data on the RxE1F1E2 output pin (as a valid Order-wire bit) into the Receive Order-Wire circuitry.
AE6	RXPOH	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block - Path Overhead Output Port - Output Pin:** This output pin, along with the RxPOHClk, RxPOHFrame and RxPOHValid function as the AU-4/VC-4 Mapper POH Processor block - POH Output port. These pins serially output the POH data that have been received by the Receive AU-4/VC-4 Mapper POH Processor block (via the incoming STS-3 data-stream). Each bit, within the POH bytes is updated (via these output pins) upon the falling edge of RxPOHClk. As a consequence, external circuitry receiving this data, should sample this data upon the rising edge of RxPOHClk.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AG4	RXPOHCLK	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block - Path Overhead Output Port - Clock Output Signal:** This output pin, along with RxPOH, RxPOHFrame and RxPOHValid function as the AU-4/VC-4 Mapper POH Processor block - POH Output Port. These output pins function as the Clock Output signals for the AU-4/VC-4 Mapper POH Processor Block- POH Output Port. The RxPOH, RxPOHFrame and RxPOHValid output pins are updated upon the falling edge of this clock signal. As a consequence, the external circuitry should sample these signals upon the rising edge of this clock signal.
AE7	RXPOHFRAME	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block - Path Overhead Output Port - Frame Boundary Indicator:** This output pin, along with the RxPOH, RxPOHClk and RxPOHValid output pins function as the AU-4/VC-4 Mapper POH Processor Block - Path Overhead Output Port. These output pins will pulse "High" coincident with the very first POH byte (J1), of a given STS-1 frame, is being output via the corresponding RxPOH output pin.
AD9	RXPOHVALID	O	CMOS	**Receive AU-4/VC-4/STS-3c Mapper POH Processor Block - Path Overhead Output Port - Valid POH Data Indicator:** This output pin, along with RxPOH, RxPOHClk and RxPOHFrame function as the AU-4/VC-4 Mapper POH Processor block - Path Overhead Output port. These output pins will toggle "High" coincident with when valid POH data is being output via the RxPOH output pins. This output is updated upon the falling edge of RxPOHClk. Hence, external circuitry should sample these signals upon rising edge of RxPOHClk.
AF5 AG5 AF8	RxPOH_0 RxPOH_1 RxPOH_2	O	CMOS	**Receive SONET POH Processor Block - Path Overhead Output Port - Output Pin:** These output pins, along with the RxPOHClk_n, RxPOHFrame_n and RxPOHValid_n function as the Receive SONET POH Processor block - POH Output port. These pins serially output the POH data that have been received by each of the Receive SONET POH Processor blocks (via the incoming STS-3 data-stream). Each bit, within the POH bytes is updated (via these output pins) upon the falling edge of RxPOHClk_n. As a consequence, external circuitry receiving this data, should sample this data upon the rising edge of RxPOHClk_n.
AE8 AE9 AG6	RxPOHClk_0 RxPOHClk_1 RxPOHClk_2	O	CMOS	**Receive SONET POH Processor Block - Path Overhead Output Port - Clock Output Signal:** These output pins, along with RxPOH_n, RxPOHFrame_n and RxPOHValid_n function as the Receive SONET POH Processor block - POH Output Port. These output pins function as the Clock Output signals for the Receive SONET POH Processor block - POH Output Port. The RxPOH_n, RxPOHFrame_n and RxPOHValid_n output pins are updated upon the falling edge of this clock signal. As a consequence, the external circuitry should sample these signals upon the rising edge of this clock signal.

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
AF6A D10A E10	RxPOHFrame_0 RxPOHFrame_1 RxPOHFrame_2	O	CMOS	**Receive SONET POH Processor Block - Path Overhead Output Port - Frame Boundary Indicator:** These output pins, along with the RxPOH_n, RxPOHClk_n and RxPOHValid_n output pins function as the Receive SONET POH Processor Block - Path Overhead Output Port. These output pins will pulse "High" coincident with the very first POH byte (J1), of a given STS-1 frame, is being output via the corresponding RxPOH_n output pin.
AC10 AF7A C11	RxPOHValid_0 RxPOHValid_1 RxPOHValid_2	O	CMOS	**Receive SONET POH Processor Block - Path Overhead Output Port - Valid POH Data Indicator:** These output pins, along with RxPOH_n, RxPOHClk_n and RxPOHFrame_n function as the Receive SONET POH Processor block - Path Overhead Output port. These output pins will toggle "High" coincident with when valid POH data is being output via the RxPOH_n output pins. This output is updated upon the falling edge of RxPOHClk_n. Hence, external circuitry should sample these signals upon rising edge of RxPOHClk_n.
AD11	LOF	O	CMOS	**Receive STS-3 LOF (Loss of Frame) Indicator:** This output pin indicates whether or not the Receive STS-3 TOH Processor block (within the device) is currently declaring the LOF defect condition as described below. "Low" - Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the LOF defect condition. "High" - Indicates that the Receive STS-3 TOH Processor block is currently declaring the LOF defect condition.
AF9	SEF	O	CMOS	**Receive STS-3 SEF (Severed Errored Frame) Indicator:** This output pin indicates whether or not the Receive STS-3 TOH Processor block (within the device) is currently declaring the SEF defect condition as described below. "Low" - Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the SEF defect condition. "High" - Indicates that the Receive STS-3 TOH Processor block is currently declaring the SEF defect condition.
AG7	LOS	O	CMOS	**Receive STS-3 LOS (Loss of Signal) Defect Declared Indicator:** This output pin indicates whether or not the Receive STS-3 TOH Processor block (within the device) is currently declaring the LOS defect condition as described below. "Low" - Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the LOS defect condition. "High" - Indicates that the Receive STS-3 TOH Processor block is currently declaring the LOS defect condition.
GENERAL PURPOSE INPUT/OUTPUT				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
W25 AC27 V23 AB26 Y25 AC26 W24 AA25	GPI0_0 GPI0_1 GPI0_2 GPI0_3 GPI0_4 GPI0_5 GPI0_6 GPI0_7	I/O	TTL/ CMOS	General Purpose Input/Output pin: ***NOTE:*** *x = 0:7* This input pin can be configured to function as either an input or output pin by writing the appropriate value into Bit x (GPIO_DIR_x), within the Operation General Purpose Input/Output Direction Register - 0 (Address Location = 0x014B). If this pin is configured to be an input pin the state of this pin can be monitored by reading the state of Bit x (GPIO_x) within the Operation General Purpose Input/Output Register - Byte 0 (Address Location = 0x0147). If this pin is configured to be an output pin the state of this pin can be controlled by writing the appropriate value into Bit x (GPIO_x) within the Operation General Purpose Input/Output Register - Byte 0 (Address Location = 0x0147).
CLOCK INPUTS				
E7	REFCLK34	I	TTL	**E3 Reference Clock Input for the Jitter Attenuator within the DS3/E3 Mapper Block:** To operate any of the channels (within the XRT94L31) in the E3 Mode, apply a clock signal with a frequency of 34.368±20ppm to this input pin. This input pin functions as the timing reference for the DS3/E3/STS-1 Jitter Attenuator (within the DS3/E3 Mapper block) for E3 applications. For E3 Applications, the DS3/E3 Framer block will use this input clock signal, as a timing source in order to transmit the E3 AIS pattern, in the Egress Direction (e.g., from the XRT94L31 to the DS3/E3/STS-1 LIU IC). ***NOTE:*** *Connect this pin to GND if none of the channels of the XRT94L31 are to be operated in the E3 or if the XRT94L31 is to be operated in the SFM mode.*
D5	REFCLK51	I	TTL	**STS-1 Reference Clock Input for the Jitter Attenuator within the DS3/E3 Mapper Block.** To operate any of the channels (within the XRT94L31) in the STS-1/ STM-0 Mode, apply a clock signal with a frequency of 51.84MHz±20ppm to this input pin. This input pin functions as the timing reference for the DS3/E3/STS-1 Jitter Attenuator (within the DS3/E3 Mapper block) for STS-1 applications. ***NOTES:*** 1. *If the XRT94L31 is to be operated in the SFM Mode, apply a 12.288MHz±20ppm clock signal to this input pin.* 2. *If the user does not intend to operate any of the channels in the STS-1/STM-0 Mode, connect this input pin to GND.*

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
F7	REFCLK45	I	TTL	**DS3 Reference Clock Input for the Jitter Attenuator within the DS3/E3 Mapper Block:** To operate any of the channels of the XRT94L31 in the DS3 Mode, apply a clock signal with a frequency of 44.736±20ppm to this input pin. This input pin functions as the timing reference for the DS3/E3/STS-1 Jitter Attenuator (within the DS3/E3 Mapper block) for DS3 applications. For DS3 Applications, the DS3/E3 Framer block will use this input clock signal, as a timing source in order to transmit the DS3 AIS Pattern, in the Egress Direction (e.g., from the XRT94L31 to the DS3/E3/STS-1 LIU IC). If the user does not intend to operate any of the three (3) channels in the DS3 Mode, or if the user intends to configure the XRT94L31 to operate in the SFM Mode, connect this input pin to GND.
BOUNDARY SCAN				
F5	TDO	O	CMOS	Test Data Out: Boundary Scan Test data output
F4	TDI	I	TTL	**TEST Data In: Boundary Scan Test data input:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
D3	TRST	I	TTL	**JTAG Test Reset Input**
E4	TCK	I	TTL	**Test clock: Boundary Scan clock inputNote:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
E5	TMS	I	TTL	**Test Mode Select: Boundary Scan Mode Select inputNote:** ***NOTE:*** *This input pin should be pulled "Low" for normal operation.*
FILTERING CAPACITORS				
U6	RXCAPP	I	ANALOG	**External Loop Capacitor for Receive PLL:** This pin connects to the positive side of the external capacitor, which is used to minimize jitter peaking.
U5	RXCAPN	I	ANALOG	**External Loop Capacitor for Receive PLL:** This pin connects to the negative side of the external capacitor, which is used to minimize jitter peaking.
W6	RXCAPP_R	I	ANALOG	**External Redundant Loop Capacitor for Receive PLL:** This pin connects to the positive side of the external capacitor, which is used to minimize jitter peaking.
W5	RXCAPN_R	I	ANALOG	**External Redundant Loop Capacitor for Receive PLL:** This pin connects to the negative side of the external capacitor, which is used to minimize jitter peaking.
MISCELLANEOUS PINS				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
H5	REFSEL_L	I	TTL	**Clock Synthesizer Block Select:** This input pin is used to configure the Transmit SONET circuitry (within the XRT94L31) to use either of the following clock signals as its timing source.a. a. The Directly-Applied 19.44MHz clock signal, which is applied to the REFTTL input pin (P1) or,b. b. The output of the Clock Synthesizer block (within the chip). Setting this input pin "High" configures the Transmit SONET circuitry within the XRT94L31 to use the Clock Synthesizer block as its timing source. In this mode, the user can supply either a 19.44MHz, 38.88MHz, 51.84MHz or 77.76MHz clock signal to the REFTTL input pin. Setting this input pin "Low" by-passes the Clock Synthesizer block. In this case, the user MUST supply a 19.44MHz clock signal to the REFTTL input pin in order to insure proper performance.
K4	SFM	I	TTL	**Single Frequency Mode (SFM) Select:** This input pin is used to configure the three Jitter Attenuator (SONET/SDH De-Sync) blocks of the XRT94L31 to operate in the Single-Frequency Mode (SFM). If the XRT94L31 has been configured to operate in the SFM Mode, then the user only needs to supply a 12.288MHz clock signal to the REFCLK51 input pin. In this case, the user does not need to supply a 44.736MHz clock signal to the REFCLK45 input pin, nor a 34.368MHz clock signal to the REFCLK34 input pin. The SFM PLL (within the XRT94L31) will internally synthesize the appropriate 44.736MHz, 34.368MHz or 51.84MHz clock signals, and will route these signals to the appropriate channels (within the chip) depending upon the data rate that they are configured to operate in. Setting this input pin to a logic "Low" disables the Single-Frequency Mode. In this mode, the user must supply all of the appropriate frequencies to the REFCLK34, REFCLK45 and REFCLK51 input pins. Setting this input pin to a logic "High" configures the XRT94L31 to operate in the Single-Frequency Mode.
J3	Test Mode	I	TTL	**Test Mode Input Pin:** Connect this input pin "Low" for normal operation.
G2	FL_TSTCLK	O	CMOS	**JA Testing Clock:** This pin is used for JA testing purposes.
J2	ANALOG	O	ANALOG	**Analog Output Pin:** This output analog pin is used for testing purposes.
N1	VDCTST1	O	ANALOG	**DC Test Pin:** This pin is used for internal DC test, for example, it can be used to test for DC current, DC voltage.
N2	VDCTST2	O	ANALOG	**DC Test Pin:** This pin is used for internal DC test, for example, it can be used to test for DC current, DC voltage.
NO-CONNECT PINS				
K1	N/C			
AA1	N/C			

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
V3	N/C			
AB1	N/C			
AA2	N/C			
AC1	N/C			
R1	N/C			
AB2	N/C			
AC2	N/C			
T1	N/C			
AC4	N/C			
AB5	N/C			
AD4	N/C			
AC5	N/C			
AB7	N/C			
AC6	N/C			
AC22	N/C			
AD24	N/C			
AB21	N/C			
AC23	N/C			
AB23	N/C			
AC24	N/C			
AA23	N/C			
E24	N/C			
F23	N/C			
D24	N/C			
E23	N/C			
F21	N/C			
E22	N/C			
VDD (3.3V)				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
N23 N2 5V5 H 2L2 K3 H1 L5 U4 N3 T5 M5	Analog VDD Pins	_		

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
U3 R2 R6 C2 C1 J6 K6 W3 Y3 AE1 AE2 AF3 AB9 AB10 AB11 AB17 AB18 AB19 AF25 AE26 W22 V22 U22 L22 K22 J22 C27 C26 B25 A25 F19 F18 F17 F11 F10 F9 A3 B3 D4 C4	Digital VDD			
GROUND				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
G6	Digital Ground			
C3				
A1				
B1				
AF1				
AF2				
AA6				
AB6				
AE3				
AG1				
AG2				
AB13				
AB14				
AB15				
AG26				
AF26				
AB22				
AA22				
AE25				
AG27				
AF27				
T22				
R22				
P22				
N22				
M22				
B27				
B26				
G22				
F22				
C25				
A27				
A26				
F15				
F14				
F13				
A2B				
2F6				
V2				
W4				
Y6				
Y5				
Y4				
E6				
V4				
R5				
R3				
P4				

PIN DESCRIPTION OF THE XRT94L31 (REV. B)

PIN #	SIGNAL NAME	I/O	TYPE	DESCRIPTION
V6 L6 T4 N24 N26 R4 F1 K2 G1 L1 M6 N4 T6 J1	Analog Ground			

1.0 ELECTRICAL CHARACTERISTIC INFORMATION FOR THE XRT94L31 DEVICE

1.1 DC ELECTRICAL CHARACTERISTIC INFORMATION

TABLE 1: DC CHARACTERISTIC (APPLIES TO ALL TTL-LEVEL INPUT AND CMOS LEVEL OUTPUT PINS - AMBIENT TEMPERATURE = 25°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN	MAX	UNITS
VDDQ	I/O Supply Voltage			3.135	3.465	V
VIH	High-Level Input Voltage	VOUT ³ VOH(min)		2.0	VDD + 0.3	V
VIL	Low-Level Input Voltage	VOUT < VOL (max)		-0.3	0.3*VDD	V
VOH	High-Level Output Voltage	VDD = MINVIN = VIH	IOH = -2mA	1.9		V
VOL	Low-Level Output Voltage	VDD = MINVIN = VIL	IOL = 2mA		0.6	V
II	Input Current	VDD = MAX VIN = VDD or GND			±15	mA

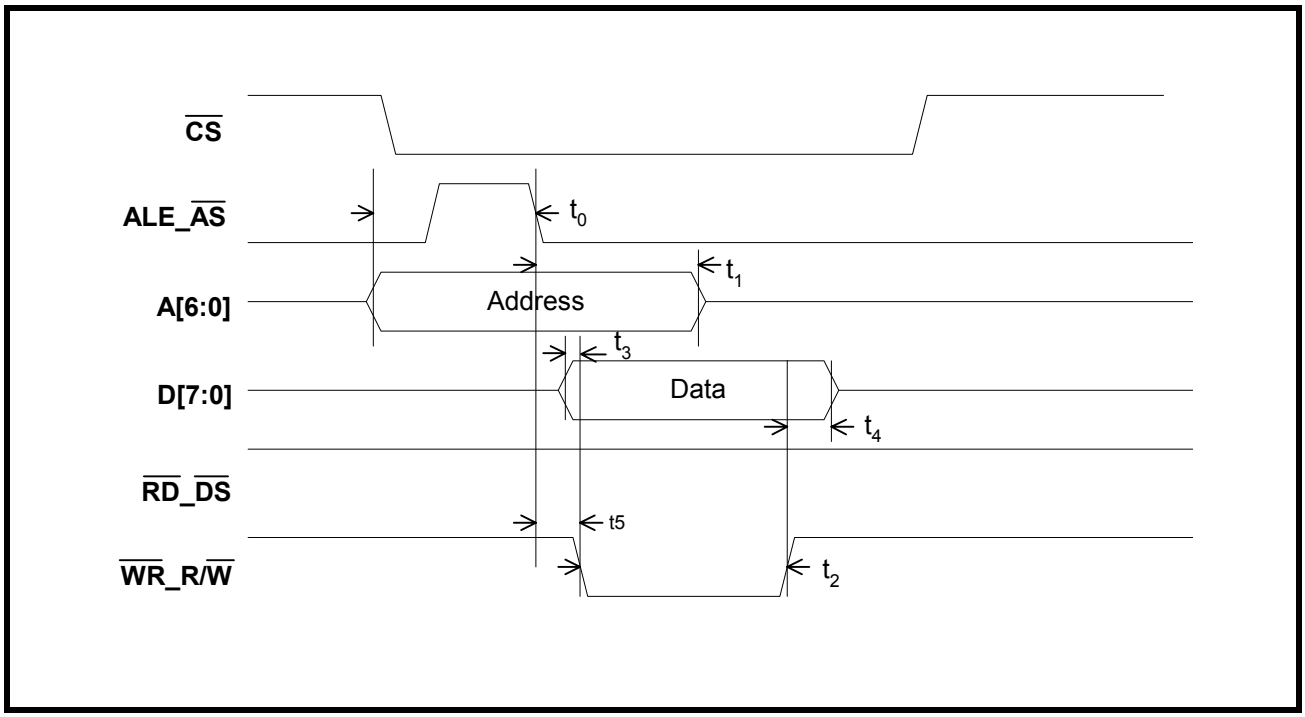
TABLE 2: DC CHARACTERISTICS (APPLIES TO ALL LVPECL INPUT AND OUTPUT PINS)

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNITS
VIH	High-Level Input Voltage			VDD + 0.4	V
VIL	Low-Level Input Voltage		-0.4		V
VICM	Input Common Mode Voltage		1.0	VDD	V
VINDIFF	Differential Input Voltage		0.2		V
VOH	High Level Output Voltage		VDD - 1.08	VDD - 0.88	V
VOL	Low-Level Output Voltage		VDD - 1.88	VDD - 1.62	V
VOUTDIFF	Differential Output Voltage		1.18	2.12	V

1.2 AC ELECTRICAL CHARACTERISTIC INFORMATION - Microprocessor Interface Timing

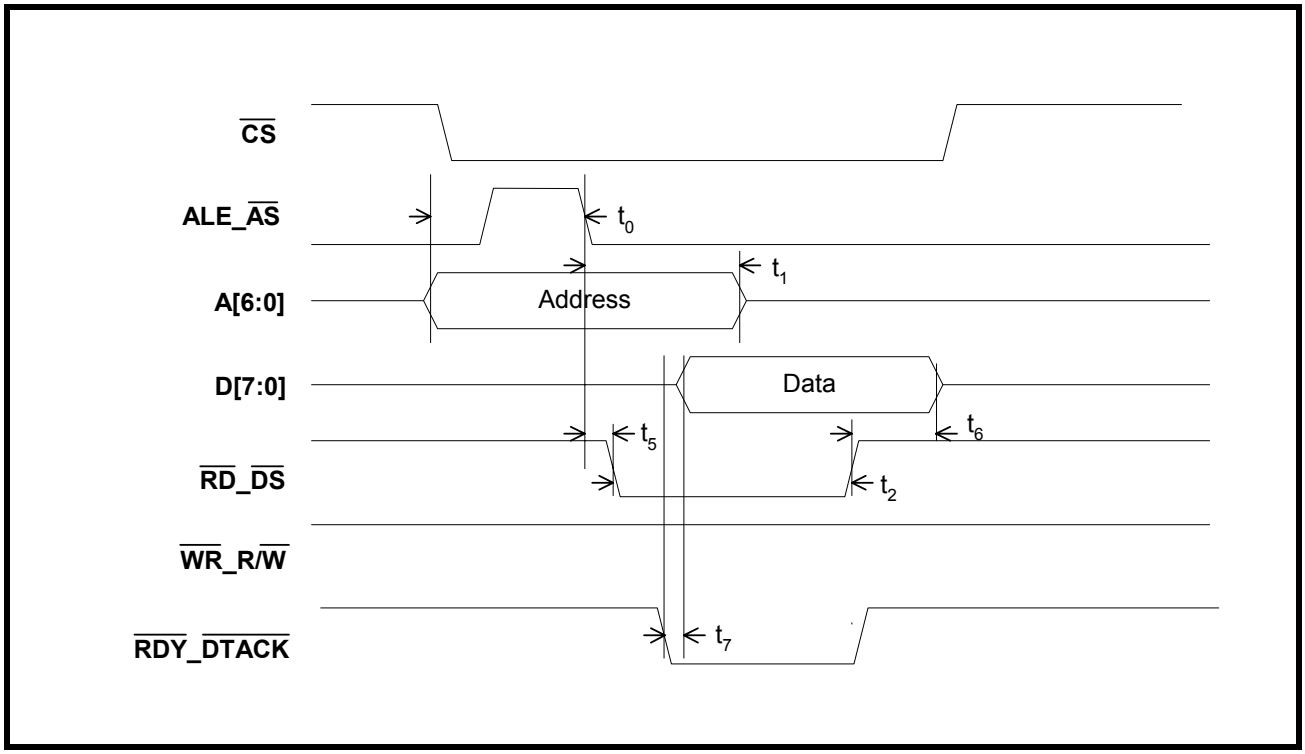
1.2.1 MICROPROCESSOR INTERFACE TIMING - ASYNCHRONOUS INTEL MODE

FIGURE 2. ASYNCHRONOUS MODE 1 - INTEL TYPE PROGRAMMED I/O TIMING (WRITE CYCLE)



NOTE: The values for t0 through t7, within this figure can be found in Table 3.

FIGURE 3. ASYNCHRONOUS MODE 1 - INTEL TYPE PROGRAMMED I/O TIMING (READ CYCLE)



NOTE: The values for t0 through t7, within this figure can be found in Table 3.

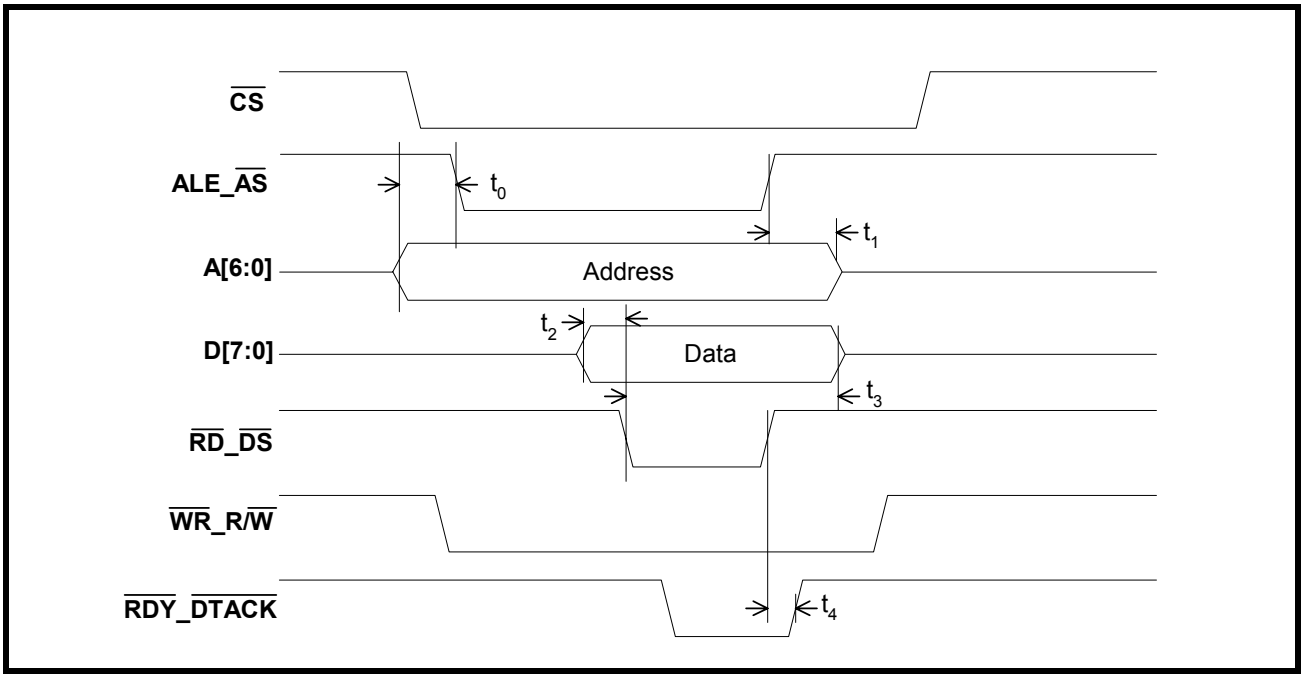
TABLE 3: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE INTEL ASYNCHRONOUS MODE

TIMING	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t0	Address setup time to pALE low	4	-	-	ns
t1	Address hold time from pALE low	4	-	-	ns
t2	pRD_L, pWR_L pulse width	320	-	-	ns
t3	Data setup time to pWR_L low	0	-	-	ns
t4	Data hold time from pWR_L high	0	-	-	ns
t5	pALE low to pRD_L, pWR_L low	5	-	-	ns
t6	Data invalid from pRD_L high	4	-	-	ns
t7	Data valid from pRDY_L low	-	-	0	ns
t8	pRDY inactive from pRD_L inactive	3		9	ns

NOTE: Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.

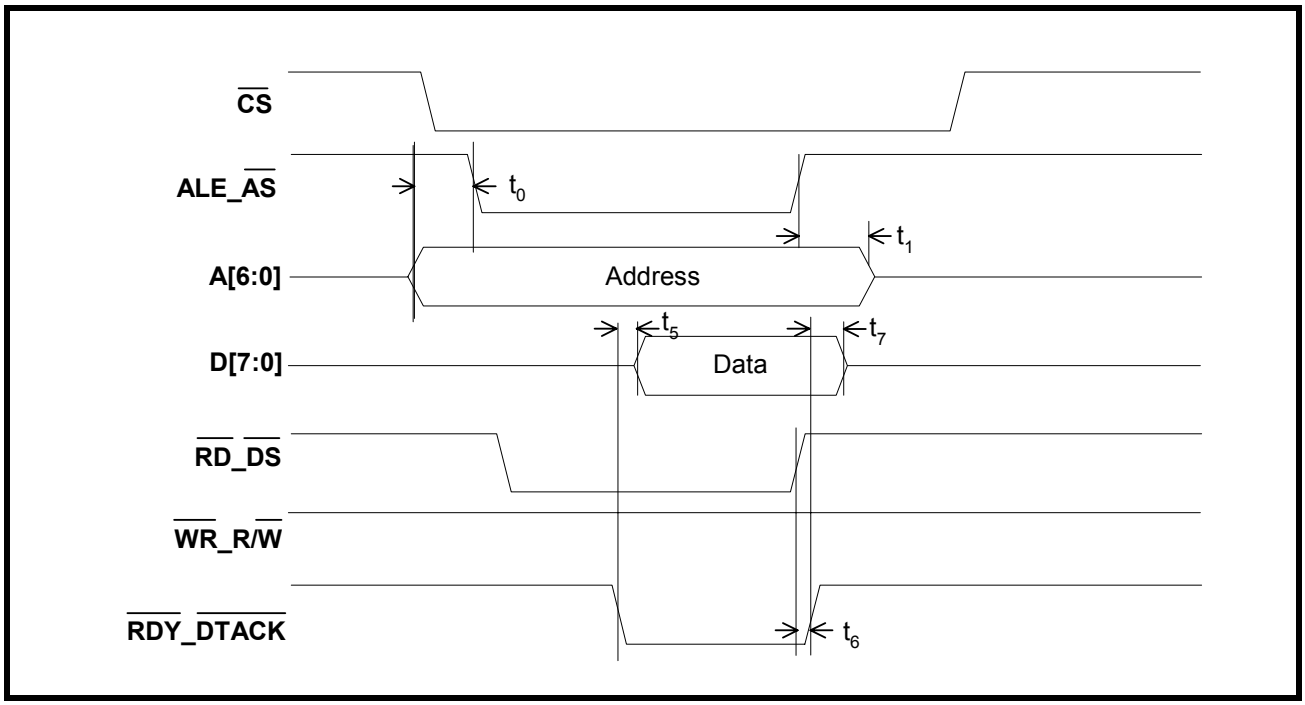
1.2.2 MICROPROCESSOR INTERFACE TIMING - ASYNCHRONOUS MOTOROLA (68K) MODE

FIGURE 4. ASYNCHRONOUS MODE 2 - MOTOROLA (68K) PROGRAMMED I/O TIMING (WRITE CYCLE)



NOTE: The values for t0 through t7 can be found in Table 4.

FIGURE 5. ASYNCHRONOUS MODE 2 - MOTOROLA (68K) PROGRAMMED I/O TIMING (READ CYCLE)



NOTE: The values for t0 through t7 can be found in **Table 4**.

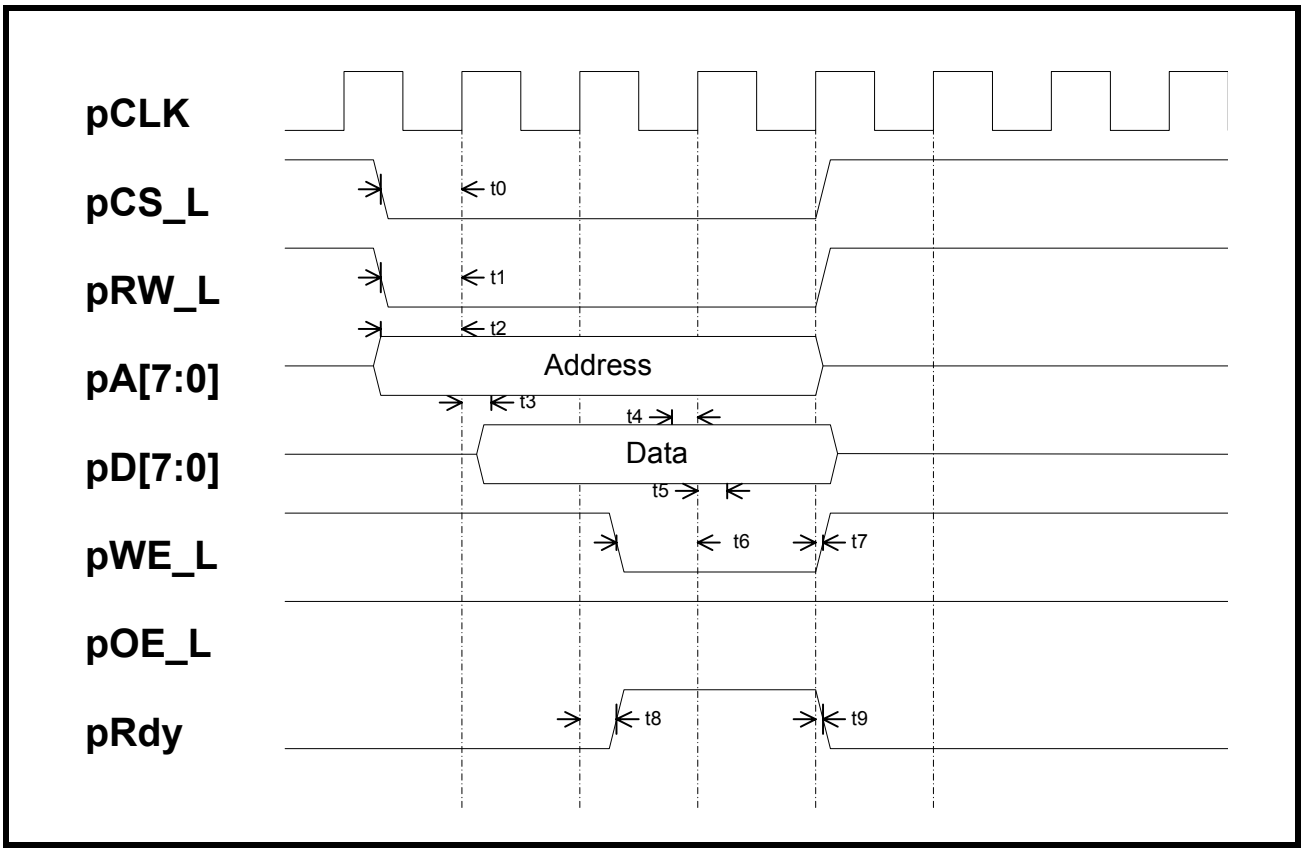
TABLE 4: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE WHEN CONFIGURED TO OPERATE IN THE MOTOROLA (68K) ASYNCHRONOUS MODE

TIMING	DESCRIPTION	MIN.	TYP.	MAX	UNITS
t0	Address setup time to pALE low	6	-	-	ns
t1	Address hold time to pALE high	6	-	-	ns
t2	Data setup time to pDS_L low	0	-	-	ns
t3	Data hold time to pDS_L low	160	-	-	ns
t4	pDS_L high to pRDY_L high (Write Cycle)	-	-	16	ns
t5	pRDY_L low to Data valid	-	-	15	ns
t6	pDS_L high to pRDY_L high (Read Cycle)	-	-	16	ns
t7	pRDY_L high to Data invalid	3	-	-	ns

NOTE: Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.

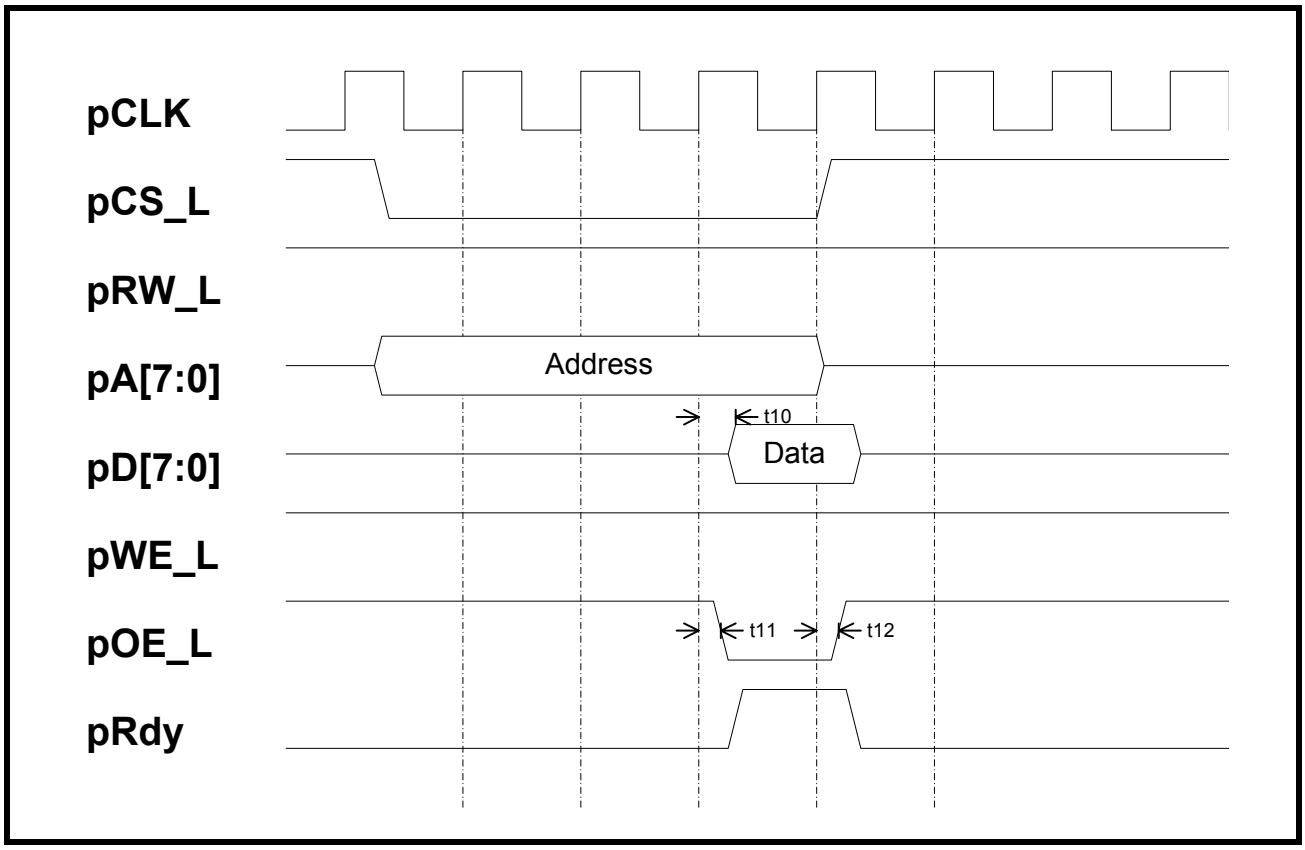
1.2.3 MICROPROCESSOR INTERFACE TIMING - POWER PC 403 SYNCHRONOUS MODE

FIGURE 6. SYNCHRONOUS MODE 3 - IBM POWERPC 403 INTERFACE TIMING (WRITE CYCLE)



NOTE: *The value for t0 through t12 can be found in* **Table 5**.

FIGURE 7. SYNCHRONOUS MODE 3 - IBM POWERPC 403 INTERFACE TIMING (WRITE CYCLE)



NOTE: The value for t0 through t12 can be found in **Table 5**.

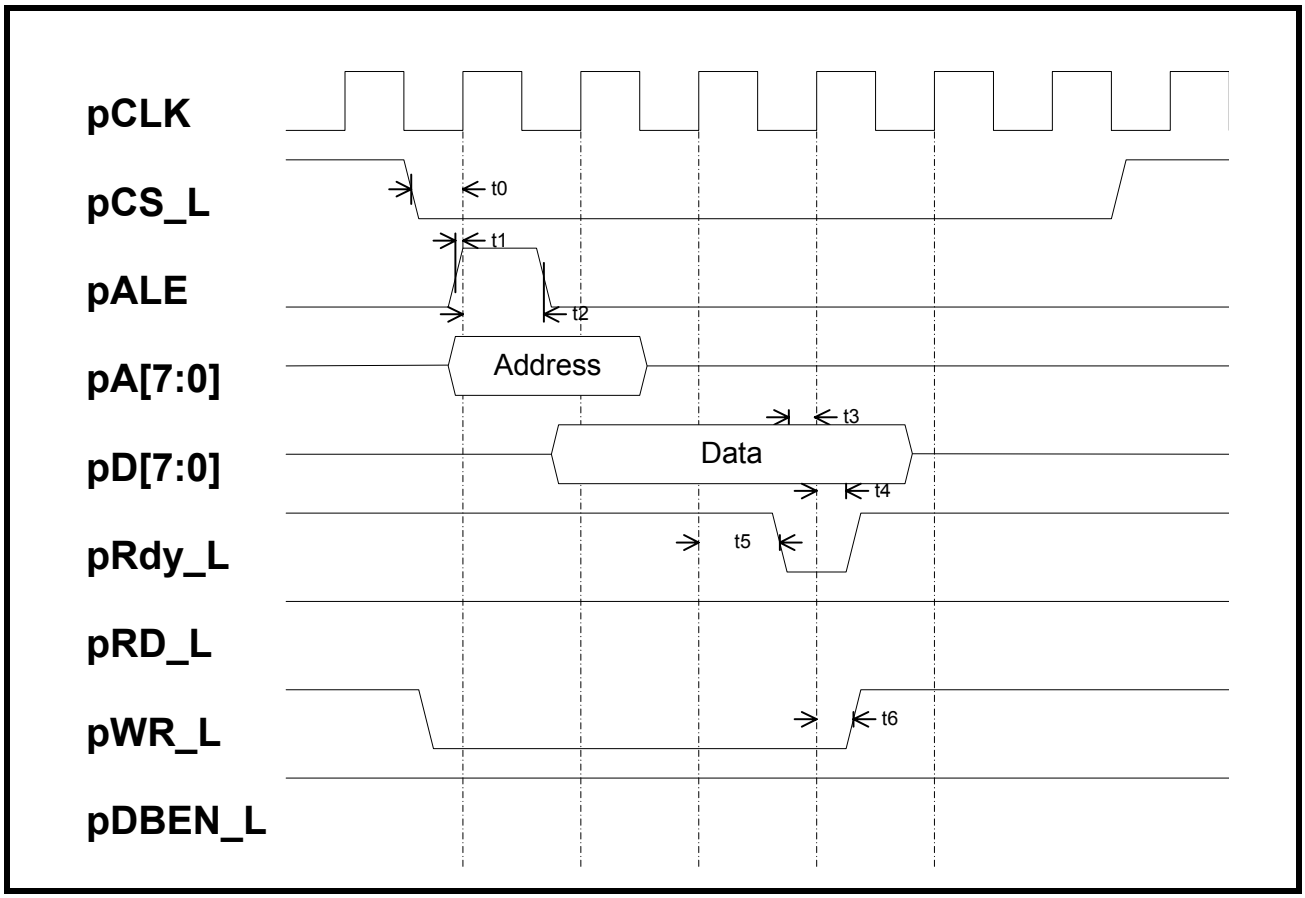
TABLE 5: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

TIMING	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t0	pCS_L low to PCLK high	4	-	-	ns
t1	pRW_L low to PCLK high	9	-	-	ns
t2	Address setup time to PCLK high	4	-	-	ns
t3	Address hold time from PCLK high	2	-	-	ns
t4	Data setup time (WRITE cycle)	4	-	-	ns
t5	Data hold time (WRITE cycle) from PCLK High	0	-	-	ns
t6	pWE_L low to Clock high	4	-	-	ns
t7	Clock high to pWE_L high from PCLK high	0	-	-	ns
t8	Clock high to pRDY high	4.4	-	10.5	ns
t9	Clock high to pRDY low	4.2	-	10.4	ns
t10	Clock high to Data valid (READ cycle)	-	-	11	ns
t11	Clock high to pOE_L low	11	-	-	ns
t12	Clock high to pOE_L high	1.5	-	4.1	ns

NOTE: *Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.*

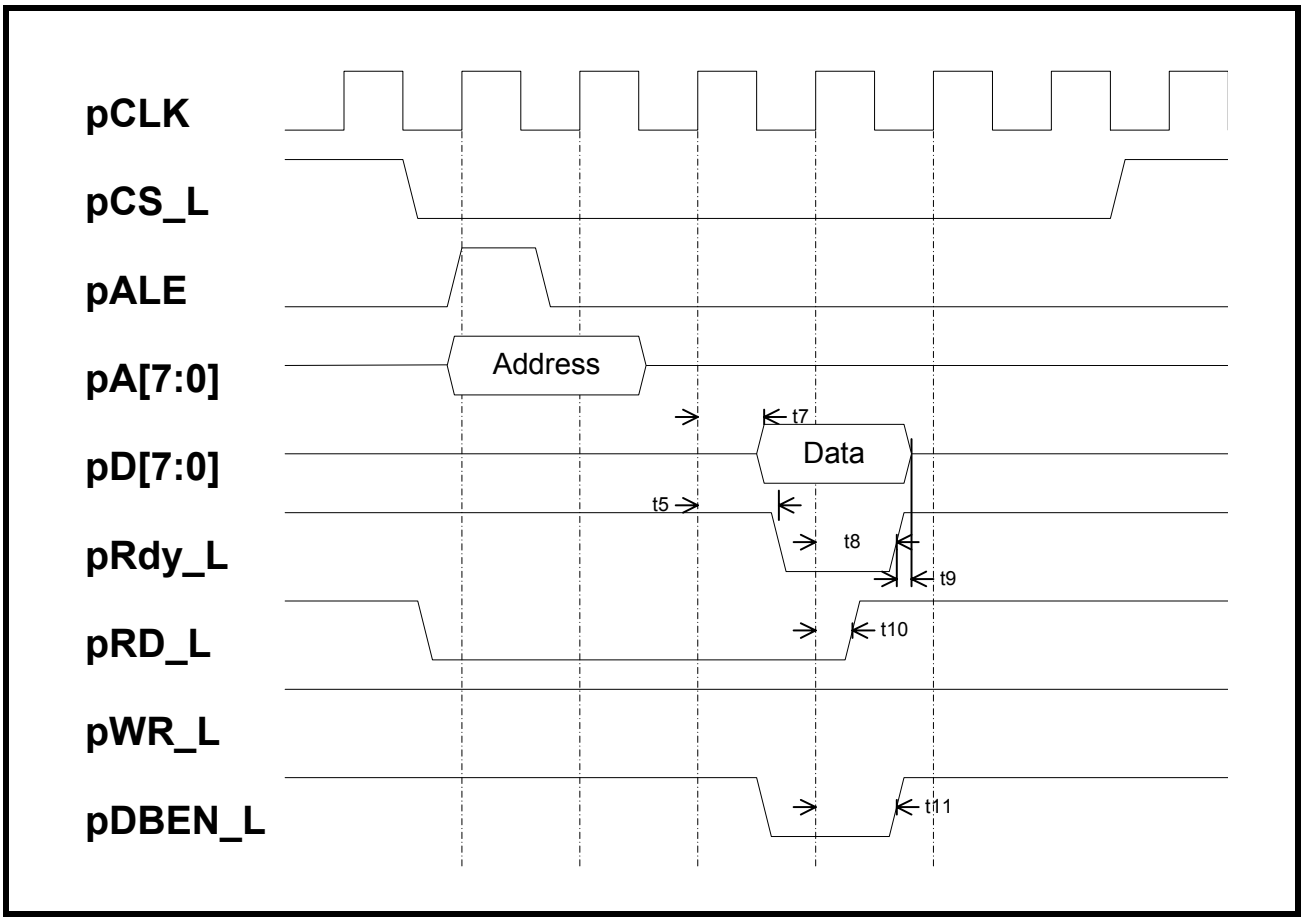
1.2.4 MICROPROCESSOR INTERFACE TIMING - IDT3051/52 MODE

FIGURE 8. SYCHRONOUS MODE 4 - IDT3051/52 INTERFACE TIMING (WRITE CYCLE)



NOTE: The values for t0 through t11 can be found in **Table 6**.

FIGURE 9. SYCHRONOUS MODE 4 - IDT3051/52 INTERFACE TIMING (READ CYCLE)



NOTE: The values for t0 through t11 can be found in **Table 6**.

TABLE 6: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

TIMING	DESCRIPTION	MIN.	TYP.	MAX	UNITS
t0	pCS_L low to Clock high	6	-	-	ns
t1	pALE high to Clock high	1	-	-	ns
t2	Clock high to pALE low	6	-	-	ns
t3	Data setup time (WRITE cycle)	-	-	N/N	ns
t4	Data hold time (WRITE cycle)	-	-	N/N	ns
t5	Clock high to pRDY_L low	-	-	11	ns
t6	Clock high to pWR_L high	6	-	-	ns
t7	Clock high to Data valid (READ cycle)	-	-	N/N	ns
t8	Clock high to pRDY_L high	-	-	11	ns
t9	pRDY_L high to Data invalid	0	-	-	ns

TABLE 6: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE IBM POWER PC403 MODE

TIMING	DESCRIPTION	MIN.	TYP.	MAX	UNITS
t10	Clock high to pRD_L high	11	-	-	ns
t11	Clock high to pDBEN_L high	10	-	-	ns

NOTE: *Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.*

1.2.5 MICROPROCESSOR INTERFACE TIMING - MPC860 MODE

FIGURE 10. MPC860 MODE - TIMING (WRITE CYCLE)

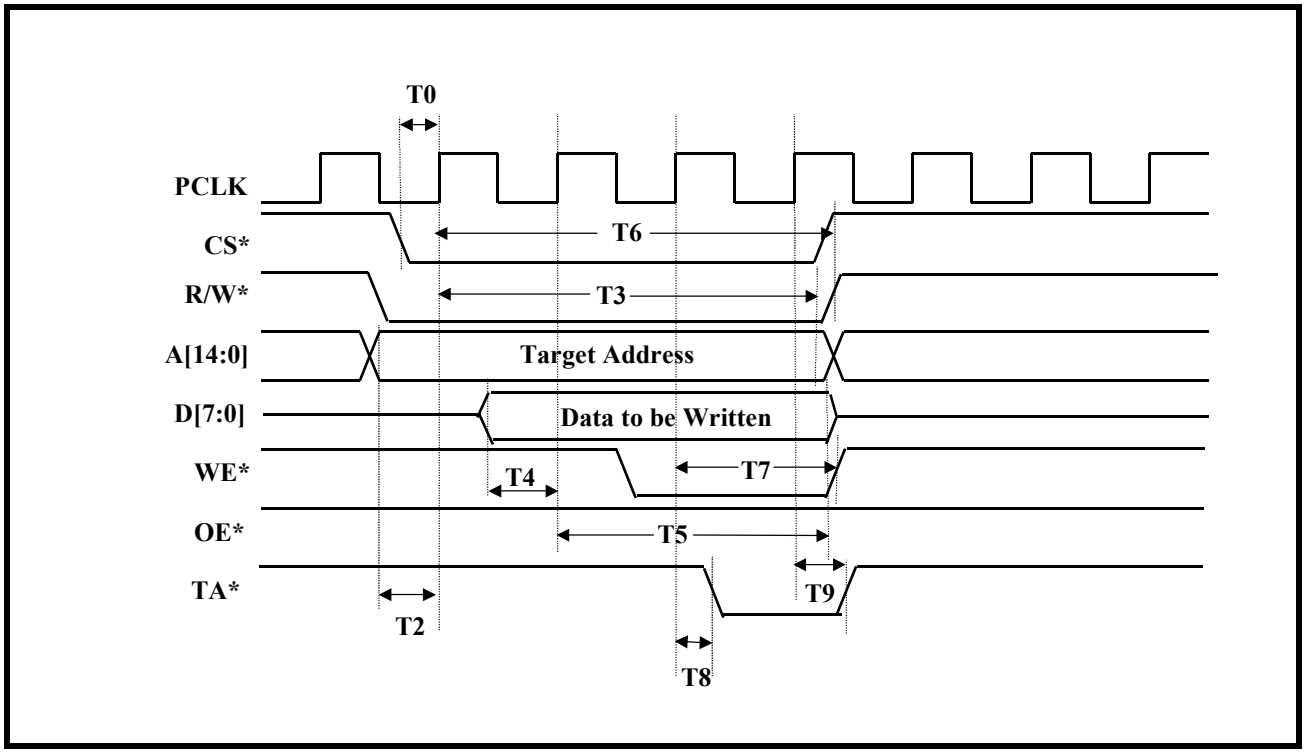
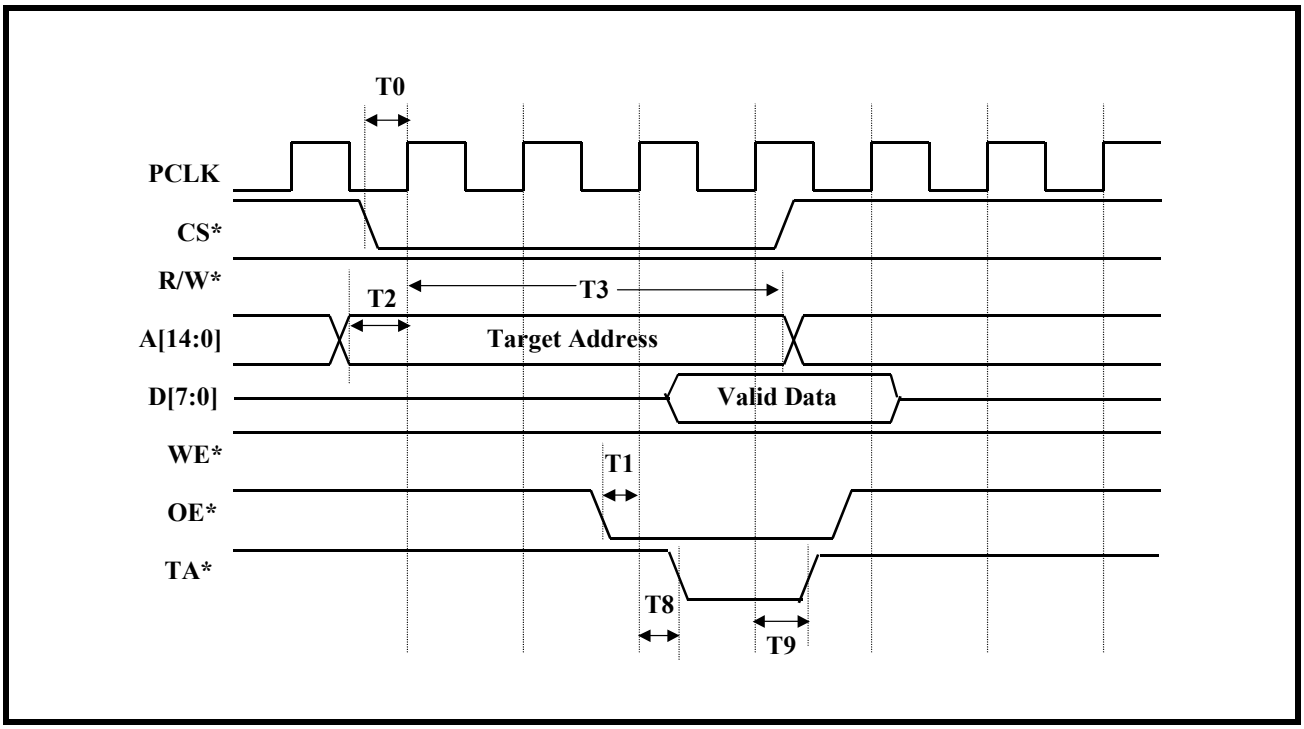


FIGURE 11. MPC860 MODE - TIMING (READ CYCLE)



NOTE: The value for t0 through t9 can be found in **Table 7**.

TABLE 7: TIMING INFORMATION FOR THE MICROPROCESSOR INTERFACE, WHEN CONFIGURED TO OPERATE IN THE MPC860 MODE

TIMING	DESCRIPTION	MIN.	TYP.	MAX	UNITS
T0	pCS* low to PCLK high set-up time	4	-	-	ns
T1	OE* low to PCLK high set-up time	4			ns
T2	A[14:0] set-up time to rising edge of PCLK	4			ns
T3	A[14:0] hold time from rising edge of PCLK	2			ns
T4	Data setup time to rising edge of PCLK (WRITE cycle)	4	-	N/A	ns
T5	Data hold time from rising edge of PCLK (WRITE cycle)	0	-	N/A	ns
T6	R/W* Active hold-time from rising edge of PCLK	4			ns
T7	WE* Active hold-time from rising edge of PCLK	0			ns
T8	Rising edge of PCLK to TA* Active (LOW) Delay	4.13	-	10.07	ns
T9	Rising edge of PCLK to TA* In-Active (HIGH) Delay	4.31	-	10.09	ns
T10	OE* Inactive to Data Invalid Delay	1.66		4.33	ns

NOTE: Test Conditions: TA = 25°C, VCC = 3.3V±5% and 2.5V±5%, unless otherwise specified.

1.3 STS-3/STM-1 TELECOM BUS INTERFACE TIMING INFORMATION

1.3.1 STS-3/STM-1 Telecom Bus Interface Timing Information

This section presents the timing requirements for the STS-3/STM-1 Telecom Bus Interface. In particular this section prsents the following.

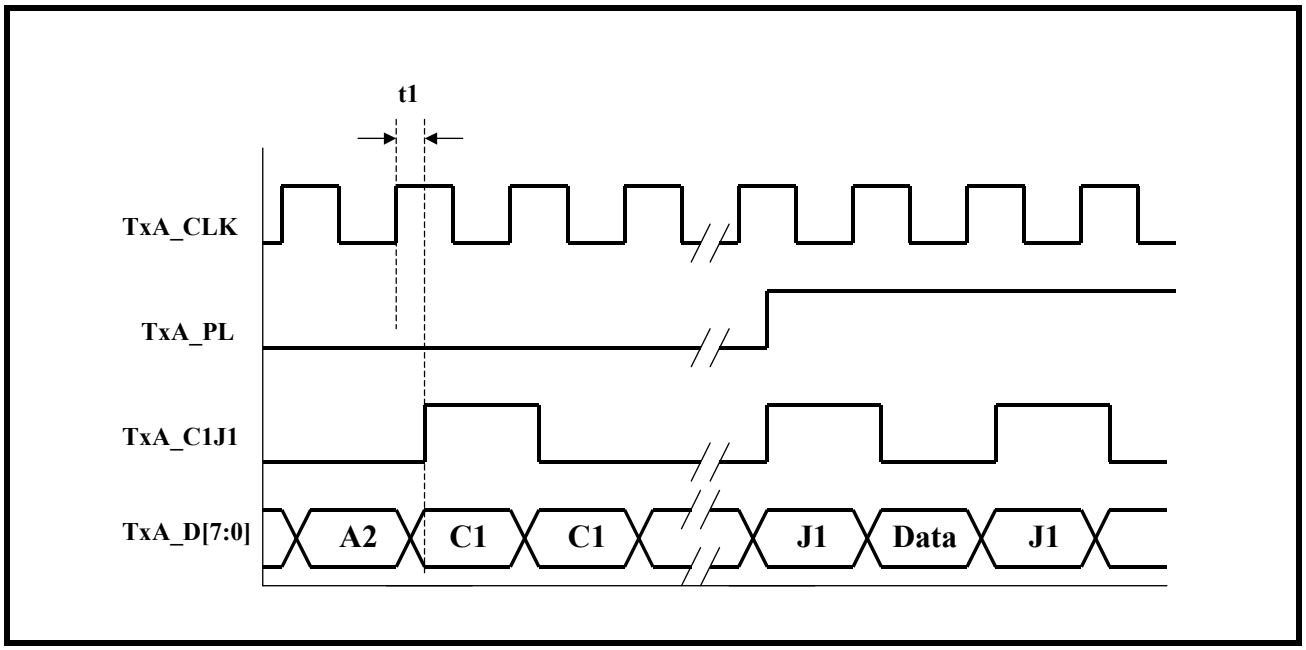
1. Identifies which edge of TxA_CLK in which the TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP output pins are updated on.
2. The clock to output delays (from the rising edge of TxA_CLK to the instant that the TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP output pins are updated.
3. Identifies which edge of RxD_CLK that the RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP input pins are sampled on.
4. The set-up time requirements (from an update in the RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP input signals to the rising edge of RxD_CLK).
5. The hold-time requirements (from the rising edge of RxD_CLK to a change in the RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP input signals)

1.3.1.1 The Transmit STS-3/STM-1 Telecom Bus Interface Timing

In the Transmit STS-3/STM-1 Telecom Bus Interface, all of the signals (which are output via this Bus Interface) are updated upon the rising edge of TxA_CLK (19.44MHz clock signal).

Figures 12 and 13 presents an illustration of the waveforms of the signals that will be output via the Transmit STS-3/STM-1 Telecom Bus Interface, as well as the timing parameter (t1).

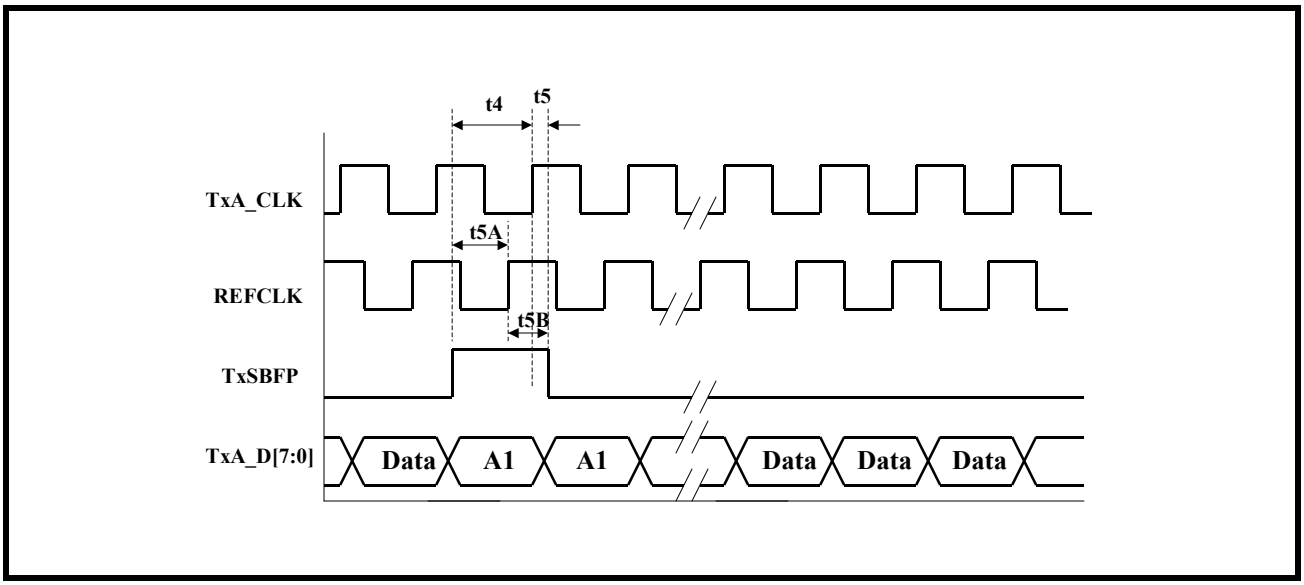
FIGURE 12. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STS-3/STM-1 TELECOM BUS INTERFACE.



NOTE: The value for t1 can be found in Table 8.

The TxSBFP input signal is sampled upon the rising edge of TxA_CLK by the Transmit STS-3/STM-1 Telecom Bus Interface circuitry, as illustrated below in Figure 13.

FIGURE 13. AN ILLUSTRATION OF THE TIMING RELATIONSHIPS BETWEEN THE TXSBFP INPUT PIN AND THE TXA_CLK OUTPUT PIN WITHIN THE TRANSMIT STS-3/STM-1 TELECOM BUS INTERFACE



NOTE: The value for t4, t5, t5A and t5B can be found in Table 8.

TABLE 8: TIMING INFORMATION FOR THE TRANSMIT STS-3/STM-1 TELECOM BUS INTERFACE

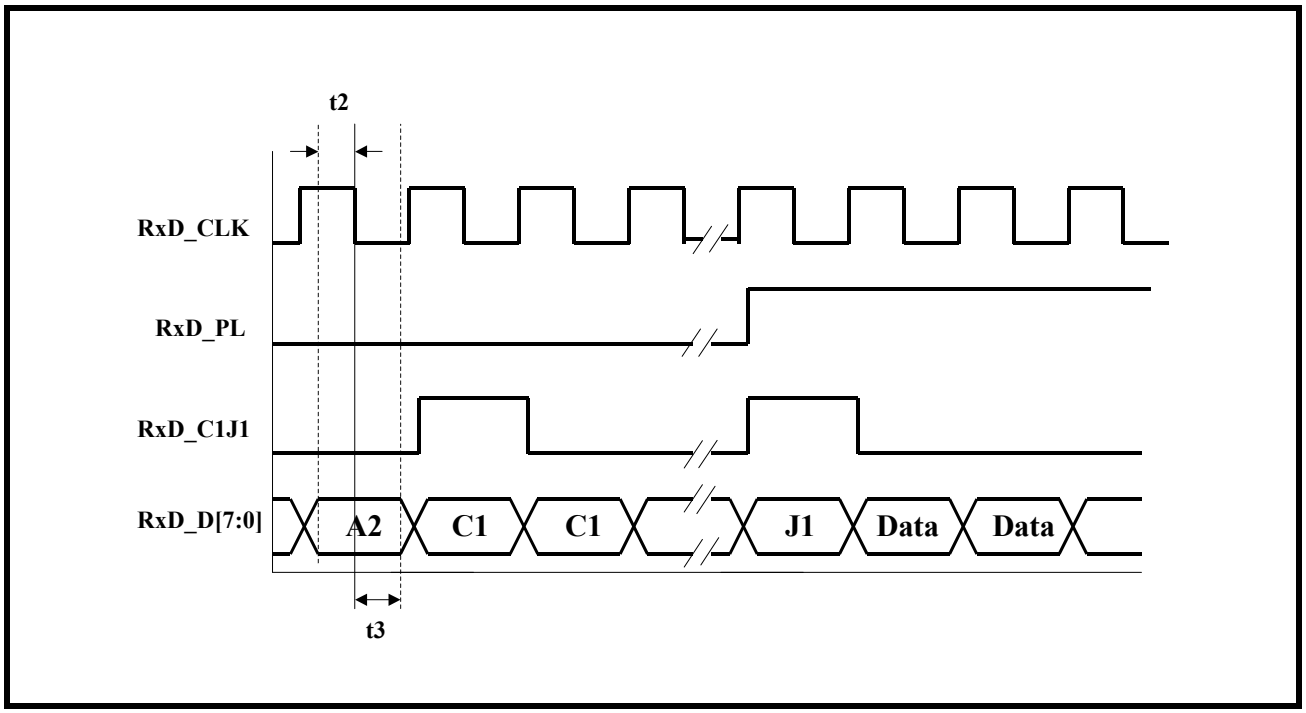
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t1	Rising edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1 and TxA_DP	1.7ns		7.7ns
t4	TxSBFP Set-up time to rising edge of TxA_CLK	8.5ns		
t5	TxA_CLK rising edge to TxSBFP Hold time	0ns		
t5A	TxSBFP Set-up time to rising edge of REFCLK	5ns		
t5B	Rising edge of REFCLK to TxSBFP Hold Time	0ns		

1.3.1.2 The Receive STS-3/STM-1 Telecom Bus Interface Timing

In the Receive STS-3/STM-1 Telecom Bus Interface, all of the signals (which are input via this Bus Interface) are sampled upon the rising edge of RxD_CLK (19.44MHz clock signal).

Figure 14 presents an illustration of the waveforms and the timing parameters (t2 and t3) of the signals that will be received by the Receive STS-3/STM-1 Telecom Bus Interface.

FIGURE 14. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE RECEIVE STS-3/STM-1 TELECOM BUS INTERFACE



NOTE: The value for t2 and t3 can be found in Table 9.

TABLE 9: TIMING INFORMATION FOR THE RECEIVE STS-3/STM-1 TELECOM BUS INTERFACE

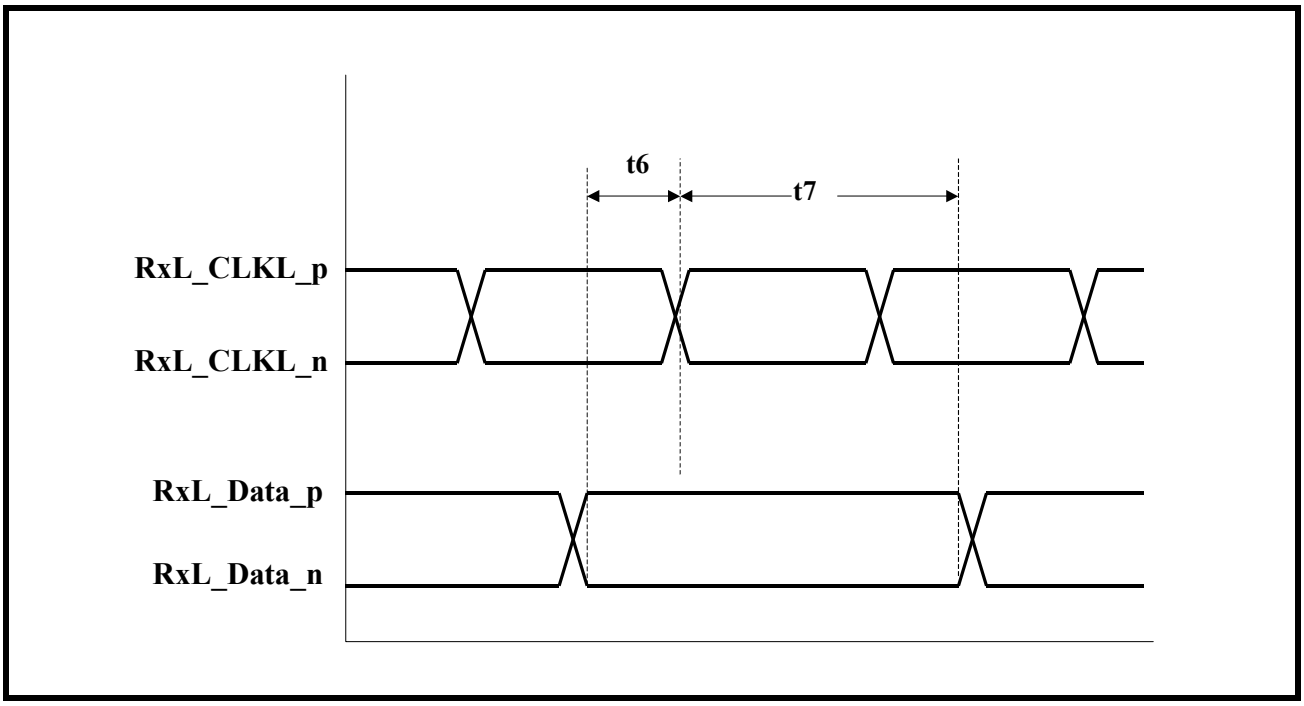
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t2	RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP to falling edge of RxD_CLK set-up time requirements	4 ns		
t3	Falling edge of RxD_CLK to RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP hold time requirements	0 ns		

1.3.2 STS-3/STM-1 PECL INTERFACE TIMING INFORMATION

1.3.2.1 The Receive STS-3/STM-1 PECL Interface Timing

The Receive STS-3/STM-1 PECL Interface block samples the incoming STS-3/STM-1 signal (which is present on the RxL_Data_p/RxL_Data_n input pins) upon the rising edge of the RxL_CLKL_p/RxL_CLKL_n input clock signal.

FIGURE 15. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE RECEIVE STS-3/ STM-1 PECL INTERFACE



NOTE: **Table 10** *presents information on the Timing parameters for the Receive STS-3/STM-1 PECL Interface*

TABLE 10: TIMING INFORMATION FOR THE RECEIVE STS-3/STM-1 PECL INTERFACE

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t6	RxL_DATA to rising edge of RxL_CLKL set-up time requirements	200ps		
t7	Rising edge of RxL_CLKL to RxL_DATA hold time requirements	200ps		

These timing requirements apply to both the Primary and the Redundant Receive STS-3/STM-1 PECL Interface blocks.

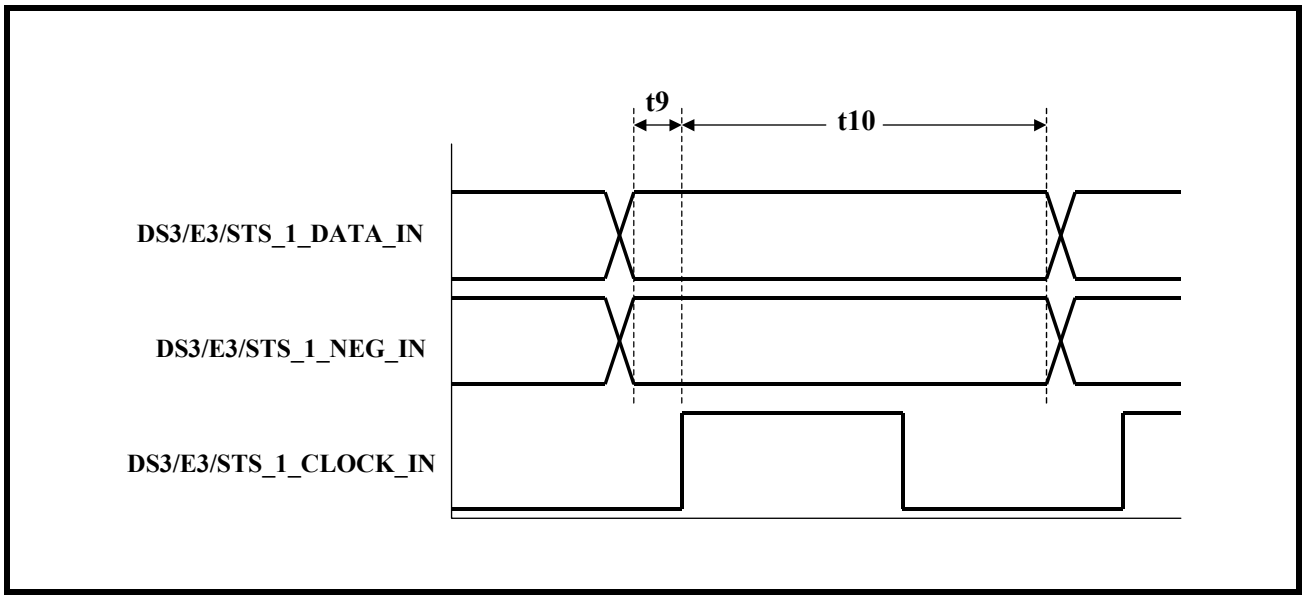
1.3.3 DS3/E3/STS-1 LIU INTERFACE TIMING INFORMATION

1.3.3.1 Ingress DS3/E3/STS-1 Interface Timing

The user should be aware of the following things about the Ingress DS3/E3/STS-1 Interface Timing.

1. If a given channel is configured to operate in the DS3/E3 Mode, then the DS3/E3 Framer block can be configured to sample the DS3/E3/STS_1_DATA_IN and the DS3/E3/STS_1_NEG_IN input pins upon either the rising or falling edge of DS3/E3/STS_1_CLOCK.
2. If a given channel is configured to operate in the STS-1/STM-0 Mode, then the Receive STS-1 TOH Processor block will be operating in the Single-Rail Mode (e.g., the Receive STS-1 TOH Processor block will ONLY sample the DS3/E3/STS_1_DATA_IN input signal. It will not sample the DS3/E3/ STS_1_NEG_IN input signal.
3. Further, if a given channel is configured to operate in the STS-1/STM-0 Mode, then the Receive STS-1 TOH Processor block can be configured to sample the DS3/E3/STS_1_DATA_IN input signal, upon either the **rising or falling edge** of DS3/E3/STS_1_CLOCK_IN.

FIGURE 16. AN ILLUSTRATION OF THE WAVEFORMS OF THE DS3/E3/STS-1 SIGNALS THAT ARE INPUT TO THE DS3/E3/STS-1 LIU INTERFACE (IN THE INGRESS DIRECTION)



NOTE: The values for t9 and t10 are presented in Tables 11, 12, 13 *and* 14.

1.3.4 Ingress Timing for DS3/E3 Applications

Table 11 presents information on the Timing parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Ingress Direction) for DS3/E3 Applications, and when the DS3/E3 Framer block has been configured to sample the DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_NEG_IN signals upon the **rising edge** of DS3/E3/STS_1_CLOCK_IN.

TABLE 11: TIMING INFORMATION FOR THE INGRESS DS3/E3/STS-1 LIU INTERFACE FOR DS3/E3 APPLICATIONS (RISING EDGE OF DS3/E3/STS_1_CLOCK_IN)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t9	DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_NEG_IN to rising edge of DS3/E3/STS_1_CLOCK_IN set-up time requirements	4ns		
t10	Rising edge of DS3/E3/STS_1_CLOCK_IN to DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_NEG_IN Hold time requirements	0ns		

Table 12 presents information on the Timing parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Ingress Direction) for DS3/E3 Applications, and when the DS3/E3 Framer block has been configured to sample the DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_NEG_IN signals upon the **falling edge** of DS3/E3/STS_1_CLOCK_IN.

TABLE 12: TIMING INFORMATION FOR THE INGRESS DS3/E3/STS-1 LIU INTERFACE FOR DS3/E3 APPLICATIONS(FALLING EDGE OF DS3/E3/STS_1_CLOCK_IN)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t9	DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_NEG_IN to falling edge of DS3/E3/STS_1_CLOCK_IN set-up time requirements	4ns		
t10	Falling edge of DS3/E3/STS_1_CLOCK_IN to DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_NEG_IN Hold time requirements	0ns		

1.3.5 Ingress Timing for STS-1/STM-0 Applications

Table 13 presents information on the Timing parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Ingress Direction) for STS-1/STM-0 Applications and when the Receive STS-1 TOH Processor block has been configured to sample the DS3/E3/STS_1_DATA_IN signal upon the **rising edge** of DS3/E3/STS_1_CLOCK_IN.

TABLE 13: TIMING INFORMATION FOR THE INGRESS DS3/E3/STS-1 LIU INTERFACE FOR STS-1/STM-0 APPLICATIONS(RISING EDGE OF DS3/E3/STS_1_CLOCK_IN)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t9	DS3/E3/STS_1_DATA_IN to rising edge of DS3/E3/STS_1_CLOCK_IN set-up time requirements	4ns		
t10	Rising edge of DS3/E3/STS_1_CLK_IN to DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_CLOCK_IN Hold time requirements	0ns		

Table 14 presents information on the Timing parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Ingress Direction) for STS-1/STM-0 Applications and when the Receive STS-1 TOH Processor block has been configured to sample the DS3/E3/STS_1_DATA_IN signal upon the **falling edge** of DS3/E3/STS_1_CLOCK_IN.

TABLE 14: TIMING INFORMATION FOR THE INGRESS DS3/E3/STS-1 LIU INTERFACE FOR STS-1/STM-0 APPLICATIONS(FALLING EDGE OF DS3/E3/STS_1_CLOCK_IN)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t9	DS3/E3/STS_1_DATA_IN to falling edge of DS3/E3/STS_1_CLOCK_IN set-up time requirements	4ns		
t10	Falling edge of DS3/E3/STS_1_CLK_IN to DS3/E3/STS_1_DATA_IN and DS3/E3/STS_1_CLOCK_IN Hold time requirements	0ns		

1.3.6 The Egress DS3/E3/STS-1 Interface Timing

The user should be aware of the followings things about the Egress DS3/E3/STS-1 Interface timing.

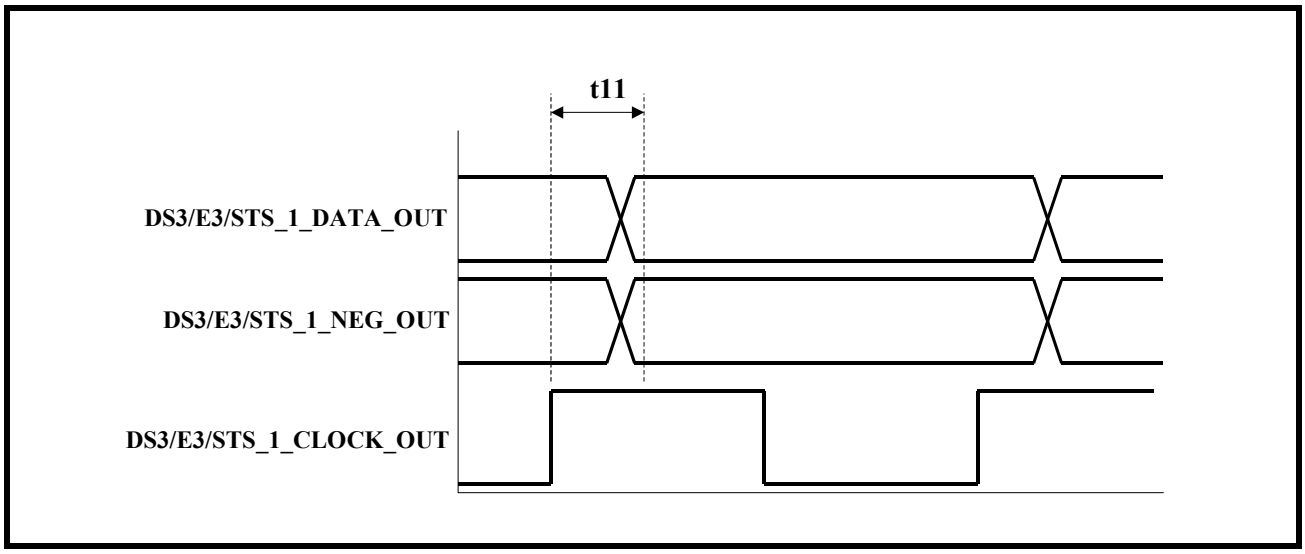
a. If a given channel is configured to operate in the DS3/E3 Mode, then the DS3/E3 Framer block can be configured to output the outbound DS3/E3 data (via the DS3/E3/STS_1_DATA_OUT and DS3/E3/STS_1_NEG_OUT output pins) upon either the rising or falling edge of DS3/E3/STS_1_CLOCK_OUT.

b. If a given channel is configured to operate in the STS-1/STM-0 Mode, then the Transmit STS-1 TOH Processor block will be operating in the Single-Rail Mode (e.g., the Transmit STS-1 TOH Processor block will output all outbound STS-1/STM-0 data via the DS3/E3/STS_1_DATA_OUT output pin. No data will be output via the DS3/E3/STS_1_NEG_OUT output pin).

c. Further, if a given channel is configured to operate in the STS-1/STM-0 Mode, then the Transmit STS-1 TOH Processor block can be configured to output the outbound STS-1/STM-0 data (via the DS3/E3/STS_1_DATA_OUT pin) either upon the rising or falling edge of DS3/E3/STS_1_CLOCK_OUT.

The Timing Diagram for the Egress DS3/E3/STS-1 Interface is presented below in Figure 17.

FIGURE 17. AN ILLUSTRATION OF THE WAVEFORMS OF THE DS3/E3/STS-1 SIGNALS THAT ARE OUTPUT FROM THE DS3/E3/STS-1 LIU INTERFACE (IN THE RECEIVE/EGRESS DIRECTION)



NOTE: The value for t11 is presented in Tables 15, 16, 17 *and* 18

1.3.7 Egress Timing for DS3/E3 Applications

Table 15 presents information on the Timing Parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Egress Direction) for DS3/E3 Applications and when the DS3/E3 Framer block has been configured to output the outbound DS3/E3 data (via the DS3/E3/STS_1_DATA_OUT and DS3/E3/STS_1_NEG_OUT signal upon the **rising edge** of DS3/E3/STS_1_CLOCK_OUT.

TABLE 15: TIMING INFORMATION FOR THE EGRESS DS3/E3/STS-1 LIU INTERFACE FOR DS3/E3 APPLICATIONS(RISING EDGE OF DS3/E3/STS_1_CLOCK_OUT)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t11	Rising edge of DS3/E3/STS_1_CLK_OUT to DS3/E3/STS_1_DATA_OUT & DS3/E3/STS_1_NEG_OUT output delay	2.1ns		7.8ns

Table 16 presents information on the Timing Parameters for the DS3/E3/STS-1 LIU Interface Signal (in the Egress Direction) for DS3/E3 Applications and when the DS3/E3 Framer block has been configured to output the outbound DS3/E3 data (via the DS3/E3/STS_1_DATA_OUT and DS3/E3/STS_1_NEG_OUT signals upon the **falling edge** of DS3/E3/STS_1_CLOCK_OUT.

TABLE 16: TIMING INFORMATION FOR THE EGRESS DS3/E3/STS-1 LIU INTERFACE FOR DS3/E3 APPLICATIONS(FALLING EDGE OF DS3/E3/STS_1_CLOCK_OUT)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t11	Rising edge of DS3/E3/STS_1_CLK_OUT to DS3/E3/STS_1_DATA_OUT & DS3/E3/STS_1_NEG_OUT output delay	1.6ns		6.5ns

1.3.8 Egress Timing for STS-1/STM-0 Applications

Table 17 presents information on the Timing parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Egress Direction) for STS-1/STM-0 Applications and when the Transmit STS-1 TOH Processor block has been configured to output the DS3/E3/STS_1_DATA_OUT signal upon the **rising edge** of DS3/E3/STS_1_CLOCK_OUT.

TABLE 17: TIMING INFORMATION FOR THE EGRESS DS3/E3/STS-1 LIU INTERFACE FOR STS-1/STM-0 APPLICATIONSAPPLICATIONS(RISING EDGE OF DS3/E3/STS_1_CLOCK_OUT)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t11	Rising edge of DS3/E3/STS_1_CLK_OUT to DS3/E3/STS_1_DATA_OUT output delay	0ns		4.5ns

1.3.9 Egress Timing for STS-1/STM-0 Applications (Continued)

Table 18 presents information on the Timing parameters for the DS3/E3/STS-1 LIU Interface Signals (in the Egress Direction) for STS-1/STM-0 Applications and when the Transmit STS-1 TOH Processor block has been configured to output the DS3/E3/STS_1_DATA_OUT signal upon the **falling edge** of DS3/E3/STS_1_CLOCK_OUT.

TABLE 18: TIMING INFORMATION FOR THE EGRESS DS3/E3/STS-1 LIU INTERFACE FOR STS-1/STM-0 APPLICATIONSAPPLICATIONS(FALLING EDGE OF DS3/E3/STS_1_CLOCK_OUT)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t11	Rising edge of DS3/E3/STS_1_CLK_OUT to DS3/E3/STS_1_DATA_OUT output delay	0ns		3.3ns

1.4 STS-1/STM-0 TELECOM BUS INTERFACE TIMING INFORMATION

STS-1/STM-0 Telecom Bus Interface Timing Information

This section presents the timing requirements for the STS-1/STM-0 Telecom Bus Interface. In particular this section indicates the following.

a. Identifies which edge of RxD_CLK in which the RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP output pins are updated on.

b. The clock to output delays (from the rising edge of RxD_CLK to the instant that the RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP output pins are updated.

c. Identifies which edge of TxA_CLK that the TxA_D[7:0], TxA_PL, TxA_C1J1 and TxA_DP input pins are sampled on.

d. The set-up time requirements (from an update in the TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP input signals to the rising edge of TxA_CLK).

e. The hold-time requirements (from the rising edge of TxA_CLK to a change in the TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP input signals)

1.4.1 SOME NOTES ABOUT THE STS-1/STM-0 TELECOM BUS INTERFACE

1. In contrast to the names that are given to the Transmit and Receive STS-3/STM-1 Telecom Bus Interface, the Transmit STS-1/STM-0 Telecom Bus interface will have the responsibility of receiving (in lieu of transmitting) STS-1/STM-0 data from some remote entity over a Telecom Bus Interface that is clocked at 6.48MHz. Likewise, the Receive STS-1/STM-0 Telecom Bus Interface will have the responsibility of transmitting (in lieu of receiving) STS-1/STM-0 data to some remote entity over a Telecom Bus Interface that is also clocked at 6.48MHz.

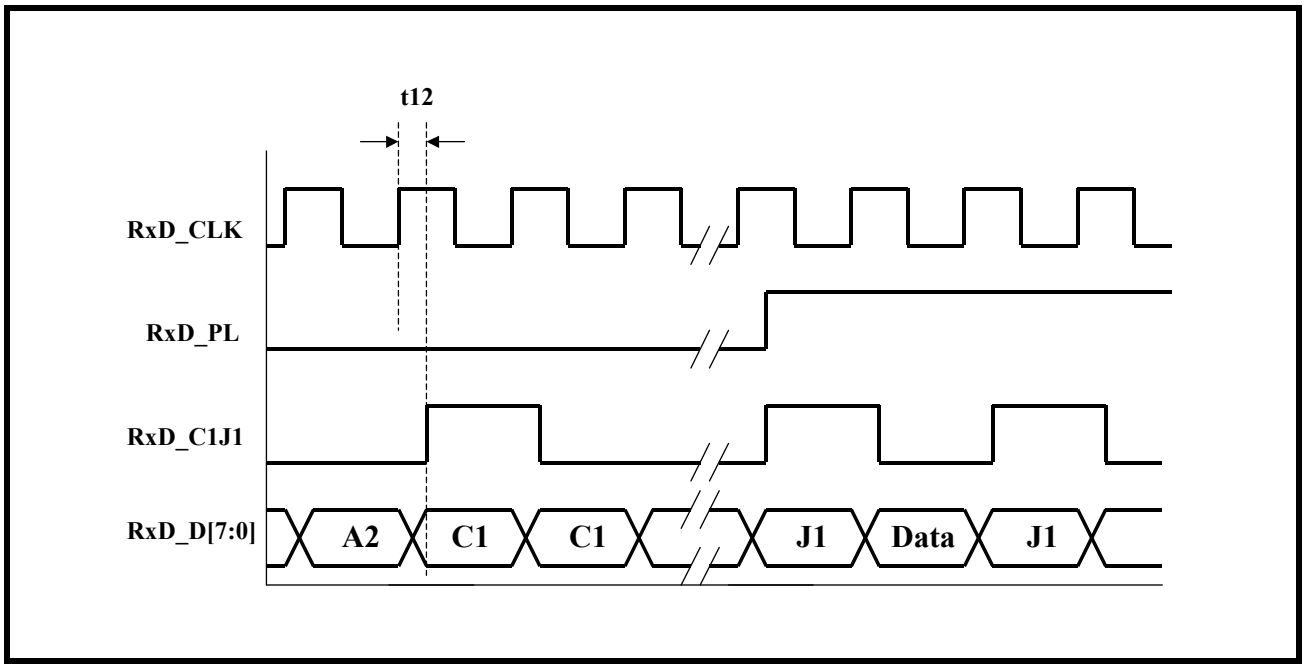
2. The STS-1/STM-0 Telecom Bus Interface, associated with Channel 0 can be configured to operate as either an STS-1/STM-0 or an STS-3/STM-1 Telecom Bus Interface. Timing Information for either of these modes will be presented in this section.

1.4.2 The Receive STS-1/STM-0 Telecom Bus Interface Timing

In the Receive STS-1/STM-0 Telecom Bus Interface, all of the signals (which are output via this Bus Interface) are updated upon the rising edge of RxD_CLK (6.48MHz clock signal).

Figure 18 presents an illustration of the waveforms of the signals that will be output via the Receive STS-1/STM-0 Telecom Bus Interface along with the timing parameter (t12).

FIGURE 18. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE STS-1/STM-0 TELECOM BUS INTERFACE



NOTE: *The value for t12 can be found in* Table 19.

TABLE 19: TIMING INFORMATION FOR THE RECEIVE STS-1/STM-0 TELECOM BUS INTERFACE

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t12	Rising edge of RxD_CLK to updates in RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP	0ns		9.4ns

1.4.3 The Receive STS-1/STM-0 Telecom Bus Interface Timing (for Channel 0 when configured to operate in the STS-3/STM-1 Mode)

In the Receive STS-1/STM-0 Telecom Bus Interface, all of the signals (which are output via this Bus Interface) are updated upon the rising edge of RxD_CLK (19.44MHz clock signal).

Figure 19 presents an illustration of the waveforms of the signals that will be output via the Receive STS-1/STM-0 Telecom Bus Interface, associated with Channel 0, whenever it is configured to operate in the STS-3/STM-1 Mode.

FIGURE 19. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE RECEIVE STS-1/STM-0 TELECOM BUS INTERFACE (FOR CHANNEL 0) WHEN CONFIGURED TO OPERATE IN THE STS-3/STM-1 MODE

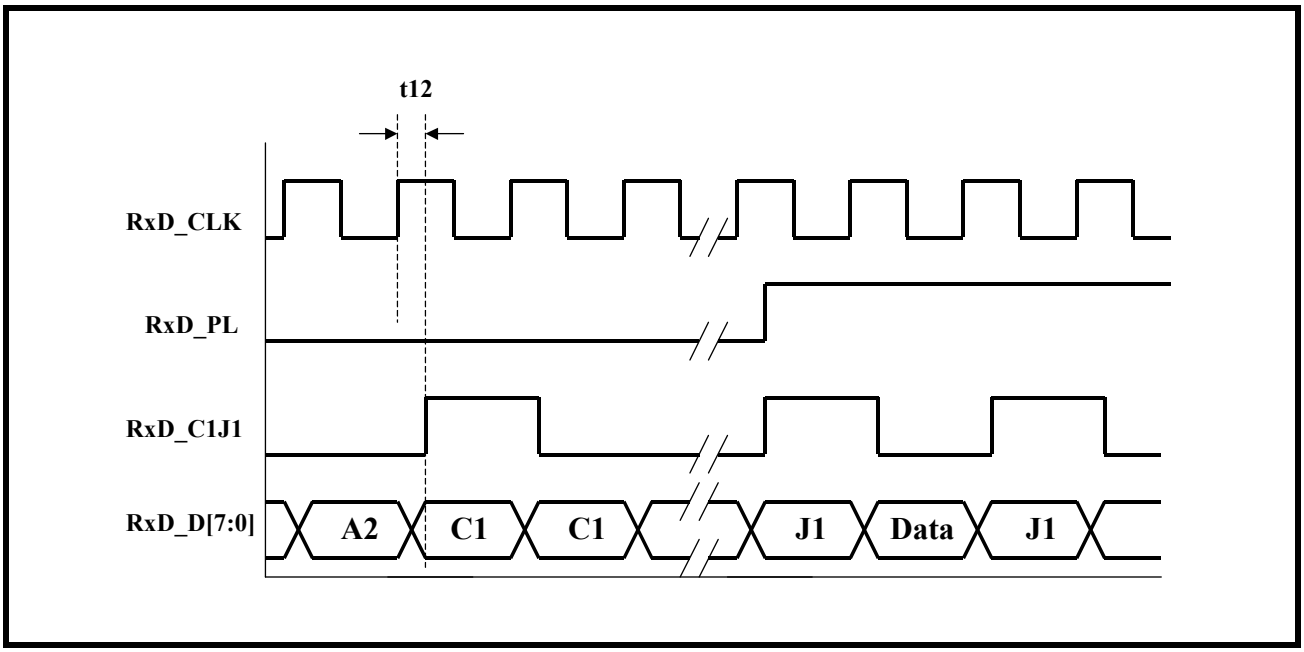


Table 20 presents information on the Timing Parameters for the Receive STS-1/STM-0 Telecom Bus Interface (when configured to operate in the STS-3/STM-1 Mode).

TABLE 20: TIMING INFORMATION FOR THE RECEIVE STS-1/STM-0 TELECOM BUS INTERFACE (WHEN CONFIGURED TO OPERATE IN THE STS-3/STM-1 MODE)

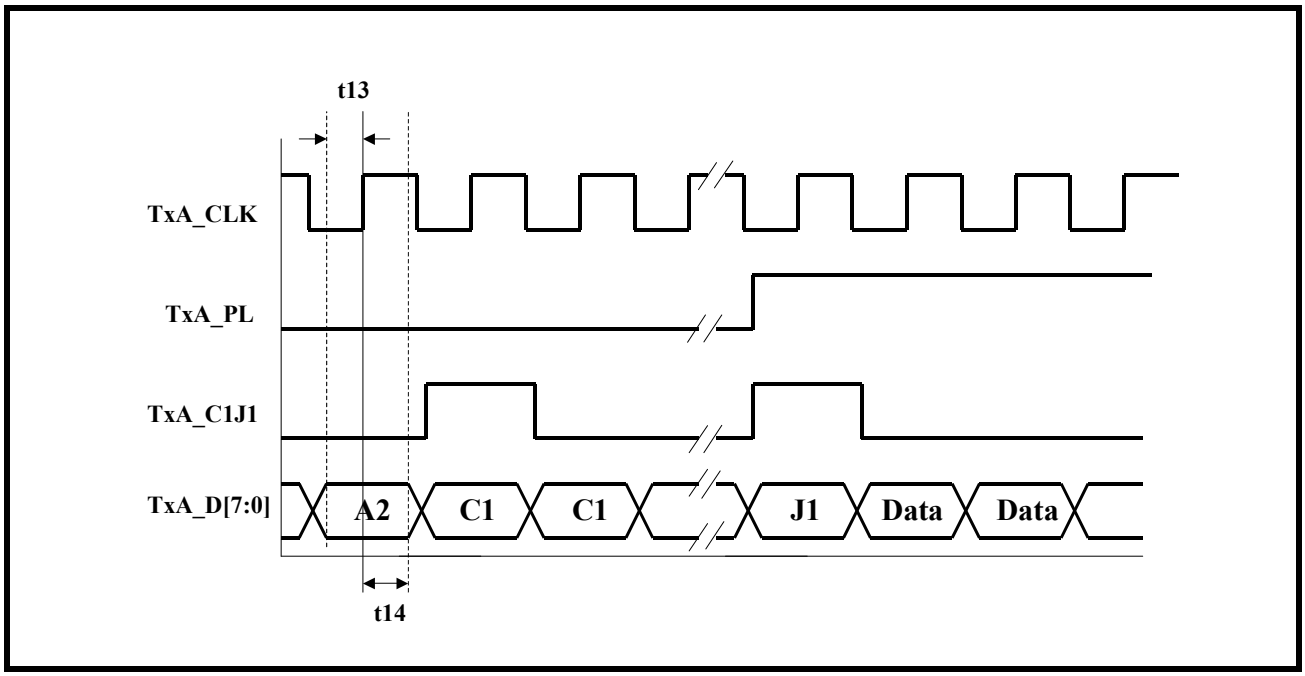
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t12	Rising edge of RxD_CLK to updates in RxD_D[7:0], RxD_PL, RxD_C1J1, RxD_ALARM and RxD_DP	1.7ns		7.7ns

1.4.4 The Transmit STS-1/STM-0 Telecom Bus Interface Timing

In the Transmit STS-1/STM-0 Telecom Bus Interface, all of the signals (which are input via this Bus Interface) are sampled upon the rising edge of TxA_CLK (6.48MHz clock signal).

Figure 20 presents an illustration of the waveforms and the timing parameters (t13 and t14) of the signals that will be received by the Transmit STS-1/STM-0 Telecom Bus Interface.

FIGURE 20. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE TRANSMIT STS-1/STM-0 TELECOM BUS INTERFACE



NOTE: The value for t13 and t14 can be found in Table 21.

TABLE 21: TIMING INFORMATION FOR THE TRANSMIT STS-1/STM-0 TELECOM BUS INTERFACE

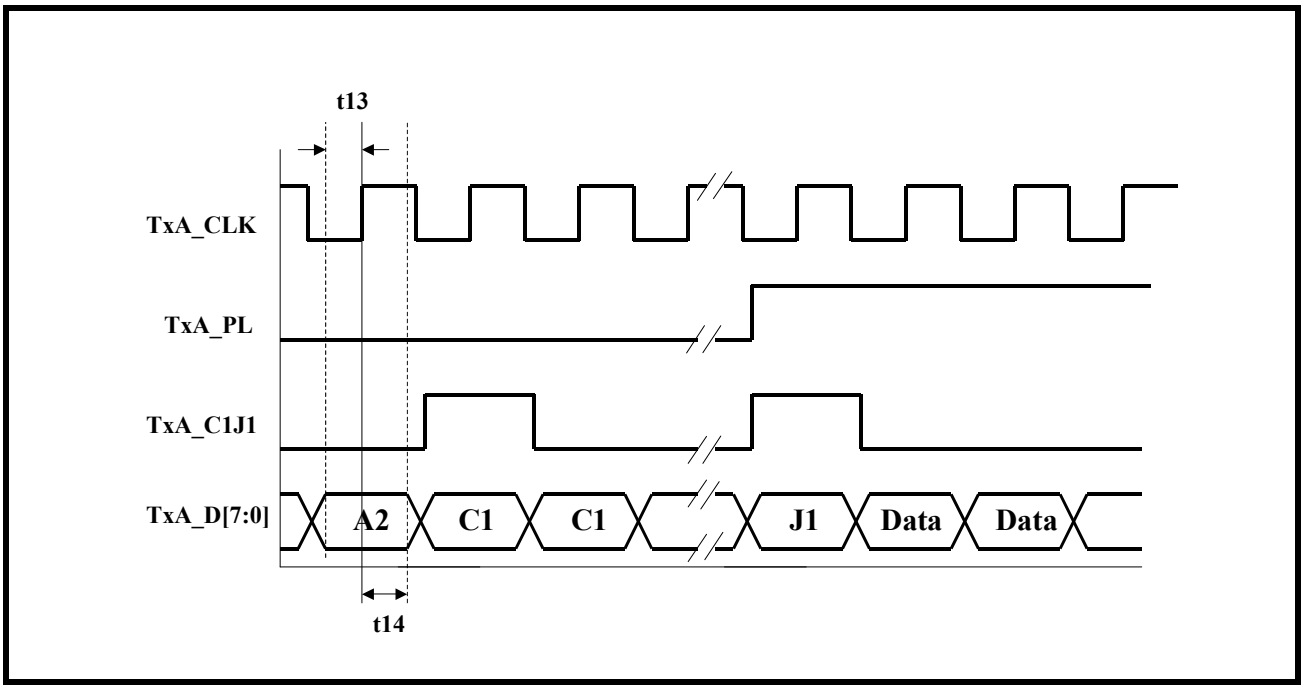
SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t13	TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP to rising edge of TxA_CLK set-up time requirements	4ns		
t14	Rising edge of TxA_CLK to TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP hold time requirements	0 ns		

1.4.5 The Transmit STS-1/STM-0 Telecom Bus Interface Timing (for Channel 0 when configured to operate in the STS-3/STM-1 Mode)

In the Transmit STS-1/STM-0 Telecom Bus Interface (associated with Channel 0) all of the signals (which are input via this Bus Interface) are sampled upon the rising edge of TxA_CLK (19.44MHz clock signal).

Figure 21 presents an illustration of the waveforms and the timing parameters (t13 and t14) of the signals that will be received by the Transmit STS-1/STM-0 Telecom Bus Interface.

FIGURE 21. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE TRANSMIT STS-1/STM-0 TELECOM BUS INTERFACE ASSOCIATED WITH CHANNEL 0 (WHEN CONFIGURED TO OPERATE IN THE STS-3/STM-1 MODE)



NOTE: The value for t13 and t14 can be found in **Table 22**.

TABLE 22: TIMING INFORMATION FOR THE TRANSMIT STS-1/STM-0 TELECOM BUS INTERFACE, FOR CHANNEL 0 WHEN IT HAS BEEN CONFIGURED TO OPERATE IN THE STS-3/STM-1 MODE

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t13	TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP to rising edge of TxA_CLK set-up time requirements	4ns		
t14	Rising edge of TxA_CLK to TxA_D[7:0], TxA_PL, TxA_C1J1, TxA_ALARM and TxA_DP hold time requirements	0 ns		

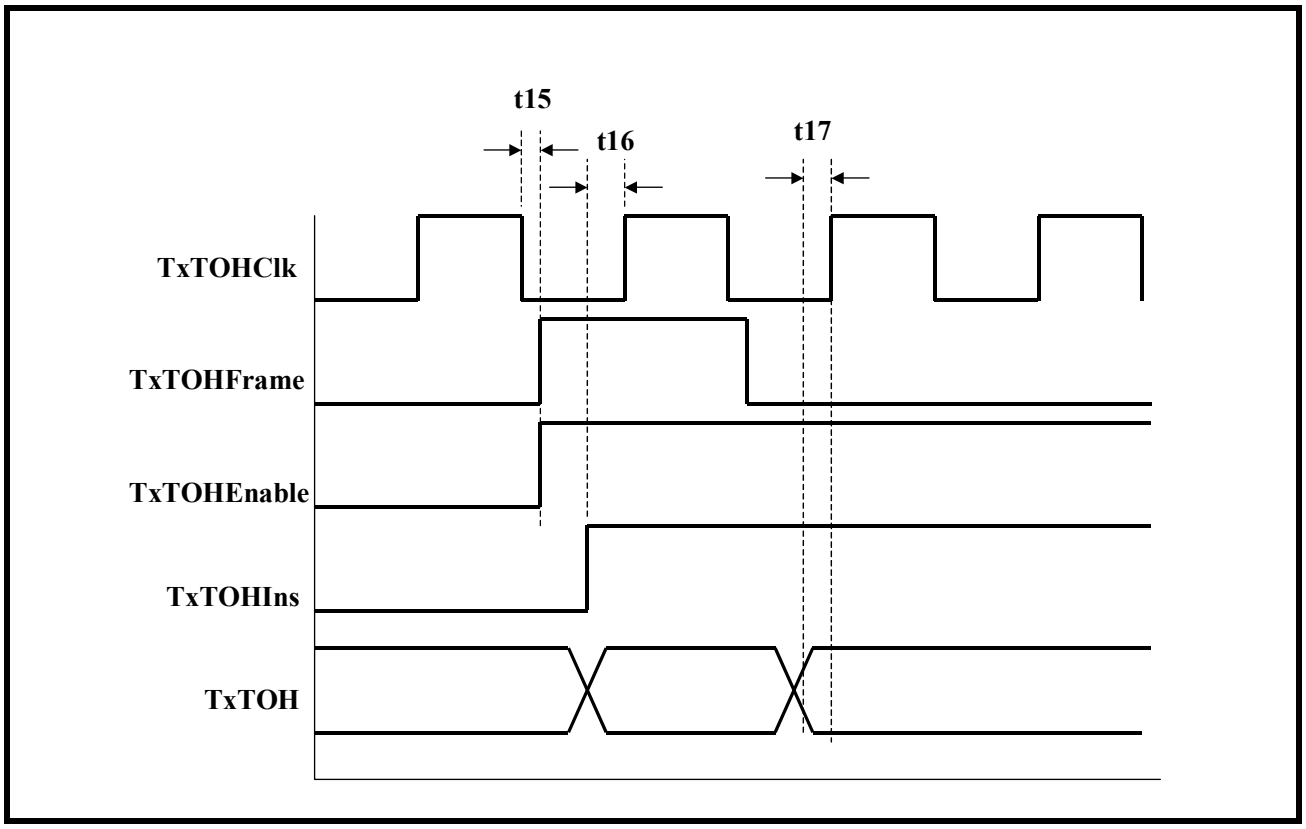
1.5 TRANSMIT TOH OVERHEAD INPUT PORT

The Transmit TOH Overhead Input Port is used to insert the users own value for the TOH bytes into the outbound STS-3/STM-1 data-stream.

NOTE: The TxTOHIns and the TxTOH input pins are sampled (by the Transmit TOH Overhead Input Port) upon the rising edge of TxTOHClk. All of the remaining signals (e.g., TxTOHFrame and TxTOHEnable) are updated upon the falling edge of TxTOHClk.

The timing wave-form and information for the Transmit TOH Overhead Input Port is presented below.

FIGURE 22. ILLUSTRATION OF TIMING WAVE-FORM OF THE TRANSMIT TOH OVERHEAD INPUT PORT



NOTE: The values for t15, t16 and t17 can be found in Table 23.

TABLE 23: TIMING INFORMATION FOR THE TRANSMIT TOH OVERHEAD INPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t15	Falling edge of TxTOHClk to rising edge of TxTOHFrame and TxTOHEnable output delay	-0.5ns		0.6ns
t16	TxTOHIns to rising edge of TxTOHClk set-up time	4ns		
t17	TxTOH Data to rising edge of TxTOHClk set-up time	4ns		

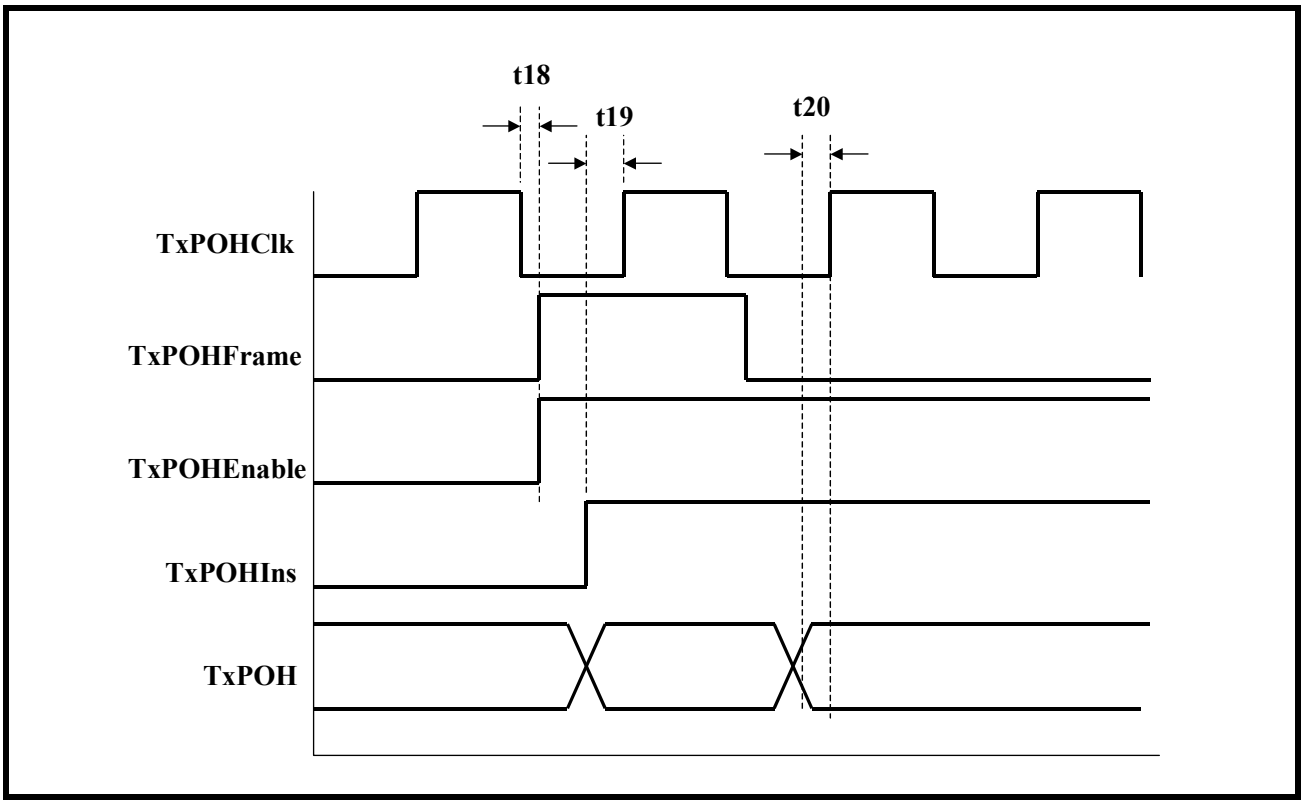
1.6 TRANSMIT POH OVERHEAD INPUT PORT

The Transmit POH Overhead Input Port is used to insert the users own value for the POH bytes into either the outbound STS-1 SPE data-stream (which is output via the Transmit STS-3/STM-1 data-stream or via the outbound STS-1 SPE data-stream (which is output via the Transmit STS-1 data-stream).

NOTE: The TxPOHIns and the TxPOH input pins are sampled (by the Transmit POH Overhead Input Port) upon the rising edge of TxPOHClk. All of the remaining signals (e.g., TxPOHFrame and TxPOHEnable) are updated upon the falling edge of TxPOHClk.

The timing wave-form and information for the Transmit POH Overhead Input Port is presented below.

FIGURE 23. ILLUSTRATION OF TIMING WAVE-FORM OF THE TRANSMIT POH OVERHEAD INPUT PORT



NOTE: The values for t18, t19 and t20 can be found in **Table 24**.

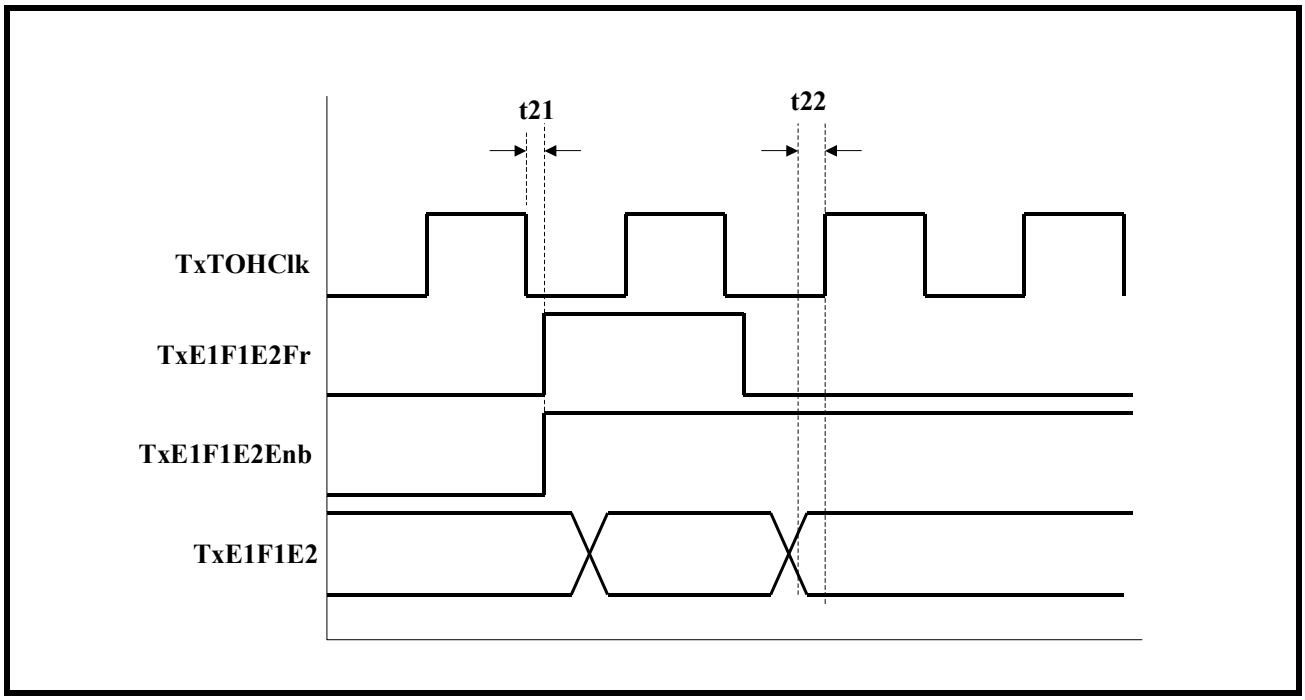
TABLE 24: TIMING INFORMATION FOR THE TRANSMIT POH OVERHEAD INPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t18	Falling edge of TxPOHClk to rising edge of TxPOHFrame and TxPOHValid output delay	-0.3ns		0.2ns
t19	TxPOHIns to rising edge of TxPOHClk set-up time	4ns		
t20	TxPOH Data to rising edge of TxPOHClk set-up time	4ns		

1.7 TRANSMIT ORDERWIRE (E1, F1, E2) BYTE OVERHEAD INPUT PORT

The Transmit Order-wire Byte Overhead Input Port provides a dedicated port for the user to insert his/her own value for the E1, F1 and E2 bytes within the outbound STS-3/STM-1 data-stream. The user should note that the TxE1F1E2 input pin is sampled (by the Transmit Order-wire Byte Overhead Input Port) upon the rising edge of TxTOHClk. All of the remaining signals (e.g., TxE1F1E2Enable, TxE1F1E2Frame) are updated upon the falling edge of TxTOHClk. The timing wave-form and information for the Transmit Order-wire Byte Overhead Input Port is presented below.

FIGURE 24. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE TRANSMIT ORDER-WIRE BYTE OVERHEAD INPUT PORT



NOTE: The values for t21 and t22 can be found in **Table 25**.

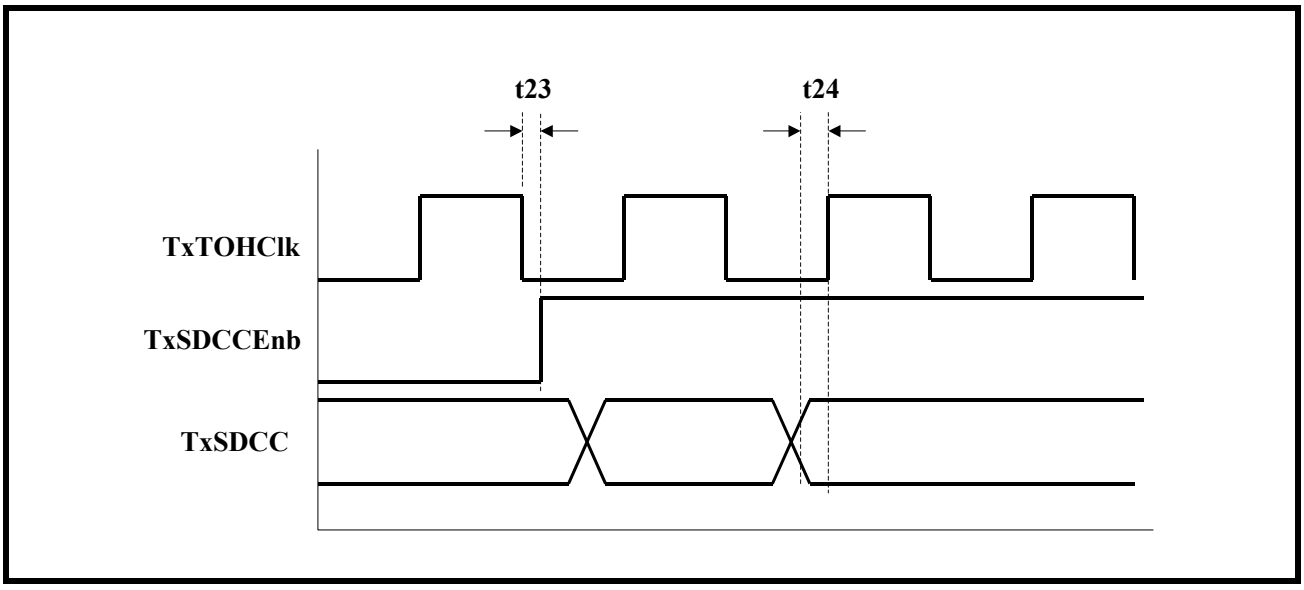
TABLE 25: TIMING INFORMATION FOR THE TRANSMIT ORDER-WIRE BYTE OVERHEAD INPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t21	Falling edge of TxTOHClk to rising edge of TxE1F1F2Enable and TxE1F1F2Frame	-0.5ns		0ns
t22	TxE1F1F2 Data to rising edge of TxTOHClk set-up time	4ns		

1.8 TRANSMIT SECTION DCC INSERTION INPUT PORT

The Transmit Section DCC Insertion Input Port provides a dedicated port for the user to insert his/her own value for the D1, D2 and D3 bytes within the outbound STS-3/STM-1 data-stream. The user should note that the TxSDCC input pin is sampled (by the Transmit Section DCC Insertion Input Port) upon the rising edge of TxTOHClk. The TxSDCCEnable output signal is updated upon the falling edge of TxTOHClk. The timing wave-form and information for the Transmit Section DCC Insertion Input Port is presented below.

FIGURE 25. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE TRANSMIT SECTION DCC OVERHEAD INSERTION PORT



NOTE: The values for t23 and t24 can be found in **Table 26**.

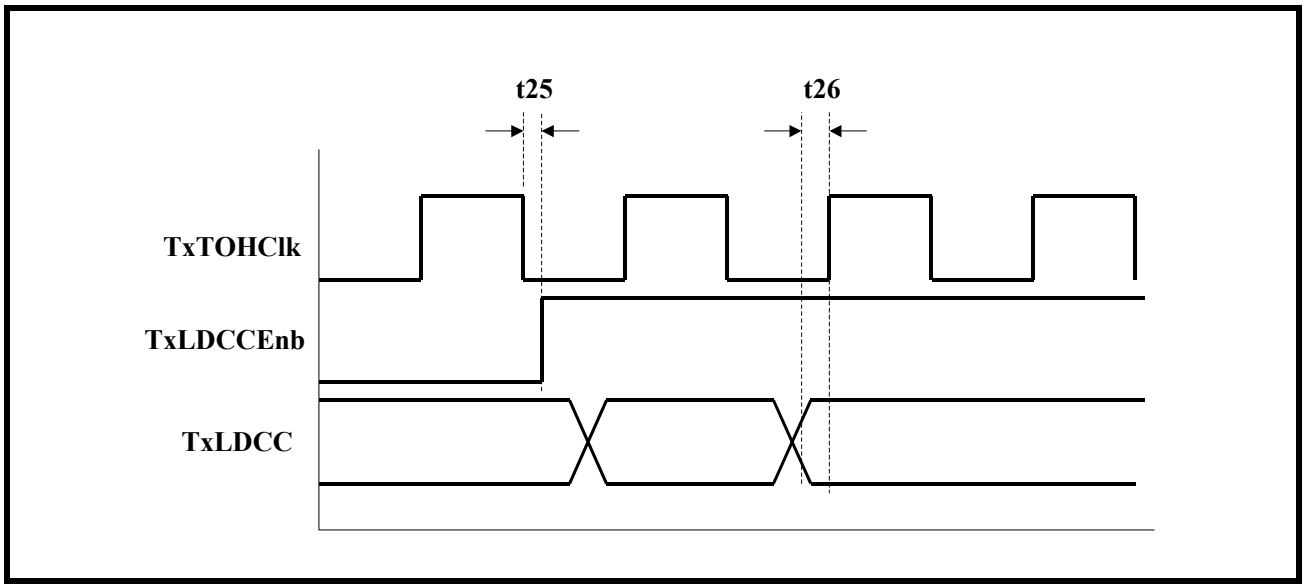
TABLE 26: TIMING INFORMATION FOR THE TRANSMIT ORDER-WIRE BYTE OVERHEAD INPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t23	Falling edge of TxTOHClk to rising edge of TxSDCCEnable output delay	-0.4ns		0.1ns
t24	TxSDCC Data to rising edge of TxTOHClk set-up time	4ns		

1.9 TRANSMIT LINE DCC INSERTION INPUT PORT

The Transmit Section DCC Insertion Input Port provides a dedicated port for the user to insert his/her own value for the D4 through D12 bytes within the outbound STS-3/STM-1 data-stream. The user should note that the TxLDCC input pin is sampled (by the Transmit Section DCC Insertion Input Port) upon the rising edge of TxTOHClk. The TxLDCCEnable output signal is updated upon the falling edge of TxTOHClk. The timing wave-form and information for the Transmit Line DCC Insertion Input Port is presented below.

FIGURE 26. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE TRANSMIT LINE DCC INSERTION INPUT PORT



NOTE: The values for t25 and t26 can be found in **Table 27**

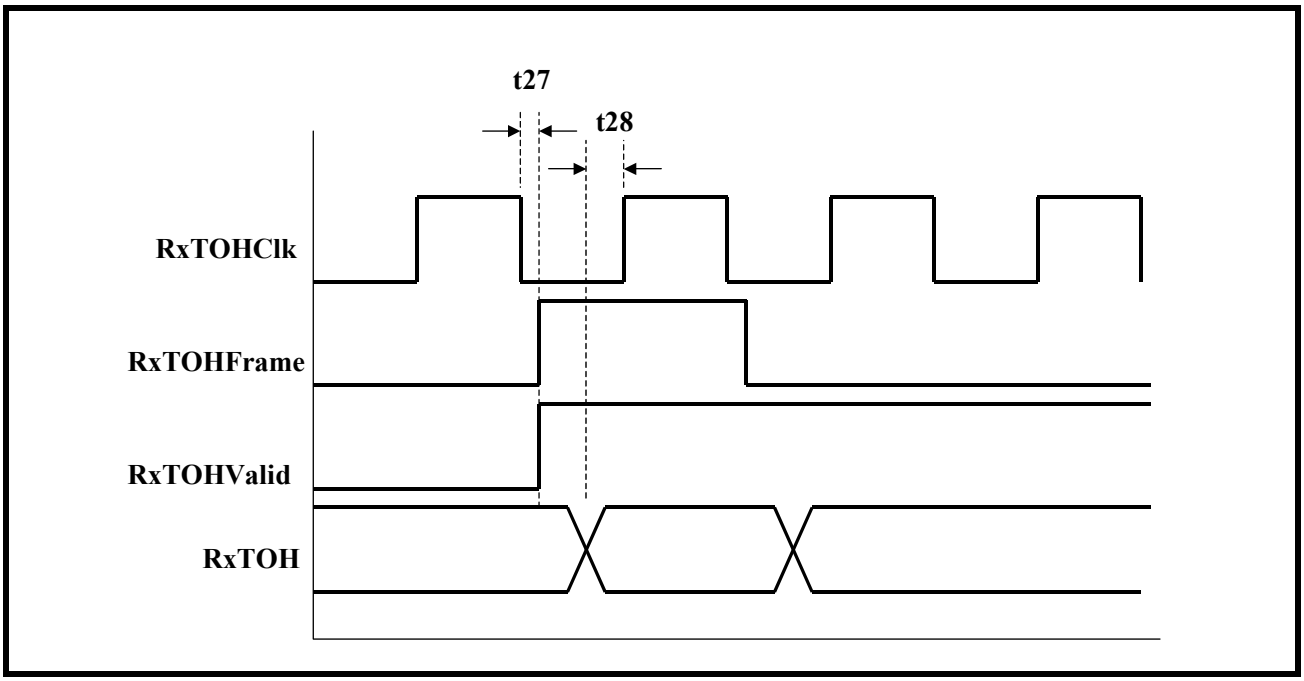
TABLE 27: TIMING INFORMATION FOR THE TRANSMIT LINE DCC INSERTION INPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t25	Falling edge of TxTOHClk to rising edge of TxLDCCEnable	-0.5ns		0.2ns
t26	TxLDCC Data to rising edge of TxTOHClk set-up time	4ns		

1.10 RECEIVE TOH OVERHEAD OUTPUT PORT

The Receive TOH Overhead Output port is used to extract out the values of the TOH bytes within the incoming STS-3/STM-1 data-stream. All of the Receive TOH Overhead Output port signals are updated upon the falling edge of RxTOHClk. The timing wave-form and information for the Receive TOH Overhead Output Port is presented below.

FIGURE 27. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE TOH OVERHEAD OUTPUT PORT



NOTE: The values for t27 and t28 can be found in Table 28.

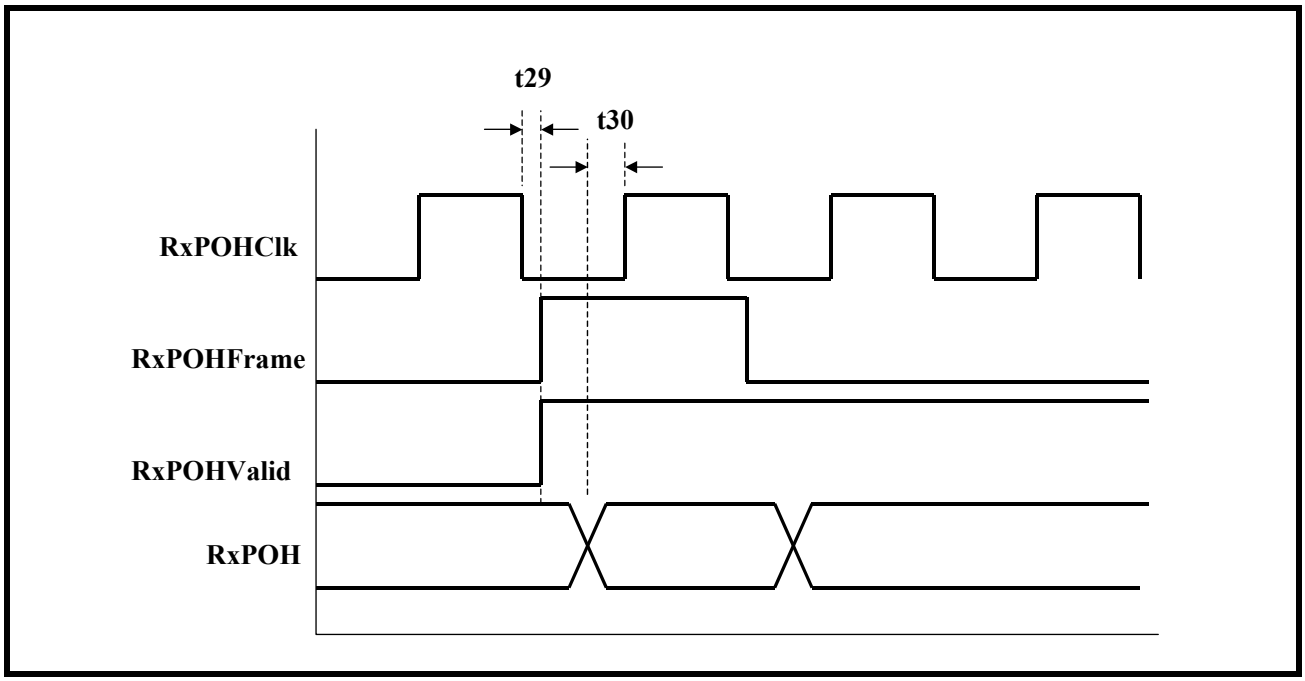
TABLE 28: TIMING INFORMATION FOR THE RECEIVE TOH OVERHEAD OUTPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t27	Falling edge of RxTOHClk to rising edge of RxTOHFrame and RxTOHValid	-0.5ns		0.4ns
t28	Falling edge of RxTOHClk to RxTOH output delay	-0.5ns		0.5ns

1.11 RECEIVE POH OVERHEAD OUTPUT PORT

The Receive POH Overhead Output port is used to extract out the values of the POH bytes within the incoming STS-3/STM-1 data-stream. All of the Receive POH Overhead Output port signals are updated upon the falling edge of RxPOHClk. The timing wave-form and information for the Receive POH Overhead Output Port is presented below.

FIGURE 28. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE POH OVERHEAD OUTPUT PORT



NOTE: The values for t29 and t30 can be found in **Table 29**.

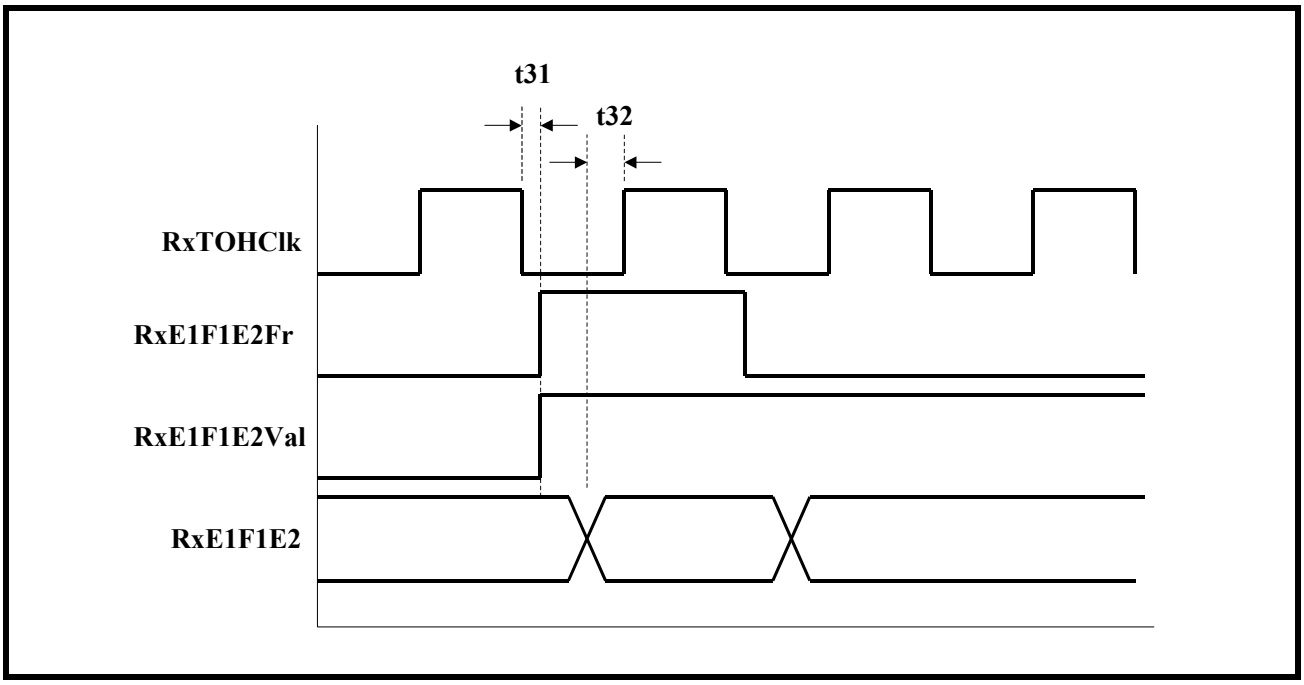
TABLE 29: TIMING INFORMATION FOR THE RECEIVE POH OVERHEAD OUTPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t29	Falling edge of RxPOHClk to rising edge of RxPOHFrame and RxPOHValid	-0.3ns		0ns
t30	Falling edge of RxPOHClk to RxPOH output delay	-0.3ns		0ns

1.12 RECEIVE ORDERWIRE (E1, F1, E2) BYTES OVERHEAD OUTPUT PORT

The Receive Order-wire Byte Overhead output port provides a dedicated port for the user to extract out the Order-wire (e.g., the E1, F1 and E2) bytes from that within the incoming STS-3/STM-1 data-stream. The user should note that all of the output signals (of this port) are updated upon the falling edge of RxTOHClk. The timing wave-form and information for the Receive Order-wire Byte Overhead output port is presented below.

FIGURE 29. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE ORDER-WIRE BYTE OVERHEAD OUTPUT PORT



NOTE: The values for t31 and t32 can be found in Table 30.

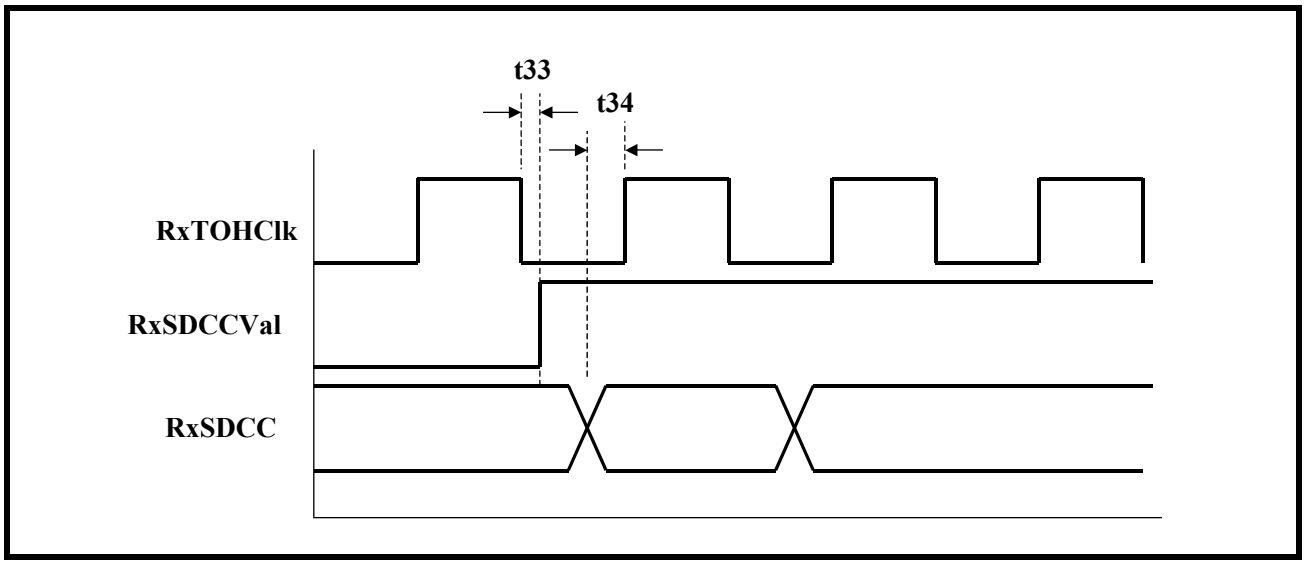
TABLE 30: TIMING INFORMATION FOR THE RECEIVE ORDER-WIRE BYTE OVERHEAD OUTPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t31	Falling edge of RxTOHClk to rising edge of RxE1F1E2Frame and RxE1F1E2Valid	-0.6ns		0.4ns
t32	Falling edge of RxTOHClk to RxE1F1E2 output delay	0.1ns		0.3ns

1.13 RECEIVE SECTION DCC EXTRACTION OUTPUT PORT

The Receive Section DCC output port provides a dedicated port for the user to extract out the Section DCC (e.g., D1, D2 and D3) bytes from that within the incoming STS-3/STM-1 data-stream. The user should note that all of the output signals (of this port) are updated upon the falling edge of RxTOHClk. The timing wave-form and information for the Receive Section DCC output port is presented below.

FIGURE 30. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE SECTION DCC OUTPUT PORT



NOTE: The values for t34 and t34 can be found in Table 31.

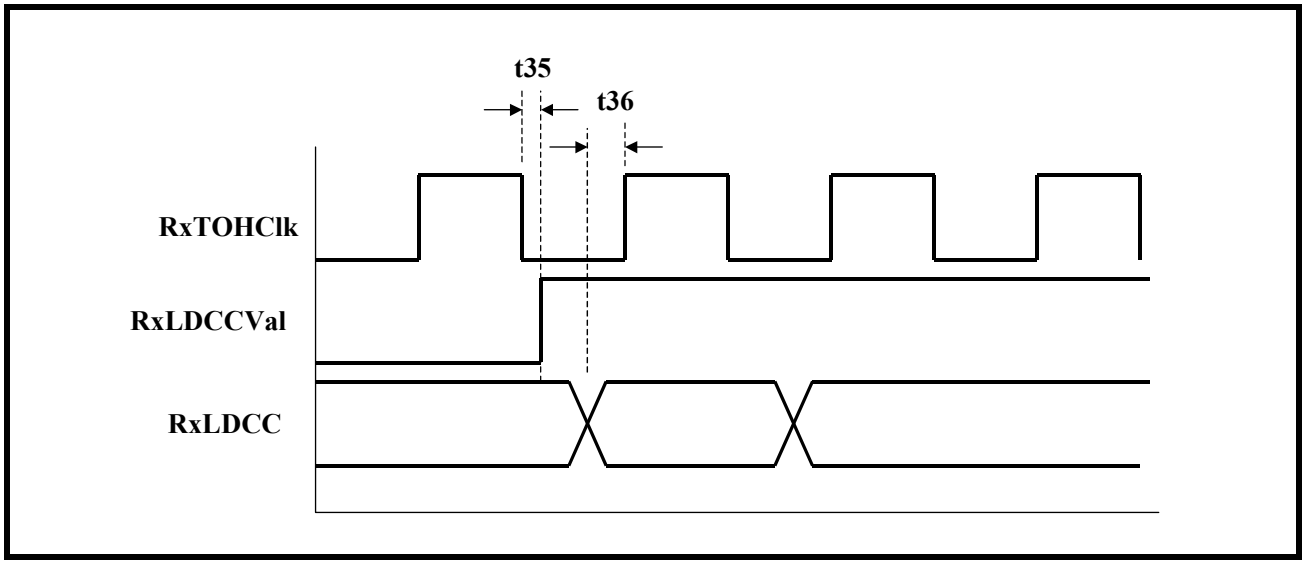
TABLE 31: TIMING INFORMATION FOR THE RECEIVE SECTION DCC OUTPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t33	Falling edge of RxTOHClk to rising edge of RxSDCCValid	0ns		0.5ns
t34	Falling edge of RxTOHClk to RxSDCC output delay	0ns		0.4ns

1.14 RECEIVE LINE DCC EXTRACTION OUTPUT PORT

The Receive Line DCC output port provides a dedicated port for the user to extract out the Line DCC (e.g., D4 through D12) bytes from that within the incoming STS-3/STM-1 data-stream. The user should note that all of the output signals (of this port) are updated upon the falling edge of RxTOHClk. The timing wave-form and information for the Receive Line DCC output port is presented below.

FIGURE 31. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE LINE DCC OUTPUT PORT



NOTE: The values for t35 and t36 can be found in **Table 32**.

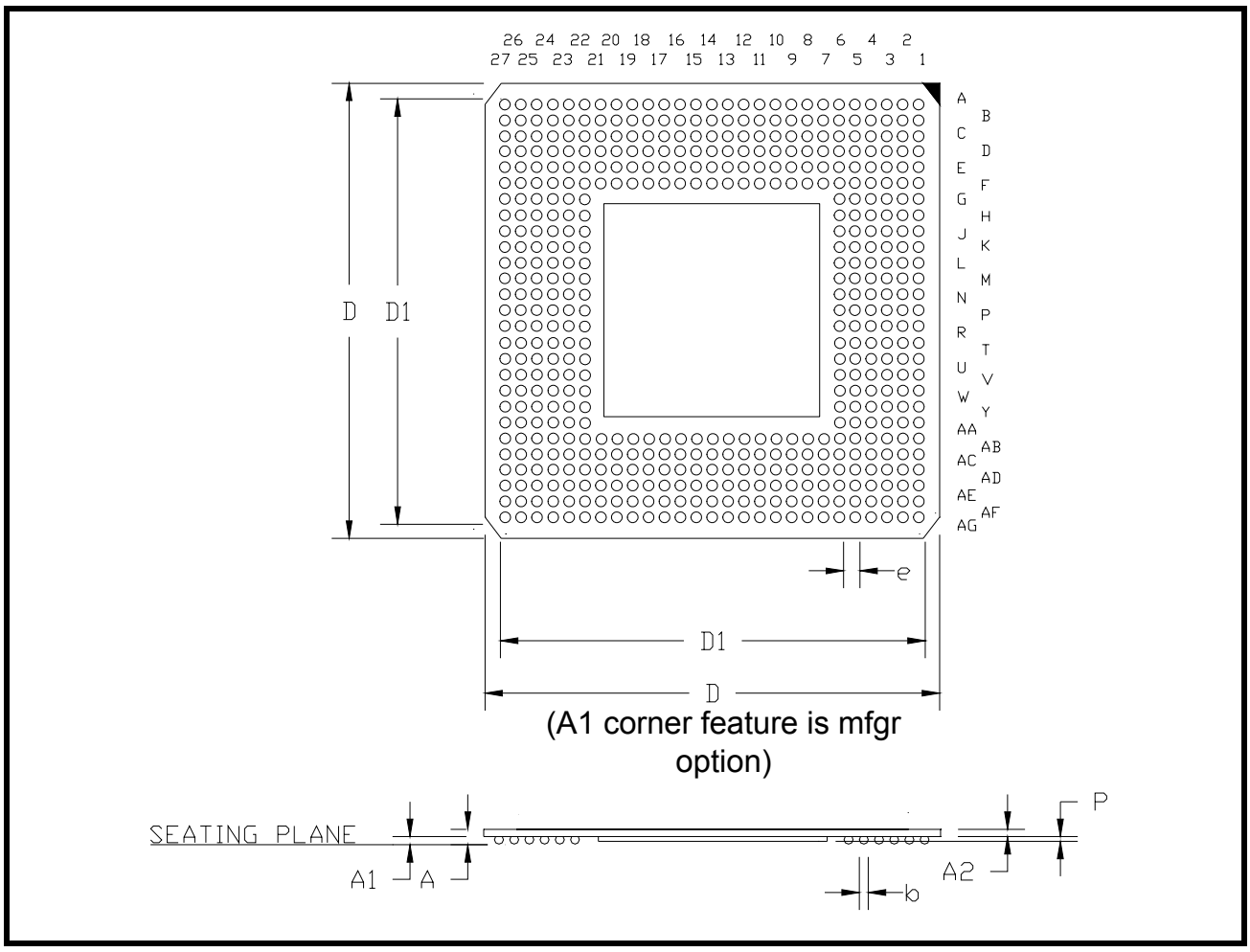
TABLE 32: TIMING INFORMATION FOR THE RECEIVE LINE DCC OUTPUT PORT

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.
t35	Falling edge of RxTOHClk to rising edge of RxLDCCValid	-0.2ns		0.4ns
t36	Falling edge of RxTOHClk to RxLDCC output delay	0ns		0.04ns

PACKAGE OUTLINE DRAWING

504 TAPE BALL GRID ARRAY
(35 MM X 35 MM - TBGA)

FIGURE 32. 94L31 PACKAGE OUTLINE DRAWING BOTTOM VIEW



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.051	0.067	1.30	1.70
A1	0.020	0.028	0.50	0.70
A2	0.031	0.039	0.80	1.00
D	1.370	1.386	34.80	35.20
D1	1.300 BSC		33.02 BSC	
b	0.024	0.035	0.60	0.90
e	0.050 BSC		1.27 BSC	
P	0.006	0.012	0.15	0.30

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REVISIONS

REV #	DATE	DESCRIPTION
P1.0.0	06/01/06	Initial issue.
1.0.0	10//26/06	Removed the preliminary designation.
1.0.1	03/14/07	Added package outline Drawing

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