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SIEMENS

S/T Bus Interface Circuit (SBC)

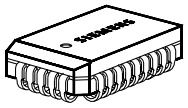
PEB 2080
PEF 2080

Preliminary Data

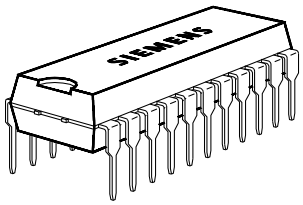
CMOS IC

1 Features

- Full duplex 2B + D S/T-interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T and IOM® interfaces
- D-channel access control
- Activation and deactivation procedures according to CCITT I.430
- Built-in wake-up unit for activation from power-down state
- Adaptively switched receive thresholds
- Control via IOM interface
- Several operating modes
- Receive timing recovery according to selected operating mode
- Frame alignment with absorption of phase wander in trunk line applications
- Switching of test loops
- Advanced CMOS technology
- Low power consumption:
  PEB 2080: standby less than 5 mW
  active max. 65 mW
  PEF 2080: standby less than 6.5 mW
  active max. 70 mW



P-LCC-28-R



P-DIP-22

Type	Ordering Code	Package
PEB 2080-N	Q67100-H8395	P-LCC-28-R (SMD)
PEB 2080-P	Q67100-H2954	P-DIP-22
PEF 2080-N	Q67100-H6097	P-LCC-28-R (SMD)

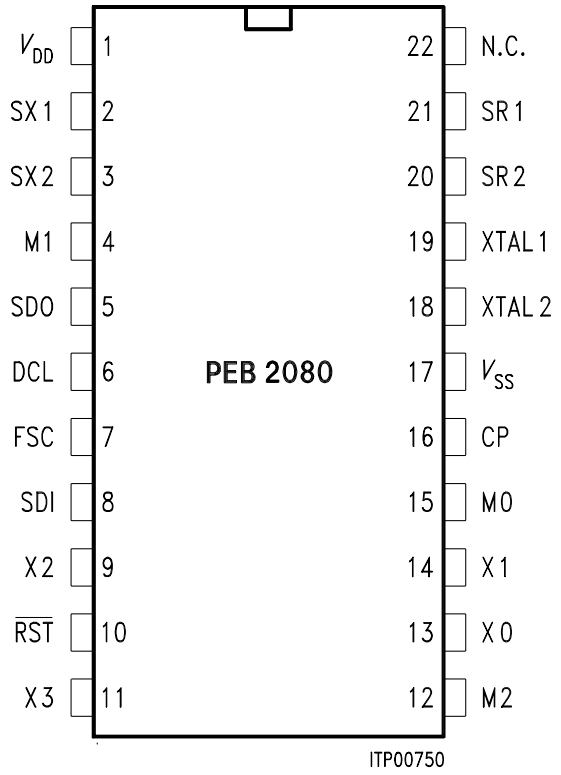
The S-Bus Interface Circuit (SBC) PEx 2080 implements the four-wire S/T-interface used to link voice/data terminals to an ISDN. Through selection of operating mode, the device may be employed in all types of applications involving an S interface. Two or more SBC´s can be used to build a point-to-point, passive bus, extended passive bus or star configuration.

Specific ISDN applications of the SBC include: ISDN terminals, ISDN network termination (Central Office and PABX applications), and PABX trunk lines to Central Office.

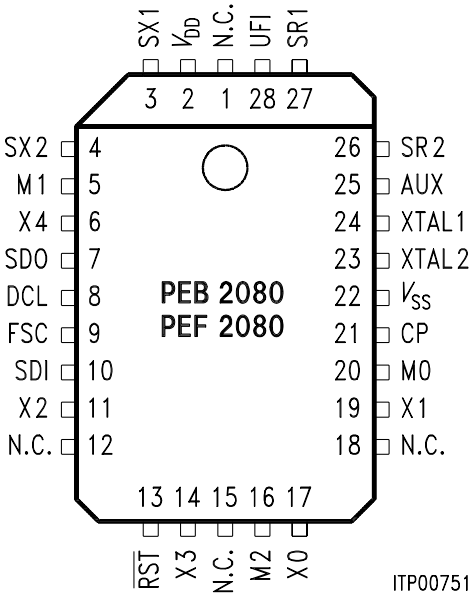
The device provides all electrical and logical functions according to CCITT recommendation I.430. These include: mode-dependent receive timing recovery, D-channel access and priority control, and automatic handling of activation/deactivation procedures. The SBC does not require direct microprocessor control.

The SBC is an IOM compatible, 22-pin CMOS device. It operates from a single + 5 V supply and features a power-down state with very low power consumption.

Pin Configuration
(top view)



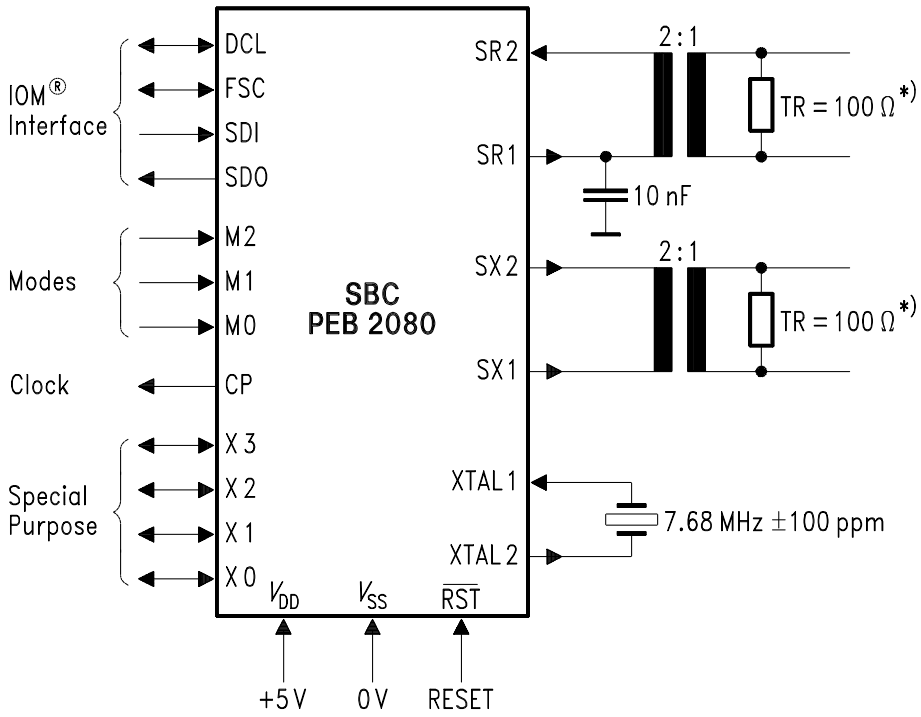
P-DIP-22



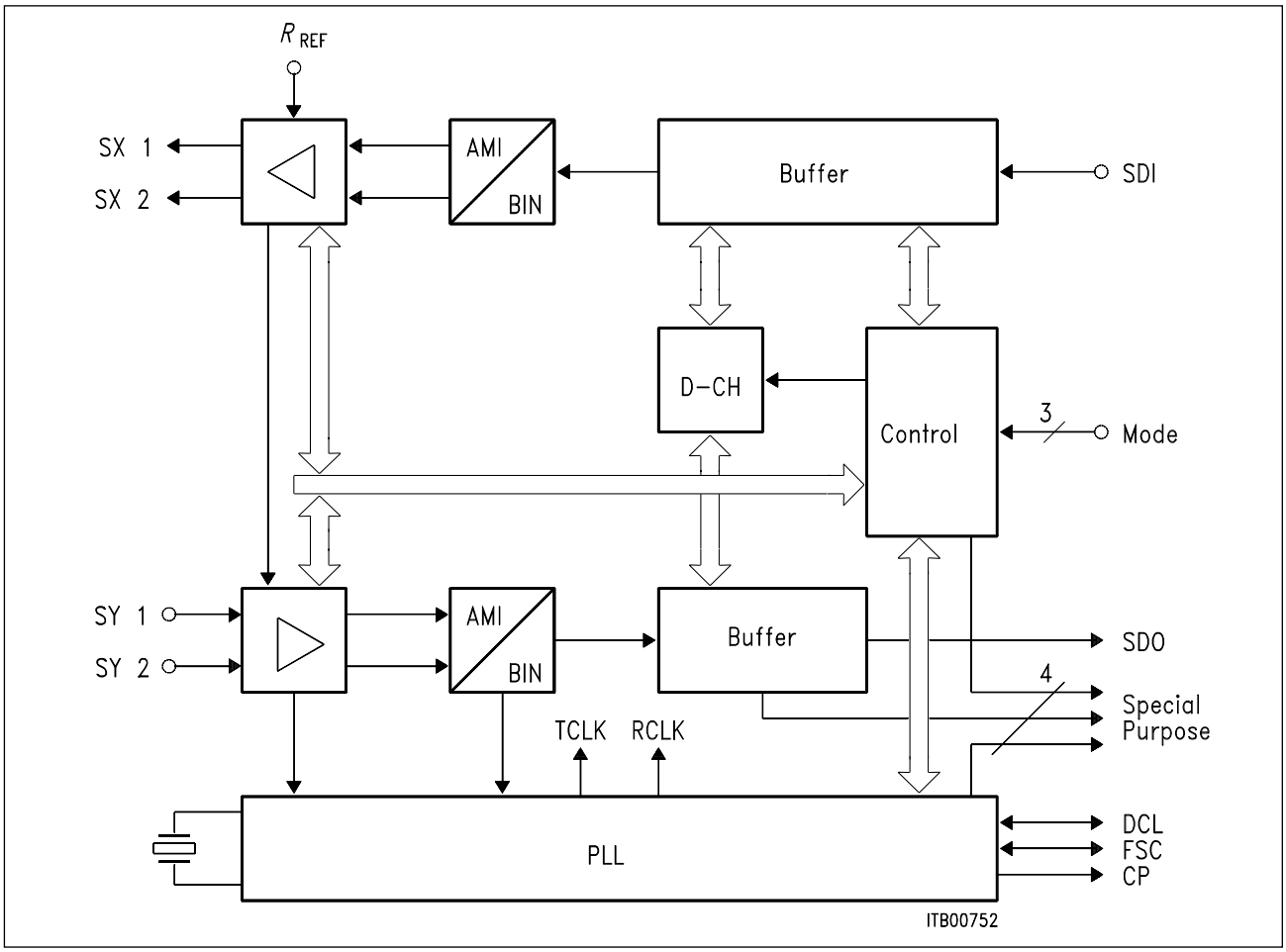
P-LCC-28-R

1.1 Pin Definitions and Functions

Pin No. P-LCC	Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
3	2	SX1	O	Positive output S-bus transmitter
4	3	SX2	O	Negative output S-bus transmitter
7	5	SDO	O	Serial Data Out, IOM interface
10	8	SDI	I	Serial Data In, IOM interface
8	6	DCL	I/O	Serial Data Clock, IOM interface
9	7	FSC	I/O	Frame sync, IOM interface
16 5 20	12 4 15	M2 M1 M0	I I I	Setting of operation mode
14 11 19 17	11 9 14 13	X3 X2 X1 X0	I I/O I/O I/O	Functions depending on the selected operating mode see chapter 2.2
21	16	CP	I/O	Clock Pulse/special purpose
24	19	XTAL1	I	Connection for external crystal, or input for external clock generator
23	18	XTAL2	O	Connection for external crystal, n.c. when external clock generator is used
26	20	SR2	I	S-bus receiver, signal input
27	21	SR1	O	S-bus receiver, 2.5 V reference output
2	1	VDD	I	Power supply, + 5 V $\pm$ 5 %
22	17	VSS	I	Power supply, ground
13	10	$\overline{\text{RST}}$	I	Reset, active low
6	-	X4	I	External filter connection, active low
28	-	UFI	O	Opamp output for external filter
25	-	AUX	I	Auxiliary input: V_{DD} or V_{SS} to be applied
15 18 1	- - -	N.C.	- - -	not connected



Logic Symbol



Block Diagram

1.2 System Integration

The SBC implements the four-wire S and T interfaces used in the ISDN basic access. It may be used at both ends of these interfaces.

The applications include:

ISDN terminals (TE)

ISDN network termination (NT)

ISDN subscriber line termination (LT-S)

ISDN trunk line termination (LT-T) (PABX connection to Central Office).

These applications are shown in **figure 1**, where the usual nomenclature as defined by the CCITT for the basic access functional blocks and reference points, has been used.

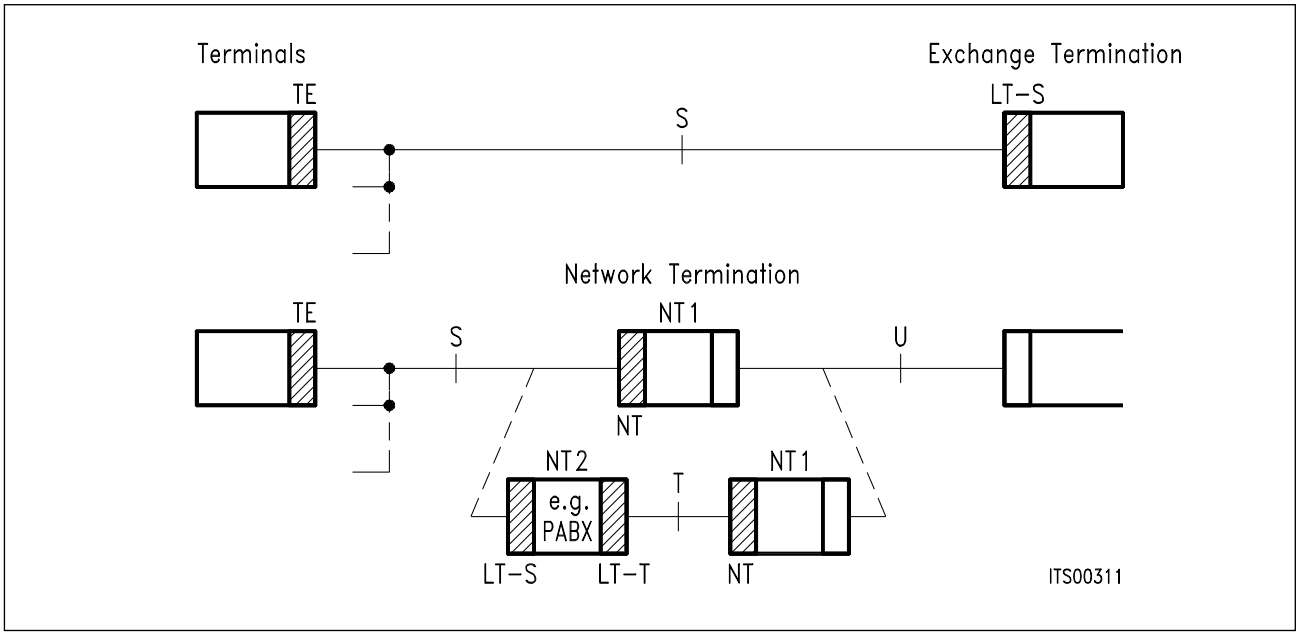


Figure 1
Applications of SBC

Some of the S interface wiring configurations possible with the SBC are shown in **figure 2** with approximate typical distances.

*) (N.B.: “TR” stands for terminating resistor of value 100 Ω).

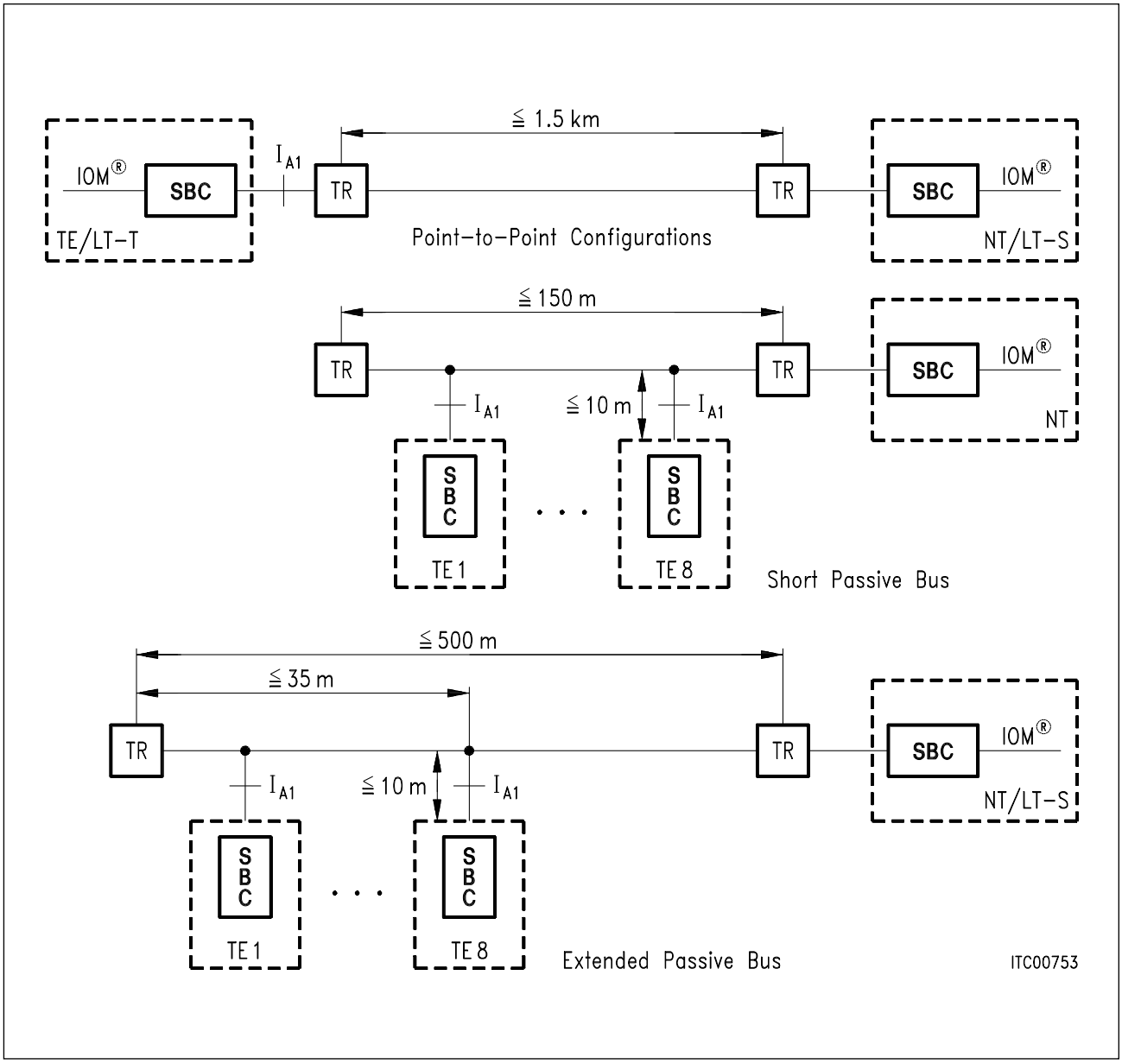


Figure 2
Some S-Interface Wiring Configurations

*) The maximum line attenuation tolerated by the SBC is 10 dB at 96 kHz

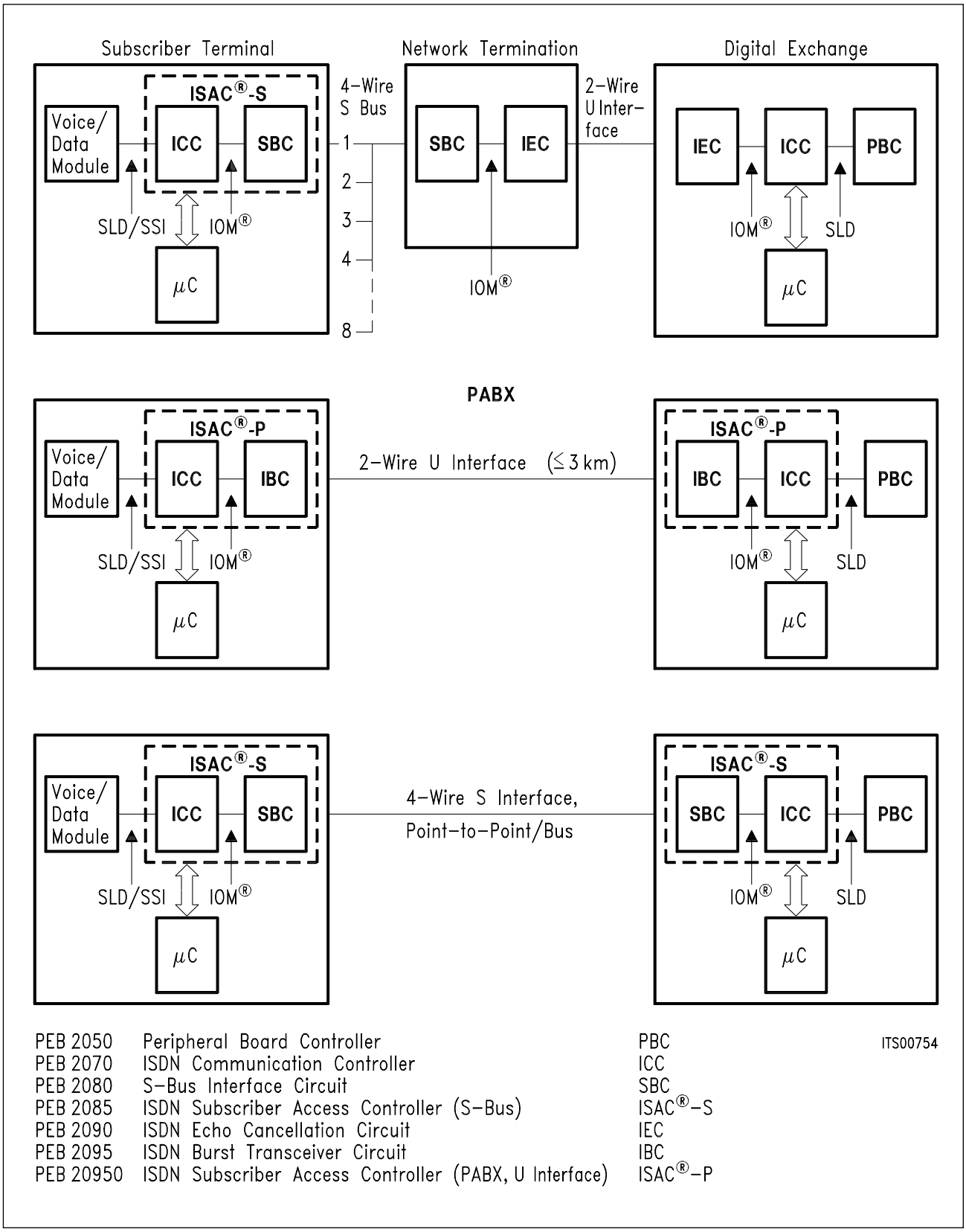


Figure 3
ISDN Oriented Modular (IOM®) Architecture

Figure 3 gives an example of an application of the SBC in an IOM (ISDN Oriented Modular) architecture.

By separate implementation of OSI layer-1 and layer-2 functions, and through unified control procedures, the architecture provides flexibility with respect to various transmission techniques. The IOM devices are all low-power, high integration, single + 5 V supply CMOS devices. Through mode switching, each device may be used in several applications: thus with one and the same limited set of devices all ISDN basic access configurations are covered. Note that one of the compatible layer-1 devices (SBC, IBC, IEC) requires direct microprocessor control. This is, of course, due to the fact that the IOM interface provides all the necessary functions for layer-1/layer-2 communication.

2 Functional Description

The S-bus interface circuit PEx 2080 performs the layer-1 functions for the S/T interface of the ISDN basic access.

2.1 General Functions and Device Architecture

The common functions for all operating modes are:

- line transceiver functions for the S interface according to the electrical specifications of CCITT I.430;
- dynamically adaptive threshold control for the receiver;
- conversion of the frame structure between IOM and S interfaces;
- conversion from/to binary to/from pseudo-ternary code.

Mode specific functions are:

- receive timing recovery;
- S-timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation;
- activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO's received from the line;
- frame alignment according to CCITT Q.503;
- execution of test loops.

Analog Functions

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as a current limited voltage source. A voltage of 2.1 V is delivered between SX1-SX2, which yields a current of 7.5 mA over 280 Ω.

The receiver is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2.

An external transformer of ratio 2:1 is needed in both receive and transmit direction to provide for isolation and transform voltage levels according to CCITT recommendations.

Digital Functions

A DPLL circuitry working with a frequency of 7.68 MHz ± 100 ppm serves to generate the 192-kHz line clock from the reference clock delivered by the network and to extract the 192-kHz line clock from the receive data stream.

The 7.68-MHz clock may be generated with the use of an external crystal between pins XTAL1 and XTAL2. It may also be provided by an external oscillator, in which case XTAL2 is left unconnected.

The “Control” block includes the logic to detect layer-1 commands and to communicate with external layer-1 or layer-2 devices via the IOM interface.

An incorporated finite state machine controls ISDN layer-1 activation/deactivation.

The D-channel access procedure according to CCITT I.430 including priority management is fully implemented in the SBC. When used as an S-bus master in a multipoint configuration, the device generates the echo bits necessary for D-channel collision detection. In the NT-mode, moreover, the echo channel may be made externally available through an auxiliary pin and thus “intelligent NT’s” (star configuration) may be implemented.

In terminal applications (TE) the Q channel as specified by I.430 is supported (stepping A6 and up. The SBC sends a binary one in F_A-bit position to allow another terminal to use the extra transmission capacity.)

The buffer memory serves to adapt the different bit rates of the S and the IOM interface. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503 (slip detection).

2.2 Operating Modes

The operating modes are determined by pin strapping on pins M0 to M2. The four basic operating modes are: TE, NT, LT-S, LT-T.

In three of these operating modes, the IOM may be programmed to function in the IOM-1 mode, in the IOM -2 mode or in the inverted mode. To see which IOM timing mode is applicable in the four basic operating modes, refer to **table 1**.

In **table 1**, the functions of the operating mode specific pins are given: these pins are DCL (IOM interface data clock, input/output), FSC (IOM interface frame sync, input/output), CP (auxiliary clock/test pin), and X0 to X3.

Depending on the selected mode, pins CP, X2 and X1 provide auxiliary clocks, either asynchronous or synchronous to the S-interface:

3840 kHz 2560 kHz 1280 kHz	clocks derived from the 7680-kHz crystal
1536 kHz 512 kHz	clocks synchronized to S interface

These auxiliary clocks may be used to drive, e.g. a codec filter, or a microprocessor system (TE applications).

Table 1
Operating Modes and Functions of Mode Specific Pins of SBC

	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation of IOM Interface	Inverted Mode	Inverted Mode	IOM-1 Mode	IOM-2 Mode or Invert. Mode	IOM-1 Mode	IOM-1 Mode	IOM-2 Mode or Invert. Mode	IOM-1 Mode	IOM-1 Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCL	o: 512 kHz*	o: 512 kHz*	o: 512 kHz*	i: 4096 kHz	i: 512 kHz	i: 512 kHz	i: 4096 kHz	i: 512 kHz	i: 512 kHz
FSC	o: 8 kHz*	o: 8 kHz*	o: 8 kHz*	i: 8 kHz	i: 8 kHz	i: 8 kHz	i: 8 kHz	i: 8 kHz	i: 8 kHz
CP	o: 1536 kHz*	o: 1536 kHz*	o: 512 kHz*	o: 512 kHz*	o: 512 kHz*	i:$\overline{\text{SCZ}}$	i:fixed at 0	i:fixed at 0	i:fixed at 0
X3	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:$\overline{\text{ENCK}}$	i:fixed at 1	i:fixed at 0	i:BUS	i:BUS	i:BUS	i:BUS
X2	o: 2560 kHz	o: 1280 kHz	o: ECHO	i:TS2	i:fixed at 0	i:$\overline{\text{SSZ}}$	i:TS2	i:fixed at 0	o: 192 kHz*
X1	o: 3840 kHz	o: 3840 kHz	o: 3840 kHz	i:TS1	i:fixed at 0	i:DEX	i:TS1	o: 7680 kHz	o: 7680 kHz
X0	o:RDY	o:RDY	i:CON	i:TS0	i:CON	i/o:DE	i:TS0	i:fixed at 0	i:fixed at 1

*) synchronized to S/T interface
i:input
o:output

The other uses of the auxiliary pins are:

$\overline{\text{ENCK}}$	input	Enable Clock. At “0”, forces the SBC to deliver IOM timing at all times, regardless of SDI input level; in TE mode, pin X3.
BUS	input	At “1”, specifies a bus configuration (as opposed to point to point or extended passive bus); in NT and LT-S modes, pin X3.
ECHO	output push-pull	Reproduces the E bits received from the S interface synchronously to IOM frame “D” bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary “1”; in TE mode, pin X2.
$\overline{\text{SSZ}}$	input	Send Single Zeros. At “0”, forces the SBC to transmit alternating pulses at 250 s intervals (period 2 kHz) on S-interface for test purposes; X2 in NT mode.
RDY	output	Ready. Provides a signal logically equal push to bit 3 of MONITOR channel. Signals the pull D-channel status (“0” = occupied, “1” = free) to layer-2 component; X0 in TE mode.
CON	input	Connected. At “0”, prevents the SBC from activating and transmitting on the S interface. Indicates whether the device is connected to the S interface or not; X0 in TE and LT-T modes.
DEX	input	External D-channel Echo enable. At “1”, makes the E-bit dependent on the DE (X0) input. Used in NT mode to build a star configuration; X1 in NT mode.
DE	input/output open drain with integrated pull-up resistor	D-channel Echo. The DE outputs should be tied together (open drain) in an NT-star configuration, to obtain the global echo bit; X0 in NT mode.
TS0 to TS2	inputs	Time Slot 0 to 7. IOM interface time slot to be used = 4 x TS2 + 2 x TS1 + TS0; LT-T and LT-S in IOM-2 mode and inverted mode.

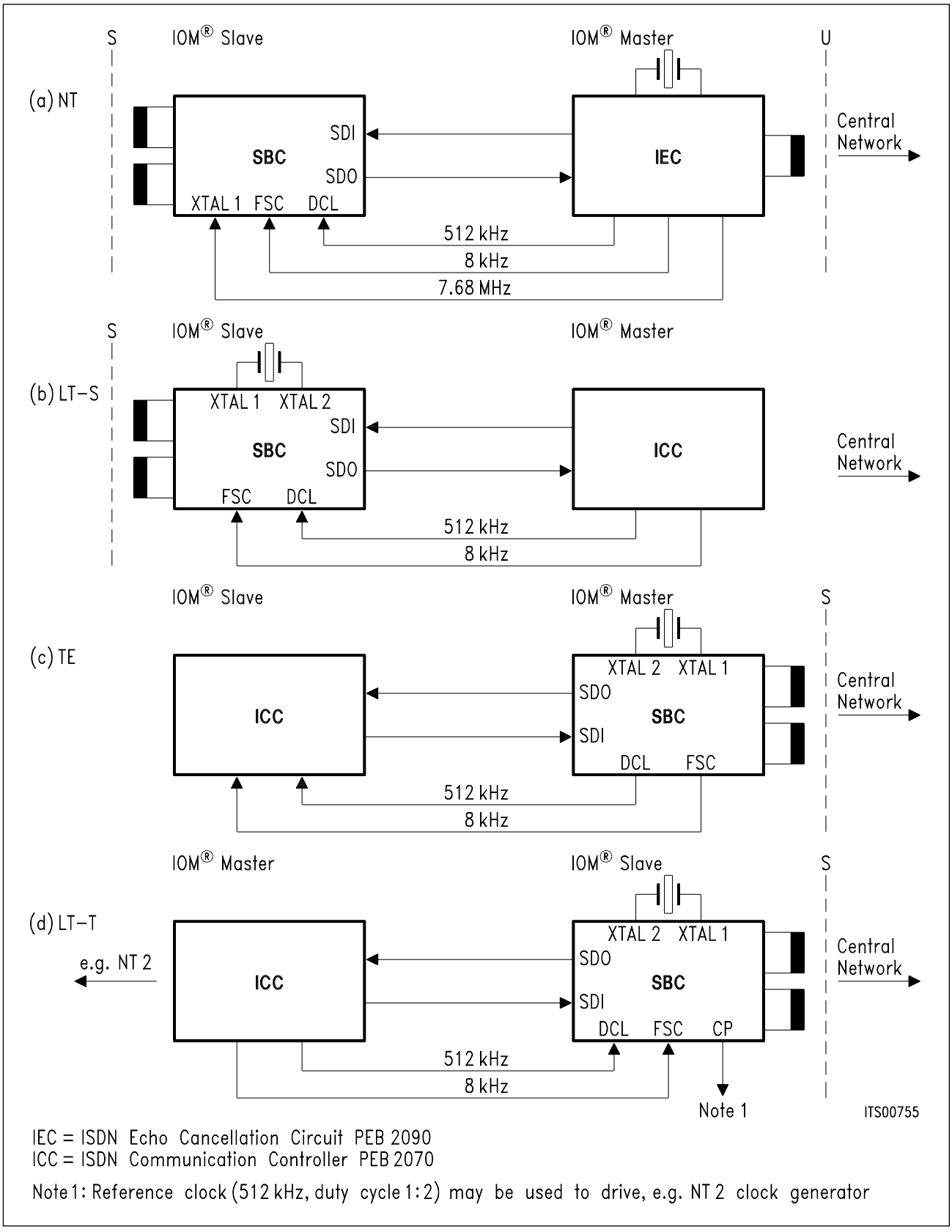


Figure 4
Clocking of SBC in Different Operating Modes

2.3 Interfaces

S Interface

According to CCITT recommendation I.430, pseudo-ternary encoding with 100 % pulse width is used on the S interface. A logical 1 corresponds to a neutral level (no current), whereas logical 0´s are encoded as alternating positive and negative pulses. An example is shown in **figure 5**.

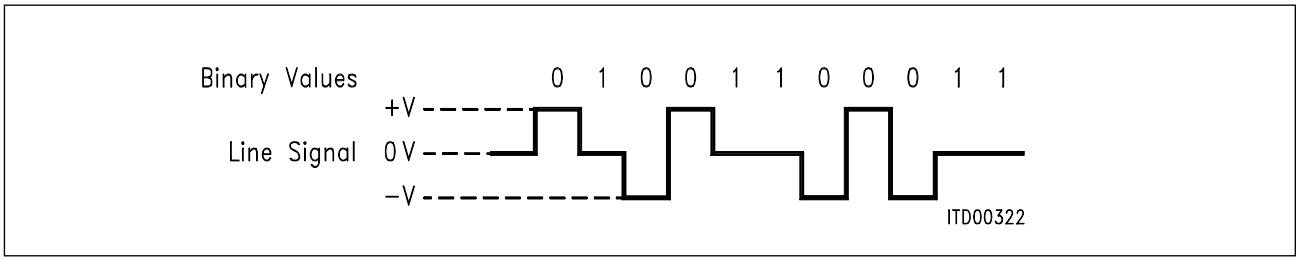


Figure 5
S-Interface Line Code

One S frame consists of 48 bits, at a nominal bit rate of 192 kbit/s. Thus each frame carries two octets of B1, two octets of B2, and four D bits, according to the B1 + B2 + D structure defined for the ISDN basic access (total useful data rate: 144 kbit/s). Frame begin is marked using a code violation (no mark inversion). The frame structures (from network to subscriber, and subscriber to network) are shown in **figure 6**.

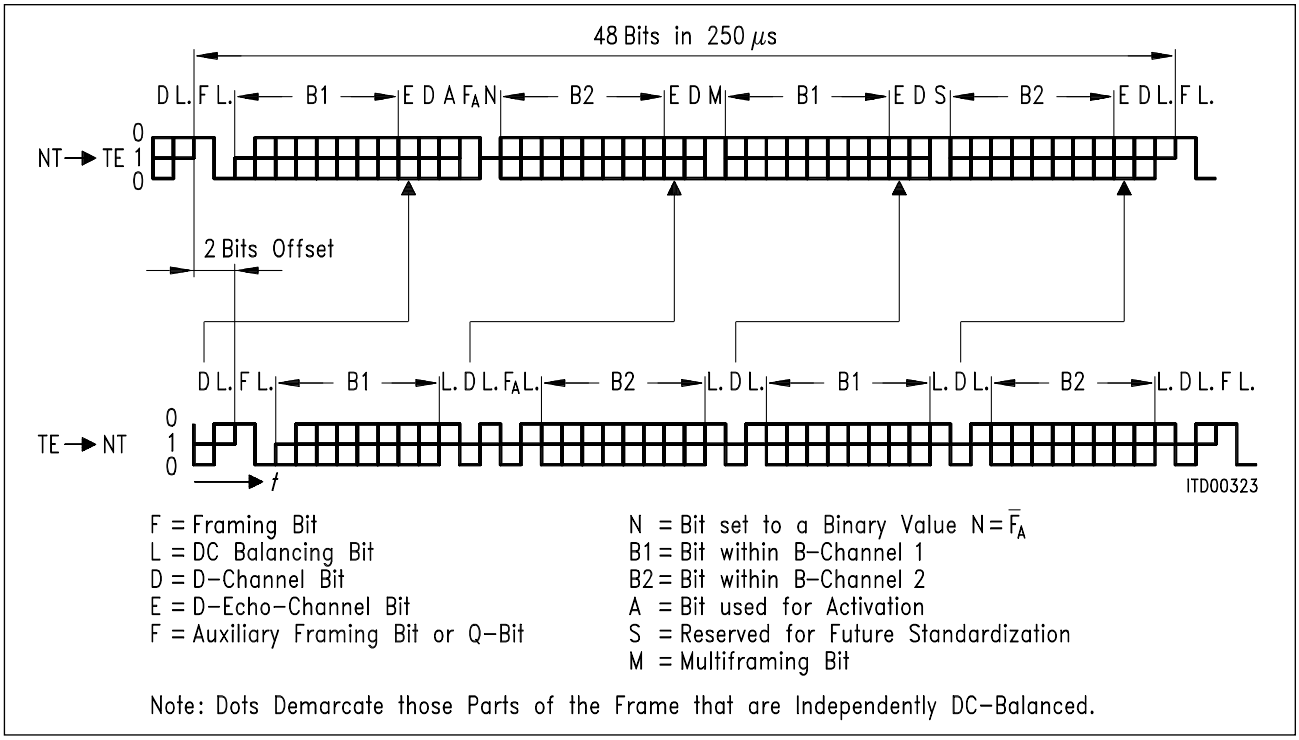


Figure 6
Frame Structure at Reference Ponts S and T (CCITT I.430)

Digital Interface

IOM Frame Structure

The SBC is provided with a digital interface, the IOM interface, for communication with other ISDN devices, in other words with units realizing OSI layer-1 functions (such as the ISDN Echo Cancellation Circuit IEC PEB 2090) or layer-2 functions (such as the ISDN Communication Controller ICC PEB 2070).

The IOM interface is a four-wire serial interface with: a bit clock, a frame clock and one data line per direction (**figure 7**).

The ISDN data rate of 144 kbit/s (B1 + B2 + D) is transmitted transparently in both directions over the interface. In addition, it is necessary to interchange control information for activation and deactivation of OSI layer 1 and for switching of test loops. This information is transferred using time division multiplexing with a 125-µs total frame length.

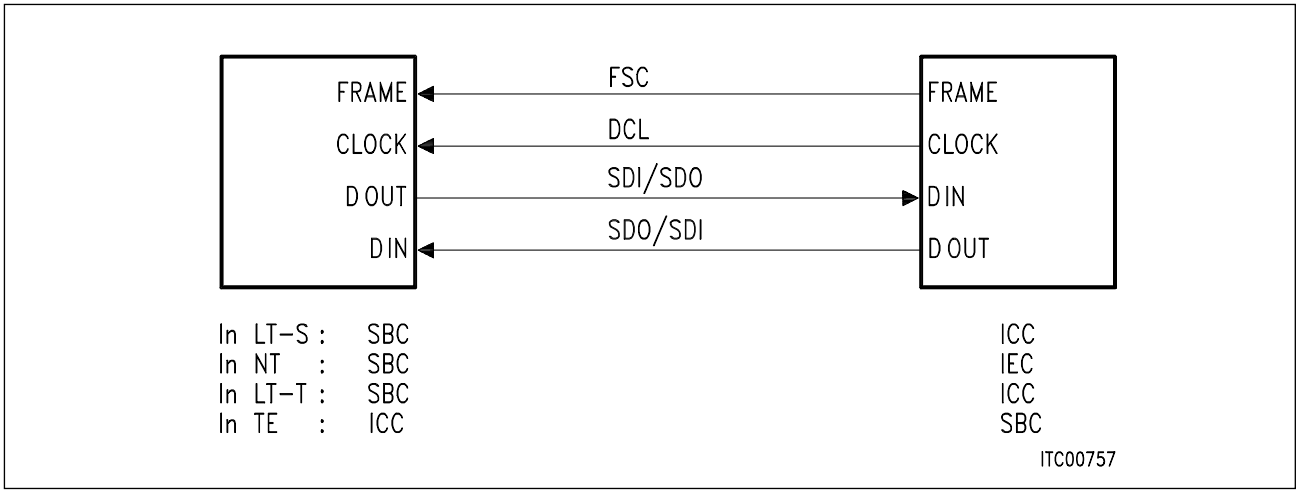


Figure 7
IOM® Interface Signals

The basic frame consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 bits of MONITOR and control information. The data in both directions are synchronous and in phase (**figure 8**).

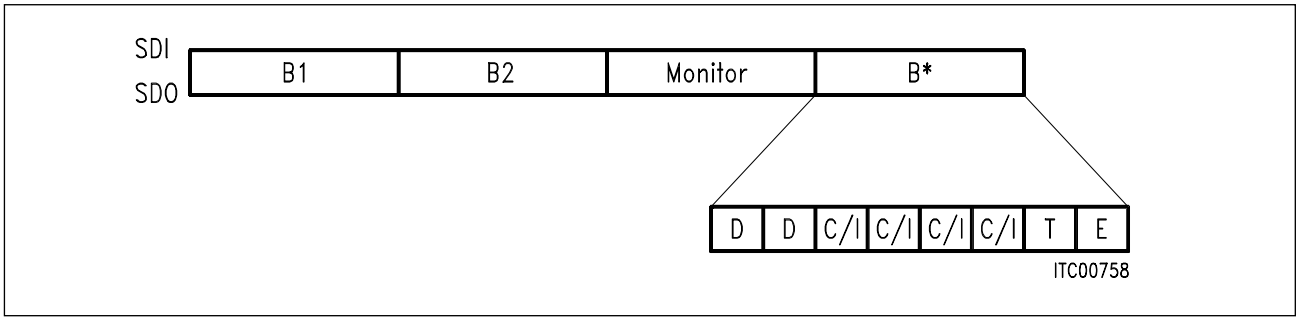


Figure 8
IOM® Interface Frame Structure

1st octet B1: B channel (64 kbit/s), most significant bit first
2nd octet B2 -"- -"-
3rd octet: MONITOR channel (64 kbit/s) -"-
4th octet B*: 2-bit D channel (16 kbit/s)
4-bit C/I channel
T channel: not used with SBC
E bit: not used with SBC.

The C/I channel is used for communication between the SBC and a processor via a layer-2 device, to control and MONITOR layer-1 functions. The codes originating from layer-2 devices are called "commands", those sent by the SBC are called "indications". For a list of the C/I codes and their use, refer to chapter 4.

Three modes of the IOM are distinguished. These modes differ only with respect to the physical data rate (256 or 8 x 256 kbit/s) and to polarity of the clocks.

IOM-1 Mode

This timing mode is applicable in all operating modes of the SBC.

Nominal bit rate of data (SDI and SDO):	256 kbit/s
Nominal frequency of DCL:	512 kHz
Nominal frequency of FSC:	8 kHz

Transitions of the data occur after even-numbered rising edges of DCL. Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of FSC and every second rising edge thereafter.

The frame is earmarked by the rising edge of FSC.

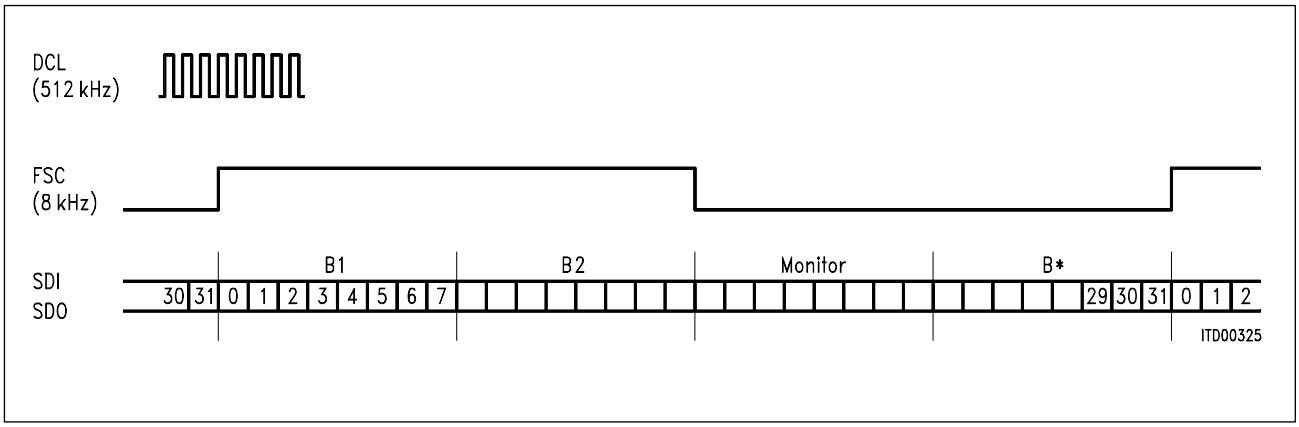


Figure 9
Timing of Data and Clocks of IOM® in the Normal Mode

Inverted Mode

Timing mode applicable in TE mode: 512 kHz

The characteristics are the same as above, except that FSC is not a signal with 50 %, duty cyc!e but an active low pulse, one DCL clock period long, which occurs in the middle of bit 27 (fourth bit of B*).

Timing mode applicable in LT-T and LT-S operating modes: 4096 kHz

Nominal bit rate of data bursts (SDI and SDO)	2048 kbit/s
Nominal frequency of DCL	4096 kHz
Nominal frequency of FSC	8 kHz.

The frame clock FSC is an active low strobe clock. The strobe earmarks the second half of bit no. 251 in the frame. The low state of the strobe is detected with the rising edge of DCL. Refer to **figure 10**.

The data at the input SDI is valid on the even-numbered rising edges of DCL. Transitions of the data on SDO occur after even-numbered falling edges of DCL. The rising edge earmarked by the frame strobe is an even-numbered rising edge of DCL. The following falling edge is an even-numbered falling edge.

The bursts are allocated to consecutive time slots in a frame by the static inputs X0 (TS0), X1 (TS1), X2 (TS2). **Table 2** indicates the allocations. **Figure 11** gives the positions of the respective frames.

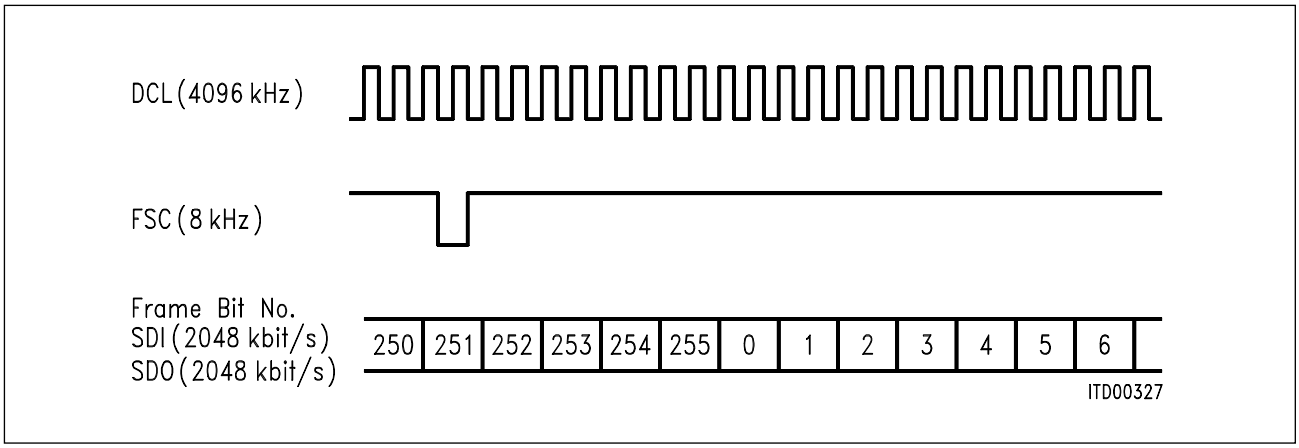


Figure 10
Timing of Data and Clocks of IOM® in the Inverted Mux Mode

IOM®-2 Mode

Timing mode applicable in LT-T and LT-S modes: 4096 kHz.

As opposed to inverted mode, data change with rising edges and frame synchronization is defined as in IOM-1 mode. (cf. IOM® Interface Specification, Rev. 2.2).

Table 2
Allocation of Time Slots

Time Slot No.	TS2	TS1	TS0	Bit No.
0	0	0	0	0 … 31
1	0	0	1	32 … 63
2	0	1	0	64 … 95
3	0	1	1	96 … 127
4	1	0	0	128 … 159
5	1	0	1	160 … 191
6	1	1	0	192 … 223
7	1	1	1	224 … 255

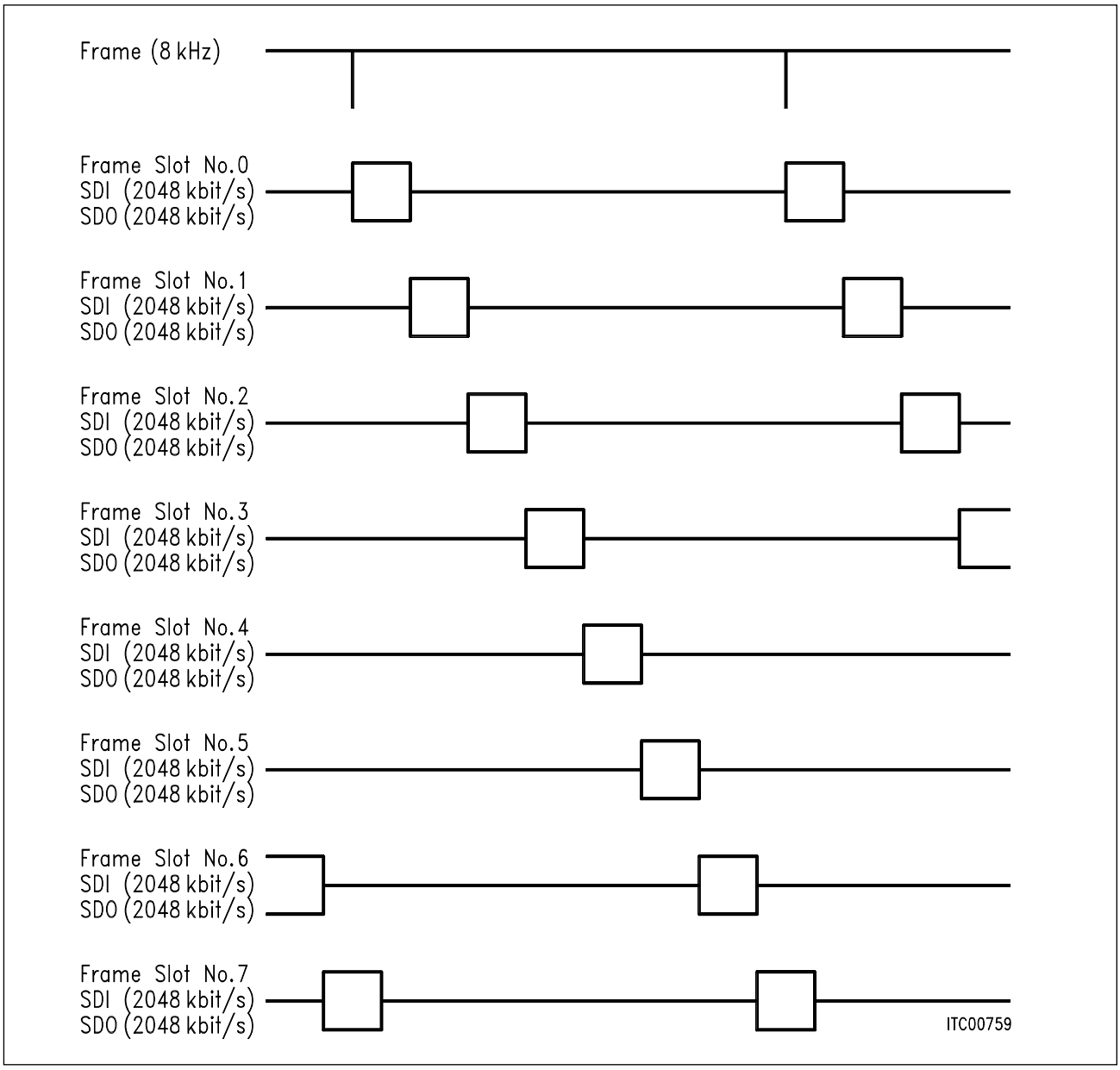


Figure 11
Position of IOM® Frames as a Function of Time Slot Allocation in IOM®-2 and Inverted Mode

The IOM-2 mode may be used to link up to eight SBC´s over a single 2048 kbit/s interface to an exchange or PABX (**figure 12**).

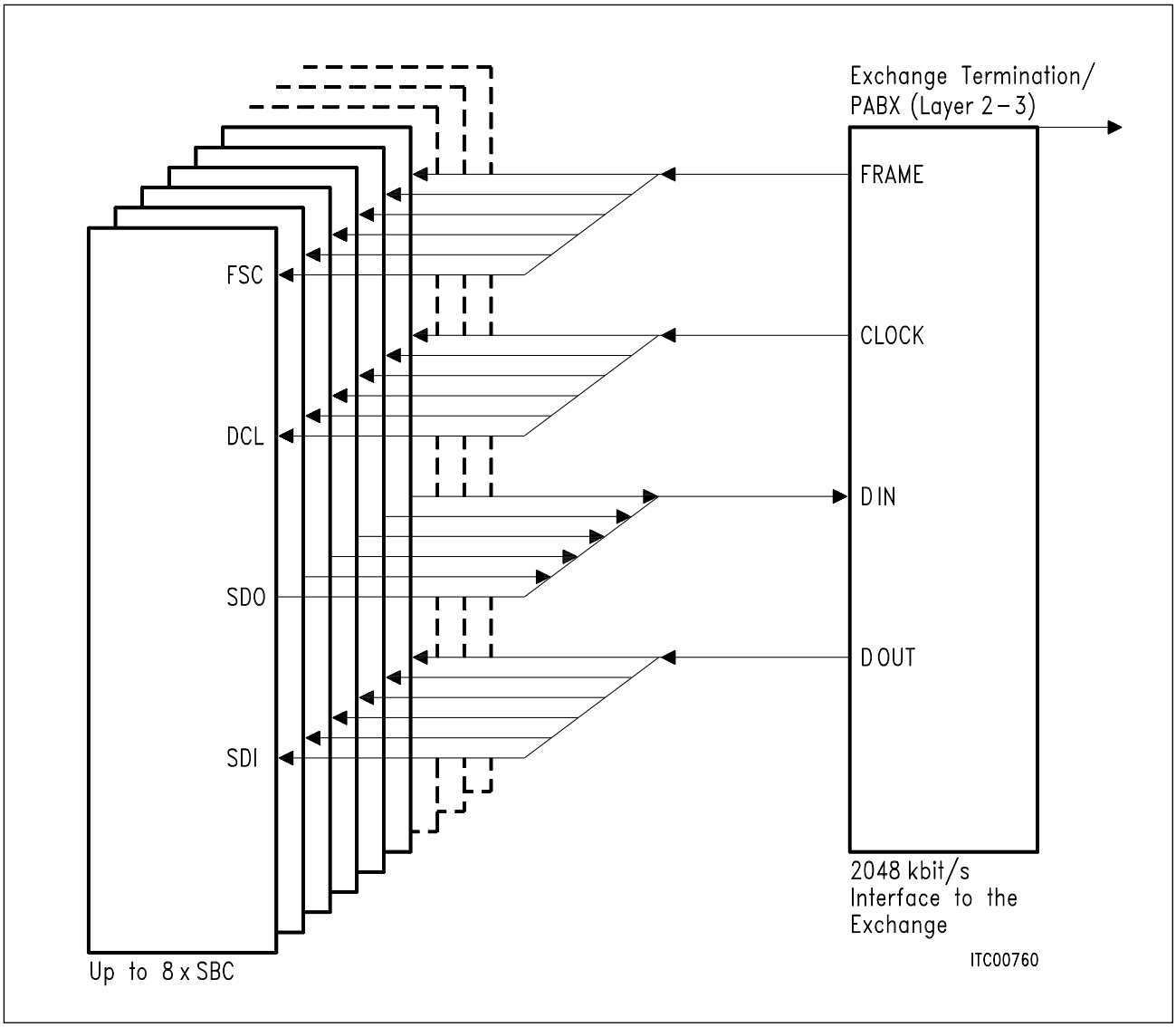


Figure 12
IOM® Interface 2048 kbit/s MUX Mode

2.4 Individual Functions

The SBC transmits data between the IOM interface and the line interface. The relative frame positions have been selected to minimize the round trip delays of the B channels, which are:

125 µs for TE, NT and LT-S in normal IOM mode, max. 250 µs for LT-T in normal IOM mode and LT-S in inverted mux mode and, finally, max. 375 µs for LT-T in inverted mux mode.

In the active state the data of the B channels are switched through transparently. The same applies to the D channel, except in TE mode where D-channel switching is subject to the S bus D-channel access procedure and collision detection.

S/T Interface Pre-Filter

In some applications it may be desirable to improve the signal-to-noise ratio of the received S/T interface signal by filtering out undesirable frequency (usually high frequency) components. This may be realized by an external pre-filter.

To simplify the implementation of this filter, an operational amplifier is integrated in the ISAC-S, as shown in **figure 13**. By connecting an RC network between input SR2 and the extra pin UFI an active RC filter of desired order can be realized (one example is shown in **figure 13b**).

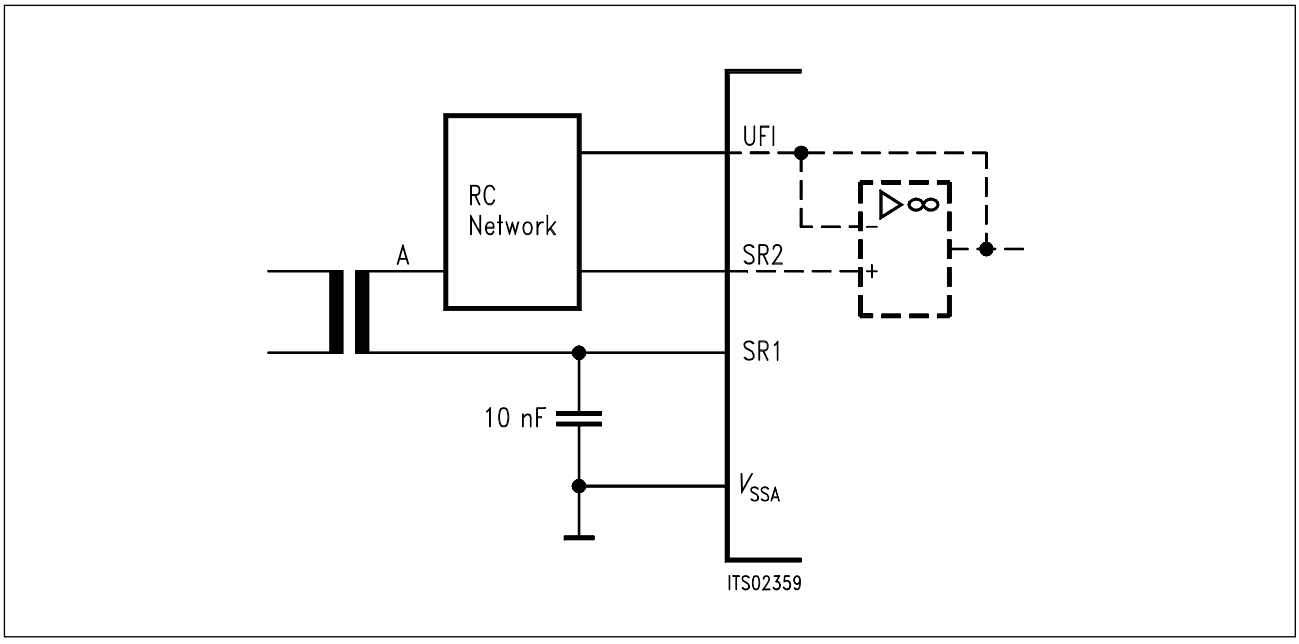


Figure 13a
Prefilter Connections

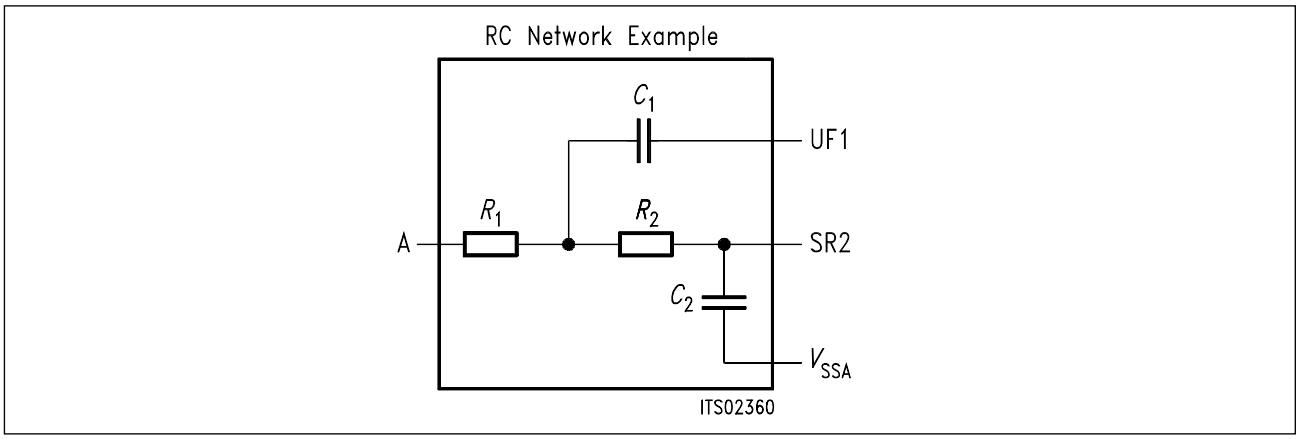


Figure 13b
Example of 2nd Order RC Network

Note:

Following component values are recommended to give a 500 kHz cutoff, and 600 nS (± 170 nS) propagation delay time:

$R_1 = R_2 =$ 10 kΩ
$C_1 =$ 13 pF
$C_2 =$ 22.5 pF

an extra delay may be introduced into the received signal by a filter.

NT and LT-S Applications

The 192-kHz transmit bit clock is synchronized to the IOM clock DCL. In the receive direction two cases have to be distinguished depending whether a bus or a point-to-point operation is programmed (pin X3:BUS).

Bus Operation

The 192-kHz receive bit clock is identical to the transmit bit clock, shifted by 4.6 µs with respect to the transmit edge. According to CCITT I.430, the receive frame shall be shifted by two bits with respect to the transmit frame.

Point-to-Point Operation

The 192-kHz receive bit clock is recovered from the receive data stream on the S interface (the sampling instant for the receive bits is shifted by 3.9 µs with respect to the leading edge of the derived receive clock). According to CCITT I.430, the receive frame can be shifted by 2-8 bits with respect to the transmit frame at the NT (LT-S) (Other shifts are allowed by SBC (including 0)).

This operation mode should also be used in extended passive bus applications.

E channel handling

For D-channel access collision resolution, the received D bit is in all cases transmitted as the E bit in the S-frames.

In addition, in the NT mode the echo bit may be made externally available, thus allowing for the implementation of a star configuration.

TE Application

The transmit and receive bit clocks are derived, with the help of the DPLL, from the S-interface

receive data strem.

The transmit frame is shifted by two bits with respect to the received frame. The output clocks CP,

DCL and FSC are synchronous to the S-interface timing.

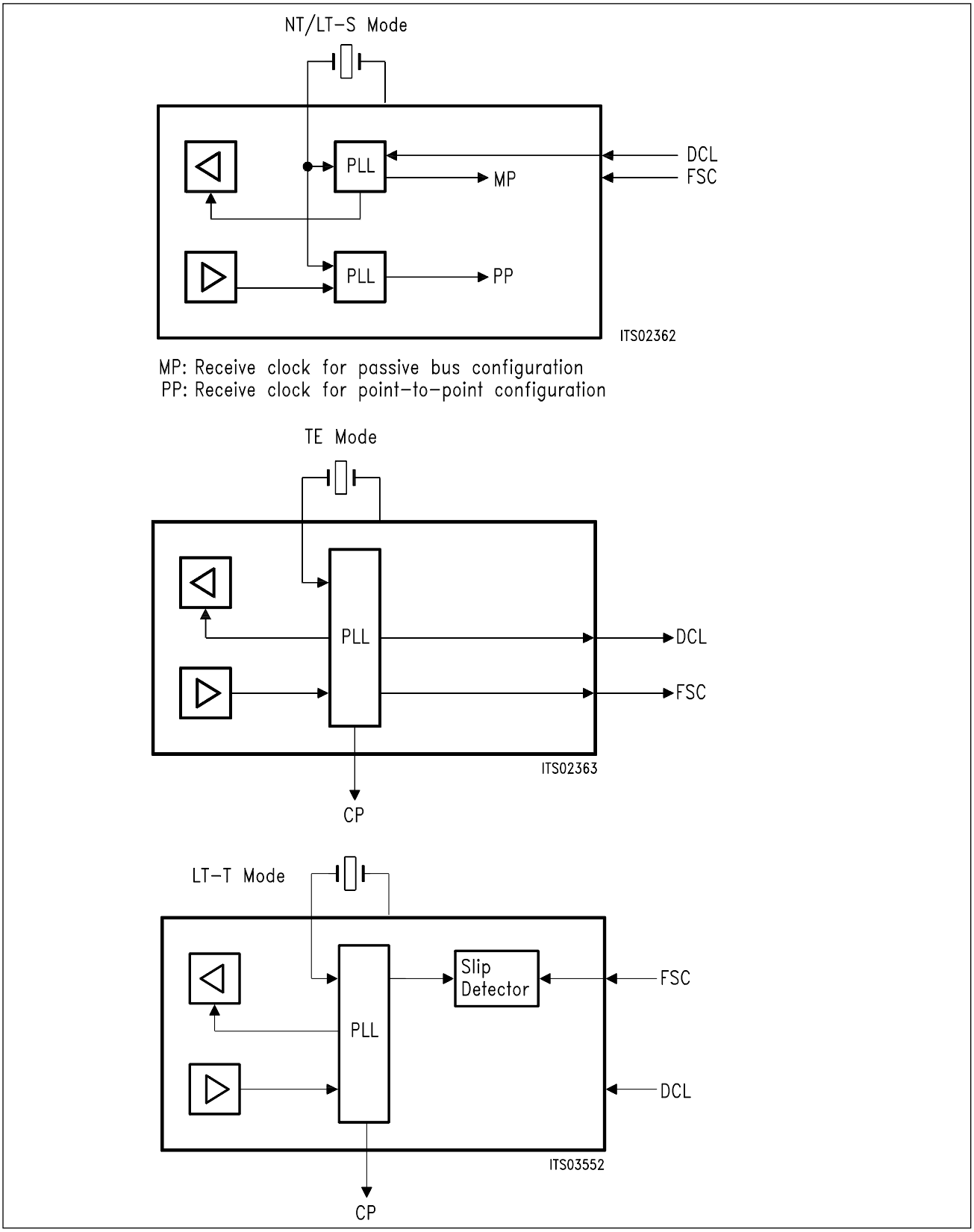


Figure 14
Clock System of the SBC

D-channel access control

The D-channel access control ensures that only one terminal shall have access to the D channel at any time. This is achieved through collision detection by each terminal (CCITT I.430). The SBC MONITORS the received D-echo channel, and, when transmission in the D channel is started, compares the echo bits to the transmitted D bits.

A mismatch between D bit and D-echo bit means that another terminal is also transmitting and a collision has taken place. This can only happen if D = 1 and D-echo = 0, since on the S bus a logical 0 overrides a logical 1 (thus the comparison of D echo with D bit is performed only when D echo = logical 0). The SBC immediately ceases transmission, returns to the D-channel monitoring state and sends 1's in the D channel. D-channel access is possible only after x consecutive 1's have been received in the echo channel. Depending on the priority class, x can be either eight or ten. If a terminal has successfully transmitted a complete HDLC frame, x is automatically increased by 1. X is reset to its initial value of eight (ten) when nine (eleven) consecutive 1's are received in the echo channel.

To enable initiating and interrupting HDLC frame transmission in the D channel, the SBC has to inform the layer-2 controller (ISDN Communication Controller) of the D-channel status — "ready" or "busy". For this, bit 20 of the IOM frame, in other words the fourth bit from the right in the MONITOR channel, is used: **see figure 15**.

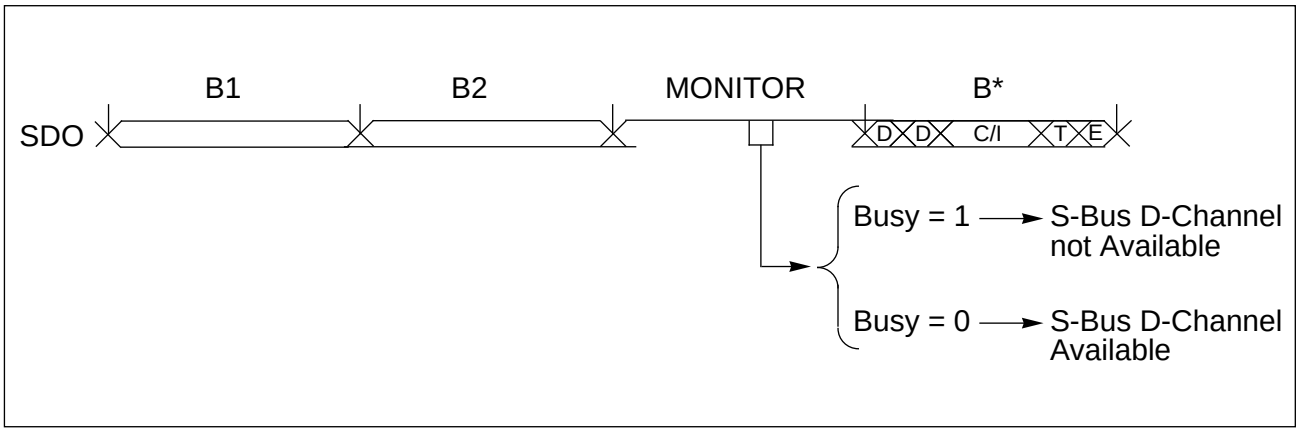


Figure 15
Position of BUSY Bit in IOM® Frame

By sending the BUSY bit at 0 to the ISDN Communication Controller in anticipation of the S-bus D-channel “ready” state, the first valid D bits will emerge from the SBC at exactly the moment an access is allowed.

D-channel switching (blocked: D = 1, or transparent: D = HDLC) is described by the state diagram in **figure 15a** with BUSY bit states “ready” and “busy” as input variables. **Figure 15b** shows the status diagram for “ready” and “busy”, with the following variables:

P: priority (8 or 10), set by a C/I channel command
C: number of consecutive ones appearing in the echo channel
V: V = 1 if: transmitted D bit = received D-echo bit
V = 0 otherwise
D_P: priority decrement for priority class P
(P = 8 or 10).

Thus state 1 is the state where a D-channel access may be attempted. The transition “1” - “2” occurs at the first zero of an opening flag (C = 0: zero observed in D-echo channel, and V = 1: a zero has actually been transmitted). Transition “i - 0” (i = 1,2,3) occurs at the first monitored zero in the echo channel when the station is idle (“1” - “0”), or if a collision either within an opening flag (“2” - “0”) or between the opening and closing flags (“3” - “0”) of an HDLC frame is observed. The successful transmission of a closing flag (“3” - “0” conditioned by C = 6) must be followed by a decrement in the priority class (D_P = 1). D_P is reset when 9 or 11 consecutive 1’s are observed (state “1”): cf CCITT I.430.

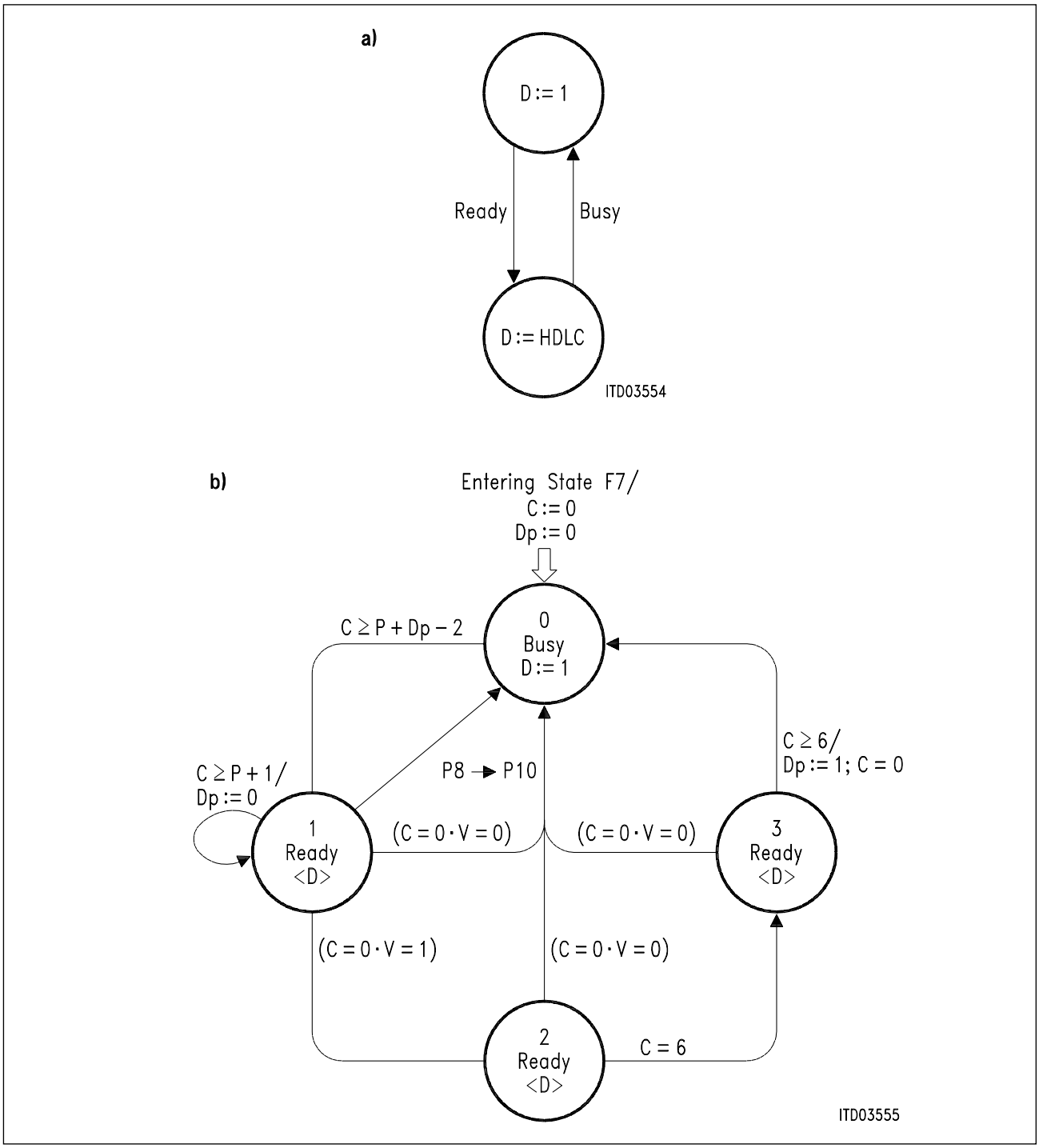


Figure 16
D-Channel Access Control of the SBC

Q Channel

The SBC provides Q-channel support by transmitting a binary “1” in each frame in which a “1” is received in the F_A-bit position of the NT-to-TE frame. Thus interference of F_A bits from one TE with the Q bits in passive bus configurations is avoided.

LT-T Application

As in TE applications, the receive 192-kHz clock is adaptively derived from the S-interface data. The transmit frame is shifted by two bits with respect to the receive frame.

The SBC provides a 512-kHz clock, CP, derived from the 192-kHz receive line clock with the DPLL. If necessary, this reference clock may be used to synchronize the central system (“NT2”) clock generator. The system timing is input over IOM interface bit and frame clocks, DCL and FSC. The relative position of the S and IOM frame is arbitrary. Moreover, the SBC prevents a slip from occurring if the wander between the DCL and CP clocks does not exceed a limit (The SBC enables intermediate storage of: $3xB_1$, $3xB_2$ and four D bits, for phase difference and wander absorption). ln case a wander greater than 24 µs is exceeded (cf CCITT Q.503), a warning is sent twice by the SBC in the C/l channel (“slip”).

If the analog test loop (TL3) is closed, the 192-kHz line clock is internally derived from DCL: therefore no slips can occur in this case.

Since only point to point configurations can be realized with the LT-T application, bus availability indication is not required. However, the D-echo bit is still monitored and interference-free transmission is indicated by the BUSY bit.

2.5 Additional Functions

Test Functions

Test loops

Two kinds of test loops may be closed in the SBC, which depend on the selected mode of operation. In both test loops, all three channels (B1, B2 and D) are looped back. In a “transparent loop” the data are also sent forward (in addition to being looped back), whereas in a “non-transparent loop” the forward data path is blocked (CCITT I.430). These test loops are shown in **figure 17**.

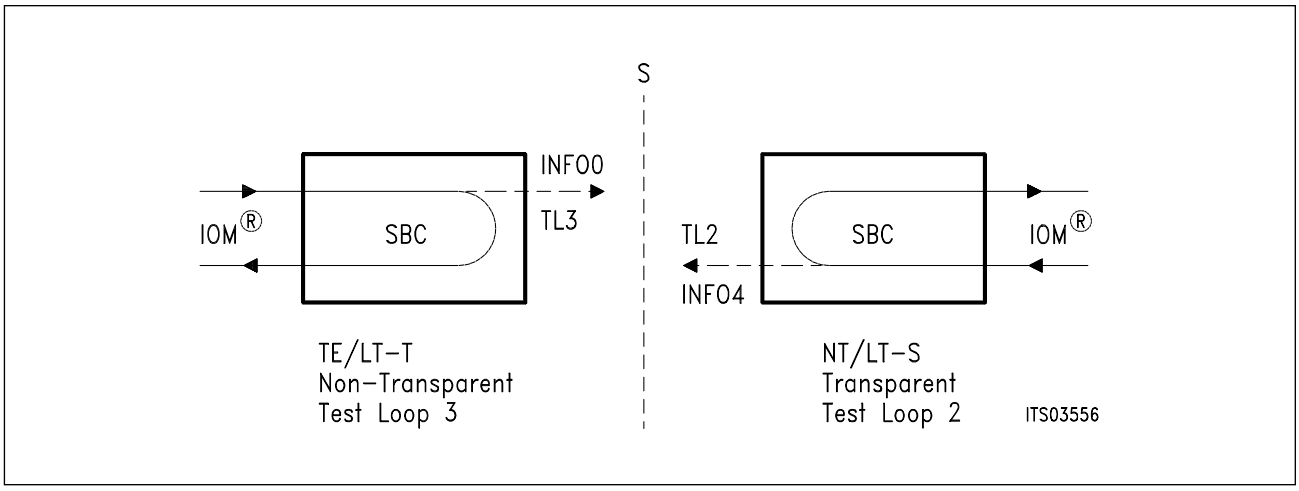


Figure 17
Test Loops of SBC

Test loop 3 is activated with the C/I channel command Activate Request Loop (ARL). An S interface is not required since INFO3 is looped back to the receiver. When the receiver has synchronized itself to this signal, the message “Test Indication’’ (or “Awake Test Indication”) is delivered in the C/I channel. No signal is transmitted over the S interface.

Test loop 2 is likewise activated over the IOM interface with Activate Request Loop (ARL). No S line is required. INFO4 is looped back to the receiver and also sent to the S interface. When the receiver is synchronized, the message “AIU” is sent in the C/I channel. In the test loop mode the S-interface awake detector is disabled, and echo bits are set to logical “0”.

Test Signals

Two kinds of test signals may be sent by the SBC: single pulses and continuous pulses.

The single pulses are of alternating polarity, one S-interface bit period wide, 0.25 ms apart, with a repetition frequency 2 kHz. Single pulses can be sent in all applications. The corresponding C/I command in TE, LT-S and LT-T applications is SSZ (Send single zeros). Alternatively, this test mode can be effected by pulling pin $\overline{\text{SSZ}}$ (pin X2, NT mode only) to logical “0”.

Continuous pulses are likewise of alternating polarity, one S-interface bit period wide, but they are sent continuously. The repetition frequency is 96 kHz. Continuous pulses may be transmitted in all applications. This test mode is entered in LT- S, LT-T and TE applications with the C/I command SCZ. Alternatively, pin $\overline{\text{SCZ}}$ (pin CP, NT mode only) can be pulled to logical “0”.

Special Applications

The mode specific pins X0-3 allow for special applications to be implemented, some of which are mentioned in the following.

Star Configuration

In NT mode, the SBC transmits the D-bit state over pin X0 (DE). A star configuration may be implemented by connecting pins X0 of several SBC’s together (open drain with integrated pull up). With X1 (DEX, **D**-E-**Ex**ternal mirrowing) tied to logical “1”, the SBC transmits the resulting DE (wired AND for all SBC’s) as the S-interface echo bit. **See figure 18**.

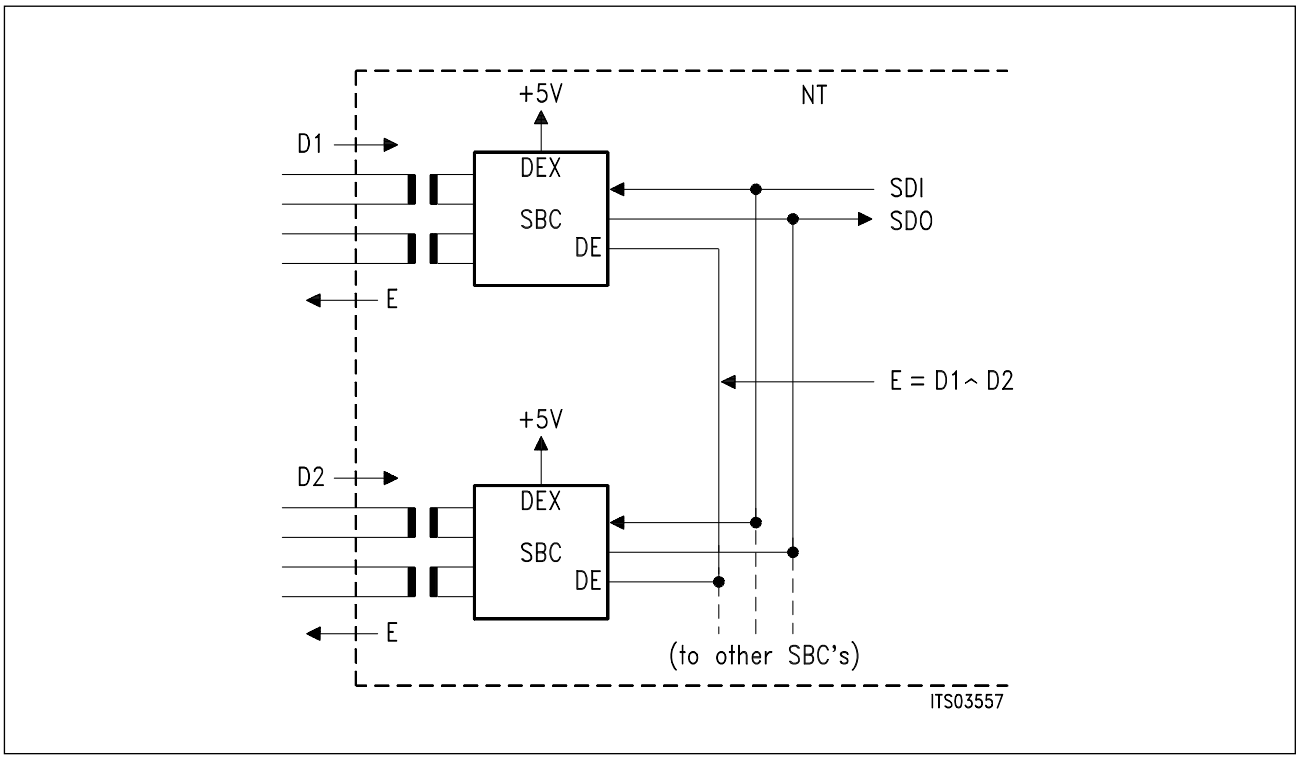


Figure 18
Star Configuration in NT

Use of ECHO

Local communication of terminals connected to an S bus may be implemented by using the auxiliary ECHO output (pin X2, in TE mode only). The timing of ECHO is identical to that of output SDO: however, the signal is “1” everywhere except in bit positions 24 and 25 of the IOM frame, where it is equal to the echo bits received from the S interface. Thus a layer-2 device (e.g. the ISDN Communication Controller PEB 2070) connected to ECHO is able to receive or “hear” all other terminals. As a special application, an S-bus local area network may be built using several TE SBC’s and one NT (or an NT star configuration). Communication in the D and E channel is half duplex.

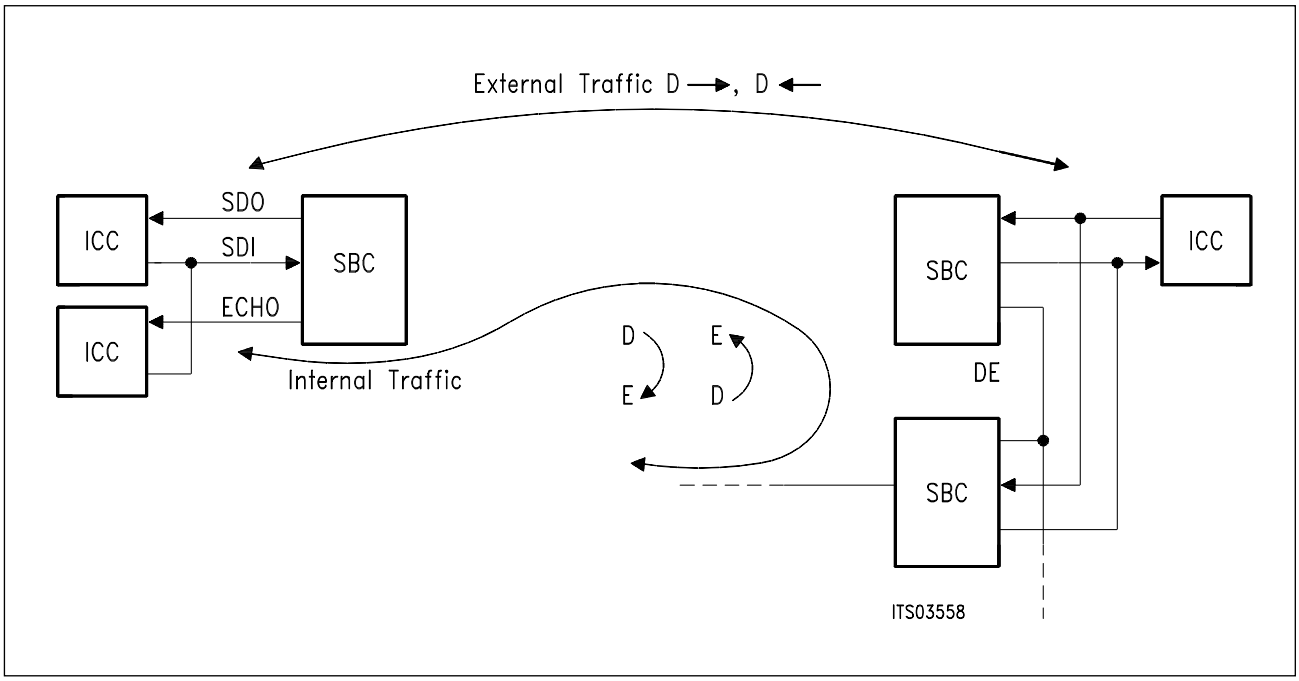


Figure 19
Star Configuration in NT

3 Operational Description

3.1 General

The internal finite state machine of the SBC controls the activation/deactivation procedures, switching of test loops and transmission of special pulse patterns. Such actions can be initiated by signals on the S transmission line (INFO's) or by control (C/I) codes sent over the IOM interface.

The exchange of control information in the C/I channel is state oriented. This means that a code in the C/I channel is repeated in every IOM frame until a change is necessary. A new code must be found in two consecutive IOM frames to be considered valid (double last look criterion).

3.2 Clocking, Reset and Initialization

In LT-T and LT-S applications the IOM interface should be kept active, i.e. the clocks DCL and FSC are always present. In this case commands in the C/I channel may also be handed over to the SBC in the "power down" state (state F3 for LT-T/state G1 for LT-S: **see figures 24 and 25**).

In TE and NT applications the IOM interface can be switched off in the inactive state, reducing power consumption to a minimum (on the order of 5 mW and 6.5 mW for PEB and PEF, respectively). In this deactivated state the clock lines are low and the data lines are high.

For the TE case the procedure is shown in **figure 20**. After detecting the code DIU (Deactivate Indication Upstream, i.e. from TE to NT/LT-S) from the downstream unit, the SBC responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I channel bit of the fourth frame.

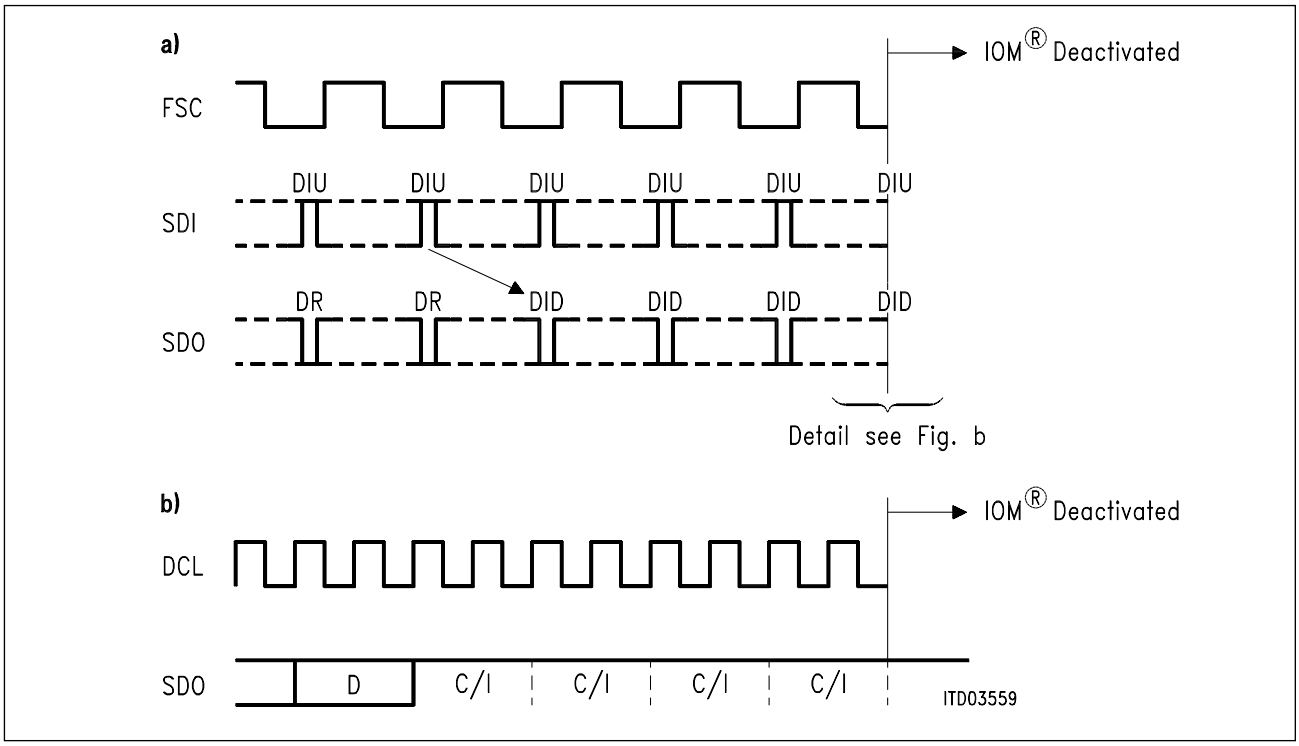


Figure 20
Deactivation of the IOM® Interface

In NT mode the IOM interface is activated by the upstream unit turning on the clocking signals. Simultaneously the upstream unit must send the desired command in the C/I channel. In the case where activation is requested from a terminal, the NT SBC first requests timing on the IOM interface by pulling SDO to a static low level. The SBC enters the power-up state immediately after timing has been applied. The clock signals may be switched off after the code Deactivation Indication Downstream has been sent twice by the upstream unit.

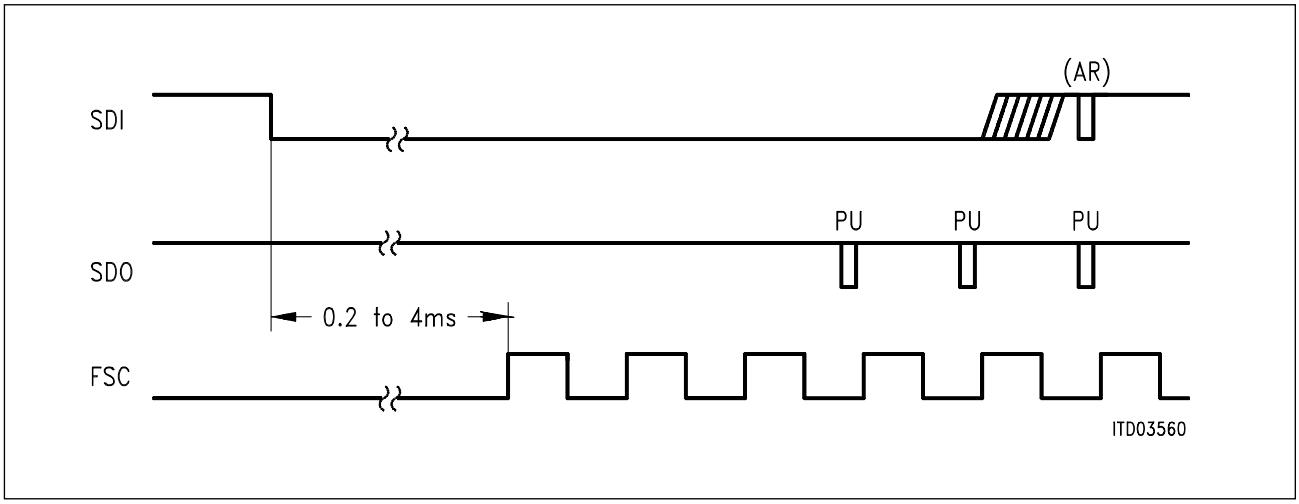


Figure 21
Activation of the IOM® Interface

As an alternative to clock activation via SDI, the asynchronous wake-up pin $\overline{\text{ENCK}}$ (X3 in TE mode) can be grounded. In this case the timing given in **figure 22** applies. When $\overline{\text{ENCK}}$ is tied to ground the IOM-clock pulses are delivered by SBC at all times.

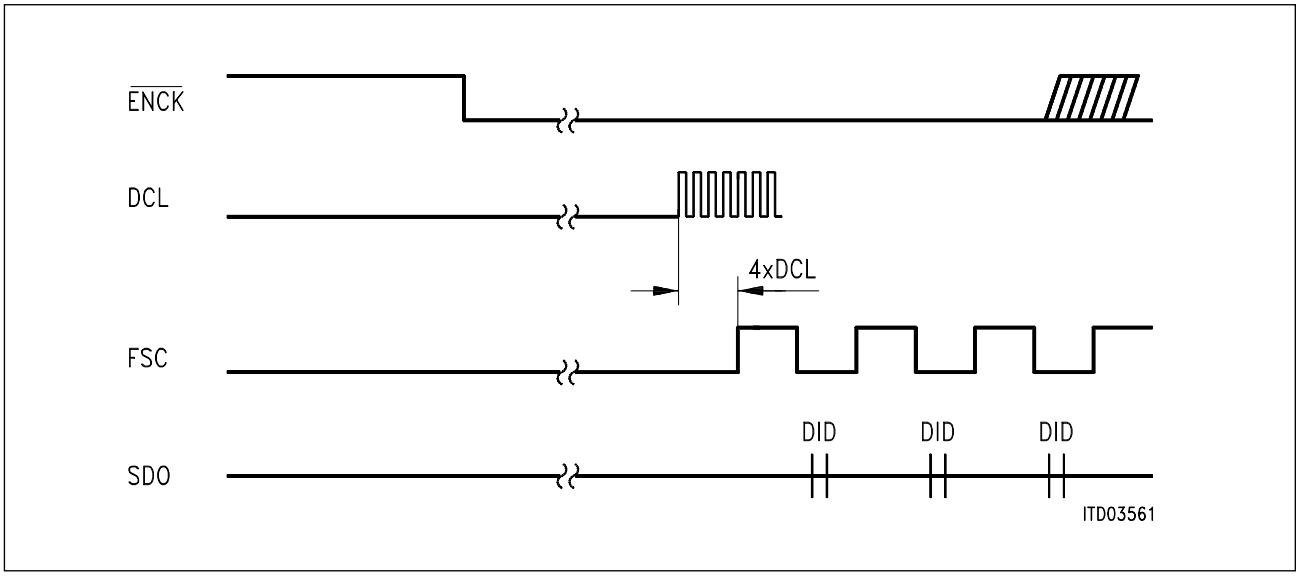


Figure 22
Activation of the IOM® Interface via $\overline{\text{ENCK}}$ (pin X3) in TE Mode (NB: DCL out of scale)

The clock pulses will be enabled again when the SBC recognizes a low level on SDI (command Timing TIM = “0000”) or when a non-zero level on the S line interface is detected. The clocks are turned on after approximately 0.5 to 4 ms (dependent on the capacitances on XTAL 1/2).

After the clocks have been enabled this is indicated by the PU code in the C/I channel. The downstream unit may then insert a valid code in the C/I channel. The continuous supply of timing signals by the SBC is ensured as long as there is no DIU command in the C/I channel. If timing signals are no longer required and activation is not yet requested, the downstream unit may indicate this by sending DIU.

At power up, a reset pulse ($\overline{\text{RST}}$) should be applied to bring the SBC to a well defined state. This state is G1 for NT or LT-S mode, and F3 for TE or LT-T mode. The oscillator and energy intensive analog components are disabled and the S-line awake detector is active after the pulse. All outputs are in high impedance state during the hardware reset pulse. In TE mode when $\overline{\text{ENCK}}$ is grounded, however, the SBC will still supply IOM timing during a reset pulse, and the message “Error Indication” EI is present in the C/I channel. Similarly, in NT mode, activation of pin CP brings the outputs to low impedance during a reset pulse and the message EI is sent in the C/I channel.

3.3 Control of Layer 1

The state diagrams are shown in **figures 24 to 26**. The activation/deactivation implemented by the SBC in its different operating modes agrees with the requirements set forth in CCITT recommendations. State identifiers F1-F8 (TE/LT-T) and G1-G4 (NT/LT-S) are in keeping with CCITT I.430. In the NT mode the four states have been expanded to implement a full handshake between the ends of the subscriber loop.

In the state diagrams a notation is employed which explicitly specifies the inputs and outputs on the S interface and in the C/I channel: **see figure 23**.

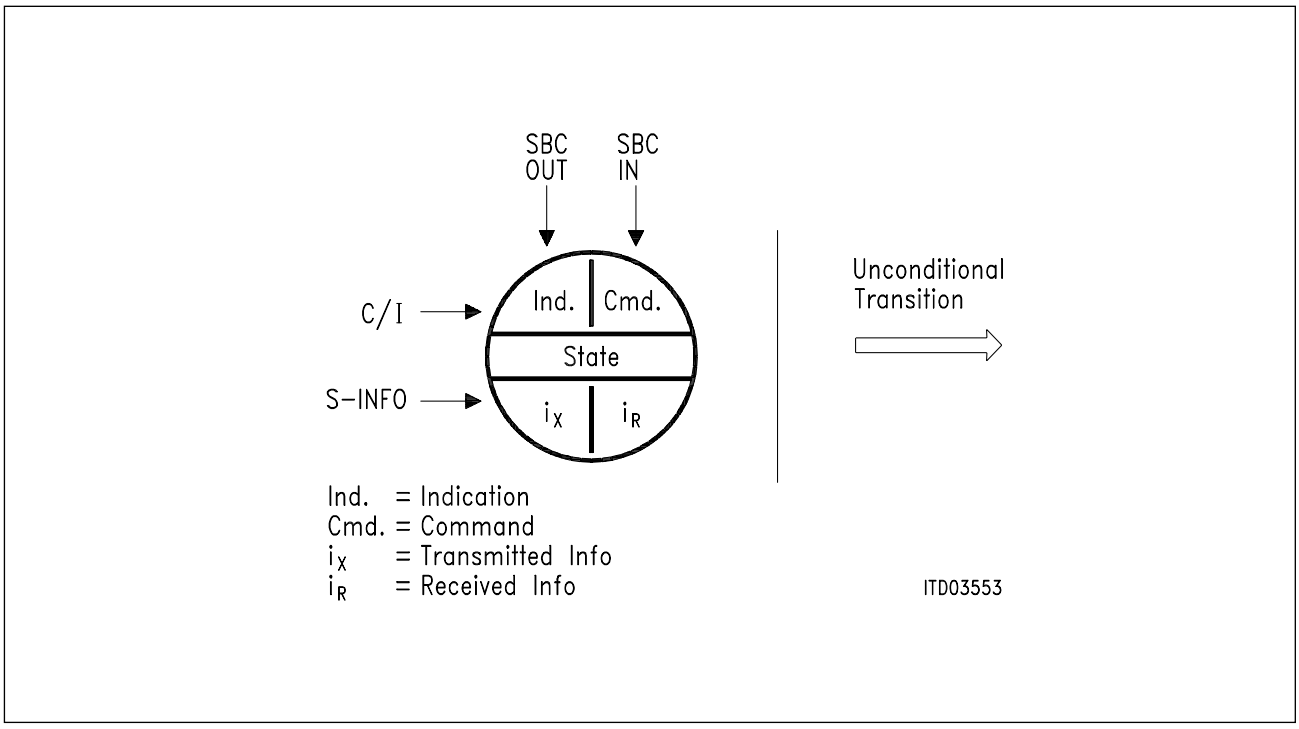


Figure 23

Commands / Indications and State Diagrams in TE / LT-T

Table 5

Command (upstream)	Abbr.	Code	Remark
Timing	TIM	0000	Activation of all output clocks is requested
Reset	RS	0001	(x)
Send continuous zeros	SCZ	0100	Transmission of pseudo-ternary pulses at 96-kHz frequency (x)
Send single zeros	SSZ	0010	Transmission of pseudo-ternary pulses at 2-kHz frequency (x)
Activate request, set priority 8	AR8	1000	Activation command, set D-channel priority to 8
Activate request, set priority 10	AR10	1001	Activation command, set D-channel priority to 10
Activate request loop	ARL	1010	Activation of test loop 3 (x)
Deactivate indication	DIU	1111	IOM interface can be disabled

Indication (downstream)	Abbr.	Code	Remark
Power up	PU	0111	IOM clocking is provided
Deactivate request	DR	0000	Deactivation request by S
Slip detected	SD	0010	Wander is larger than 24 µs peak-to-peak
Disconnected	DIS	0011	Pin CON connected to GND
Error indication	EI	0110	($\overline{RST}$ = 0 & $\overline{ENCK}$ = 0) in TE, or RS
Level detected	RSY	0100	Signal received, receiver not synchronous
Activate request	ARD	1000	Info 2 received
Test indication	TI	1010	Test loop 3 activated or continuous zeros transmitted
Awake test indication	ATI	1011	Level detected during test loop
Activate indication with priority class 8	AI 8	1100	Info 4 received, D-channel priority is 8 or 9
Activate indication with priority class 10	AI 10	1101	Info 4 received, D-channel priority is 10 or 11
Deactivate indication	DID	1111	Clocks will be disabled, (in TE), quiescent state

(x) unconditional commands

TE / LT-T Mode

F3 power down

This is the deactivated state of the physical protocol.The receive line awake unit is active except during a $\overline{RST}$ pulse. Clocks are disabled if $\overline{ENCK}$ = 1 (TE mode). The power consumption in this state is approximately 22 mW when the clock is running, and 4 mW otherwise.

F3 power up

This state is identical to “F3 power down”, except for the C/I output message. The state is invoked by a C/I command TIM = “0000” (or SDI static low). After the subsequent activation of the clocks the PU message is outputted. This occurs 0,5 ms to 4 ms after application of TIM, depending on crystal capacitances. If, however, the SBC is disconnected from the S interface (CON = 0), the C/I message DIS is outputted.

F3 pend. deact.

The SBC reaches this state after receiving INFO0 (from states F5 to F8) for 16 ms (64 frames). This time constant is a “flywheel” to prevent accidental deactivation. From this state an activation is only possible from the line (transition “F3 pend. deact.” to “F5 unsynchronized”). A power down state may be reached only after receiving DIU.

F4 pend. act.

Activation has been requested from the terminal, INFO1 is transmitted, INFO0 is still received, “Power Up” is transmitted in the C/I channel. This state is stable: timer T3 (I.430) is to be implemented in software.

F5 unsynchronized

At the reception of any signal from the NT, the SBC ceases to transmit INFO1 and awaits identification of INFO2 or INFO4. This state is reached at most 50 s after a signal different from INFO0 is present at the receiver of the SBC.

F6 synchronized

When the SBC receives an activation signal (INFO2), it responds with INFO3 and waits for normal frames (INFO4). This state is reached at most 6 ms after an INFO2 arrives at the SBC (when the oscillator was disabled in “F3 power down”).

F7 activated

This is the normal active state with the layer-1 protocol activated in both directions. From state “F6 synchronized”, state F7 is reached at most 0,5 ms after reception of INFO4. From state “F3 power down” with the oscillator disabled, state F7 is reached at most 6 ms after the SBC is directly activated by INFO4.

F8 lost framing

This is the condition where SBC has lost frame synchronization and is awaiting re-synchronization by INFO2 or INFO4 or deactivation by INFO0.

Unconditional States

Loop3 closed

On Activate Request Loop command, INFO3 is sent by the line transmitter internally to the line receiver (INFO0 is transmitted to the line). The receiver is not yet synchronized.

Loop3 activated

The receiver is synchronized on INFO3 which is looped back internally from the transmitter. Data may be sent. The indication “TI” or”ATI” is output depending whether or not a signal different from INFO0 is detected on the S interface.

Test mode continuous pulses

Continuous alternating pulses are sent.

Test mode single pulses

Single alternating pulses are sent (2-kHz repetition rate).

Reset state

A software reset (RS) forces the SBC to an idle state where the analog components are disabled (transmission of INFO0) and the S line awake detector is inactive. Thus activation from the NT is not possible. Clocks are still supplied (TE mode) and the outputs are in a low impedance state.

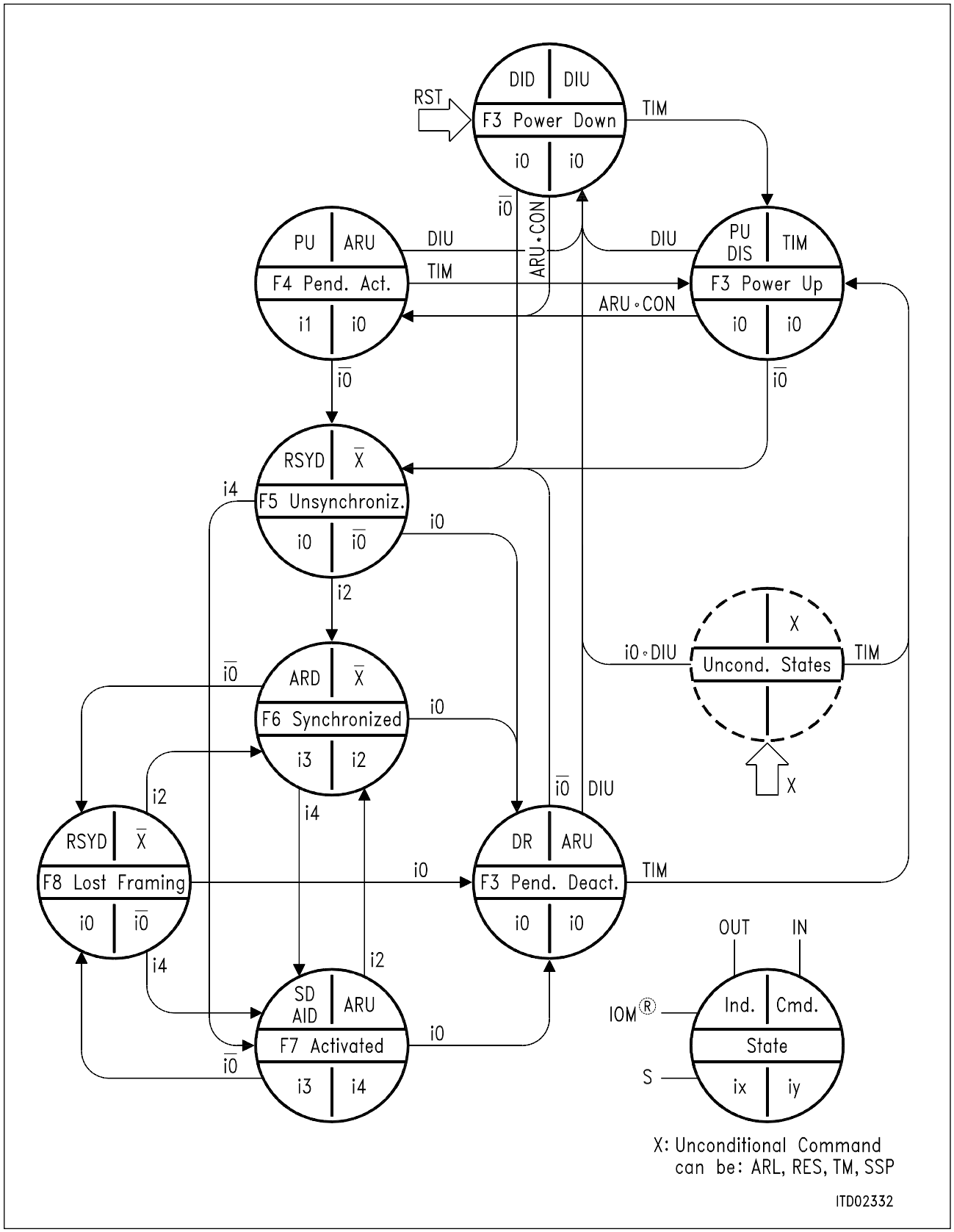


Figure 24a
State Diagram of TE/LT-T Mode

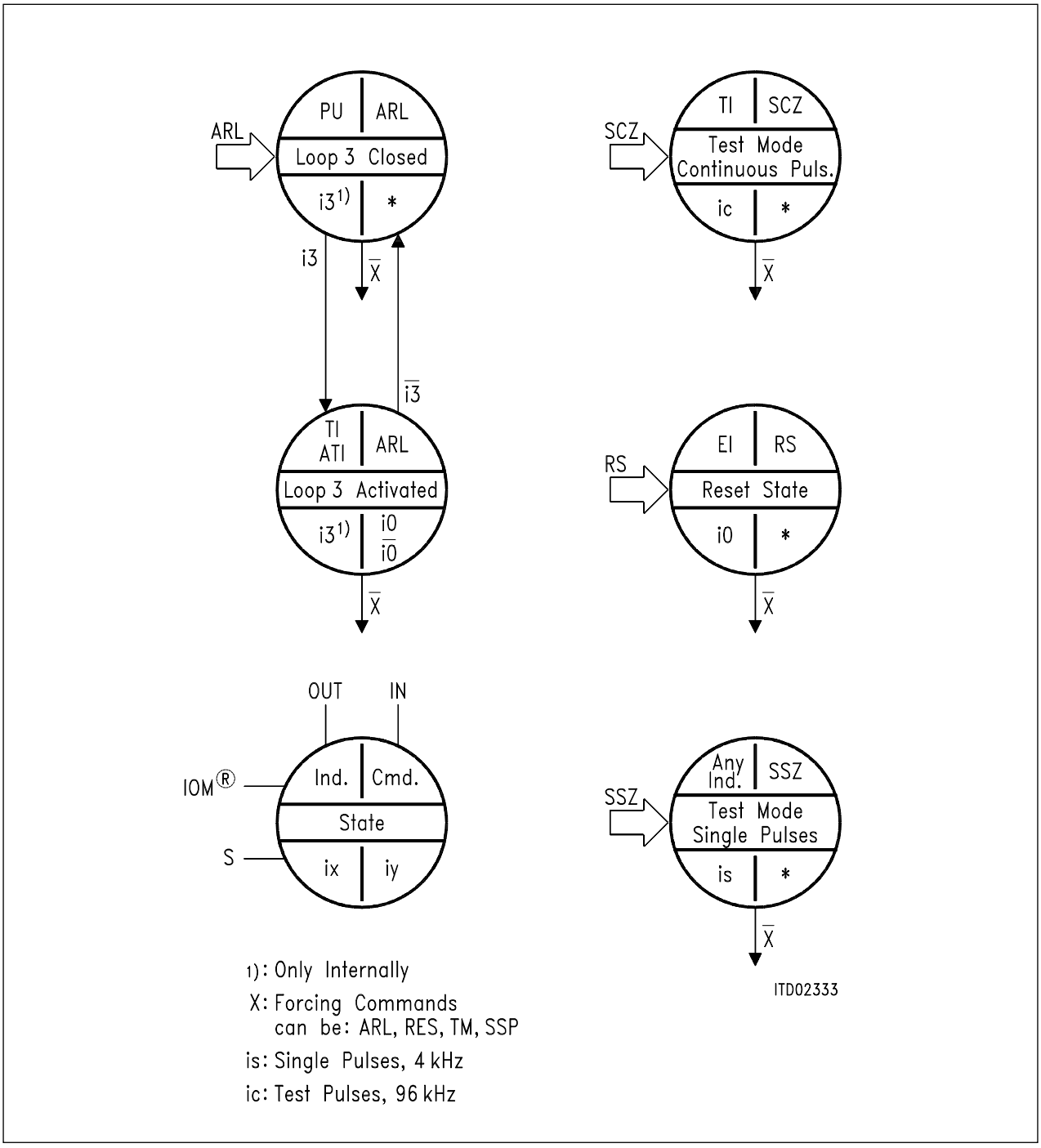


Figure 24b
State Diagram of TE/LT-T Mode: Unconditional Transitions

Commands / Indications and State Diagrams in LT-S Mode

Table 3

Command (downstream)	Abbr.	Code	Remark
Deactivate request	DR	0000	(x)
Send continuous zeros	SCZ	0010	Transmission of pseudo-ternary pulses at 96-kHz frequency (x)
Send single zeros	SSZ	0010	Transmission of pseudo-ternary pulses at 2-kHz frequency (x)
Activate request	ARD	1000	
Activate request loop	ARL	1010	Activation request for loop 2
Deactivate indication	DID	1111	Deactivation acknowledgement, quiescent state

Indication (upstream)	Abbr.	Code	Remark
Lost signal level	LSL	0001	No receive signal
Lost framing	RSYU	0100	Receiver is not synchronous
Activate request	ARU	1000	Info 1 received
Activate indication	AIU	1100	Synchronous receiver
Deactivate indication	DIU	1111	Timer (32 ms) expired or info 0 received (during 16 ms) after deactivation request

(x) unconditional commands

LT-S Mode

G1 deactivated

The SBC is not transmitting. No signal detected on the S interface, and no activation command is received in C/I channel.

G2 synchronized

As a result of an INFO1 detected on the S line or an ARD command, the SBC begins transmitting INFO2 and waits for reception of INFO3. INFO2 is sent after the awake detector has detected pulses during 4 ms. The timer to supervise reception of INFO3 is to be implemented in software.

G3 activated

Normal state where INFO4 is transmitted to the S interface. This state is reached less than 2 ms after an INFO3 first arrives at the SBC receiver. The SBC remains in this state as long as neither a deactivation or a test mode is requested, nor a reset pulse is issued.

When receiver synchronism is lost, INFO2 is sent automatically. After reception of INFO3, the transmitter keeps on sending INFO4. (Version A7 and following)

G4 pend. deact.

This state is triggered by a deactivation request DR. It is an unstable state: indication DIU (state “G4 unackn.”) is issued by the SBC when:

- either INFO0 is received during 16 ms,
- or an internal timer of 32 ms expires.

G4 unacknowleded

Final state after a deactivation request. The SBC remains in this state until a response to DIU (in other words DID) is issued, without which a new activation is impossible.

Test mode continuous pulses

Continuous alternating pulses are sent.

Test mode single pulses

Single alternating pulses are sent (2-kHz repetition rate).

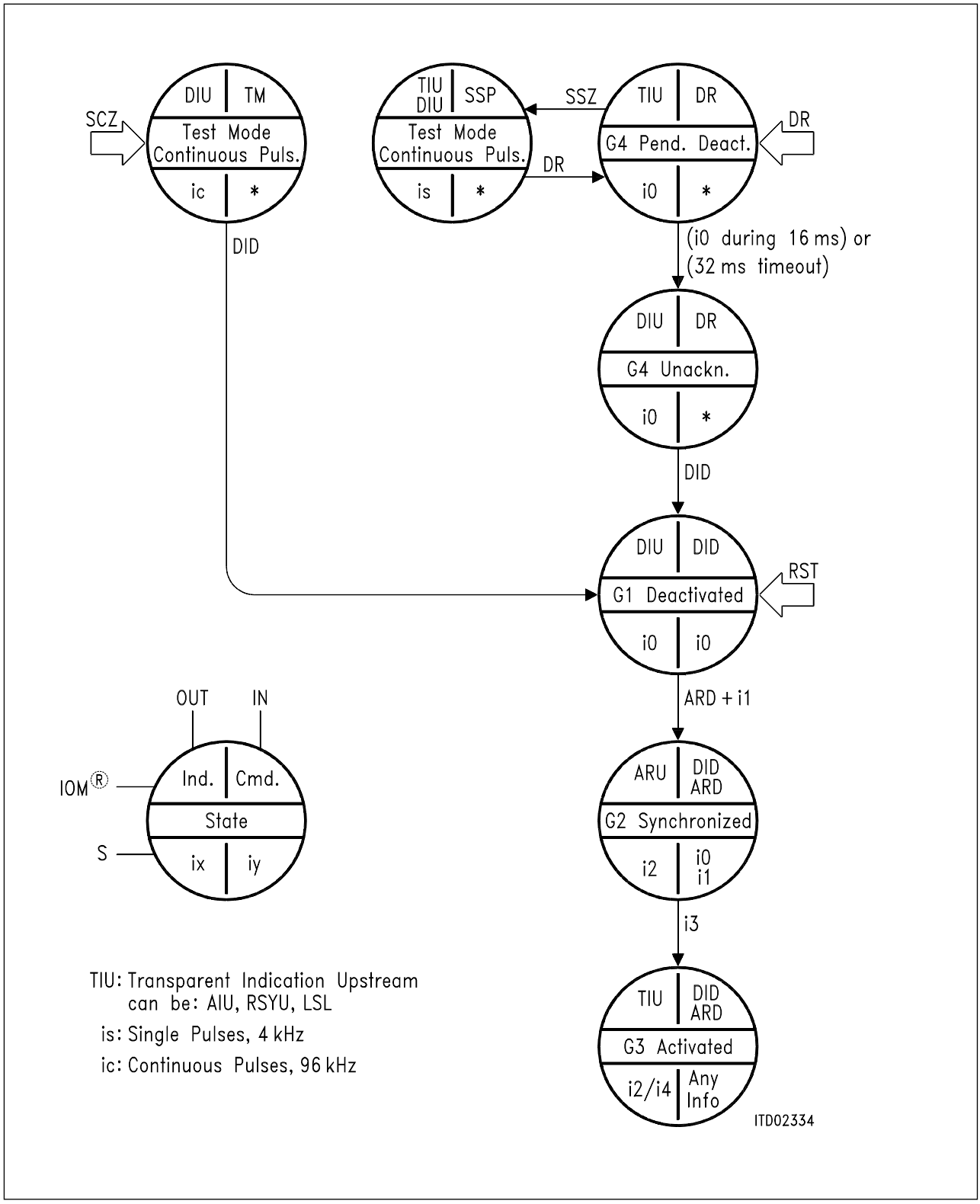


Figure 25
State Diagram of LT-S Mode

Commands / Indications and State Diagrams in NT

Table 4

Command (downstream)	Abbr.	Code	Remark
Deactivate request	DR	0000	(x)
Resynchronization of U-interface	RSYD	0100	Transmission of pseudo-ternary pulses at 96-kHz frequency after loss of synchronism of the U interface
Activate request	ARD	1000	Transmission of info 2
Activate request loop	ARL	1010	Transmission of info 2, switching of test loop 2
Deactivate indication	DID	1111	Deactivation acknowledgement, quiscent state
Activate indication	AID	1100	Transmission of info 4
Activate indication loop	AIL	1110	Transmission of info 4, switching of test loop 2
Send single zeros	SSZ	0010	Transmission of pseudo-ternary pulses at 2-kHz frequency (x)

Indication (upstream)	Abbr.	Code	Remark
Timing	TIM	0000	SBC requires clock pulses
Lost signal level	LSL	0001	No receive level
Lost framing	RSYU	0100	Receiver is not synchronous
Error indication	EI	0110	RST and SCZ both active
Activate request	ARU	1000	Info 1 received
Activate indication	AIU	1100	Synchronous receiver
Deactivate indication	DIU	1111	Timer (32 ms) expired or info 0 received (during 16 ms) after deactivation request

(x) unconditional commands

NT Mode

G1 deactivated

The SBC is not transmitting. No signal is detected on the S/T interface, and no activation command is received in C/I channel. EI is output as a response to $\overline{\text{RST}}$, DIU is output in the normal deactivated state, and TIM is output as a first step when an activation is requested from the S/T interface.

G1 i1 detected

An INFO1 is detected on the S/T interface, translated to an “Activation Request Upstream” indication in the C/I channel. The SBC is waiting for an ARD command, which normally indicates that the transmission line upstream (usually a two-wire interface) is synchronized.

G2 pend. act.

As a result of the ARD command, an INFO2 is sent on the S/T interface. INFO3 is not yet received.

G2 synchronized

INFO3 was received, INFO2 continues to be transmitted while the SBC waits for a “switch-through” command AID from the device upstream.

G3 activated

INFO4 is sent on the S/T interface as a result of the “switch through” command AID: the B and D channels are transparent. In case of loss of synchronism of the NT receiver, INFO2 is sent (Version A7 and following).

Lost framing U

On receiving a RSYD command which usually indicates that synchronization has been lost on the two-wire interface, the SBC transmits continuous alternating pulses.

G4 pend. deact.

This state is triggered by a deactivation request DR, and is an unstable state. Indication DIU (state “G4 unackn.”) is issued by the SBC when:

- either INFO0 is received during 16 ms
- or an internal timer of 32 ms expires.

G4 unacknowledged

Final state after a deactivation request. The SBC remains in this state until an “acknowledgment” to DIU (DID) is issued, without which a new activation is impossible.

Test mode continuous pulses

Continuous alternating pulses are sent.

Test mode single pulses

Single alternating pulses are sent (2-kHz repetition rate).

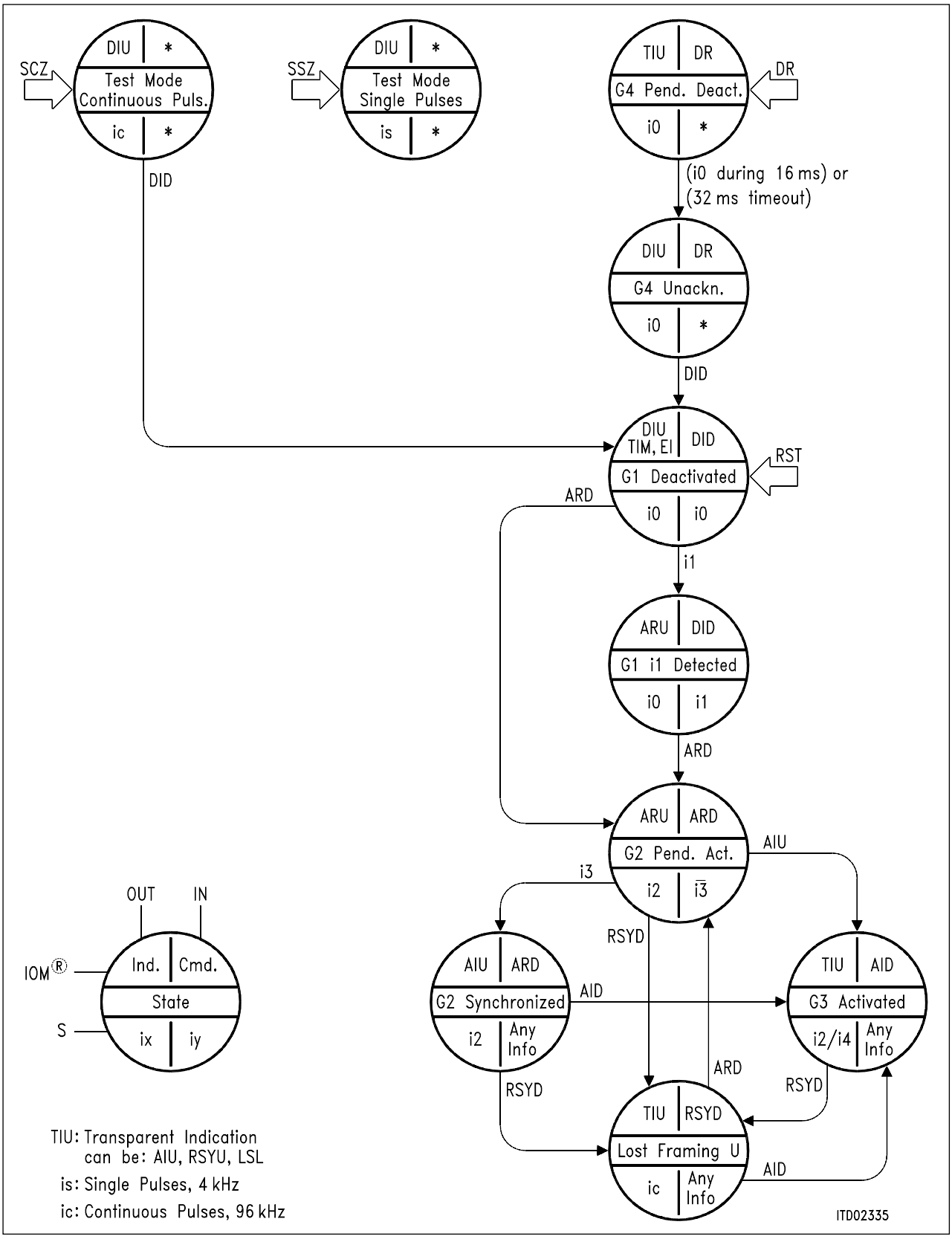


Figure 26
State Diagram of NT Mode

Example of Activation / Deactivation

An example of an activation/deactivation of the S interface, with the aforementioned time relationships, is shown in **figure 27**, in the case of an SBC in TE and LT-S modes.

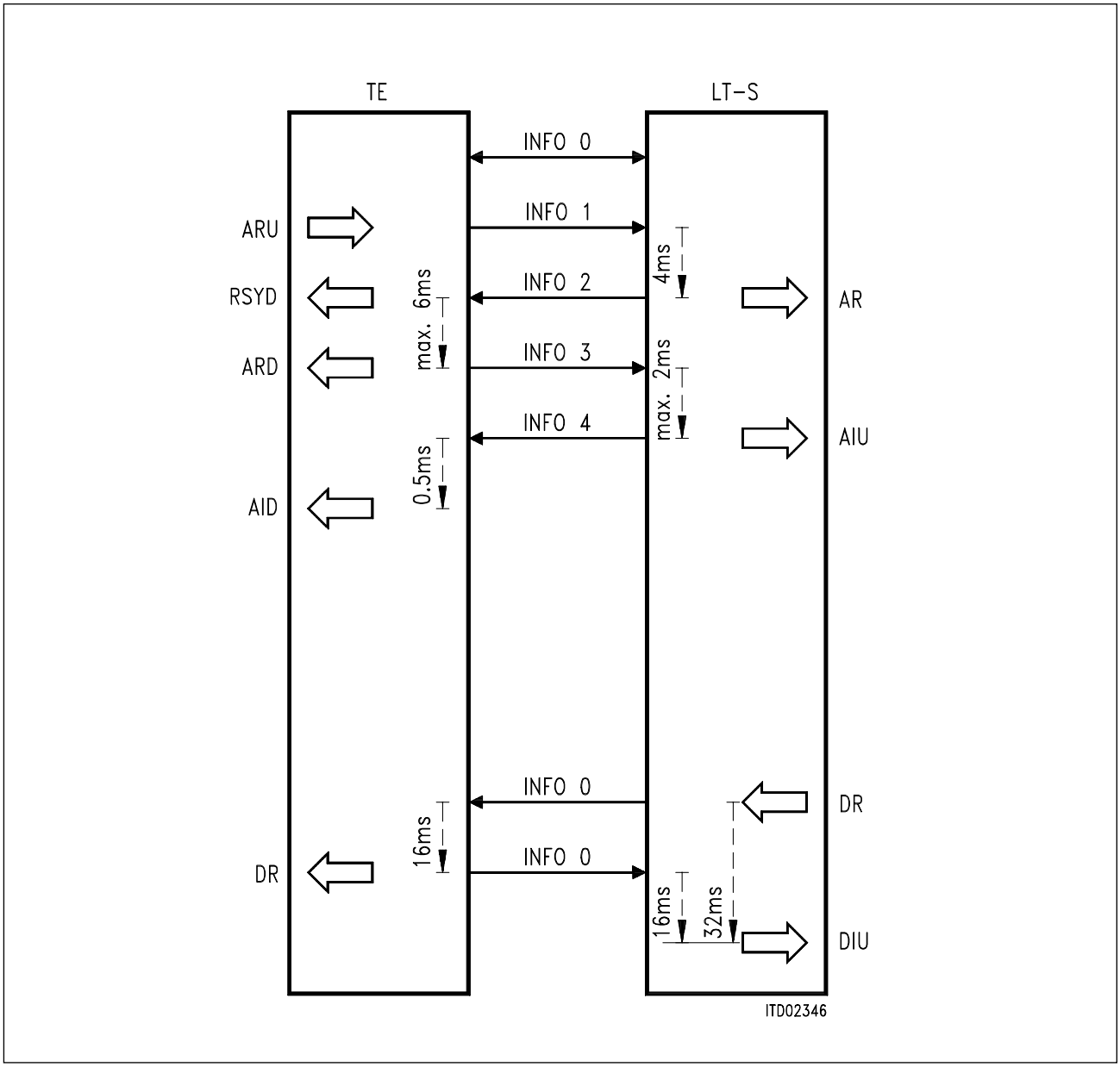


Figure 27
Example of Activation / Deactivation

4 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEB 2080 PEF 2080	 T_A T_A	 0 to 70 – 40 to 85	 ˚C ˚C
Storage temperature	T_{stg}	– 65 to 125	˚C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4 V	V
Power dissipation	P_D	1	W

Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse (**figure 28**).

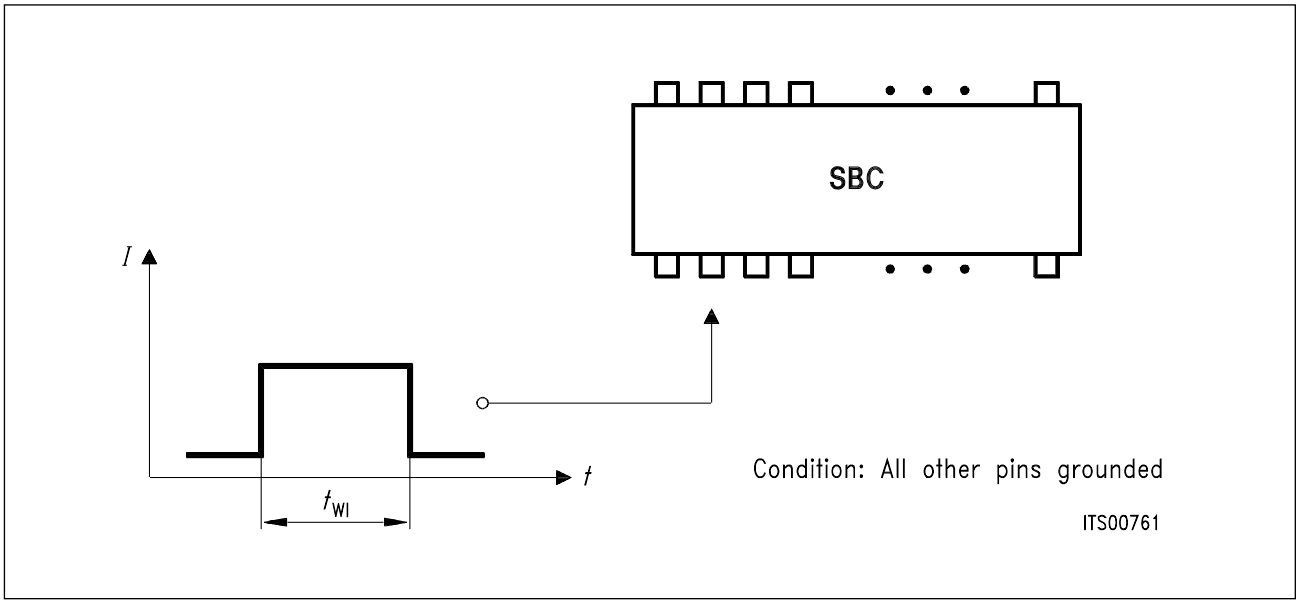


Figure 28
Test Condition for Maximum Input Current

Transmitter Input Current

The destruction limits for negative input signals with $R_i \geq 2\ \Omega$ and for positive input signals with $R_i \geq 200\ \Omega$ are given in **figure 29**.

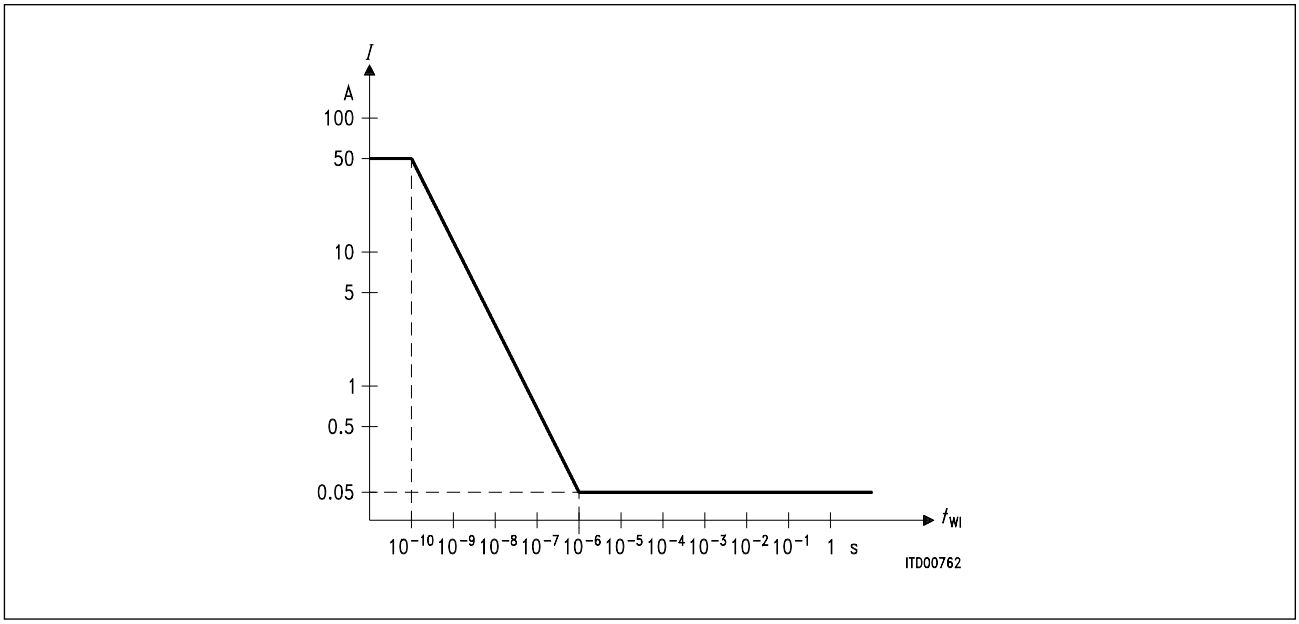


Figure 29

Receiver Input Current

The destruction limits are given in **figure 30**.

$R_i \geq 300\ \Omega$.

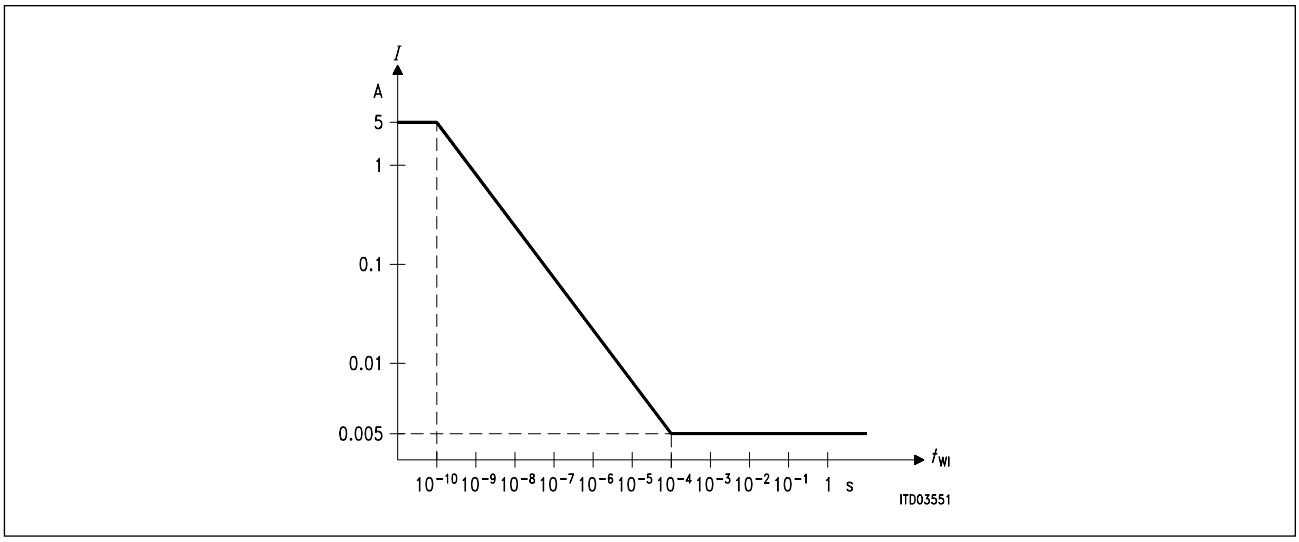


Figure 30

DC Characteristics

T_A = 0 to 70 ˚C;V_{DD} = 5 V 5 %, V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{DD} + 0.4	V	
L-output voltage L-output voltage (SDO)		V_{OL} V_{OL1}		0.45 0.45	V V	I_{OL} = 2 mA I_{OL} = 7 mA
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} – 0.5		V V	I_{OH} = – 400 µA I_{OH} = – 100 µA
Power supply current	operational	I_{CC}		13	mA	PEB 2080; V_{DD} = 5 V inputs at V_{SS}/V_{DD} no output loads
	power down			1	mA	
Power supply current	operational	I_{CC}		15	mA	PEF 2080; V_{DD} = 5 V inputs at V_{SS}/V_{DD} no output loads
	power down			1.3	mA	
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{IN} < V_{DD} to 0 V
Absolute value of output pulse amplitude (VSX2 - VSX1)		V_X	2.03 2.10	2.31 2.39	V V	R_L = 50 Ω [1) 2)] R_L = 400 Ω [1) 2)]
Transmitter output current		I_X	7.5	13.4	mA	R_L = 5.6 Ω [1)]
Transmitter output impedance		R_X	10		kΩ	inactive or during binary one
			80		Ω	during binary zero [3)] R_L = 50 Ω
Receiver output voltage		V_{SR1}	2.35	2.6	V	I_O < 5 µA
Receiver threshold voltage VSR1 - VSR2		V_{TR}	225	375	mV	dependent on peak level

Notes:

1) Due to the transformer, the load resistance as seen by the circuit is four times R_L.

2) The required 20 Ω output impedance is realised by external components.

3) The 80 Ω output impedance is required as external resistor.

Capacitances

T_A = – 40 to 85 °C, V_{DD} = 5 V ± 5 %, V_{SS} = 0 V, f_C = 1 MHz

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input capacitance I/O capacitance	C_{IN} C_{IO}		7 7	pF pF	All pins except SR1,2 XTAL1,2
Output capacitance against V_{ssa}	C_{OUT}		10	pF	SX1,2
Load capacitance	C_{LD}		50	pF	XTAL1,2

Recommended Oscillator Circuit

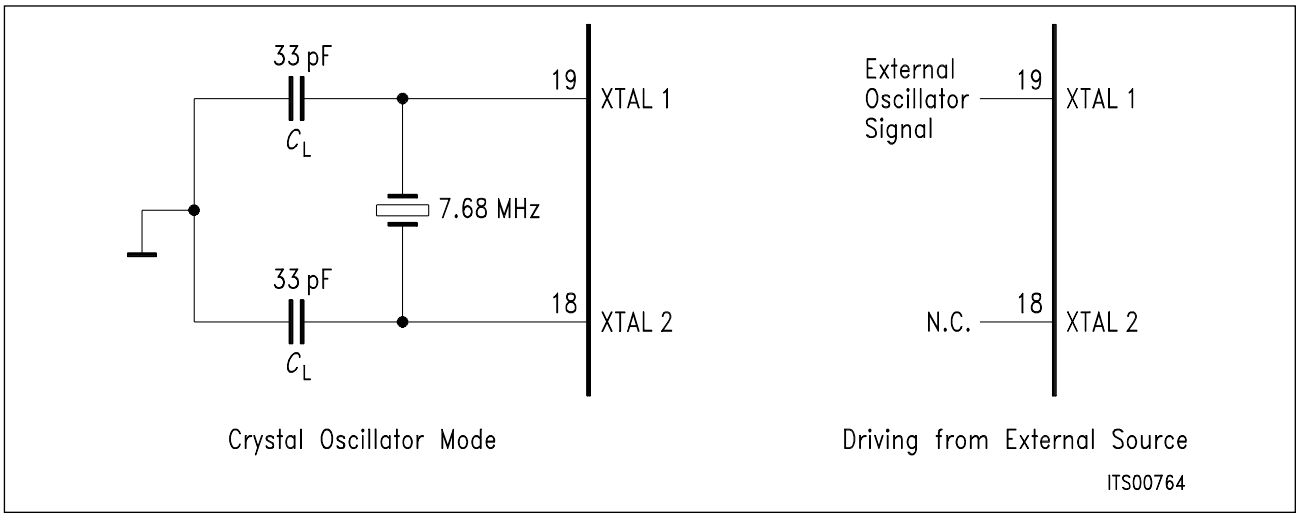


Figure 31

The integrated oscillator uses a parallel resonance crystal.

Unmeasured pins returned to ground.

Table 6
Output Stages

	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation of IOM Interface	Inverted Mode	Inverted Mode	IOM-1 Mode	IOM-2 Mode or Invert. Mode	IOM-1 Mode	IOM-1 Mode	IOM-2 Mode or Invert. Mode	IOM-1 Mode	IOM-1 Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCL	Push/ Pull	Push/ Pull	Push/ Pull						
FSC	Push/ Pull	Push/ Pull	Push/ Pull						
CP	Push/ Pull	Push/ Pull	Push/ Pull	Push/ Pull	Push/ Pull				
X2	Push/ Pull	Push/ Pull	Push/ Pull						Push/ Pull
X1	Push/ Pull	Push/ Pull	Push/ Pull					Push/ Pull	Push/ Pull
X0	Push/ Pull	Push/ Pull				open drain*			
SDO	Push/ Pull	Push/ Pull	Push/ Pull	open drain	Push/ Pull	open drain*	open drain	Push/ Pull	

*) with internal pull-up

Table 7
SBC Clock Signals

	*Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation of IOM Interface	**Inverted Mode**	**Inverted Mode**	**IOM-1 Mode**	**IOM-2 Mode or Invert. Mode**	**IOM-1 Mode**	**IOM-1 Mode**	**IOM-2 Mode or Invert. Mode**	**IOM-1 Mode**	**IOM-1 Mode**
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCL	o: 512 kHz* 1:2	o: 512 kHz* 1:2	o: 512 kHz* 2:1	i: 4096 kHz	i: 512 kHz	i: 512 kHz	i: 4096 kHz	i: 512 kHz	i: 512 kHz
FSC	o:8 kHz*	o:8 kHz*	o:8 kHz*	i:8 kHz	o:8 kHz*	1:1	i:8 kHz	i:8 kHz	i:8 kHz
CP	o: 1536 kHz 3:2	o: 1536 kHz 3:1	o: 1536 kHz 3:2*	o: 512 kHz* 2:1	o: 512 kHz* 2:1				
X2	o: 2560 kHz 1:2	o: 1280 kHz 1:2							o: 192 kHz* 1:1
X1	o: 3840 kHz 1:1	o: 3840 kHz 1:1	o: 3840 kHz 1:1					o: 7680 kHz 1:1	o: 7680 kHz 1:1
X0								i:fixed at 0	i:fixed at 0

Input and Output Pin Configurations

In TE, LT-T and LT-S IOM-1 modes an integrated pull-up resistor is connected to SDI. For output pin configurations, see **table 6**.

*) synchronized to S line

AC Characteristics

T_A = 0 to 70 ˚C, V_{DD} = 5 V ± 5 % for PEB 2080

T_A = – 40 to 85 ˚C, V_{DD} = 5 V ± 5 % for PEF 2080

The AC testing input/output waveform is shown below.

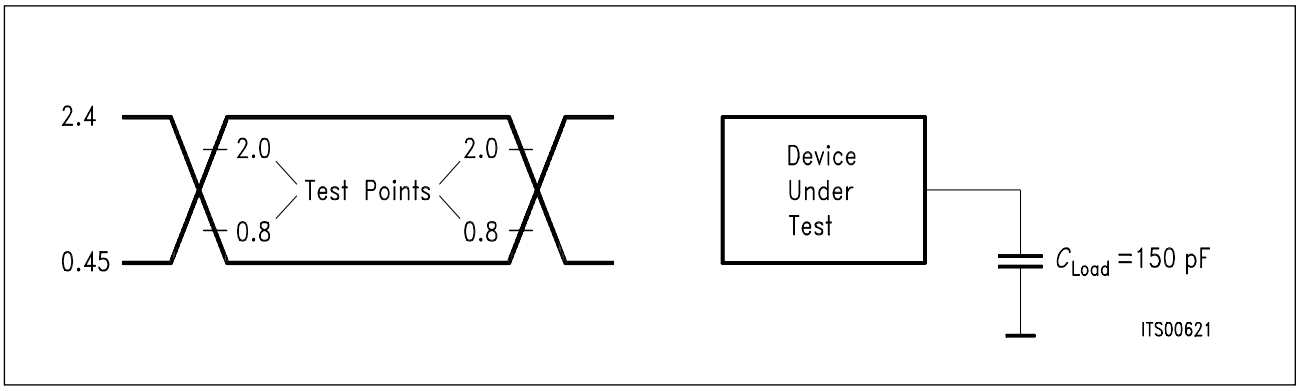


Figure 32
Input / Output Waveform for AC Test

Jitter

In TE mode, the timing extraction jitter of the SBC conforms to CCITT Recommendation I.430 (– 7 % to + 7 % of the S-interface bit period). In the NT and LT-S applications, the clock input DCL is used as reference clock to provide the 192-kHz clock for the S line interface. In the case of a plesiochronous 7.68-MHz clock generated by an oscillator, the clock DCL should have a jitter of less than 100 ns peak-to-peak. (In the case of a zero input jitter on DCL, SBC generates at most 130 ns “self-jitter” on S interface.) In the case of a synchronous (fixed divider ratio of 15 between XTAL1 and DCL) 7.68-MHZ clock (input XTAL1), the SBC transfers the input jitter of XTAL1, DCL and FSC to the S interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

Clock Timing

The clocks in the different operating modes are summarized in **table 7**, with duty ratios. Clock CP is phase-locked to the receive S signal, and is derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal (TE and LT-T). A phase tracking of CP with respect to “S” is performed once in 250 µs. As a consequence of this DPLL tracking, the high state of CP may be either reduced or extended by one 7.68 MHz period (CP duty ratio 2:2 or 4:2 instead of 3:2) once every 250 µs. Since DCL and FSC are derived from CP (TE mode), the high state (FSC) or the high or low state (DCL) may likewise be reduced or extended by the same amount once every 250 µs. (The phase adjustment may take place either in the sixth, seventh or eighth CP cycle counting from the beginning of an IOM frame in TE).

The phase relationships of the auxiliary clocks are shown in **figure 29**.

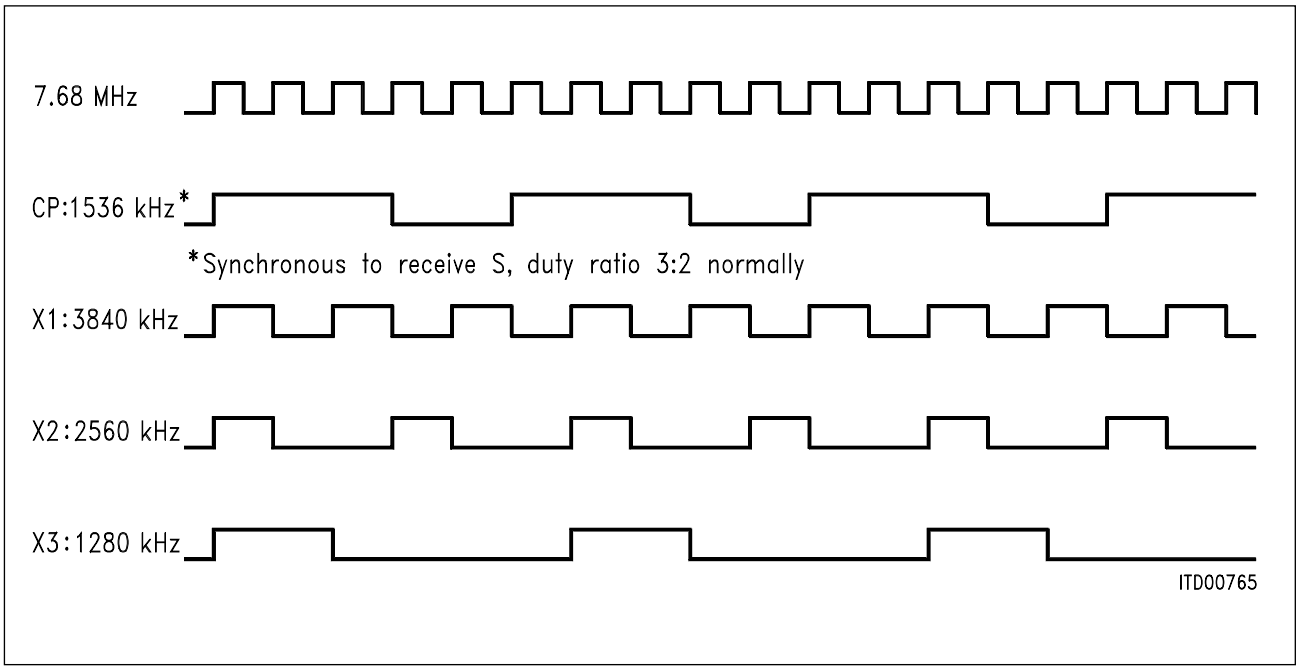


Figure 33
Phase Relationships of Auxiliary Clocks

Tables 8 to 12 give the timing characteristics of the clock.

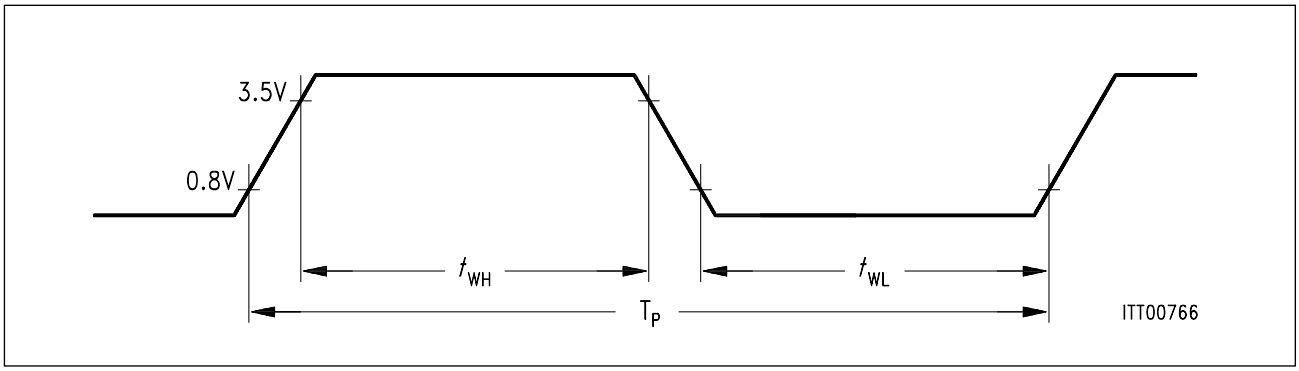


Figure 34
Definition of Clock Period and Width

Table 8
XTAL1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High phase of crystal/clock	t_{WH}	20		ns
Low phase of crystal/clock	t_{WL}	20		ns

Table 9
DCL

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
(TE) 512 kHz	t_{PQ}	1822	1953	2084	ns	OSC ± 100 ppm
(TE) 512 kHz 2:1	t_{WHQ}	1121	1302	1483	ns	OSC ± 100 ppm
(TE) 512 kHz 2:1	t_{WLQ}	470	651	832	ns	OSC ± 100 ppm
(TE) 512 kHz 1:2	t_{WHQ}	470	651	832	ns	OSC ± 100 ppm
(TE) 512 kHz 1:2	t_{WLQ}	1121	1302	1483	ns	OSC ± 100 ppm
(NT, LT-S, LT-T)	t_{WHI}	90			ns	OSC ± 100 ppm
(NT, LT-S, LT-T)	t_{WLI}	90			ns	OSC ± 100 ppm

Table 10
CP

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
(TE) 1536 kHz	t_{PQ}	520	651	782	ns	OSC ± 100 ppm
(TE) 1536 kHz	t_{WHQ}	240	391	541	ns	OSC ± 100 ppm
(TE) 1536 kHz	t_{WLQ}	240	260	281	ns	OSC ± 100 ppm
(TE, LT-T)	t_R , t_F			20 10	ns	C_L = 100 pF C_L = 50 pF
(LT-T) 512 kHz	t_{PQ}	1822	1953	2084	ns	OSC ± 100 ppm
(LT-T) 512 kHz	t_{WHQ}	1121	1302	1483	ns	OSC ± 100 ppm
(LT-T) 512 kHz	t_{WLQ}	470	651	832	ns	OSC ± 100 ppm

Table 11
X1

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
(TE) 3840 kHz	t_{PQ}	– 100 ppm	260	100 ppm	ns	OSC ± 100 ppm
(TE) 3840 kHz	$t_{W\,HQ}$	120	130	140	ns	OSC ± 100 ppm
(TE) 3840 kHz	$t_{W\,LQ}$	120	130	140	ns	OSC ± 100 ppm

Table 12
X2

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
(TE) 2560 kHz	t_{PQ}	– 100 ppm	391	100 ppm	ns	OSC ± 100 ppm
(TE) 2560 kHz	$t_{W\,HQ}$	110	130	150	ns	OSC ± 100 ppm
(TE) 2560 kHz	$t_{W\,LQ}$	250	260	270	ns	OSC ± 100 ppm
(TE) 1280 kHz	t_{PQ}	– 100 ppm	781	100 ppm	ns	OSC ± 100 ppm
(TE) 1280 kHz	$t_{W\,HQ}$	250	260	270	ns	OSC ± 100 ppm
(TE) 1280 kHz	$t_{W\,LQ}$	511	521	531	ns	OSC ± 100 ppm

CP, DCL and FSC Relationships in IOM® Master Mode

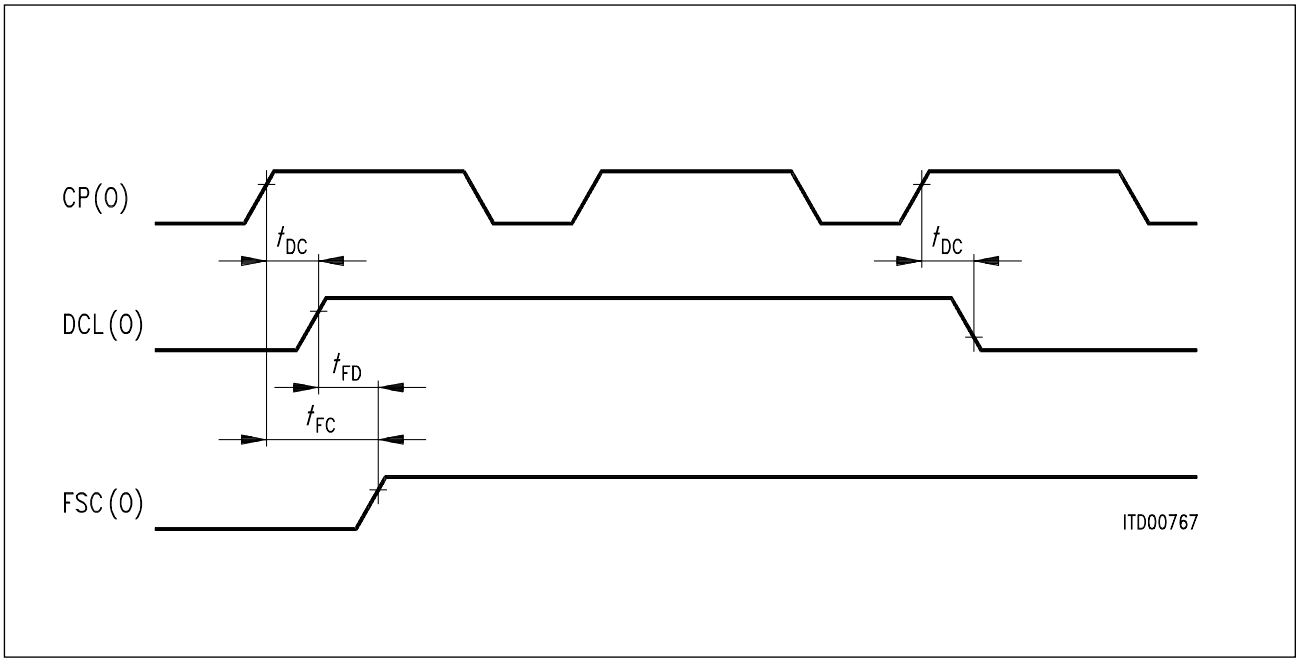


Figure 35

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Clock delay CP - DCL	t_{DC}	0	50	ns	C_L = 100 pF
Clock delay CP - FSC	t_{FC}	0	50	ns	C_L = 100 pF
Delay DCL - FSC	t_{FD}	– 20	20	ns	C_L = 100 pF

IOM® Interface

Normal Mode

Master Mode (TE)

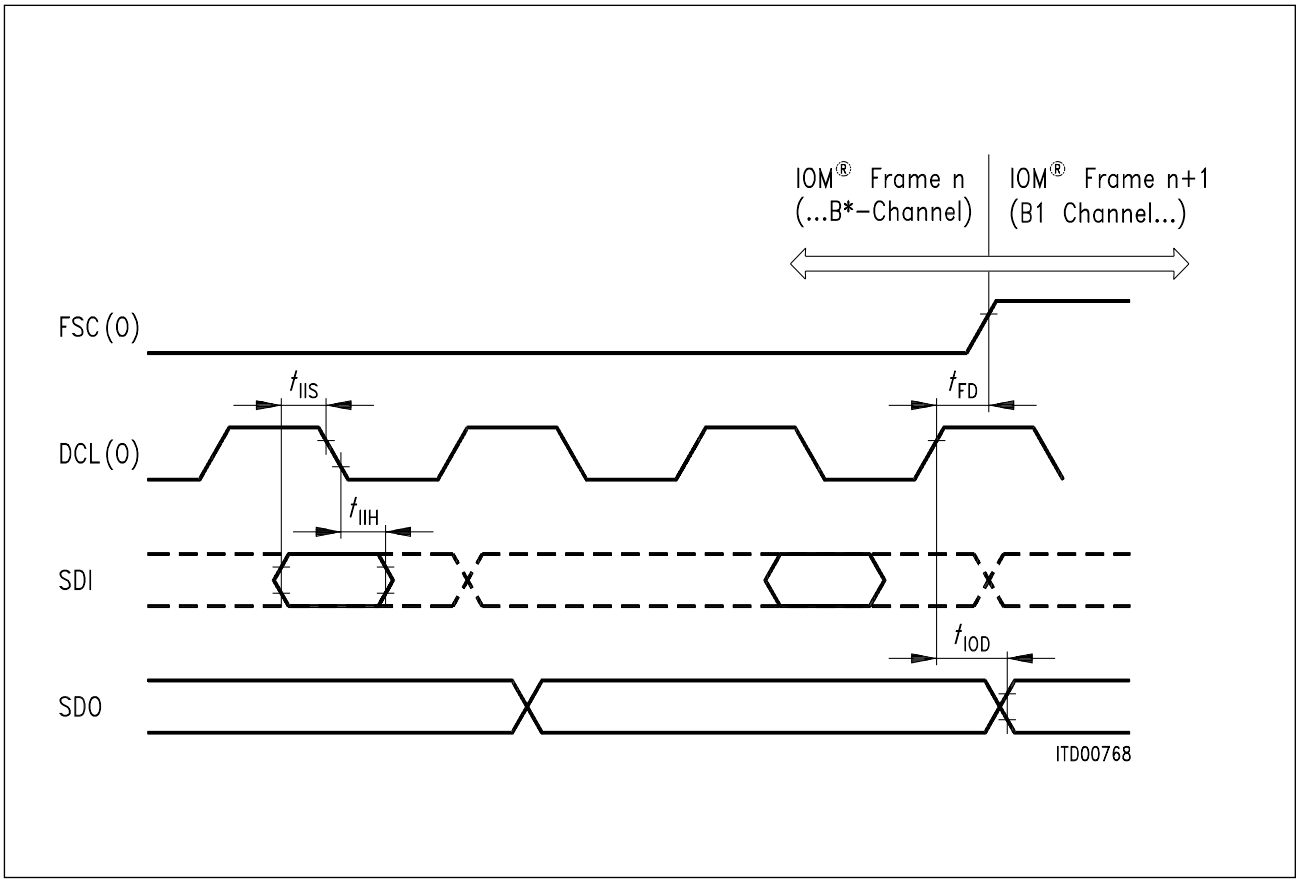


Figure 36

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync delay C_L = 100 pF	t_{FD}	– 20	20	ns
IOM output data delay C_L = 100 pF	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	50		ns

Slave Mode (NT, LT-S, LT-T)

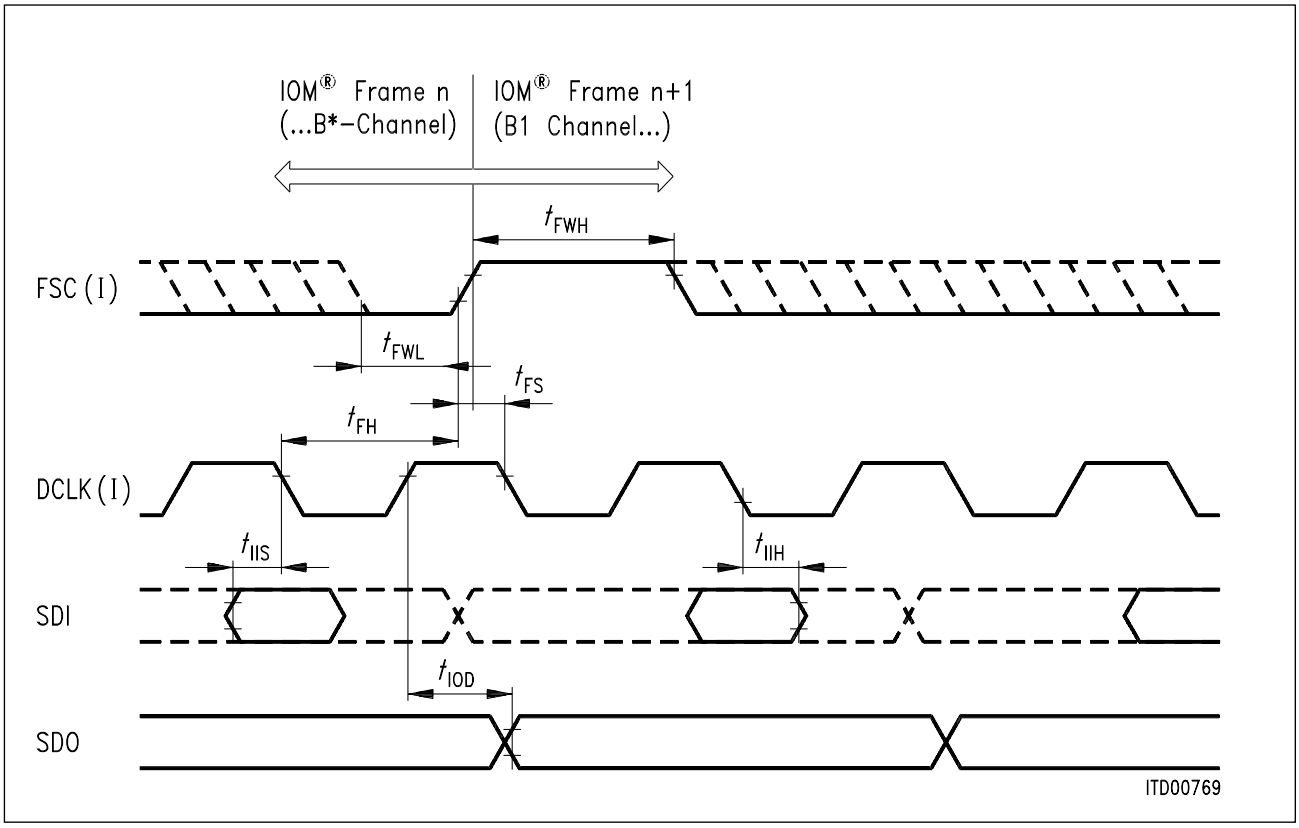


Figure 37

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	$t_{F\,H}$	30		ns
Frame sync setup	$t_{F\,S}$	50		ns
Frame sync high	$t_{F\,WH}$	40		ns
Frame sync low	$t_{F\,WL}$	2150		ns
IOM data output delay	$t_{I\,OD}$		200	ns*)
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

*) For push-pull output. For open drain output with integrated pull-up resistor, the maximum value is 900 ns.

Inverted Mode

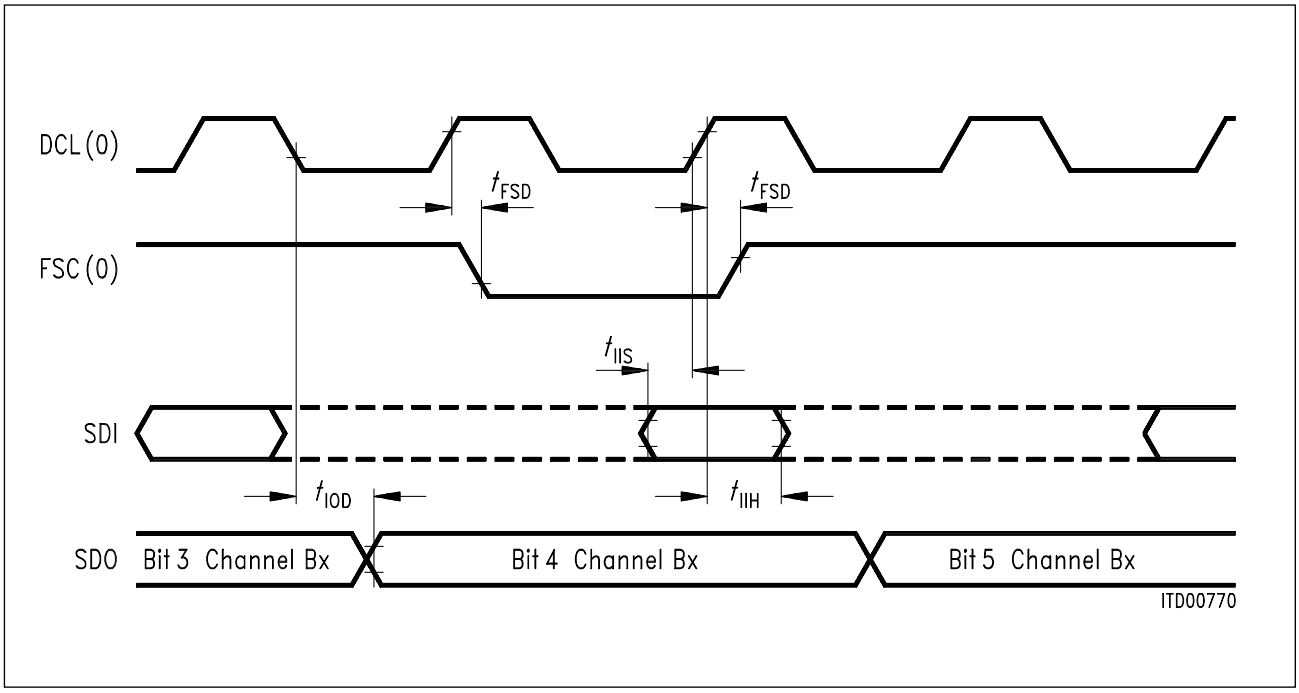


Figure 38

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync delay C_L = 100 pF	$t_{F\,SD}$	– 20	20	ns
IOM output data delay C_L = 100 pF	$t_{I\,OD}$		200	ns
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

Inverted Mux Mode

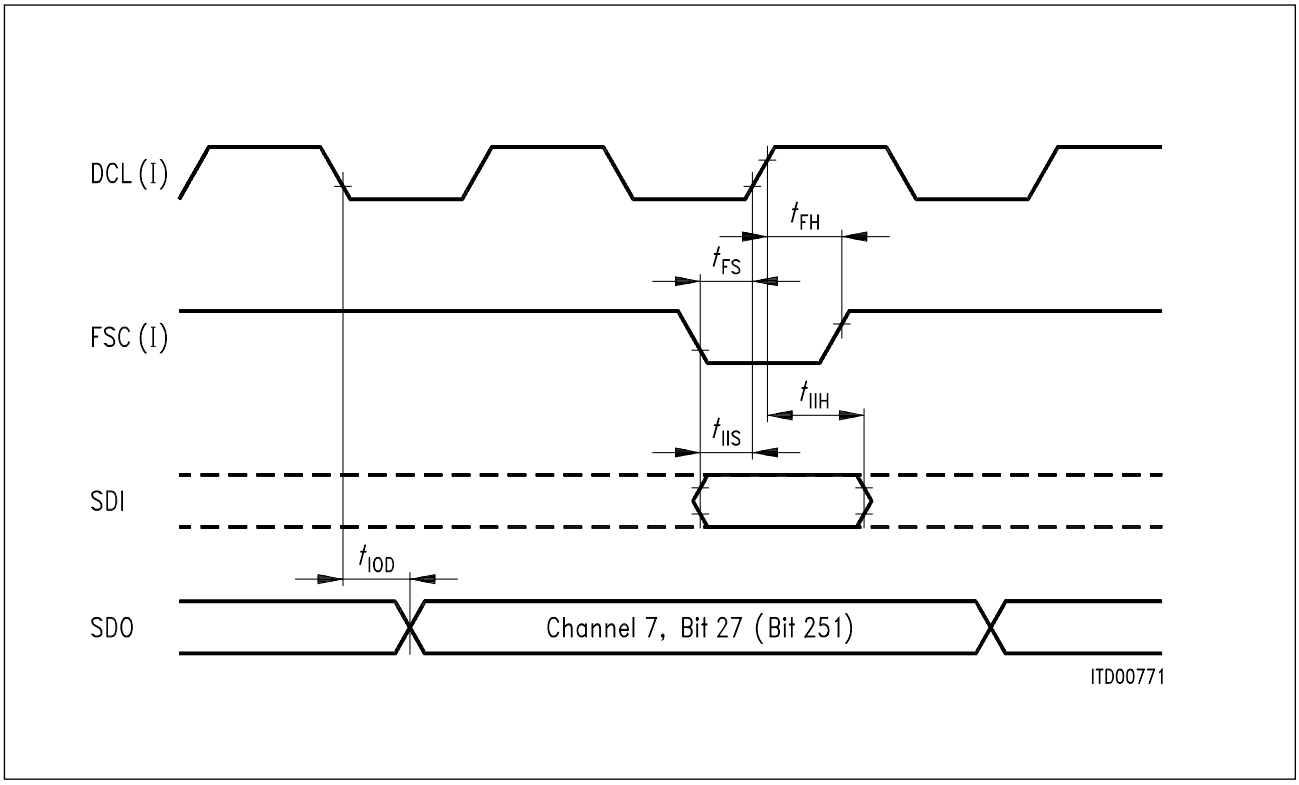


Figure 39

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	20		ns
Frame sync high	t_{FWH}	124.8		µs
Frame sync low	t_{FWL}	70	200	ns
IOM data output delay C_L = 150 pF; I_{OL} = 7 mA	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM output data hold	t_{IIH}	50		ns

Timing of Special Function Pins

$\overline{\text{RST}}$ Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of active (low) state	t_{WL}	1		ms

RDY Characteristics

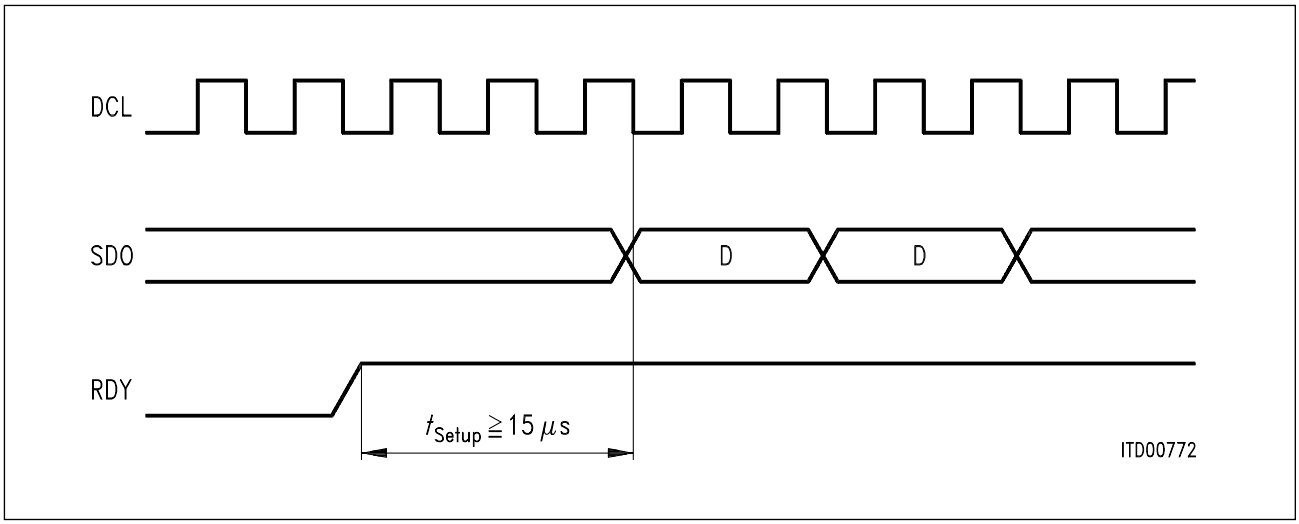


Figure 40

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of low state	t_{WL}	360		µs
Length of high state	t_{WH}	60		µs

DE Characteristics

The form of the DE input/output (pin X0, NT mode) is given by **figure 41** for the case of two S interfaces having a minimum frame delay and a maximum frame delay, respectively.

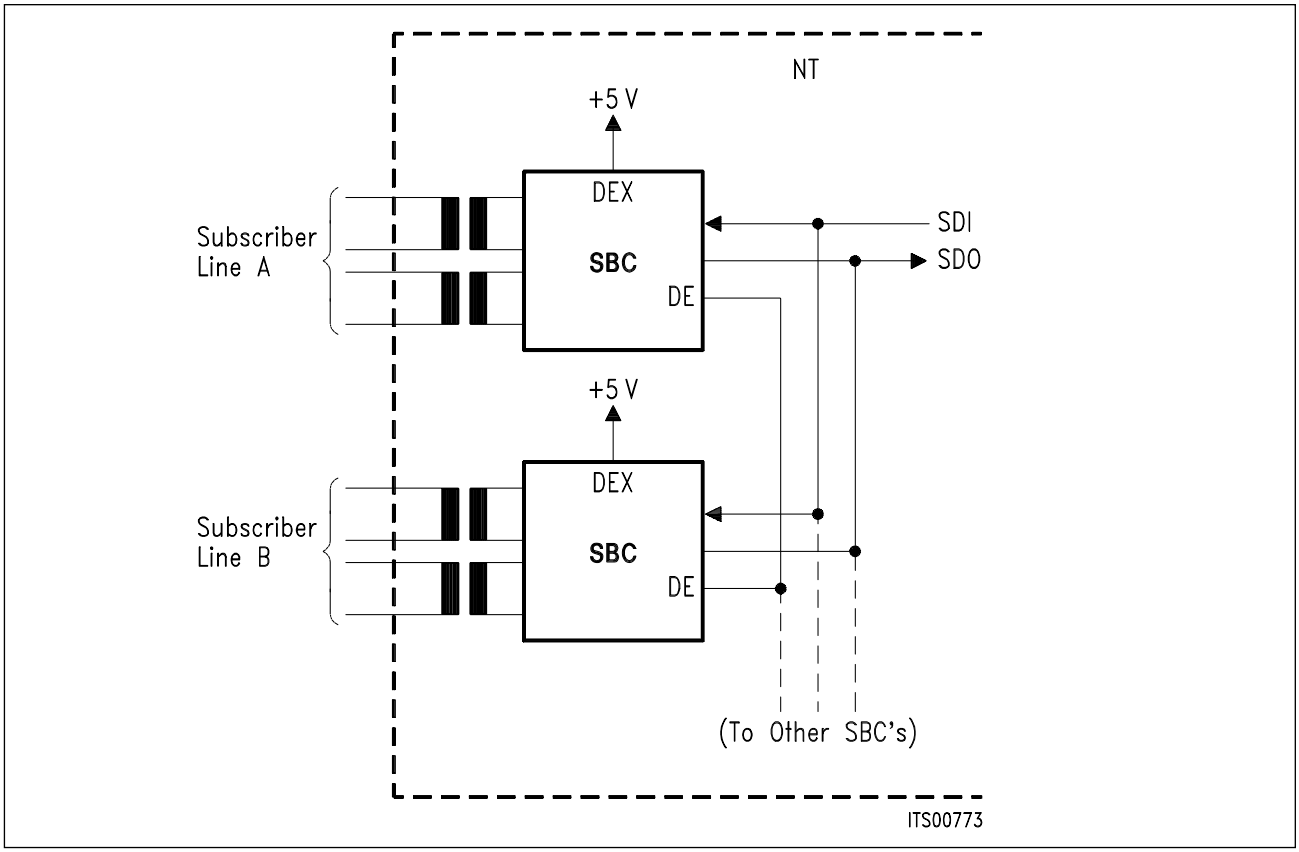


Figure 41
Star Configuration in NT

The AC characteristics of DE output and input are shown in **figure 42** and **43** and **table 13**.

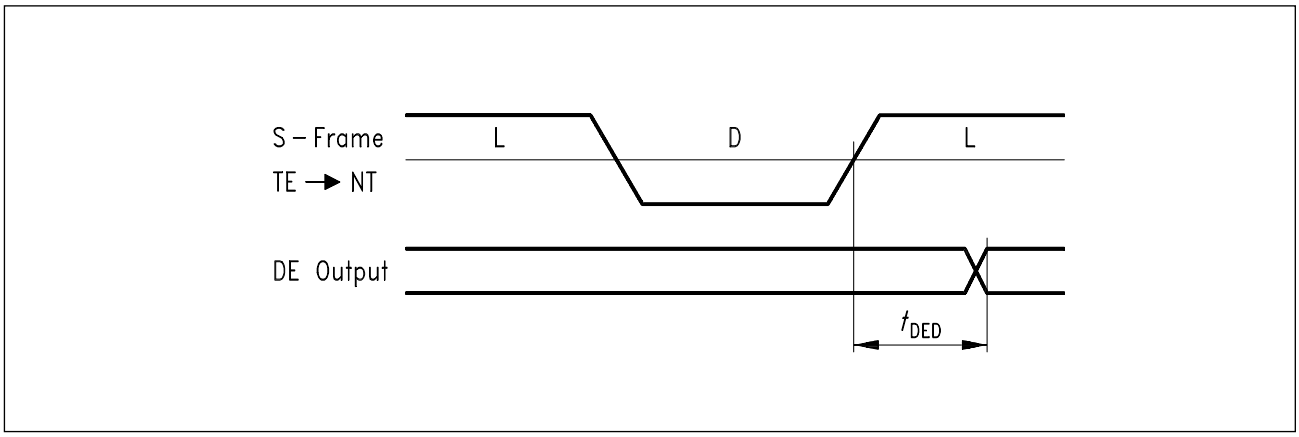


Figure 42
Timing of DE Output

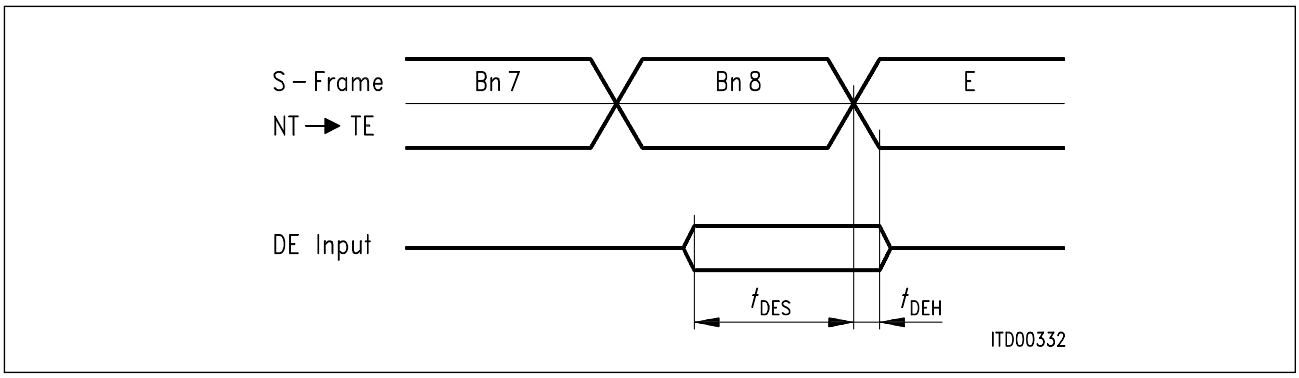


Figure 43
Timing of DE Input

Table 13

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DE delay C_L = 100 pF	t_{DED}		2	µs
DE setup	t_{DES}	3		µs
DE hold	t_{DEH}	0		µs

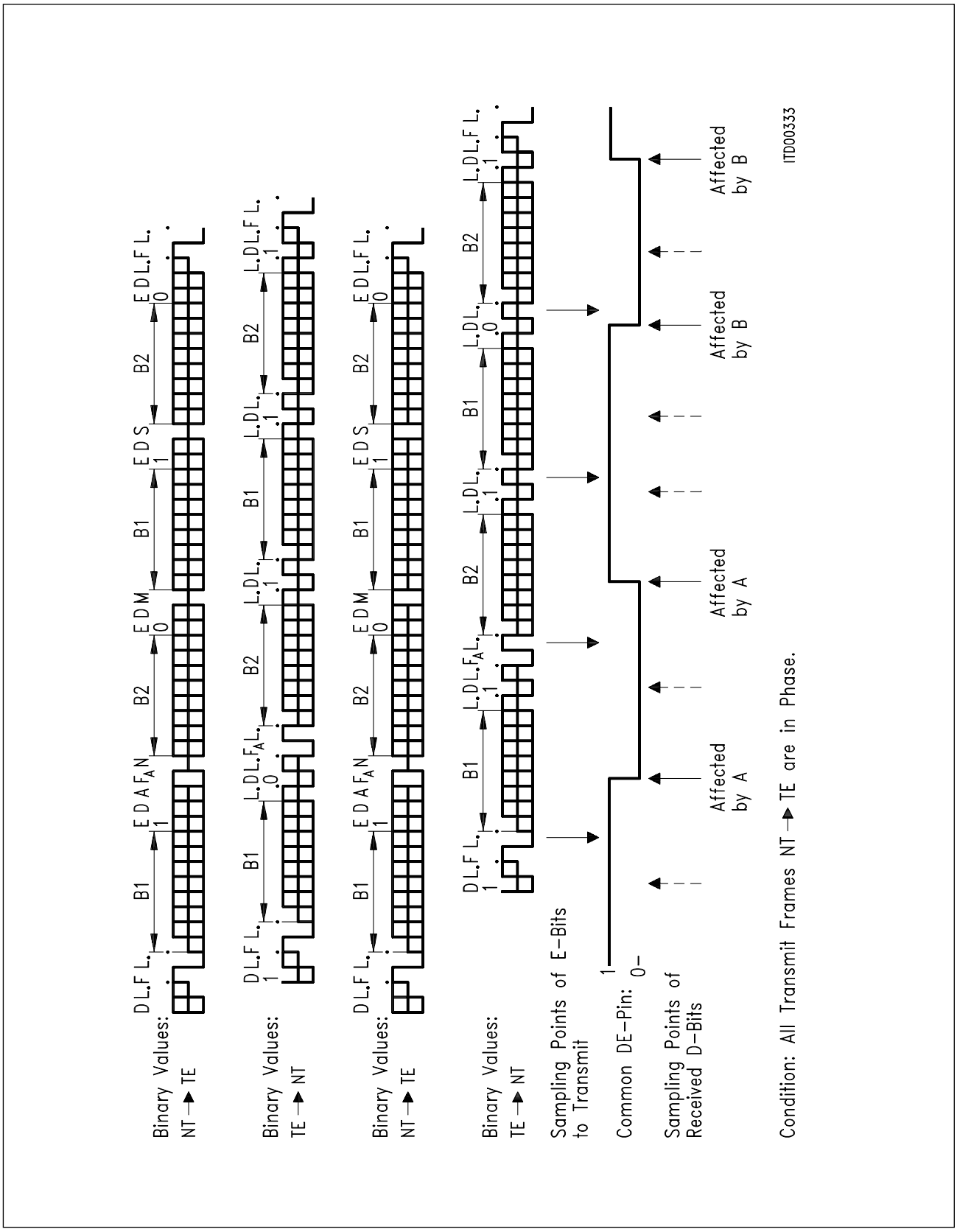


Figure 44
Timing of DE

ECHO Characteristics

The timing of the ECHO output (pin X2, TE mode) is identical with that of output SDO: however, the signal is “1” everywhere except in bit positions 24 and 25 (“D”-bit positions) of IOM frame, where it is equal to the E bits received from the S interface.

Adaptive Receiver Characteristics

The integrated receiver uses an adaptively switched threshold detector. The detector controls the switching of the receiver between two sensitivity levels. The hysteresis characteristics of the receiver are shown in **figure 45**.

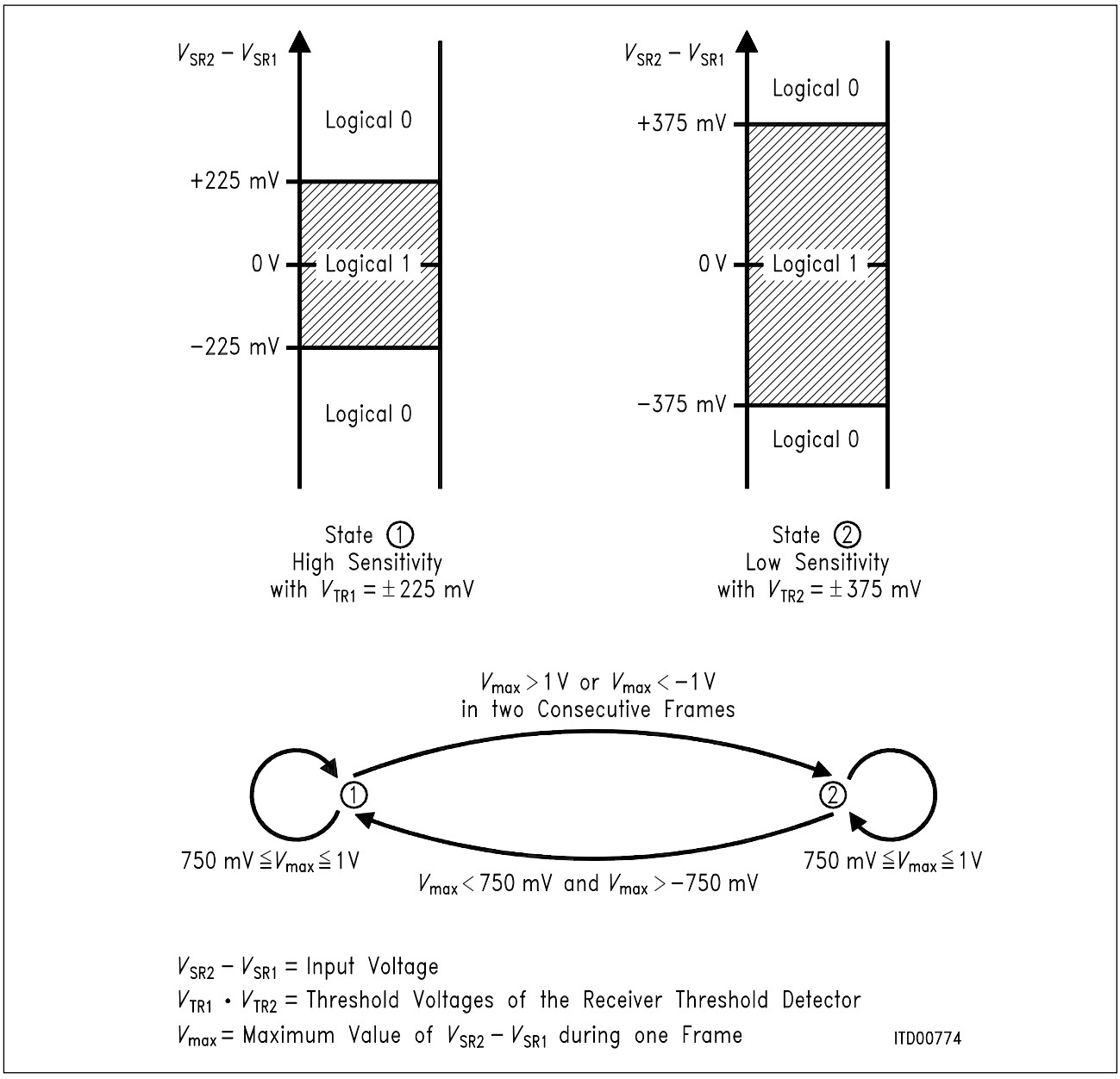
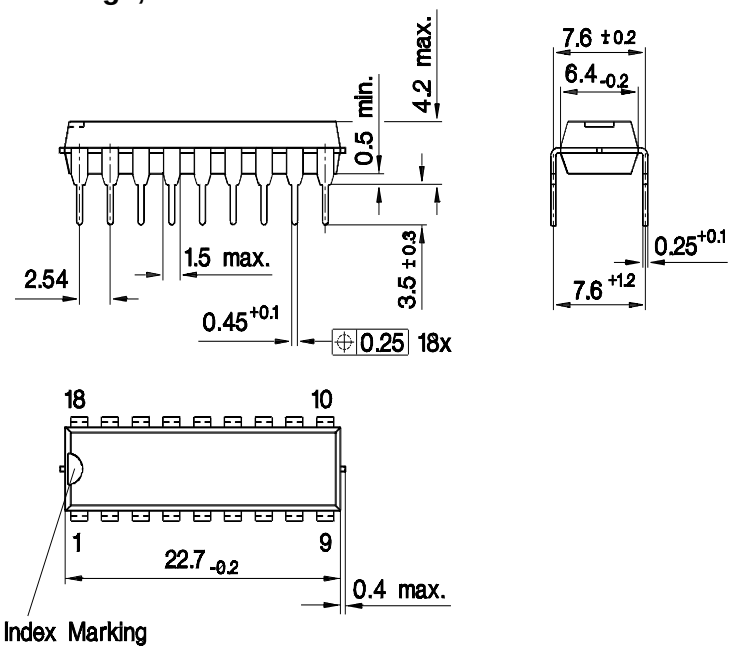


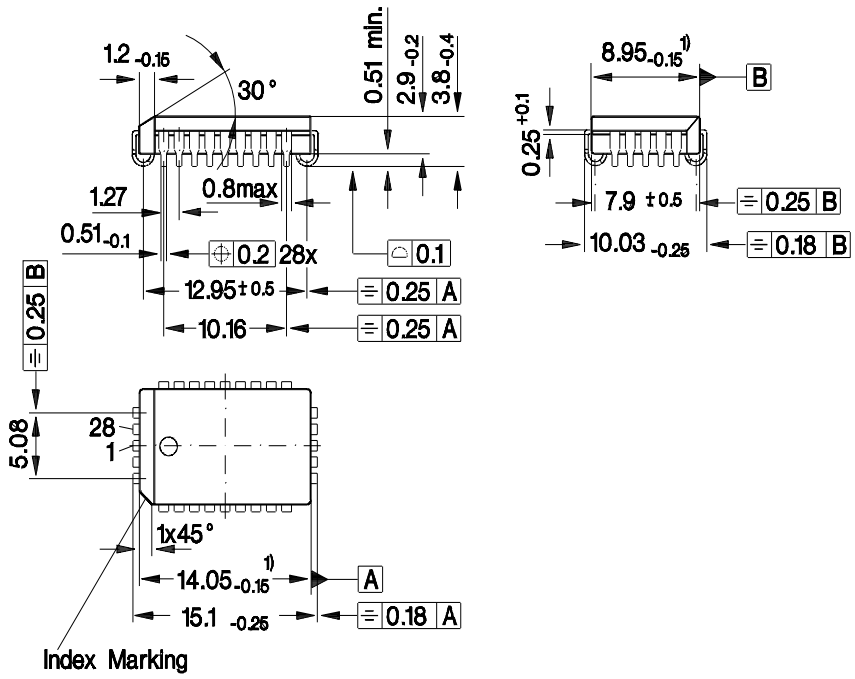
Figure 45
Switching of the Receiver between High Sensitivity and Low Sensitivity

5 Package Outlines

Plastic Dual-in-Line Package, P-DIP-22



Plastic-Leaded Chip Carrier, P-LCC-28-R (SMD)



1) Does not include plastic or metal protrusion of 0.15 max. per side

SMD = Surface Mounted Device

Dimensions in mm