PMU for Alkaline Battery-Powered Applications

Check for Samples: TPS80010

FEATURES

- **1.8-V Buck DC/DC Converter**
- **3.1-V Boost DC/DC Converter with 3-V Post-Regulation LDO**
- **Over 91% Conversion Efficiency**
- **Current-Limited Start-Up for Both DC/DC Converters**
- **Load Switch With Current-Limited Turnon**
- **Battery-Level Monitor Switch**
- **32-Pin, 4-mm × 4-mm × 1-mm VQFN Package**
- **ESD Performance Tested per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **500-V Charged-Device Model (C101)**

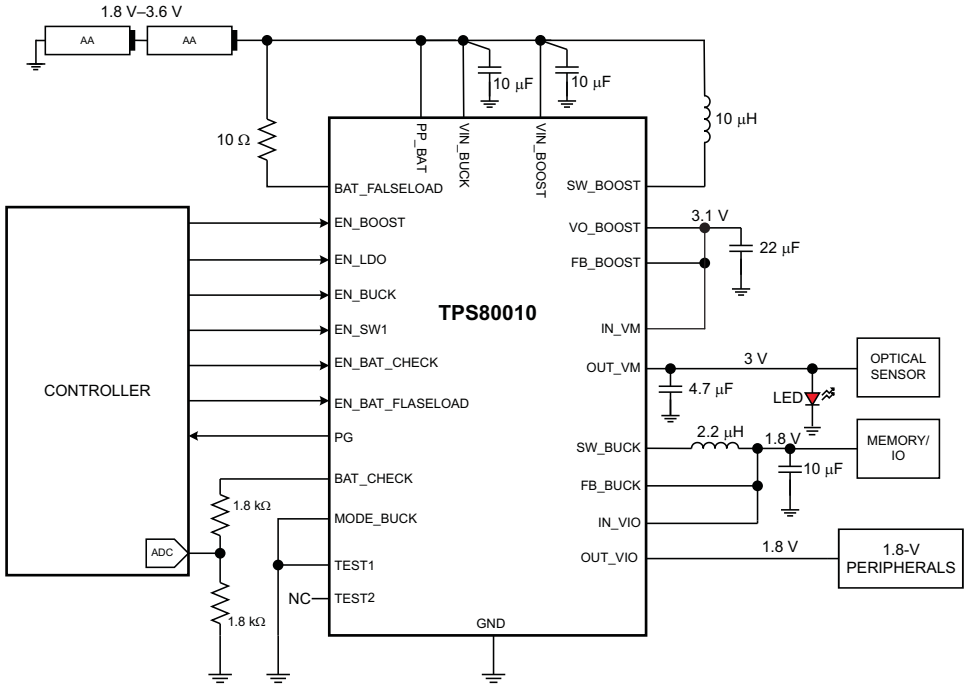
APPLICATIONS

- **Wireless Mice**
- **Wireless Keyboards**
- **Game Controllers**

DESCRIPTION

The TPS80010 provides an integrated power-management solution for 2-cell alkaline battery applications such as wireless mice, keyboards, and video game controllers. The VBUCK 1.8-V output is powered by a buck converter with a load capacity of 100 mA. A power-good (PG) signal is generated when VBUCK is above 90% of its target output voltage. Integrated in the TPS80010 is an 80-mΩ load switch that can be connected to the VBUCK output, allowing more system design flexibility when connecting to multiple loads. The 3.1-V VBOOST output is powered by a boost converter. The VBOOST output voltage is post-regulated by the integrated 3-V LDO. This post-regulation provides a low-noise supply level through the specified battery range.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either VCC or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

ORDERING INFORMATION(1)

DEVICE	TEMPERATURE	PACKAGE	ORDERING CODE	MARKING
TPS80010	–40°C to 85°C	VQFN	TPS80010ARSMR	RSM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range on all pins		–0.3	3.6	V
V_O	Output voltage range on all pins		–0.3	3.6	V
T_J	Junction temperature range		–40	125	°C
T_{stg}	Storage temperature range		–65	150	°C
V_{ESD}	ESD rating	Charged-device model (CDM) on all pins	–500	500	V
		Human-body model (HBM) on all pins	–2	2	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS80010 VQFN 32 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.9	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance (3)	25.2	°C/W
θ_{JB}	Junction-to-board thermal resistance (4)	8	°C/W
ψ_{JT}	Junction-to-top characterization parameter (5)	0.12	°C/W
ψ_{JB}	Junction-to-board characterization parameter (6)	7.5	°C/W
$\theta_{JC(bottom)}$	Junction-to-case (bottom) thermal resistance (7)	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

T_A = 0°C to 85°C; typical values are at T_A = 25°C

		MIN	TYP	MAX	UNIT
V_{BAT}	Input voltage, VIN BOOST, VIN_BUCK, PP_BAT pins	1.95		3.6	V
V_{IO} (IN_VIO)	Digital I/O operating voltage range		1.8	V_{BAT}	V
T_A	Ambient temperature	0	25	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current	V_{BAT} = 3 V, all modules enabled		51		µA
I_{OFF}	Off current	V_{BAT} = 3 V		1		µA
DIGITAL I/O						
$R_{PULLDOWN}$	Internal pulldown resistor	EN_BOOST, EN_LDO, EN_SW1, EN_BAT_CHECK, EN_BAT_FALSELOAD	157	275	383	kΩ
V_{IH}	Input logic-high voltage	EN_BOOST, EN_LDO, EN_SW1, EN_BAT_CHECK, EN_BAT_FALSELOAD	0.7×V_{IO}			V
		EN_BUCK, BUCK_MODE	0.7×V_{BAT}			
V_{IL}	Input logic-low voltage	EN_BOOST, EN_LDO, EN_SW1, EN_BAT_CHECK, EN_BAT_FALSELOAD			0.3×V_{IO}	V
		EN_BUCK, BUCK_MODE			0.7×V_{BAT}	
V_{OH}	Output logic-high voltage	PG	V_{IO} – 0.2			V
V_{OL}	Output logic-low voltage	PG			0.2	V
I_{L_DIG}	Logic-output load current				1	mA
BUCK CONVERTER						
V_{IN}	Input voltage at VIN_BUCK		1.95		3.6	V
I_O	Output current				100	mA
V_{FB}	Feedback voltage (output accuracy)	PWM, I_O = 0 mA to 100 mA, V_{IN} ≥ 1.85 V to 3.6 V, V_{BUCK} = 1.8 V	–1.5%		1.5%	
		PFM		1		
V_{BUCK}	Buck output voltage			1.8		V
I_{SW}	Switch current limit		0.56	0.7	0.84	A
I_{RUSH}	Inrush current	V_{IN} = 2 V		150		mA
	Line regulation	PWM, I_O = 100 mA		0.9%		
		PFM, I_O = 100 mA		0.9%		
	Load regulation	PWM, V_{IN} = 2.4 V, I_O = 0 mA to 100 mA		–0.5%		
		PFM, V_{IN} = 2.4 V, I_O = 0 mA to 100 mA		0.5%		
	Efficiency	PFM , I_O = 100 mA, V_{IN} = 2.4 V, V_{BUCK} = 1.8 V		92%		
		PWM, I_O = 100 mA, V_{IN} = 2.4 V, V_{BUCK} = 1.8 V		90%		
I_Q	Quiescent current	PFM, I_O = 0 mA, no switching		21		µA
		PFM, I_O = 0 mA, switching		25		
		PWM, I_O = 0 mA		5		mA
	Shutdown current			0.005	0.15	µA
	Leakage current into SW_BUCK			0.01	1	µA
R_{REC}	Rectifier on-resistance	V_{GS} = 3.6 V		185	380	mΩ
R_{MAIN}	Main SW on-resistance	V_{GS} = 3.6 V		240	480	mΩ
ΔV_{LN}	Line transient output variation	PFM, I_O = 50 mA, V_{IN} = 2 V → 3.6 V, Δt = 25 µs		10	20	mV
ΔV_{LD}	Load transient output variation	PFM, V_{IN} = 2.4 V, V_{BUCK} = 1.8 V, I_O = 1 mA → 100 mA, Δt = 1 µs		30	40	mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = 0°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK CONVERTER (Continued)						
V_{RIP}	Output ripple	PWM, I_O = 100 mA, V_{IN} = 2.4 V		1	10	mVpp
		PFM, I_O = 10 mA, V_{IN} = 3.6 V		10	20	
f_{SW}	Switching frequency		2	2.25	2.5	MHz
UVLO	Undervoltage lockout threshold			1.7		V
t_{START}	Start-up time				10	ms
C_L	Load capacitance			10		µF
L	Inductor			2.2		µH
LOAD SWITCH						
R_{ON}	Switch on-resistance	V_{GS} = 1.8 V		80	120	mΩ
	Maximum load current				360	mA
	Turnon inrush current				100	mA
	Output rise time	10%–90% of final V_O, C_L = 100 µF		2	4	ms
I_{OFF}	Off-state current	Switch turned off, I_O = 0 mA			1	µA
t_{ON}	Turnon time	C_L = 100 µF			6	ms
t_{OFF}	Turnoff time	C_L = 100 µF			10	ms
POWER-GOOD RESET						
V_{THRESH}	Power-good threshold voltage		1.68	1.7	1.72	V
Δt_{PG}	Power-good time-out delay		100	150	200	ms
V_{HYS}	Power-good hysteresis			10	15	mV
BOOST CONVERTER						
V_{IN}	Input voltage at VIN_BOOST	Boost mode	1.8		3.1	V
		V_{IN} > V_{BOOST} mode, V_{BOOST} = V_{IN}	3.1		3.6	
V_{BOOST}	Output voltage	T_A = 0°C–50°C, V_{IN} = 1.8 V to 3.1 V, I_O = 0 mA to 50 mA	3	3.1	3.2	V
I_O	Output current	V_{IN} = 1.8 V to 3.6 V			50	mA
I_{SW}	Switch current limit		200	350	475	mA
I_{RUSH}	Inrush current	V_{IN} = 2 V		150		mA
R_{REC}	Rectifier on-resistance	V_{BOOST} = 3.1 V		1		Ω
R_{MAIN}	Main SW on-resistance			1		Ω
	Line regulation	V_{IN} = 2 V to 3 V, I_O = 50 mA		0.5%		
	Load regulation	V_{IN} = 2 V, I_O = 0–50 mA		0.5%		
	Boost efficiency	V_{IN} = 2.4 V, I_O = 5 mA		91%		
f_{SW}	Oscillator frequency	V_{IN} = 2.4 V, I_O = 50 mA		91		kHz
				625		
I_Q	Quiescent current	From V_{IN} supply, I_O = 0 mA, V_{IN} = 1.8 V, V_{BOOST} = 3.1 V		1	2.5	µA
		From V_{BOOST}, I_O = 0 mA, V_{IN} = 1.8 V, V_{BOOST} = 3.1 V		4	6.5	
	Shutdown current			0.1	1	
	Leakage current into SW_BOOST			0.1	1	
V_{UVLO}	V_{IN} decreasing			0.5	0.7	V
ΔV_{LN}	Line transient output variation	I_O = 10 mA, V_{IN} = 1.8 V → V_{BOOST}, ΔT = 25 µs		10		mV
ΔV_{LD}	Load transient output variation	V_{IN} = 2.4 V, V_{BOOST} = 3.1 V, I_O = 1 mA → 50 mA, Δt = 1 µs		5	10	mV
V_{RIP}	Output ripple	V_{IN} = 1.8 V, I_O = 50 mA		4	10	mVpp

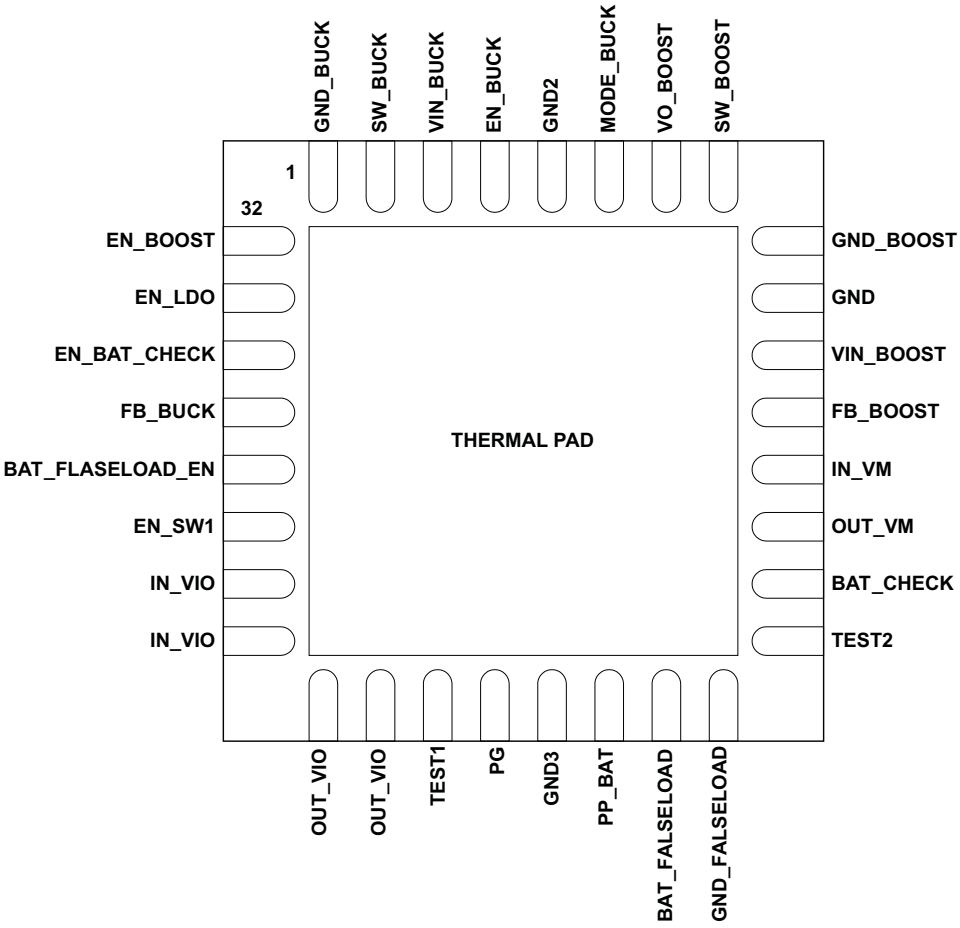
ELECTRICAL CHARACTERISTICS (continued)

T_A = 0°C to 85°C; typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER (Continued)						
I_{OFF}	Off-mode current			0.1	1	µA
t_{START}	Start-up time	From enable, V_{BOOST} = 10% → 90%		0.25	10	ms
C_L	Load capacitance		6	10	22	µF
L	Inductance			10		µH
POST REGULATION LDO						
V_{IN}	Input voltage at IN_VM		3.1		3.6	V
V_{LDO}	Output voltage	10 µA ≤ I_O ≤ I_{OMAX}	2.91	3	3.09	V
I_O	Output current	Normal mode			50	mA
I_{LIMIT}	Current limit	V_{LDO} > 1 V	300	400	500	mA
I_{SHORT}	Short-circuit current	Output shorted to ground	30	60	150	mA
VREG	Line regulation	dV_{LDO}/dV_{IN} at I_O = Max			0.2	%
LREG	Load regulation	V_{LDO} (I_{OMIN}) – V_{LDO}(I_{OMAX})			40	mV
ΔV_{LN}	Load transient response	I_O = 20 mA/µs, V_{IN} = 3.1 V		50	100	mV
I_Q	Quiescent current	I_O = 0 mA		16	17.6	µA
PSRR	Power-supply ripple rejection	f = 120 Hz to 1 kHz at I_O = I_{OMAX}/2, V_{IN} = 3.1 V	40			dB
V_{RIP_NORM}	Output ripple	V_{BAT} < 3.1 V, I_O = 50 mA, V_{IN} = V_{BOOST}		0.1	1	mVpp
V_{RIP_HIBAT}	Output ripple	V_{BAT} > 3.1 V, I_O = 50 mA, V_{IN} = V_{BOOST}		4	10	mVpp
	Boost plus LDO efficiency	V_{BAT} = 2.4 V, I_O = 5 mA, V_{IN} = V_{BOOST}		87%		
		V_{BAT} = 2.4 V, I_O = 50 mA, V_{IN} = V_{BOOST}		88%		
t_{ON}	Turn-on time	I_O = 0 mA, V_{LDO} = 90%, C_L = 2.9 µF		130	500	µs
t_{OFF}	Turn-off time	I_O = 0 mA, V_{LDO} < 0.5 V, C_L = 2.9 µF		3.9	5	ms
C_L	Load capacitance	Ceramic capacitor, ESR = 10 mΩ to 150 mΩ	4.7	10	22	µF
BATTERY LOAD MONITOR						
V_{OP}	Operating voltage			1.8	3.6	V
V_{IN}	Input voltage at PP_BAT		1.8		3.6	V
V_{OUT}	Output voltage at BAT_CHECK				V_{IN}	V
I_{LOAD}	Load current				10	mA
R_{ON}	Switch on-resistance	V_{IN} = 1.8 V to 3.6 V		12	15	Ω
BATTERY LOAD SWITCH						
V_{OP}	Operating voltage			1.8	3.6	V
V_{IN}	Input voltage at BAT_FALSELOAD				3.6	V
I_{IN}	Input current			240	360	mA
R_{ON}	Switch on-resistance				500	mΩ

DEVICE INFORMATION

RSM PACKAGE
(BOTTOM VIEW)



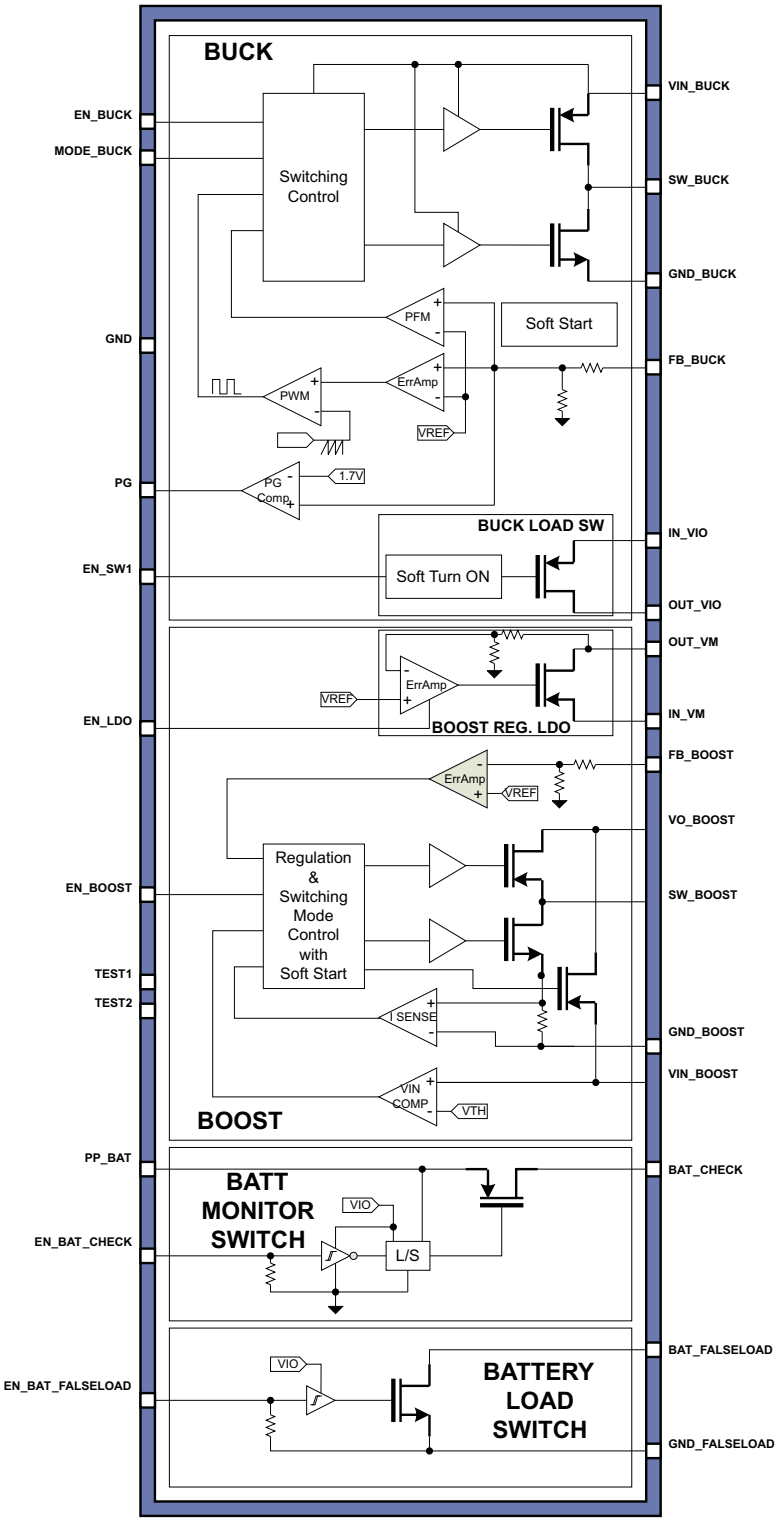
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BAT_CHECK	15	O	Battery monitor switch output. Connect to ADC for battery-level check.
BAT_FALSELOAD	18	I	Battery monitor input for false-load check
BAT_FALSELOAD_EN	28	I	Battery false load switch enable
EN_BAT_CHECK	30	I	Battery-check path enable
EN_BOOST	32	I	Boost converter enable
EN_BUCK	4	I	Buck converter enable
EN_LDO	31	I	Boost post-regulation LDO enable
EN_SW1	27	I	Buck-load switch (SW1) enable
FB_BOOST	12	I	Boost-converter feedback input
FB_BUCK	29	I	Buck converter feedback input
GND	10	–	GND
GND2	5	–	Device ground
GND3	20	–	Device ground
GND_BOOST	9	–	Boost converter ground
GND_BUCK	1	–	Buck converter ground

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
GND_FALSELOAD	17	O	False load ground
IN_VIO	25, 26	–	Internal I/O power supply. Load switch 1 input. Connect externally to buck output
IN_VM	13	I	Boost post-regulation LDO input. Connect externally to VO_BOOST.
MODE_BUCK	6	I	Buck converter mode control. High for PWM, low for PFM
OUT_VIO	23, 24	O	Load switch 1 output
OUT_VM	14	O	Boost post-regulation LDO output
PG	21	O	Buck power-good indication output. High when V_{BUCK} > 1.7 V
PP_BAT	19	I	Battery input for level check
SW_BOOST	8	IO	Boost converter switching node. Inductor connection
SW_BUCK	2	O	Buck converter switching output. Inductor connection
TEST1	22	IO	Test pin1 (tie to GND)
TEST2	16	O	Test pin 2 (do not connect)
VIN_BOOST	11	–	Boost-converter power supply
VIN_BUCK	3	–	Buck converter power supply
VO_BOOST	7	O	Boost converter regulated output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

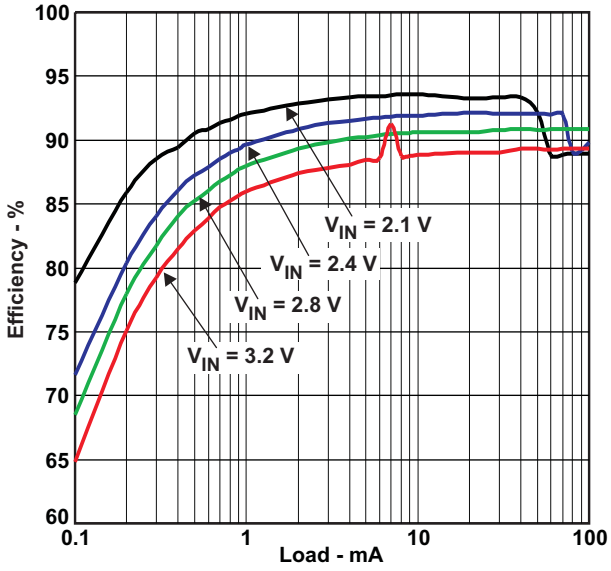


Figure 1. Buck Efficiency – MODE_BUCK = 0

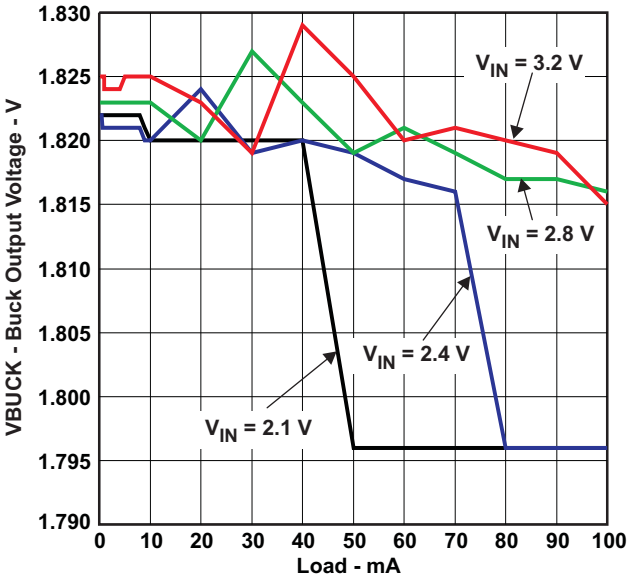


Figure 2. Buck Output Voltage vs Load – MODE_BUCK = 0

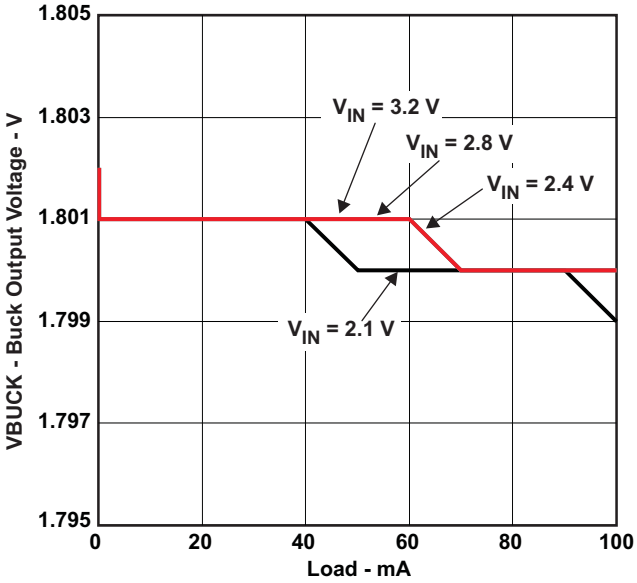


Figure 3. Buck Output Voltage vs Load – MODE_BUCK = 1

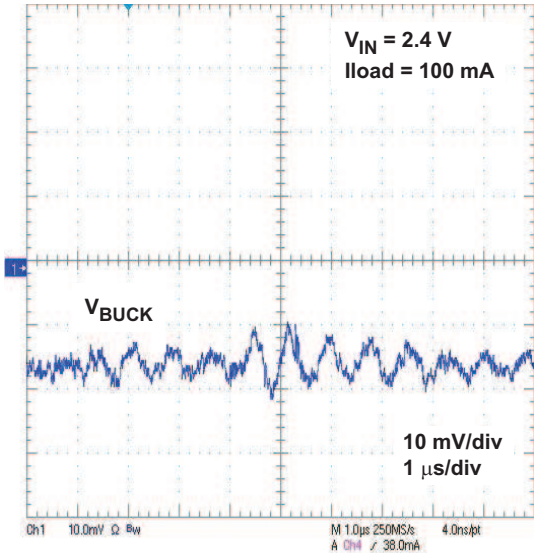


Figure 4. Buck Output-Voltage Ripple – PWM

TYPICAL CHARACTERISTICS (continued)

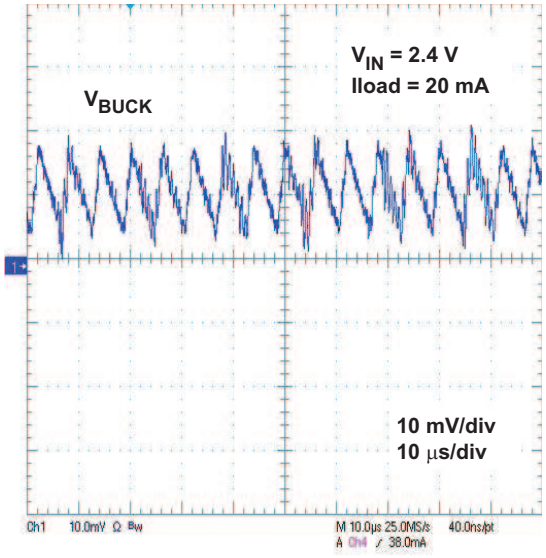


Figure 5. Buck Output-Voltage Ripple – PFM

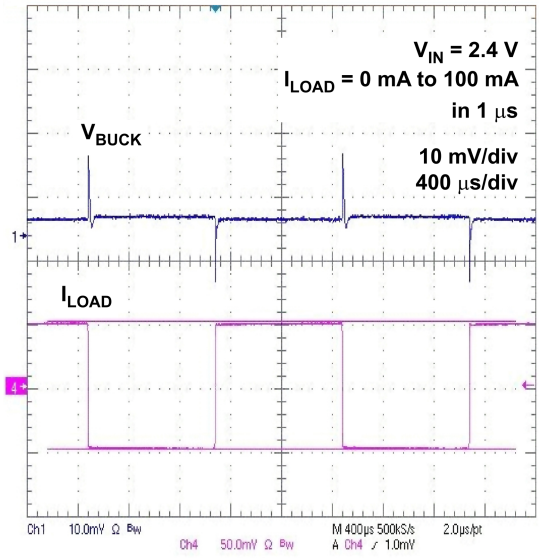


Figure 6. Buck Output Load Transient Response

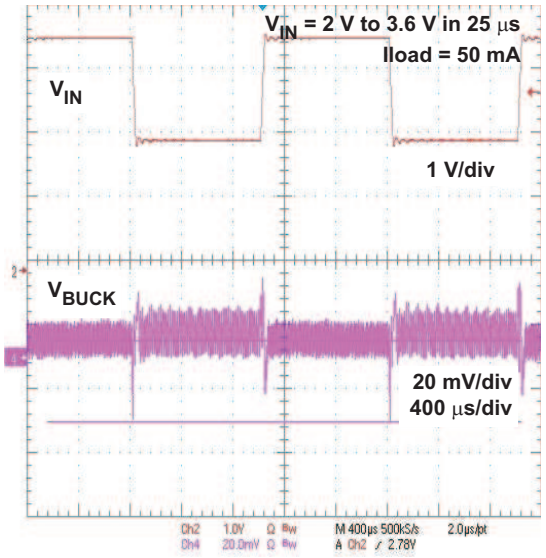


Figure 7. Buck Output Line Transient Response

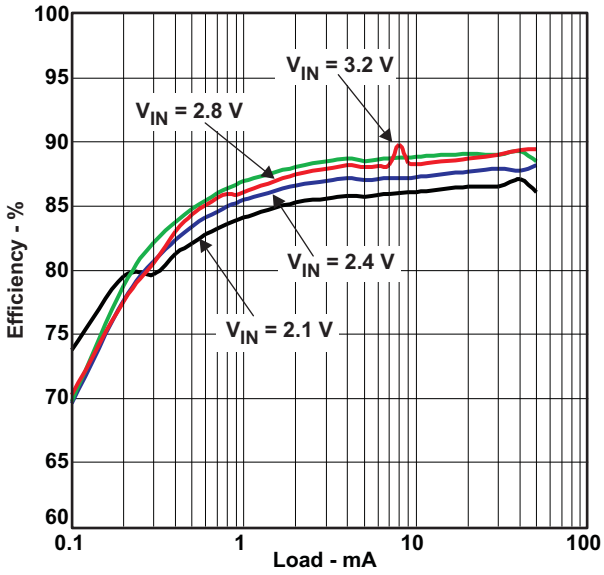


Figure 8. Boost With LDO Efficiency

TYPICAL CHARACTERISTICS (continued)

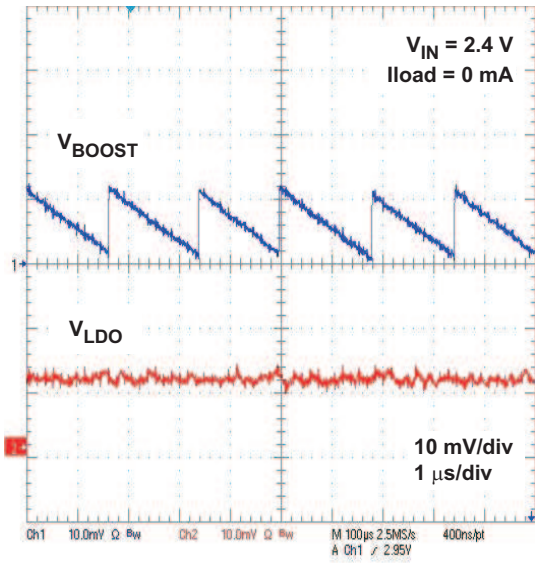


Figure 9. Boost Output Voltage Ripple

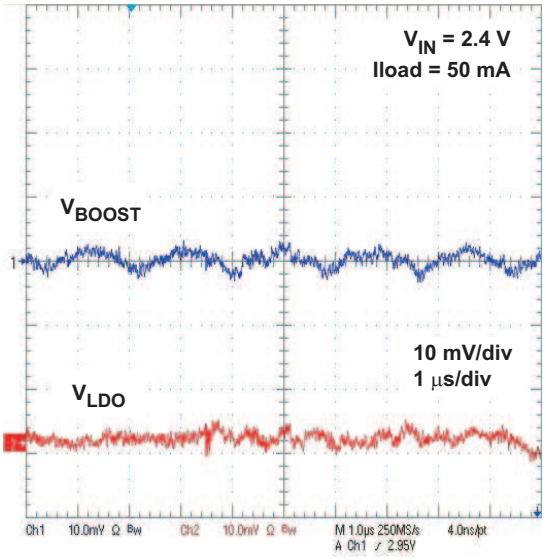


Figure 10. Boost Output Voltage Ripple

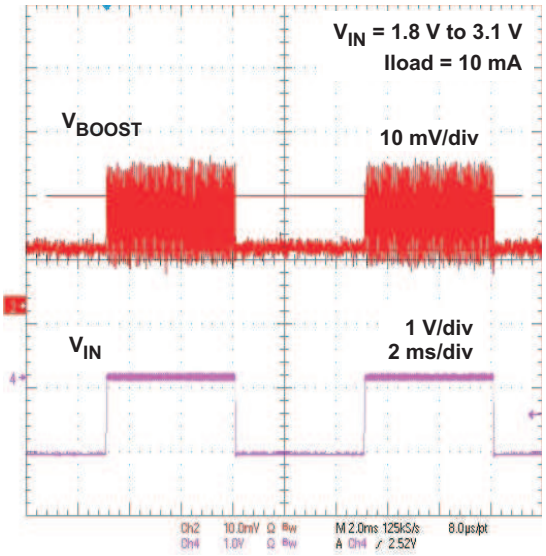


Figure 11. Boost Line Transient Response

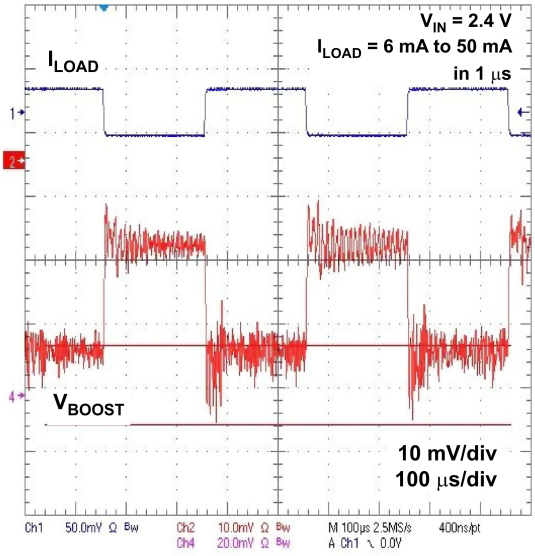


Figure 12. Boost Load Transient Response

TYPICAL CHARACTERISTICS (continued)

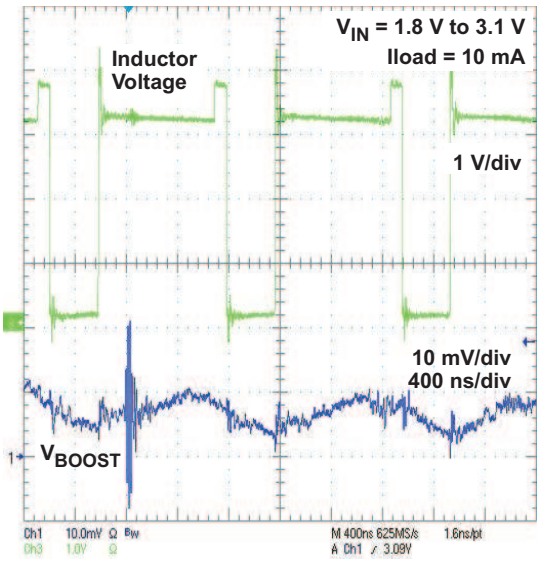


Figure 13. Boost Switching Waveform – Continuous-Current Mode

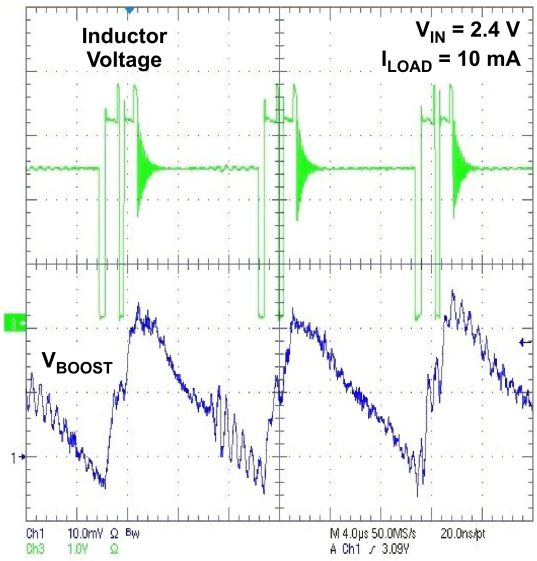


Figure 14. Boost Switching Waveform – Discontinuous-Current Mode

THEORY OF OPERATION

Enable

The TPS80010 includes two dc-dc converters, a load switch, post-regulation LDO, and battery monitoring switch. Each of these circuits has a dedicated enable pin with an internal pulldown resistor, $R_{PULLDOWN}$, that can be driven by standard logic or by an open-drain driver. The EN_BUCK pin not only enables the buck converter, but also serves as the master enable for the device. No other circuitry in the TPS80010 can operate without EN_BUCK set high.

Buck DC-DC Converter and Load Switch

The synchronous step-down (buck) converter in the TPS80010 provides a fixed 1.8-V output with a load capacity of 150 mA. This converter operates with a fixed switching frequency of 2.25 MHz during pulse-width-modulation (PWM) operation at moderate to heavy loads. As the load current decreases, the converter automatically switches to a power-save mode and operates in pulse-frequency-modulation (PFM) mode in order to maximize power efficiency. During PFM operation, the converter positions the output at a voltage about 1% above the nominal output voltage. This feature minimizes the output voltage drops during sudden load transients. The power-save mode can be disabled by setting the MODE_BUCK pin high.

The buck converter has internal soft-start circuitry that limits the inrush current during startup to 150 mA, allowing a slow and controlled output-voltage ramp. Once the output voltage reaches 1.7 V, the output monitoring circuitry generates a power-good (PG) output signal.

The TPS80010 also includes a load switch that is to be connected externally to the buck output voltage. This switch provides flexibility in the design and power distribution of the end application by allowing several loads (such as memory, I/O, Bluetooth, etc.) to be connected to the same supply while being able to power down or disconnect some of these loads selectively when the end application goes to a low-power mode of operation. This switch has a controlled turnon in order to limit the inrush current caused by the load, and hence the load transient to the buck converter.

Boost DC-DC Converter and Post-Regulation LDO

The TPS80010 includes a synchronous step-up (boost) converter that provides a 3.1-V fixed output at 50-mA load current. The boost converter is controlled by a hysteretic current-mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant and adjusting the offset of this inductor current depending on the output load. If the required average input current is lower than the average inductor current defined by this constant ripple, the converter goes into discontinuous-current mode (DCM) to keep the efficiency high at low-load conditions. The boost also has a soft-start circuit that limits the inrush current to 150 mA.

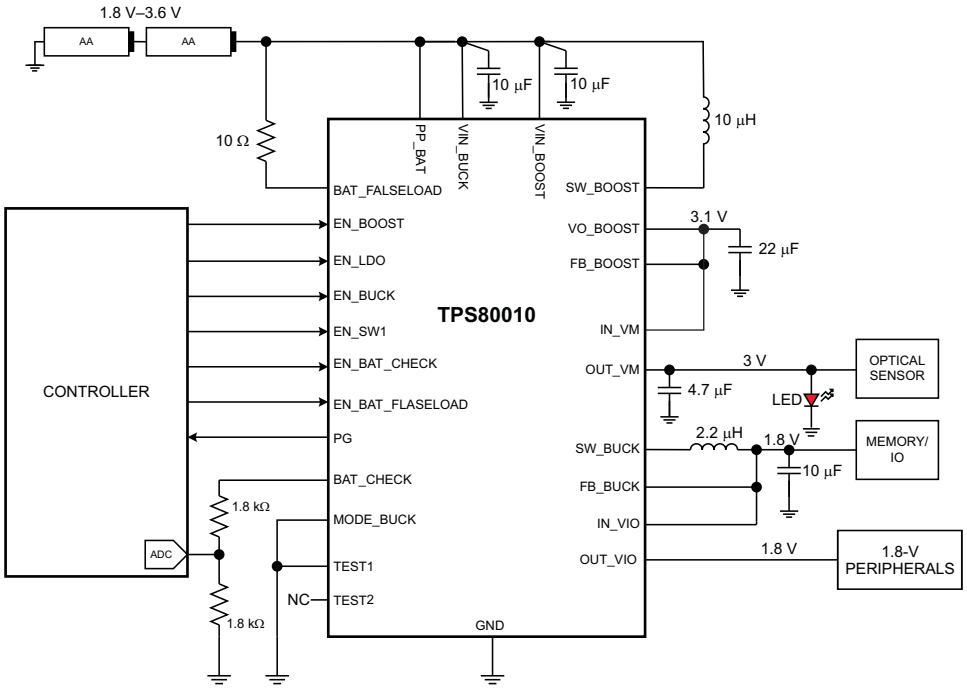
In order to provide a clean, low-noise supply when V_{BAT} > 3.1 V, the output of the boost is post-regulated by a 3-V LDO. This post-regulation allows the TPS80010 to provide a solid 3-V supply rail to the end application across the full input or battery-voltage range while minimizing the number of external components. In order to minimize power loss through the power path, the LDO allows for 100-mV input-voltage headroom at 50-mA load.

Battery Monitoring Switch and False Load

The TPS80010 implements a battery-voltage monitor switch to briefly check battery lifetime. The integrated false-load switch connects a specified load to the battery. When this *false* load is applied, the battery monitor switch is turned on, gating the sensed battery voltage to the ADC in the system. Based on this measurement, the system can determine the battery impedance, and hence, battery health.

APPLICATION INFORMATION

Typical Application



Buck Output Filter Design

The TPS80010 buck regulator is designed to operate with inductors in the range of 1.5 µH to 4.7 µH and with output capacitors in the range of 4.7 µF to 22 µF. The part is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For stable operation, the L and C values of the output filter must not fall below 1-µH effective inductance and 3.5-µF effective capacitance.

Buck Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{BUCK}.

The inductor selection also has an impact on the output-voltage ripple in PFM mode. Higher inductor values lead to lower output-voltage ripple and higher PFM frequency; lower inductor values lead to a higher output-voltage ripple but lower PFM frequency.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during heavy load transients, the inductor current rises above the calculated value.

$$\Delta I_L = V_{BUCK} \times \frac{1 - \frac{V_{BUCK}}{V_{IN}}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{Omax} + \frac{\Delta I_L}{2} \quad (2)$$

with:

f = Switching frequency (2.25 MHz typical)

L = Inductor value
ΔI_L = Peak-to-peak inductor ripple current
I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit, I_{LIMF}, of the converter.

Accepting larger values of ripple current allows the use of lower inductance values, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil have a strong impact on the efficiency of the dc-dc conversion and consist of both the losses in the dc resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Buck Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS80010 buck regulator allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V- and Z5U-dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. At nominal load current, the device operates in PWM mode and the rms ripple current is calculated as:

$$I_{RMSCout} = V_{BUCK} \times \frac{1 - \frac{V_{BUCK}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{BUCK} = V_{BUCK} \times \frac{1 - \frac{V_{BUCK}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + ESR \right) \quad (4)$$

At light load currents, the converter operates in power-save mode, and the output-voltage ripple depends on the output-capacitor and inductor values. Larger output-capacitor and inductor values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

Buck Input Capacitor Selection

An input capacitor is required for best input voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For most applications, a 4.7-µF to 10-µF ceramic capacitor is recommended. Because a ceramic capacitor loses up to 80% of its initial capacitance at 5 V, it is recommended that 10-µF input capacitors be used for input voltages > 4.5 V. The input capacitor can be increased without any limit for better input-voltage filtering. Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or V_{IN} step on the input can induce ringing at the VIN_BUCK pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part by exceeding the maximum ratings.

Table 1. Recommended Component List for Buck Converter

Component	Value	Part#	Supplier	Size
Inductor	2.2 µH	LQM2HPN2R2MJ0L	Murata	2.5 × 2 × 1.2 (1008)
		LPS3015-222ML	Coilcraft	3 × 3 × 1.5
Cacitor (IN)	10 µF	GRM188R60J106ME47D	Murata	0603
Capacitor (OUT)	10 µF	GRM188R60J106ME47D	Murata	0603

Boost Inductor Selection

To ensure proper operation of the TPS80010 boost dc-dc converter, a suitable inductor must be connected between pins VIN_BOOST and SW_BOOST. Inductor values of 4.7 μH show good performance over the whole input and output voltage range.

Choosing other inductance values affects the switching frequency f proportional to 1/L as shown in Equation 5.

$$L = \frac{1}{f \times 200\ mA} \times \frac{V_{IN} \times (V_{BOOST} - V_{IN})}{V_{BOOST}} \quad (5)$$

Choosing inductor values higher than 4.7 μH can improve efficiency due to reduced switching frequency and correspondingly reduced switching losses. Using inductor values below 2.2 μH is not recommended.

Having selected an inductance value, the peak current for the inductor in steady-state operation can be calculated. Equation 6 gives the peak current estimate.

$$I_{L,MAX} = \left\{ \frac{V_{BOOST} \times I_{BOOST}}{0.8 \times V_{IN}} + 100\ mA \right\} \quad \text{continuous current operation}$$

$$I_{L,MAX} = 200\ mA \quad \text{discontinuous current operation} \quad (6)$$

$I_{L,MAX}$ is the required minimum inductor-current rating. Note that load-transient or overcurrent conditions may require an even higher current rating.

The condition in Equation 7 provides an easy way to determine whether the device is in continuous or discontinuous operation. As long as the condition is true, the device operates in continuous-current mode. If the condition becomes false, discontinuous-current operation is established.

$$\frac{V_{BOOST} \times I_O}{V_{IN}} > 0.8 \times 100\ mA \quad (7)$$

Due to the use of current hysteretic control in the TPS80010 boost, the series resistance of the inductor can impact the operation of the main switch. There is a simple calculation that can ensure proper operation of the TPS80010 boost converter. The relationship between the series resistance (R_{IN}), the input voltage (V_{IN}), and the switch-current limit (I_{SW}) is shown in Equation 8.

$$R_{IN} < \frac{V_{IN}}{I_{SW}} \quad (8)$$

Examples:

$$I_{SW} = 400\ mA,\ V_{IN} = 2.5\ V \quad (9)$$

In Equation 9, $R_{IN} < 2.5\ V / 400\ mA$; therefore, R_{IN} must be less than 6.25 Ω.

$$I_{SW} = 400\ mA,\ V_{IN} = 1.8\ V \quad (10)$$

In Equation 10, $R_{IN} < 1.8\ V / 400\ mA$; therefore, R_{IN} must be less than 4.5 Ω.

Boost Input Capacitor

The input capacitor should be at least 10 μF to improve transient behavior of the regulator and EMI behavior of the total power-supply circuit. The input capacitor should be a ceramic capacitor and be placed as close as possible to the VIN_BOOST and GND pins of the IC. These capacitors should be X7R or X5R ceramic capacitors.

Boost Output Capacitor

For the output capacitor C_{OUT}, it is recommended to use small X7R or X5R ceramic capacitors placed as close as possible to the VO_BOOST and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, the use of a small ceramic capacitor with a capacitance value of around 4.7 μF in parallel with the larger one is recommended. This small capacitor should be placed as close as possible to the VO_BOOST and GND pins of the IC.

A minimum *effective* capacitance value of 6 μF should be used; 10 μF is recommended. If the inductor value exceeds 4.7 μH, the value of the effective output capacitance value must be half the inductance value or higher for stability reasons; see Equation 11.

$$C_{OUT} \geq \frac{L}{2} \times \frac{\mu F}{\mu H} \quad (11)$$

When choosing the output capacitor, note the effects of bias voltage, temperature, and tolerance on the effective capacitance of the component. A capacitor in a 0603 package size suffers more capacitance degradation than a 0805 package at a similar bias voltage. For example, either a 22-µF 0603-sized capacitor or a 10-µF 0805-sized capacitor would be required to work with a nominal 10-µH inductor.

The TPS80010 boost is not sensitive to ESR in terms of stability. Using low-ESR capacitors, such as ceramic capacitors, is recommended to minimize output-voltage ripple. If heavy load changes are expected, the output capacitor value should be increased to avoid output voltage drops during fast load transients.

Table 2. Recommended Component List for Boost Converter

Component	Value	Part#	Supplier	Size
Inductor	10 μH	CBC3225T100MR	Taiyo Yuden	3.2 × 2.5 × 2.5 (1210)
		DO3314-103ML	Coilcraft	3.3 × 3.3 × 1.4
Capacitor (IN)	10 μF	GRM188R60J106ME47D	Murata	0603
Capacitor (OUT)	22 μF	AMK107BJ226MA-T	Taiyo Yuden	0603

PACKAGING INFORMATION

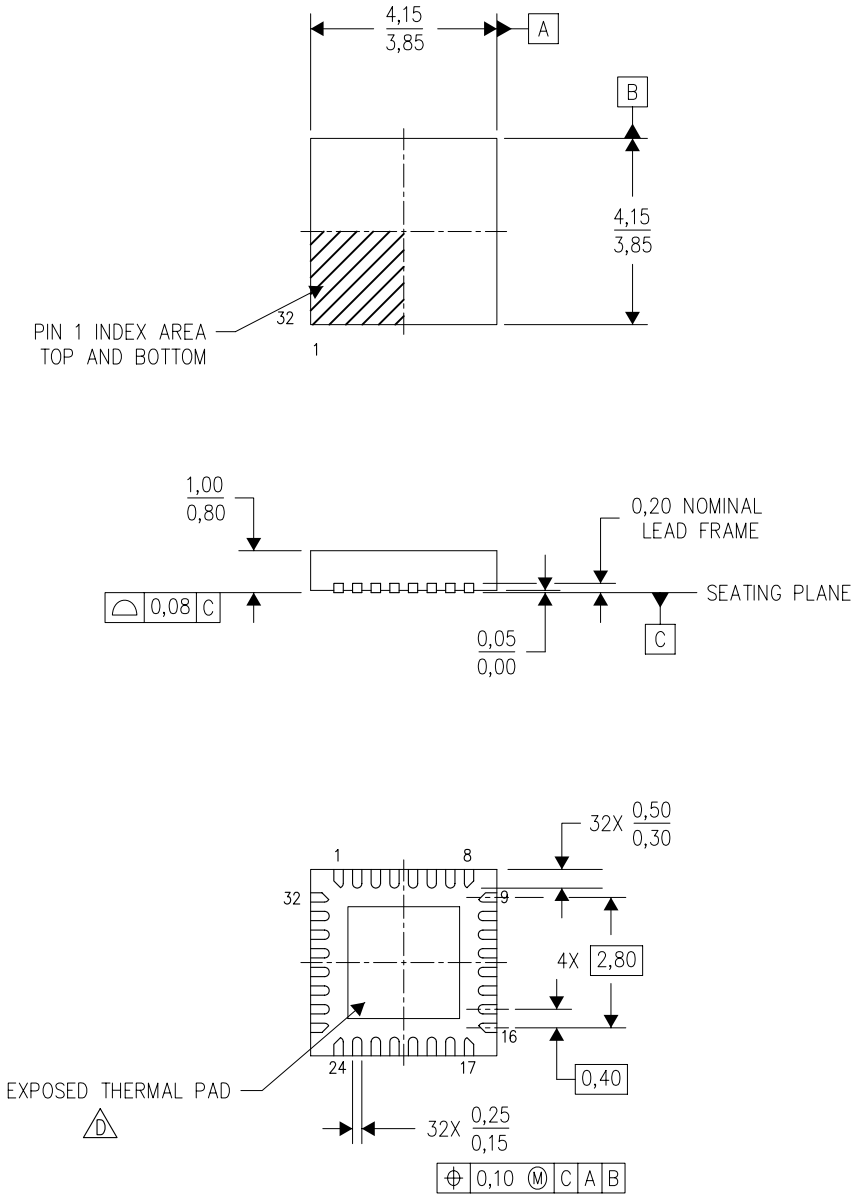
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS80010ARSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

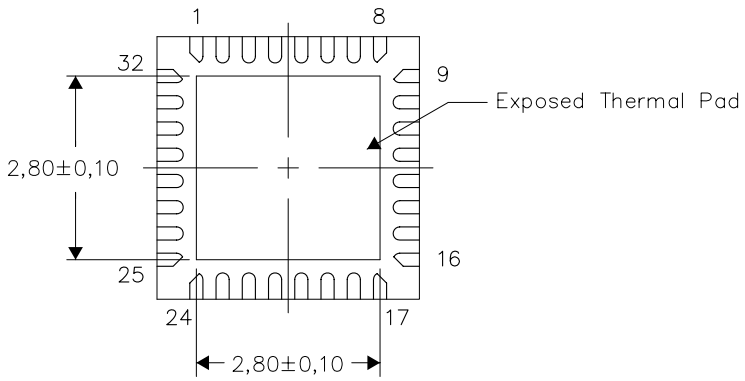
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

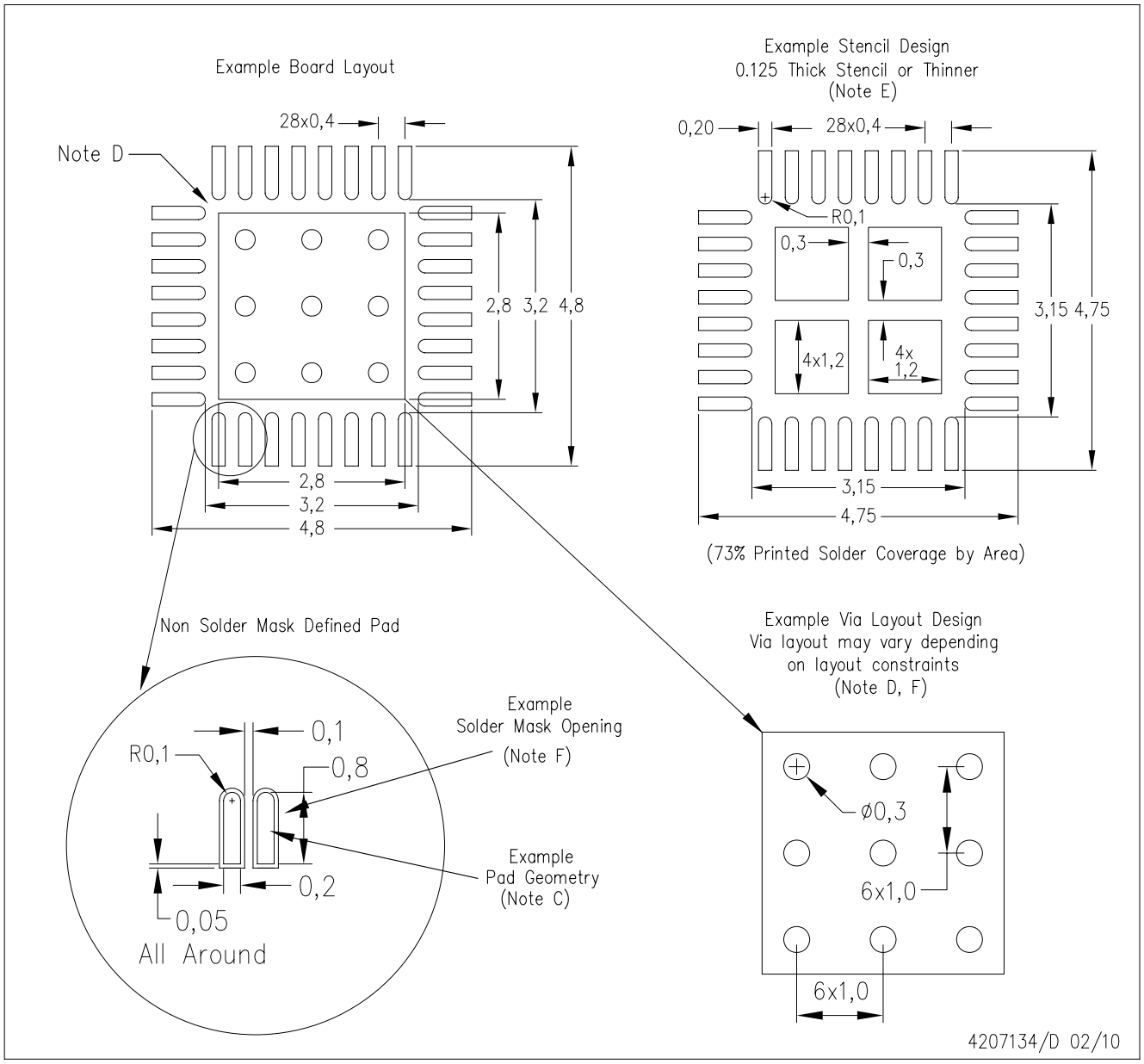


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RSM (S–PVQFN–N32)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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