



# CPH5518

## Bipolar Transistor (-50V, (-)3A, Low VCE(sat) Complementary Dual CPH5

ON Semiconductor®

<http://onsemi.com>

### Applications

- Relay drivers, lamp drivers, motor drivers

### Features

- Composite type with a PNP transistor and an NPN transistor contained in one package, facilitating high-density mounting
- The CPH5518 consists of two chips encapsulated in a package which are equivalent to the CPH3116 and the CPH3216, respectively
- Ultrasmall package facilitate miniaturization in end products (0.9mm mounting height)

### Specifications ( ) : PNP

Absolute Maximum Ratings at Ta=25°C

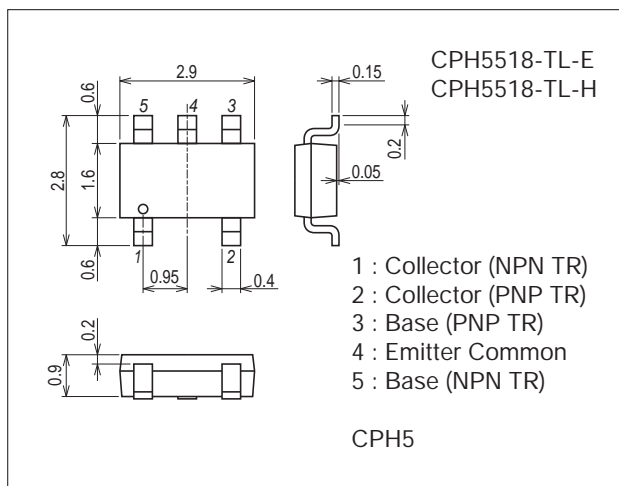
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V <sub>CB0</sub>		(-50)80	V
Collector-to-Emitter Voltage	V <sub>CEO</sub>		(-50)	V
Emitter-to-Base Voltage	V <sub>EB0</sub>		(-5)	V
Collector Current	I <sub>C</sub>		(-1.0)	A
Collector Current (Pulse)	I <sub>CP</sub>		(-3.0)	A
Base Current	I <sub>B</sub>		(-200)	mA
Collector Dissipation	P <sub>C</sub>	When mounted on ceramic substrate (600mm <sup>2</sup> ×0.8mm)1unit	0.9	W
Total Power Dissipation	P <sub>T</sub>	When mounted on ceramic substrate (600mm <sup>2</sup> ×0.8mm)	1.2	W
Junction Temperature	T <sub>j</sub>		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Package Dimensions

unit : mm (typ)

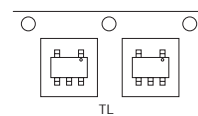
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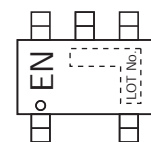
### Product & Package Information

- Package : CPH5
- JEITA, JEDEC : SC-74A, SOT-25
- Minimum Packing Quantity : 3,000 pcs./reel

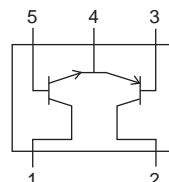
### Packing Type : TL



### Marking



### Electrical Connection

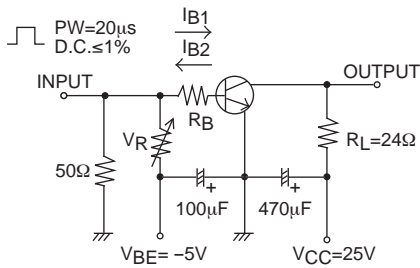


# CPH5518

## Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	$I_{CBO}$	$V_{CB}=(-)40V, I_E=0A$			(-)0.1	$\mu A$
Emitter Cutoff Current	$I_{EBO}$	$V_{EB}=(-)4V, I_C=0A$			(-)0.1	$\mu A$
DC Current Gain	$h_{FE}$	$V_{CE}=(-)2V, I_C=(-)100mA$	200		560	
Gain-Bandwidth Product	$f_T$	$V_{CE}=(-)10V, I_C=(-)300mA$		420		MHz
Output Capacitance	Cob	$V_{CB}=(-)10V, f=1MHz$		(9)6		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)500mA, I_B=(-)10mA$		(-230)130	(-380)190	mV
		$I_C=(-)300A, I_B=(-)6mA$		(-125)90	(-200)135	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=(-)500mA, I_B=(-)10mA$		(-)0.81	(-)1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu A, I_E=0A$	(-50)80			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)1mA, R_{BE}=\infty$	(-)50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=(-)10\mu A, I_C=0A$	(-)5			V
Turn-ON Time	$t_{on}$	See specified Test Circuit.		(36)38		ns
Storage Time	$t_{stg}$			(173)332		ns
Fall Time	$t_f$			(28)40		ns

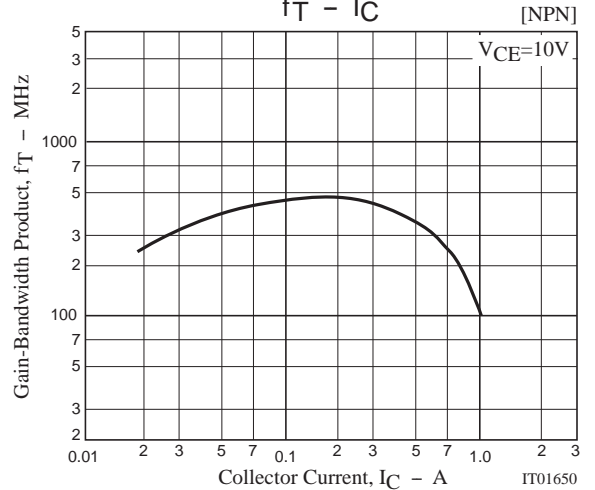
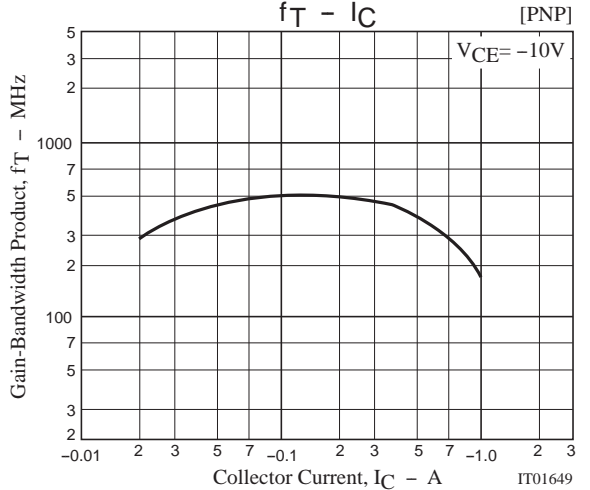
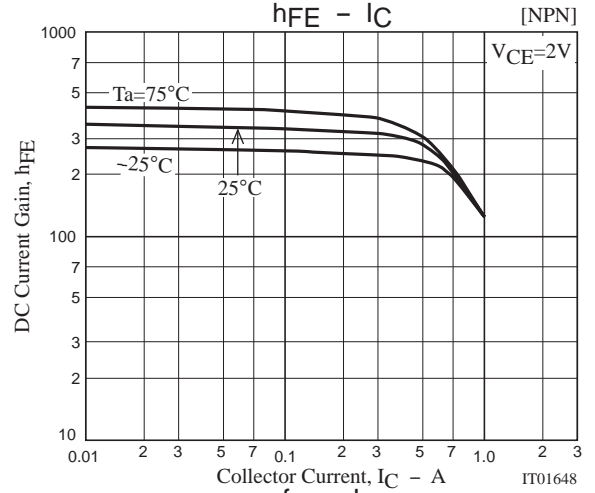
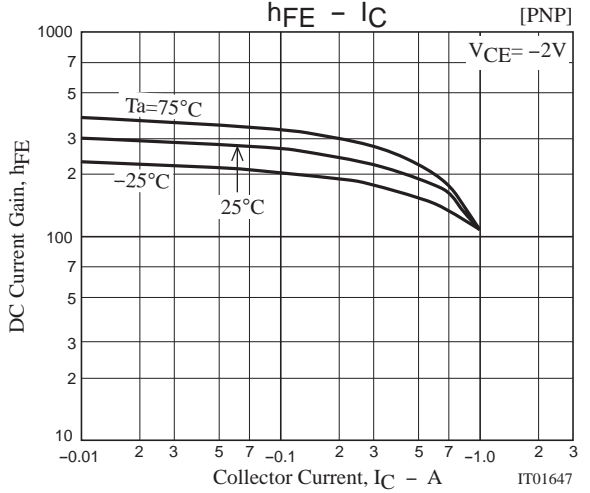
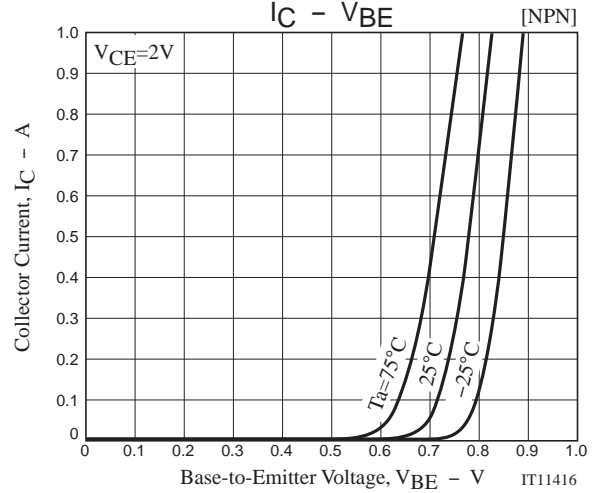
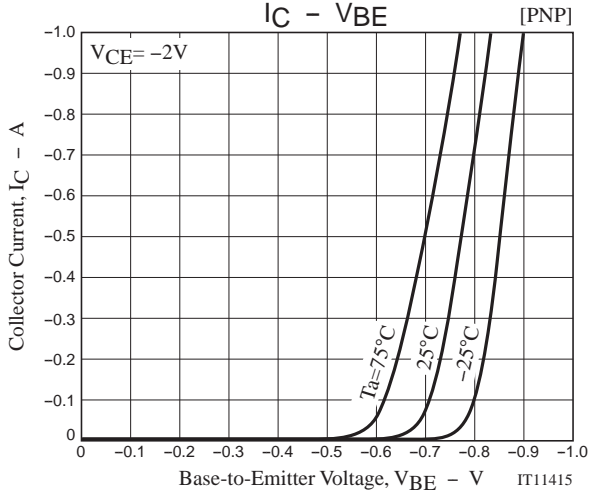
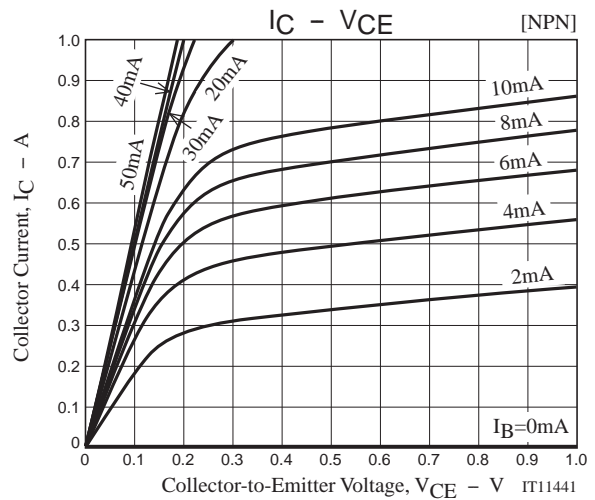
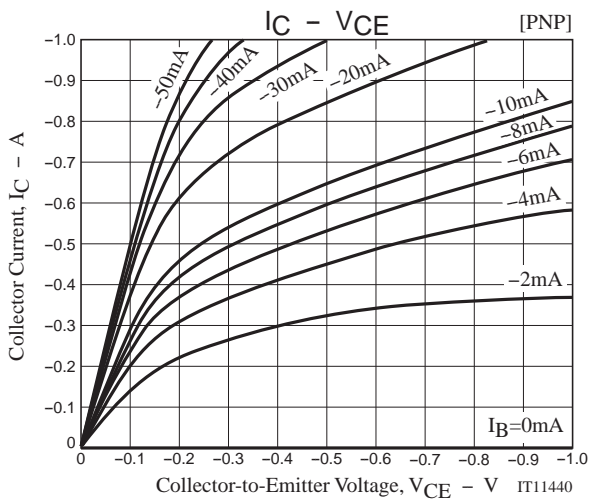
## Switching Time Test Circuit

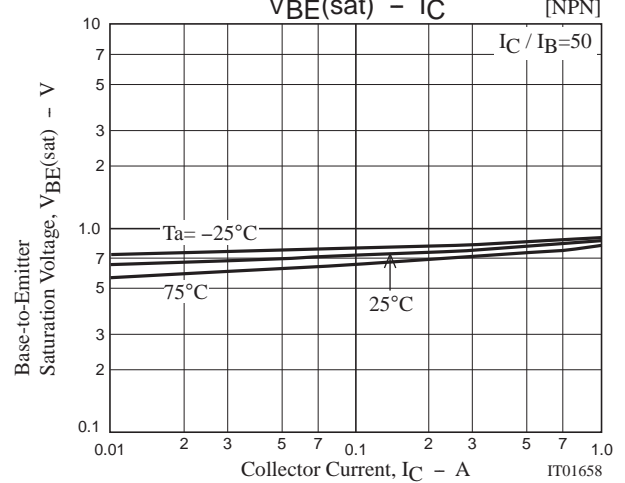
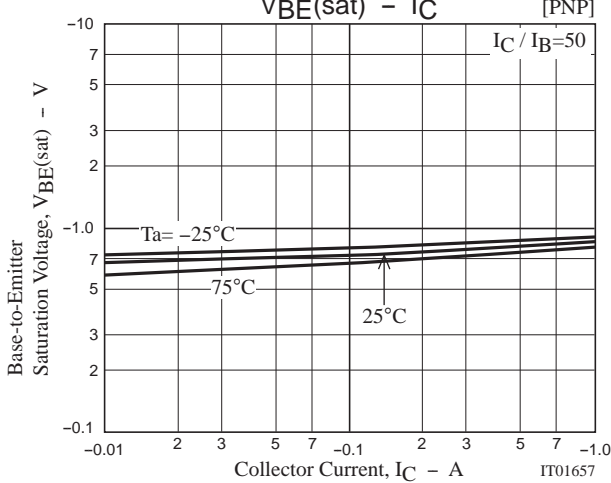
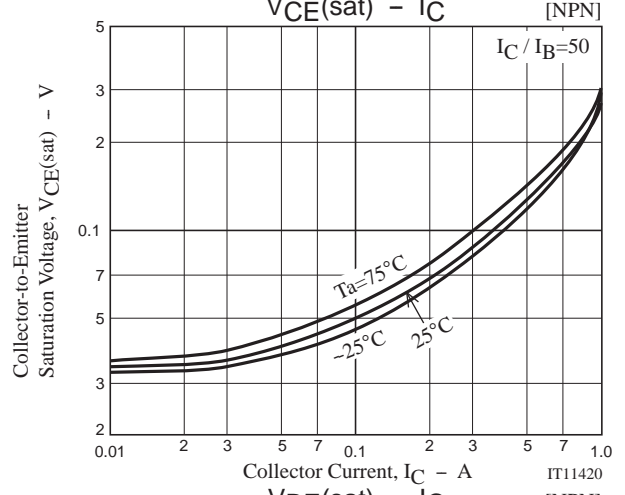
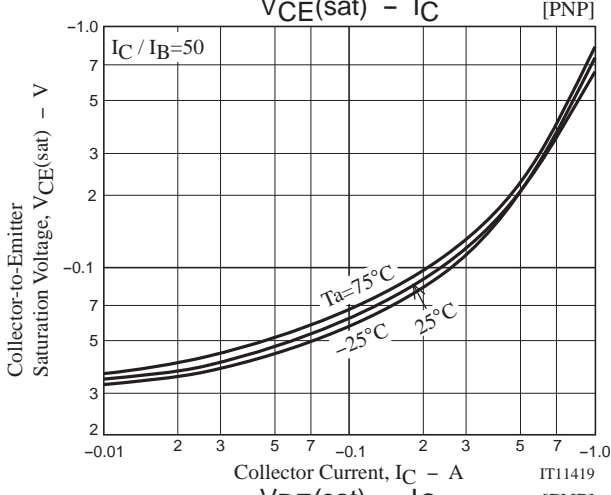
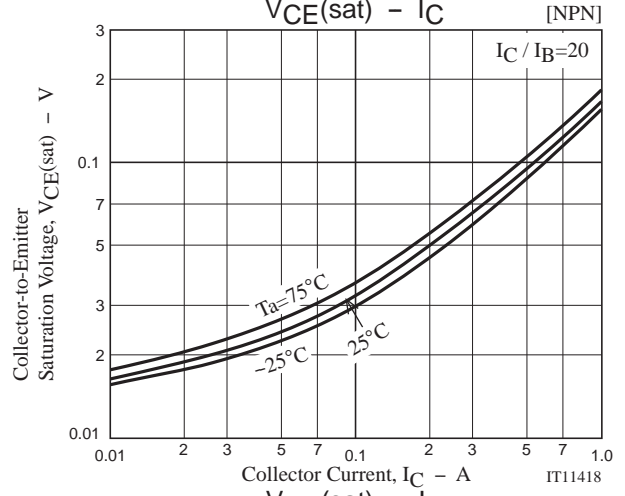
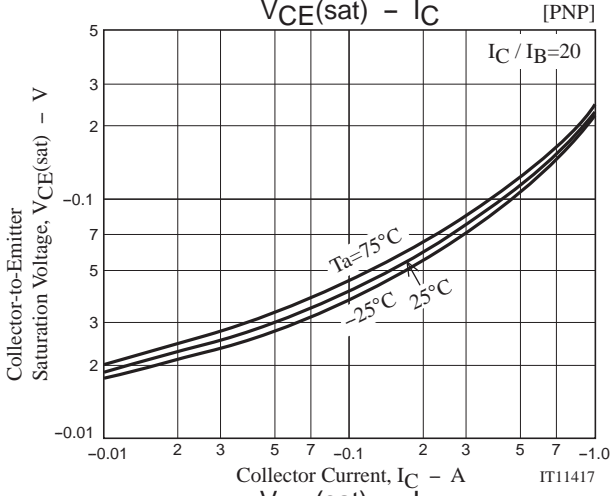
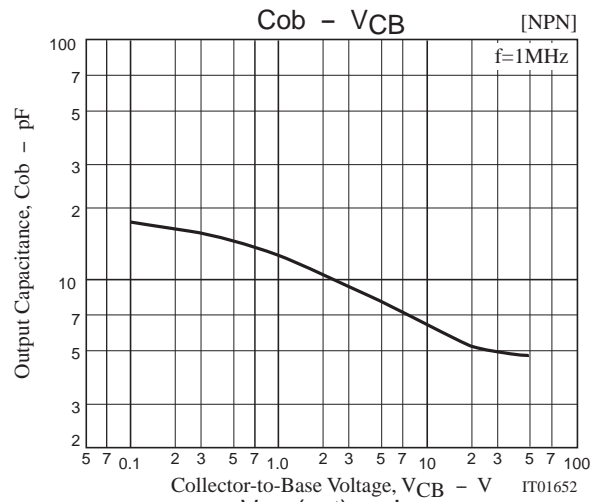
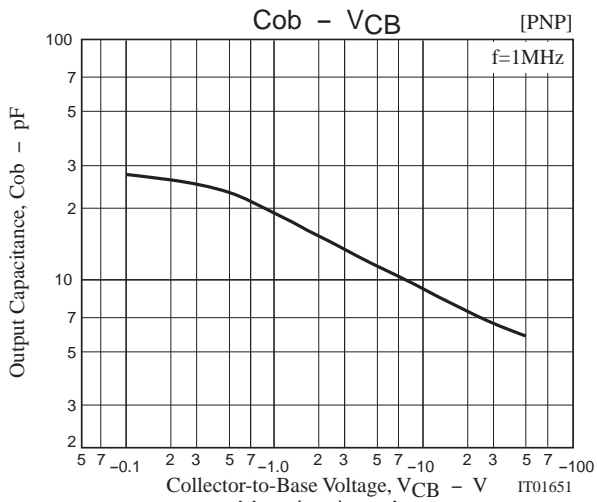


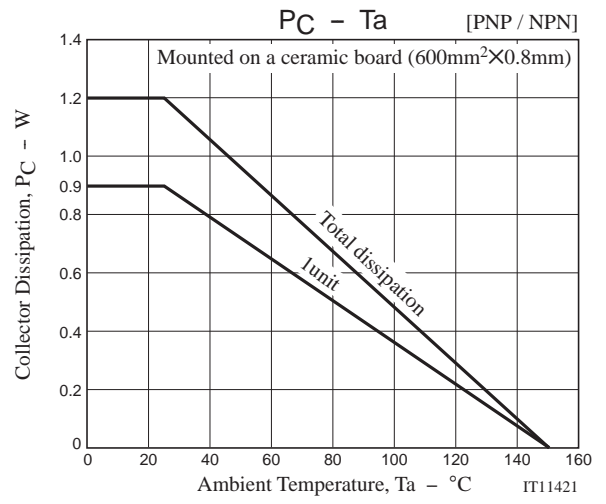
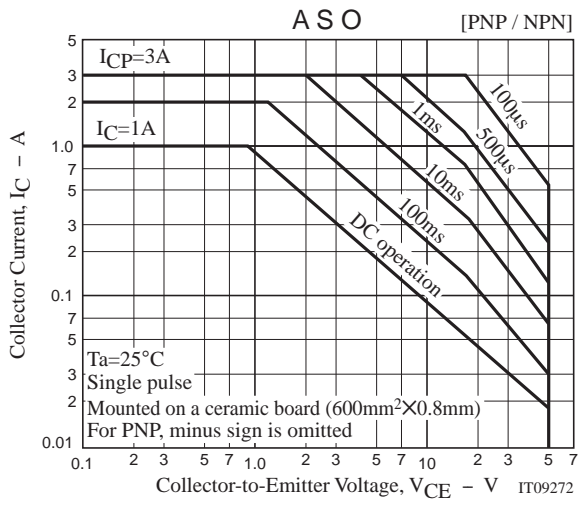
$I_C = 20I_{B1} = -20I_{B2} = 500mA$   
 (For PNP, the polarity is reversed.)

## Ordering Information

Device	Package	Shipping	memo
CPH5518-TL-E	CPH5	3,000pcs./reel	Pb Free
CPH5518-TL-H	CPH5	3,000pcs./reel	Pb Free and Halogen Free







Embossed Taping Specification

CPH5518-TL-E, CPH5518-TL-H

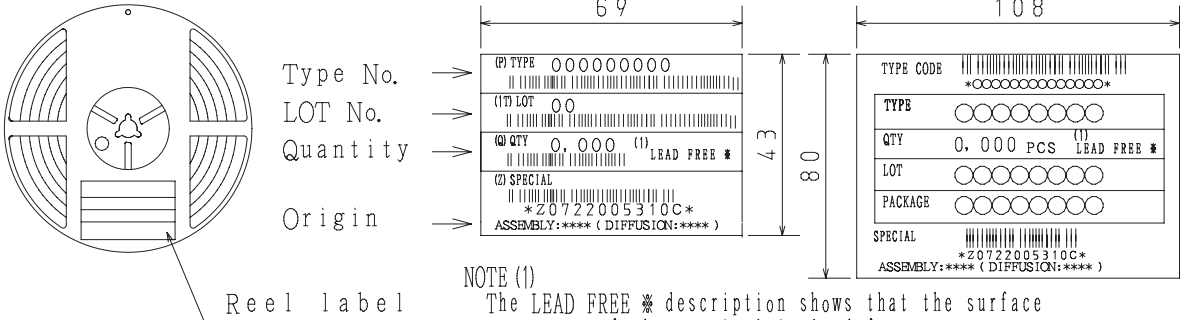
1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
CPH5	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Packing method

Reel label, Inner box label (unit:mm)      Outer box label

It is a label at the time of factory shipments.  
The form of a label may change in physical distribution process.

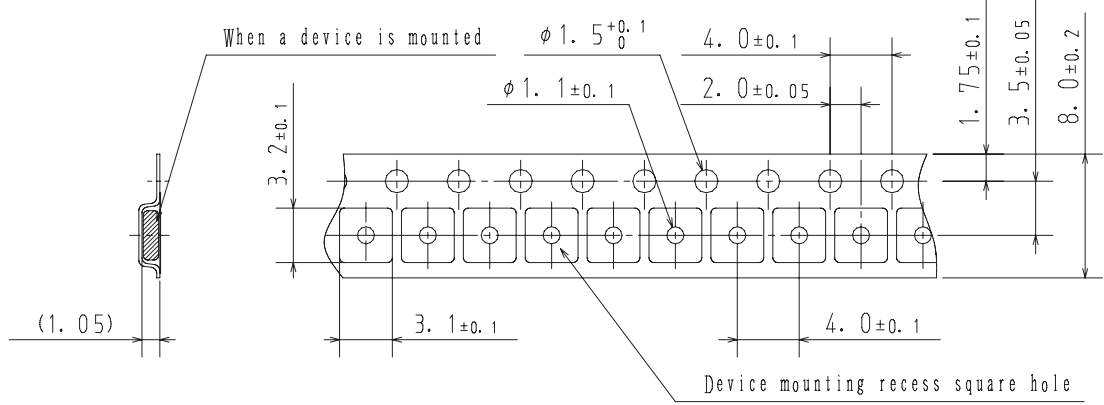


NOTE (1)  
The LEAD FREE \* description shows that the surface treatment of the terminal is lead free.

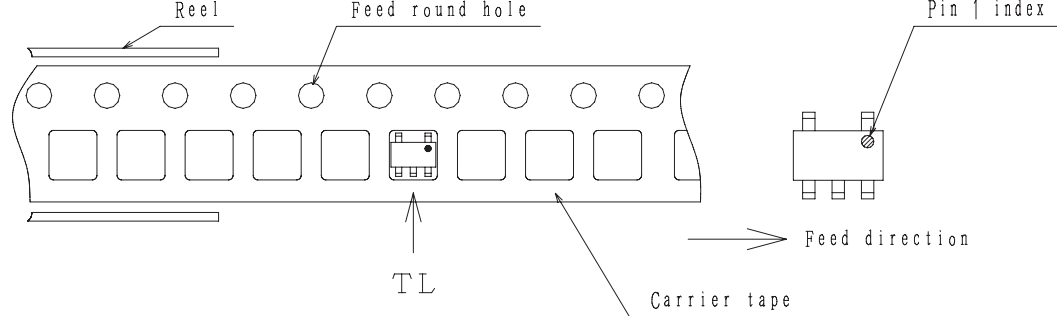
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction



Those with pin 1 index on the feed hole side.....TL

# CPH5518

## Outline Drawing

CPH5518-TL-E, CPH5518-TL-H



## Land Pattern Example



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