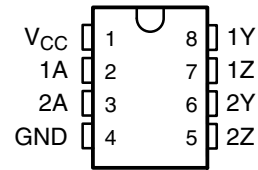


# SN75ALS191 DUAL DIFFERENTIAL LINE DRIVER

SLLS032B – DECEMBER 1987 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11
- Designed to Operate at 20 Mbaud or Higher
- TTL-and CMOS-Input Compatibility
- Single 5-V Supply Operation
- Output Short-Circuit Protection
- Improved Replacement for the  $\mu$ A9638

D OR P PACKAGE  
(TOP VIEW)



## description

The SN75ALS191 is a dual, high-speed, differential line driver designed to meet ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in eight-pin packages.

The SN75ALS191 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE  
(each driver)

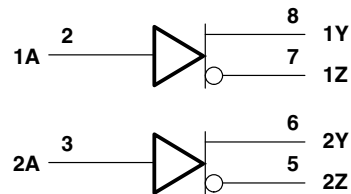
| INPUTS<br>A | OUTPUTS |   |
|-------------|---------|---|
|             | Y       | Z |
| H           | H       | L |
| L           | L       | H |

H = high level, L = low level,  
Z = high impedance

## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

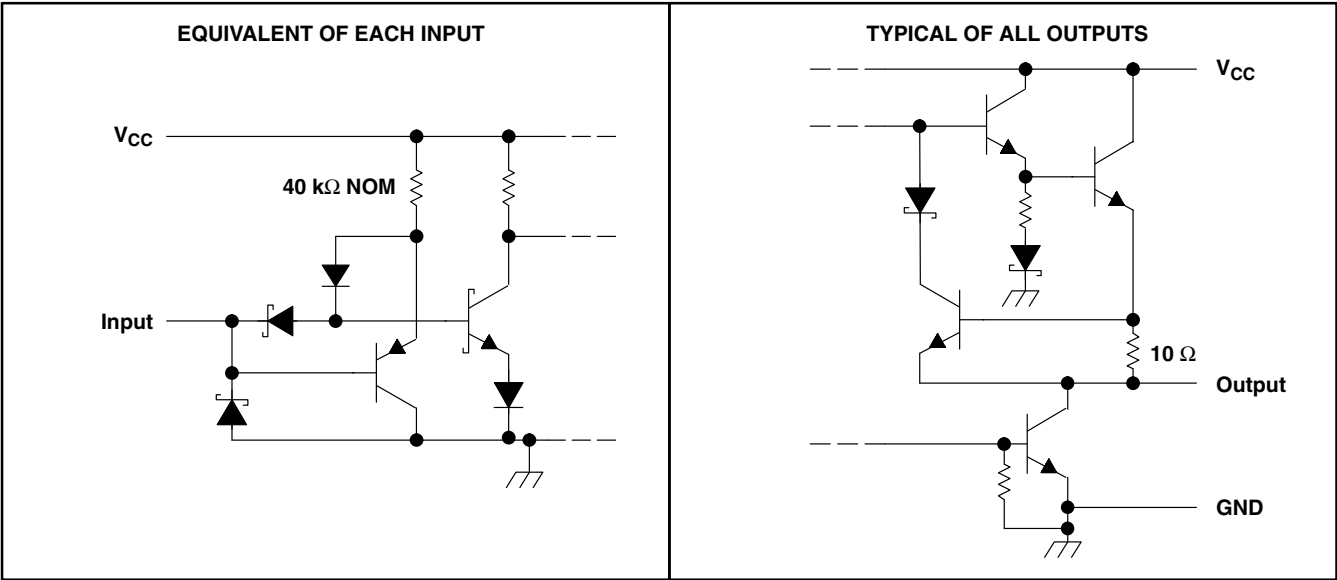
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SN75ALS191  
DUAL DIFFERENTIAL LINE DRIVER

SLLS032B – DECEMBER 1987 – REVISED MAY 1995

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                              |                              |
|--------------------------------------------------------------|------------------------------|
| Supply voltage, V <sub>CC</sub> (see Note 1)                 | 7 V                          |
| Input voltage, V <sub>I</sub>                                | 7 V                          |
| Continuous total dissipation                                 | See Dissipation Rating Table |
| Operating free-air temperature range, T <sub>A</sub>         | 0°C to 70°C                  |
| Storage temperature range, T <sub>stg</sub>                  | – 65°C to 150°C              |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential output voltage (V<sub>OD</sub>) are with respect to network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | T <sub>A</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR<br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C<br>POWER RATING |
|---------|---------------------------------------|------------------------------------------------|---------------------------------------|
| D       | 725 mW                                | 5.8 mW/°C                                      | 464 mW                                |
| P       | 1000 mW                               | 8.0 mW/°C                                      | 640 mW                                |

recommended operating conditions

|                                                | MIN  | NOM | MAX  | UNIT |
|------------------------------------------------|------|-----|------|------|
| Supply voltage, V <sub>CC</sub>                | 4.75 | 5   | 5.25 | V    |
| High-level input voltage, V <sub>IH</sub>      | 2    |     |      | V    |
| Low-level input voltage, V <sub>IL</sub>       |      |     | 0.8  | V    |
| High-level output current, I <sub>OH</sub>     |      |     | – 50 | mA   |
| Low-level output current, I <sub>OL</sub>      |      |     | 50   | mA   |
| Operating free-air temperature, T <sub>A</sub> | 0    |     | 70   | °C   |

**electrical characteristics over operating free-air temperature range (unless otherwise noted)**

| PARAMETER          |                                                     | TEST CONDITIONS                                   |                                  |                           | MIN                | TYP† | MAX  | UNIT |
|--------------------|-----------------------------------------------------|---------------------------------------------------|----------------------------------|---------------------------|--------------------|------|------|------|
| V <sub>IK</sub>    | Input clamp voltage                                 | V <sub>CC</sub> = 4.75 V, I <sub>I</sub> = −18 mA |                                  |                           |                    | −1   | −1.2 | V    |
| V <sub>OH</sub>    | High-level output voltage                           | V <sub>CC</sub> = 4.75 V, V <sub>IL</sub> = 0.8 V | V <sub>IH</sub> = 2 V,           | I <sub>OH</sub> = − 10 mA | 2.5                | 3.3  | V    |      |
|                    |                                                     |                                                   |                                  | I <sub>OH</sub> = − 40 mA | 2                  |      |      |      |
| V <sub>OL</sub>    | Low-level output voltage                            | V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 40 mA | V <sub>IH</sub> = 2 V,           | V <sub>IL</sub> = 0.8 V,  | 0.5                |      |      | V    |
| V <sub>OD1</sub>   | Differential output voltage                         | V <sub>CC</sub> = 5.25 V,                         | I <sub>O</sub> = 0               |                           | 2 V <sub>OD2</sub> |      |      | V    |
| V <sub>OD2</sub>   | Differential output voltage                         | V <sub>CC</sub> = 4.75 V to 5.25 V, See Figure 1  |                                  |                           | 2                  |      | V    |      |
| Δ  V <sub>OD</sub> | Change in magnitude of differential output voltage‡ |                                                   |                                  |                           | ± 0.4              |      |      |      |
| V <sub>OC</sub>    | Common-mode output voltage§                         |                                                   |                                  |                           | 3                  |      |      |      |
| Δ  V <sub>OC</sub> | Change in magnitude of common-mode output voltage‡  |                                                   |                                  |                           | ± 0.4              |      |      |      |
| I <sub>O</sub>     | Output current with power off                       | V <sub>CC</sub> = 0                               | V <sub>O</sub> = 6 V             |                           | 0.1                | 100  | μA   |      |
|                    |                                                     |                                                   | V <sub>O</sub> = − 0.25 V        |                           | −0.1               | −100 |      |      |
|                    |                                                     |                                                   | V <sub>O</sub> = − 0.25 V to 6 V |                           | ±100               |      |      |      |
| I <sub>I</sub>     | Input current                                       | V <sub>CC</sub> = 5.25 V,                         | V <sub>I</sub> = 5.5 V           |                           |                    | 50   | μA   |      |
| I <sub>IH</sub>    | High-level input current                            | V <sub>CC</sub> = 5.25 V,                         | V <sub>I</sub> = 2.7 V           |                           |                    | 25   | μA   |      |
| I <sub>IL</sub>    | Low-level input current                             | V <sub>CC</sub> = 5.25 V,                         | V <sub>I</sub> = 0.5 V           |                           |                    | 200  | μA   |      |
| I <sub>OS</sub>    | Short-circuit output current¶                       | V <sub>CC</sub> = 5.25 V,                         | V <sub>O</sub> = 0               |                           |                    | −50  | −150 | mA   |
| I <sub>CC</sub>    | Supply current (all drivers)                        | V <sub>CC</sub> = 5.25 V,                         | No load,                         | All inputs at 0 V         |                    | 32   | 40   | mA   |

† All typical values are at  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡  $|V_{OD}|$  and  $|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

§ In ANSI Standard EIA/TIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .

¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V}$**

| PARAMETER                                       | TEST CONDITIONS                                           | MIN | TYP# | MAX | UNIT |
|-------------------------------------------------|-----------------------------------------------------------|-----|------|-----|------|
| $t_{d(OD)}$ Differential-output delay time      | $C_L = 15\text{ pF}$ , $R_L = 100\ \Omega$ , See Figure 2 |     | 3.5  | 7   | ns   |
| $t_{t(OD)}$ Differential-output transition time |                                                           |     | 3.5  | 7   | ns   |
| Skew                                            |                                                           |     | 1.5  | 4   | ns   |

# Typical values are at  $T_A = 25^\circ\text{C}$ .

# SN75ALS191 DUAL DIFFERENTIAL LINE DRIVER

SLLS032B – DECEMBER 1987 – REVISED MAY 1995

## PARAMETER MEASUREMENT INFORMATION

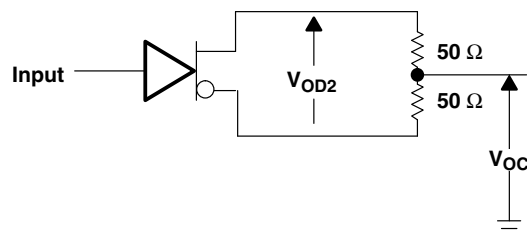
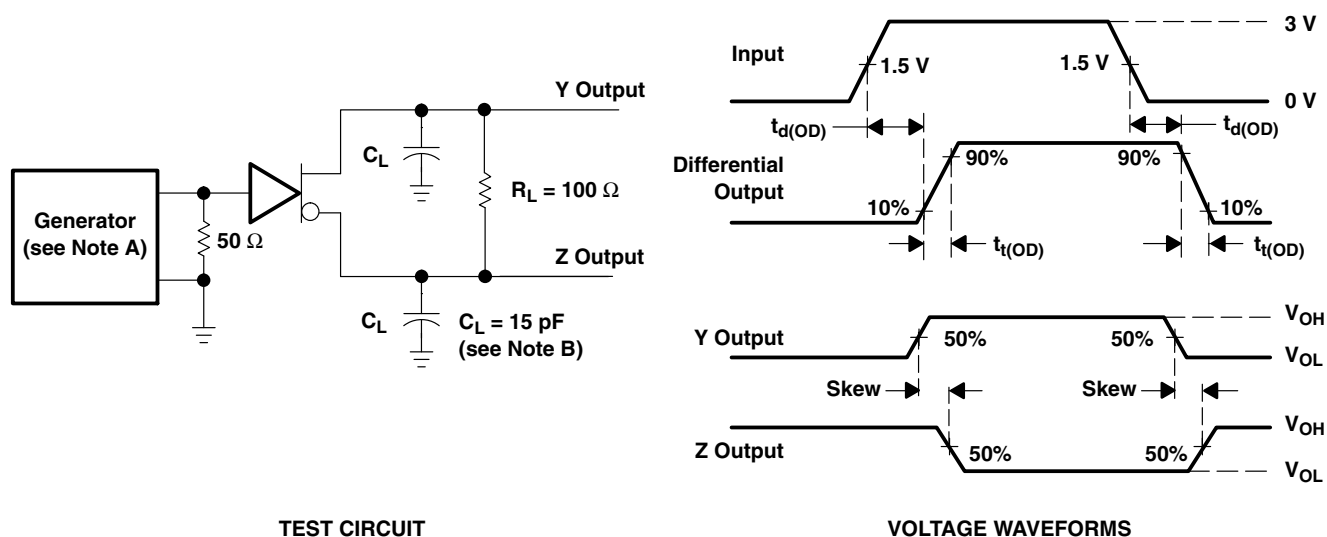


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse generator has the following characteristics:  $Z_O = 50 \Omega$ ,  $PRR \leq 500 \text{ kHz}$ ,  $t_w = 100 \text{ ns}$ ,  $t_r = \leq 5 \text{ ns}$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75ALS191D      | ACTIVE        | SOIC         | D                  | 8    | 75             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75A191                  | <a href="#">Samples</a> |
| SN75ALS191DG4    | ACTIVE        | SOIC         | D                  | 8    | 75             | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75A191                  | <a href="#">Samples</a> |
| SN75ALS191DR     | ACTIVE        | SOIC         | D                  | 8    | 2500           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75A191                  | <a href="#">Samples</a> |
| SN75ALS191P      | ACTIVE        | PDIP         | P                  | 8    | 50             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | 75ALS191                | <a href="#">Samples</a> |
| SN75ALS191PE4    | ACTIVE        | PDIP         | P                  | 8    | 50             | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | 75ALS191                | <a href="#">Samples</a> |
| SN75ALS191PSR    | ACTIVE        | SO           | PS                 | 8    | 2000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | V191                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

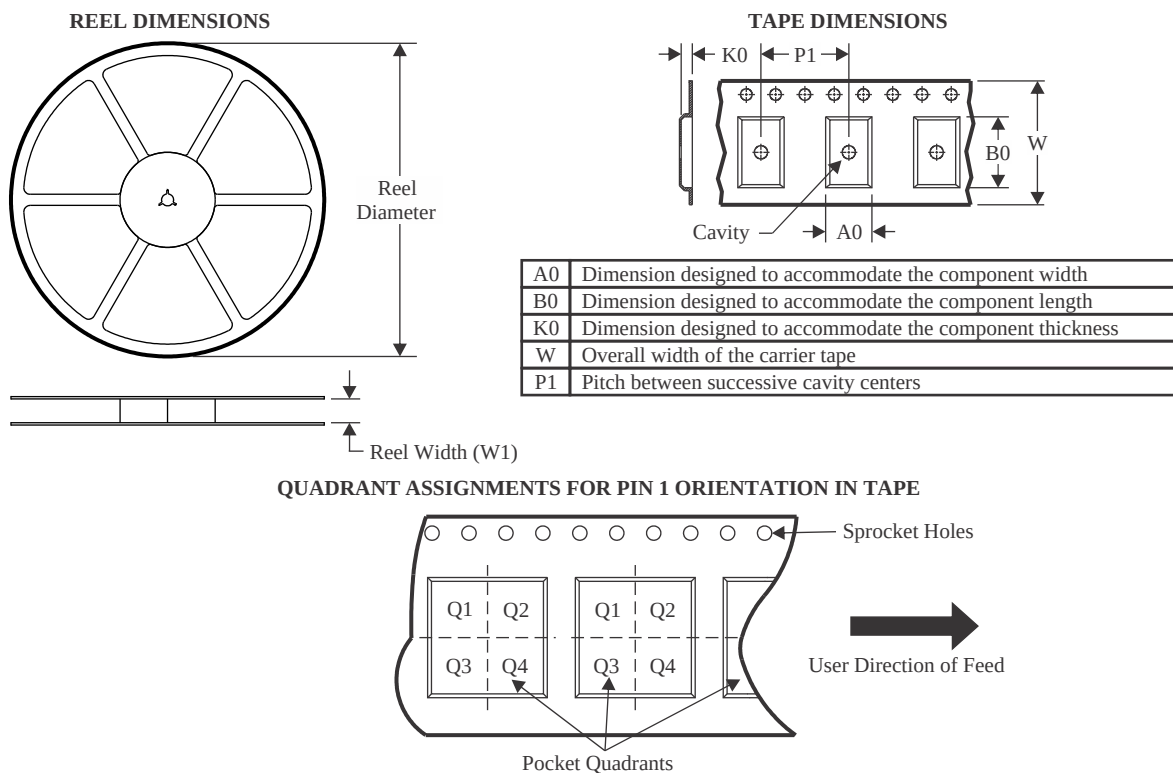
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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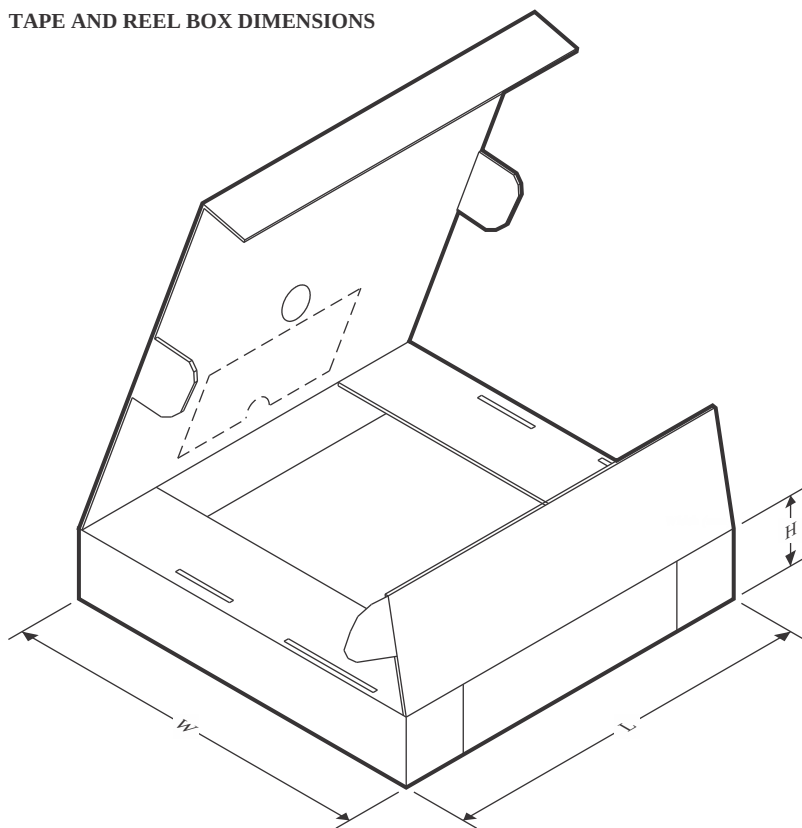
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75ALS191DR  | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN75ALS191PSR | SO           | PS              | 8    | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75ALS191DR  | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| SN75ALS191PSR | SO           | PS              | 8    | 2000 | 356.0       | 356.0      | 35.0        |

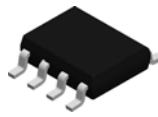


## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN75ALS191D   | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| SN75ALS191DG4 | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| SN75ALS191P   | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| SN75ALS191PE4 | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |

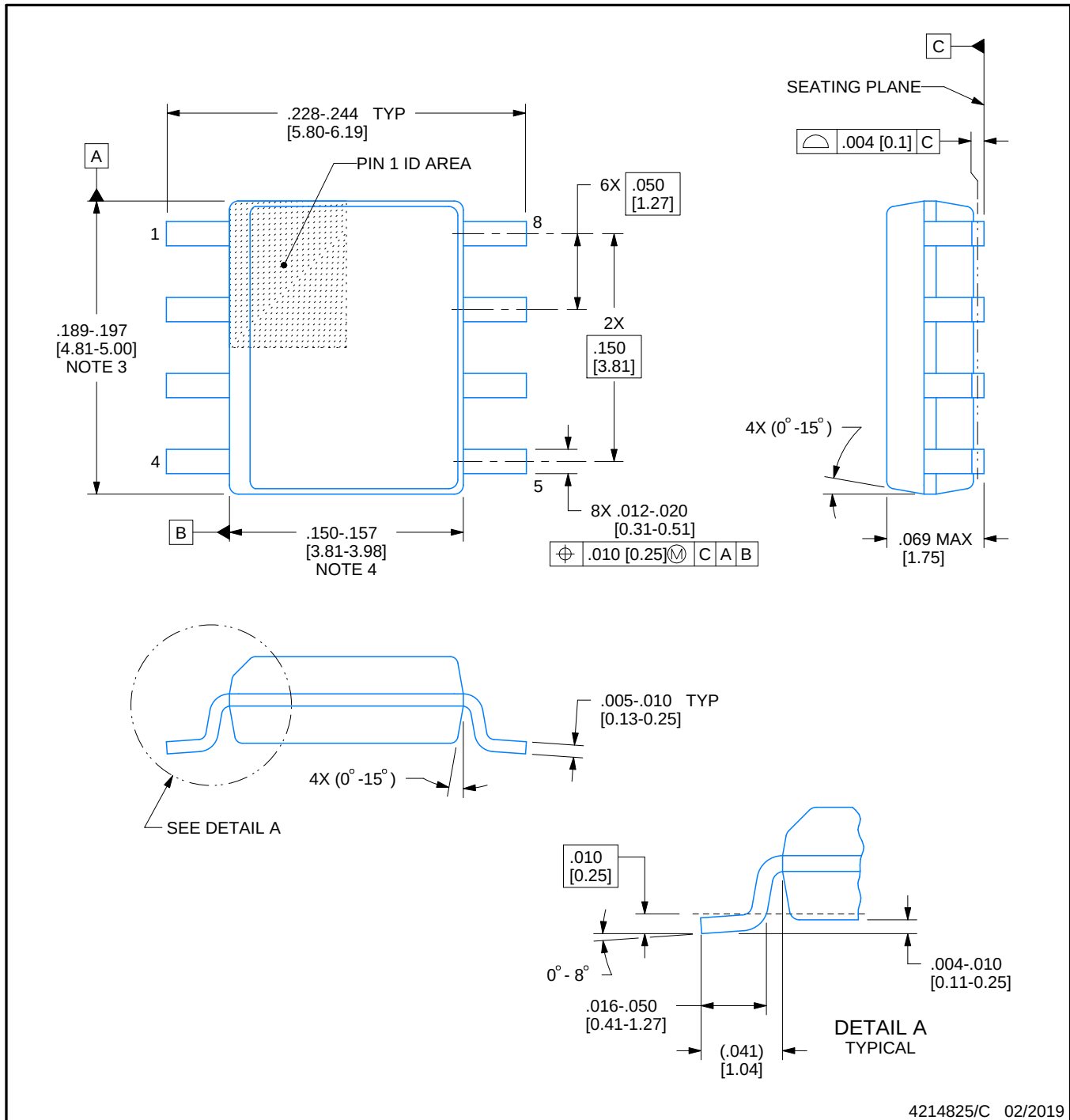


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

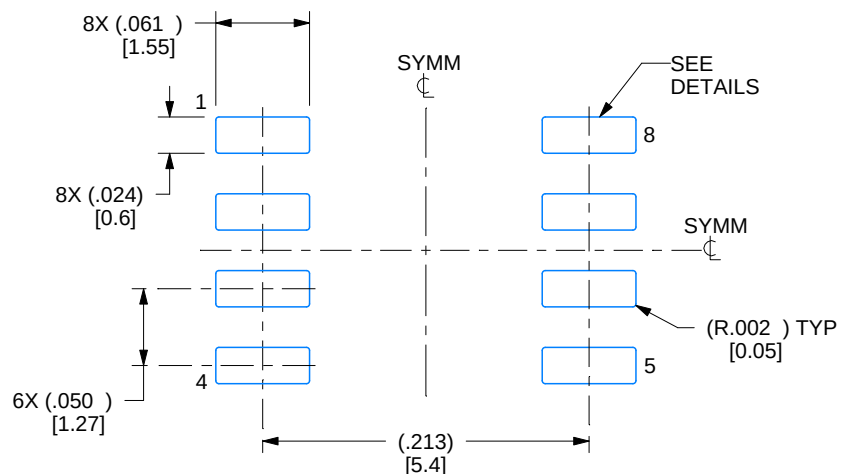
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

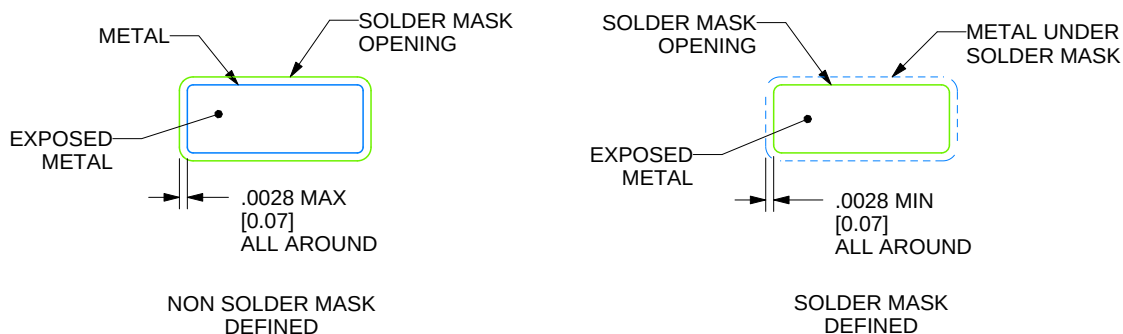
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

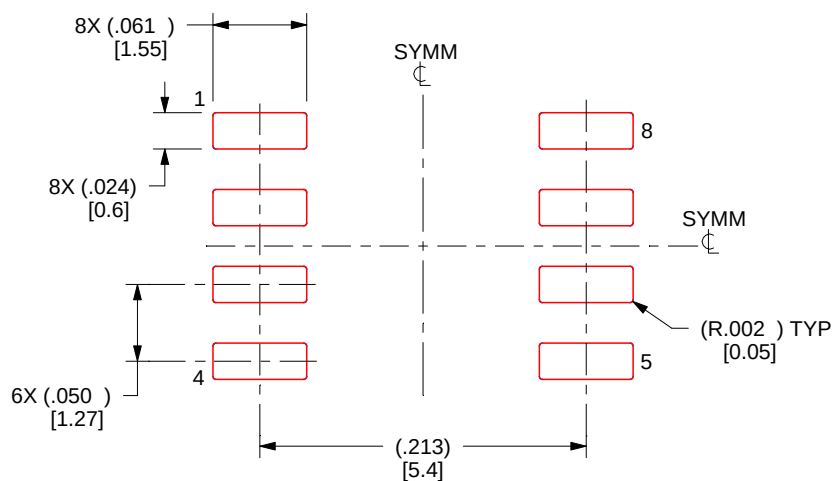
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

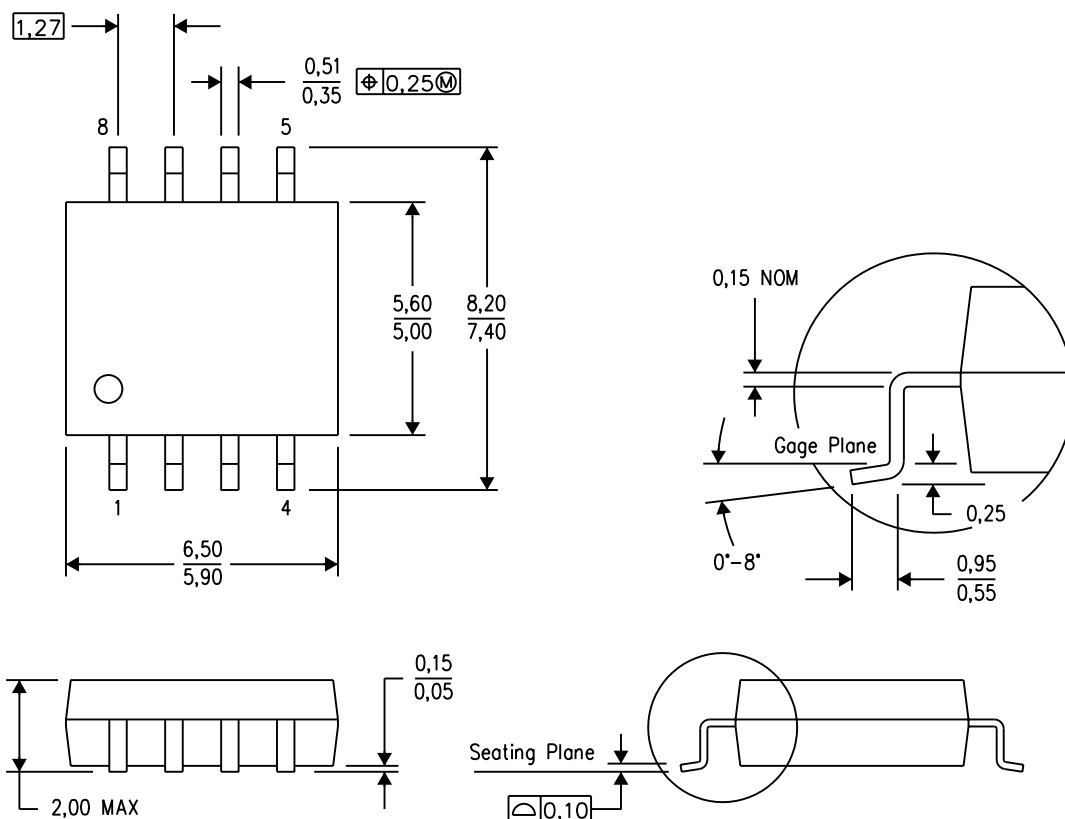
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

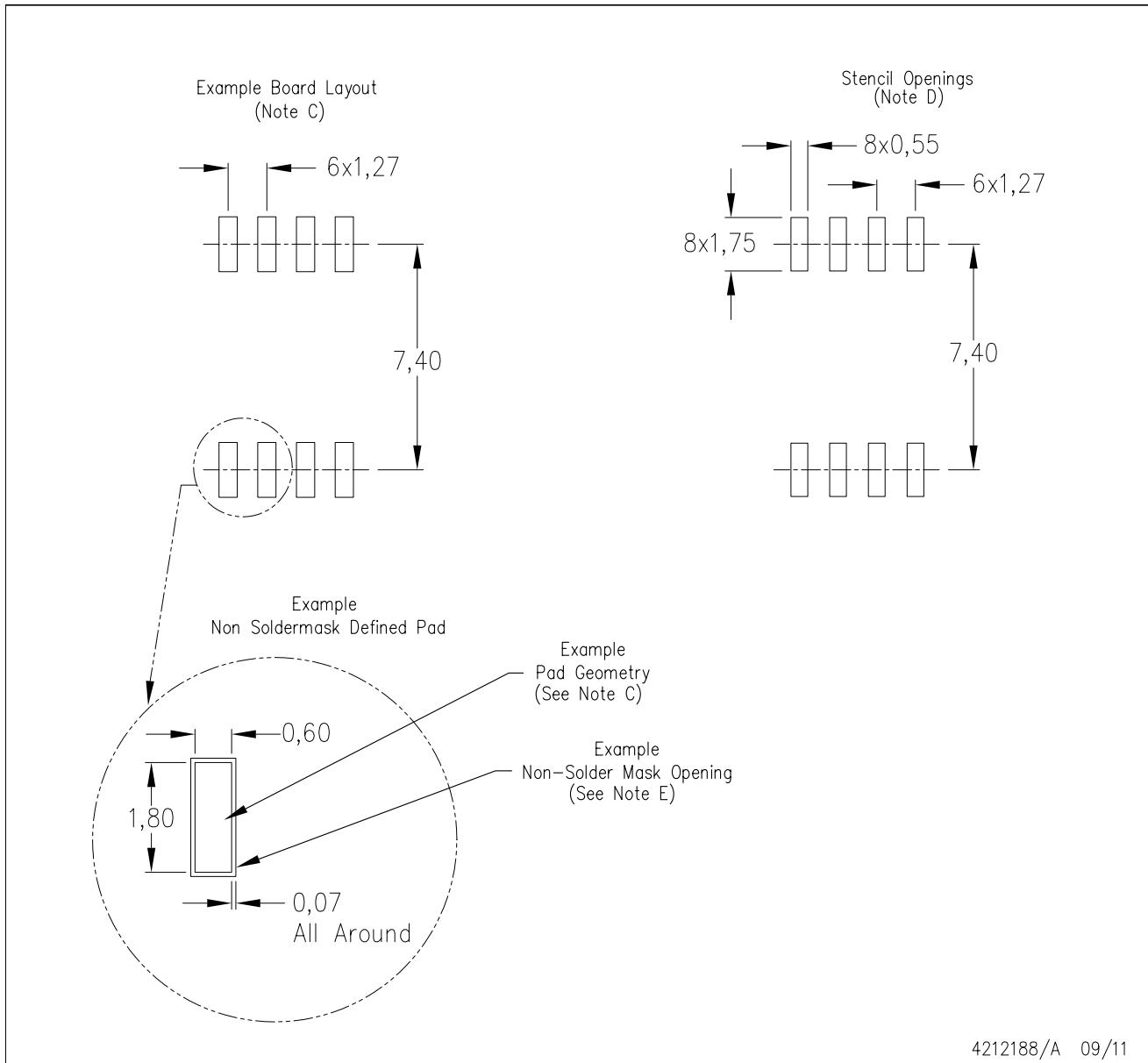


4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## PS (R-PDSO-G8)

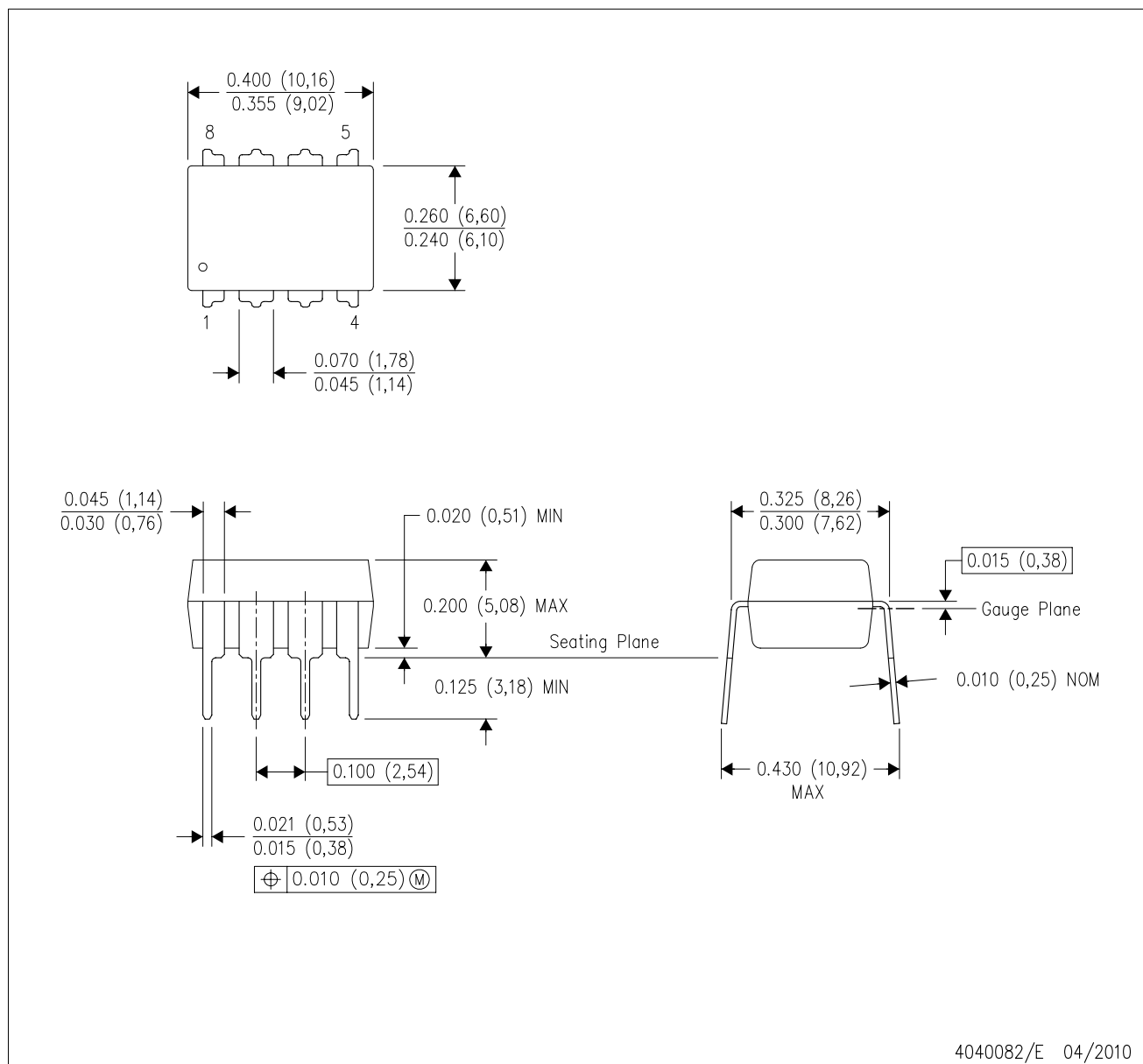
## PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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