PRELIMINARY

# DOT MATRIX LCD 80-OUT SEGMENT DRIVER

## ■ GENERAL DESCRIPTION

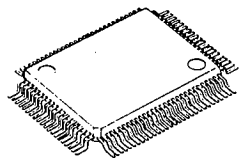
The NJU6416 is a serial input, 80-out segment driver for dot matrix LCDs, especially useful as extension driver for LCD controller drivers like NJU6426.

It consists of bidirectional shift register, 80-bit latch, and 80-out high voltage LCD drivers.

The bidirectional shift register performs the efficient extension driver allocation according to the number of characters and easy wiring with the LCD panel.

As the 80-driver has 4 level voltage input to drive the LCD, adjustable driving voltage according to the LCD panel can be supplied from the external power source.

## ■ PACKAGE OUTLINE

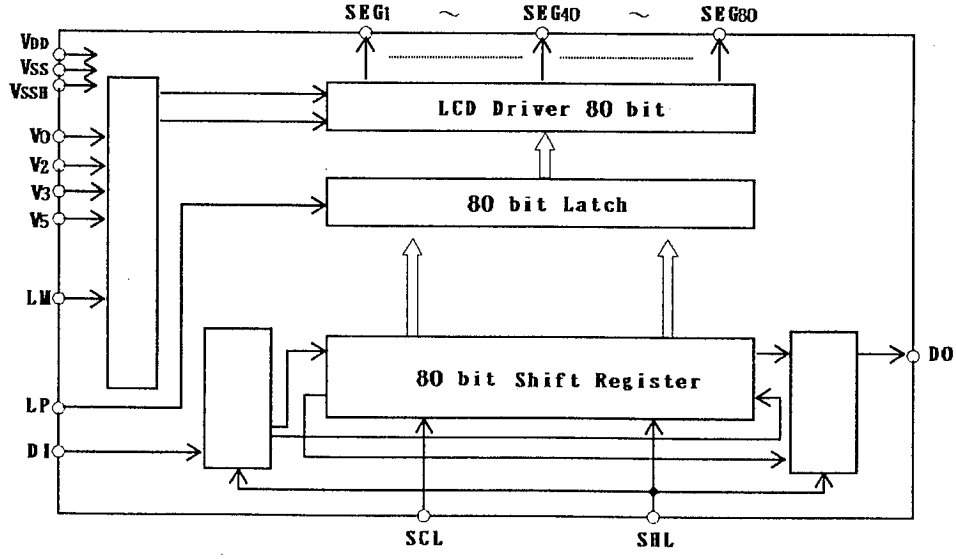


NJU6416F

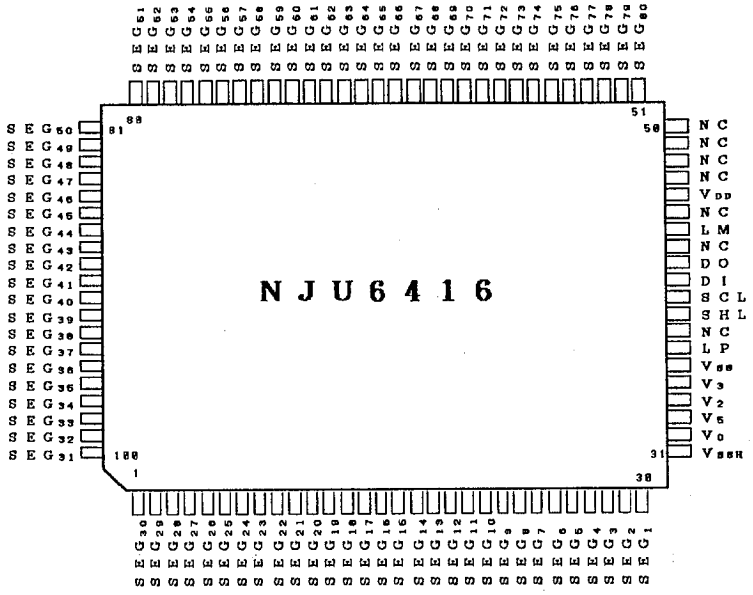
## ■ FEATURES

- 80 Segment Drivers
- 80-bit Shift Register
  ( Bidirectional Shift Register)
- Two of Shift Direction Select Terminal
- Fast Data Transmission ( Shift Clock 3.3 MHz min.)
- External Power Supply for LCD Driving Voltage
- LCD Driving Voltage --- $V_{DD}$ - 3.0V ~ $V_{DD}$ - 13.5V
- Operating Voltage --- 5.0 V ± 10 %
- Package Outline --- QFP100/Chip
- C-MOS Technology

## ■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION




## ■ TERMINAL DESCRIPTION

| NO. | SYMBOL | F U N C T I O N |
|---|---|---|
| 1~30<br>51~100 | $SEG_1$~<br>$SEG_{80}$ | LCD segment driving terminal.<br>Each terminal corresponds to each bit of shift register |
| 41 | DI | Data input terminal. The DI terminal is fixed the input terminal regardless the shift direction.<br>Display data is input synchronized with the clock signal. |
| 42 | DO | Data output terminal. The DO terminal is fixed the output terminal regardless the shift direction.<br>The data is output synchronized with the clock signal. |
| 40 | SCL | Shift register clock pulse input terminal.<br>The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time and falling time should be set less than 50ns(MAX) respectively. |
| 39 | SHL | Shift direction select terminal.<br>"H" : Shift direction is from 80th bit to 1st bit.<br>"L" : Shift direction is from 1st bit to 80th bit.<br>The DI and DO terminals are fixed input and output terminal respectively regardless this terminal input level. |
| 37 | LP | Latch pulse input terminal. The data in the shift register is latched to the Latch by this signal.<br>"H" : Data writing, "L" : Data latch |
| 44 | LM | Alternate signal input for LCD driving. |
| 46<br>36 | $V_{DD}$<br>$V_{SS}$ | Power supply terminal (connect to the controller's $V_{DD}$ terminal)<br>Power supply terminal (connect to the controller's $V_{SS}$ terminal) |
| 32,34,35,33<br>31 | $V_0$,$V_2$,$V_3$,$V_5$<br>$V_{SSH}$ | LCD driving power source terminals.<br>$V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5 \geqq V_{SSH}$ |
| 38,43,45<br>47~50 | NC | Non connection. (Normally open) |

5

## ■ FUNCTIONAL DESCRIPTION

### (1) Shift register control

The 80-bit shift register is a bidirectional register.
The shift direction of 80-bit bidirectional shift register is shown below:

| Control Terminal | Input | Shift Direction |
|---|---|---|
| SHL | "H" | 80 → 1 |
| | "L" | 1 ← 80 |

(Note) DI and DO terminals are fixed input and output terminal respectively regardless the SHL input level.

### (2) LCD driver output truth table

| Input Data | Selection/Non-selection | LM | Driver Output ($SEG_1$ to $SEG_{80}$) |
|---|---|---|---|
| "H" | Selection | H | $V_5$ |
| | | L | $V_0$ |
| "L" | Non-selection | H | $V_3$ |
| | | L | $V_2$ |

## ■ ABSOLUTE MAXIMUM RATINGS

( Ta=25°C )

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage ( 1 ) | $V_{DD}$ | - 0.3 ~ + 7.0 | V |
| Supply Voltage ( 2 ) Note 1) | $V_{DD}$ ~ $V_5$ | $V_{DD}$-13.5 ~ $V_{DD}$+0.3 | V |
| Input Voltage | $V_{IN}$ | - 0.3 ~ $V_{DD}$+0.3 | V |
| Operating Temperature | Topr | - 30 ~ + 80 | °C |
| Storage Temperature | Tstg | - 55 ~ + 150 | °C |

Note 1) The relation : $V_{DD} \geqq V_0 \geqq V_2 \geqq V_3 \geqq V_5 \geqq V_{SSH}$ must be maintained.

## ■ ELECTRICAL CHARACTERISTICS

・DC Characteristics ( $V_{DD}$=5V±10% , Ta=-20 ～ +75°C )

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input Voltage Note1) | $V_{IH}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IL}$ | | | | 0.2$V_{DD}$ | |
| Input Current Note1) | $I_{IH}$ | $V_{IH}$ = $V_{DD}$ | | | 1 | μA |
| | $I_{IL}$ | $V_{IL}$ = 0V | - 1 | | | |
| Output Voltage Note2) | $V_{OH}$ | $I_O$ = -40μA | 4.2 | | | V |
| | $V_{OL}$ | $I_O$ = 0.4mA | | | 0.4 | |
| Driver On-resistance Note3) | $R_{ON}$ | Id = 0.05mA | | | 5 | kΩ |
| Operating Current ( Logic Part ) | $I_{SSO}$ | LM,LP=130μs cycle, SCL=1.5MHz. Every one bit Inverted Data. No Load. | | 1.1 | 1.5 | mA |
| Operating Current ( LCD Driver Part ) | $I_{SSHO}$ | LM,LP=130μs cycle, SCL=1.5MHz. Every one bit Inverted Data. No Load. | | 70 | 100 | μA |
| LCD Driving Voltage | $V_{LCD}$ | $V_{SSH}$ Terminal, $V_{DD}$=5V | $V_{DD}$-3.0 | | $V_{DD}$-13.5 | V |

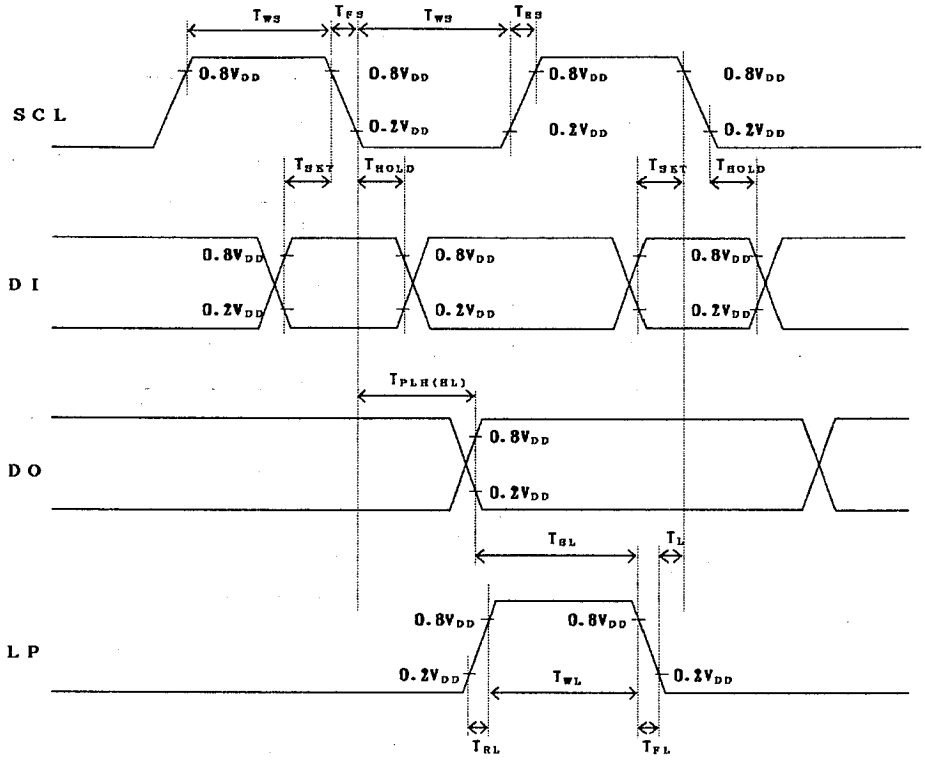
Note 1) Apply to LM, LP, SCL, SHL and DI terminals.
Note 2) Apply to DO terminal.
Note 3) Apply to $SEG_1$ ～ $SEG_{80}$ terminals.

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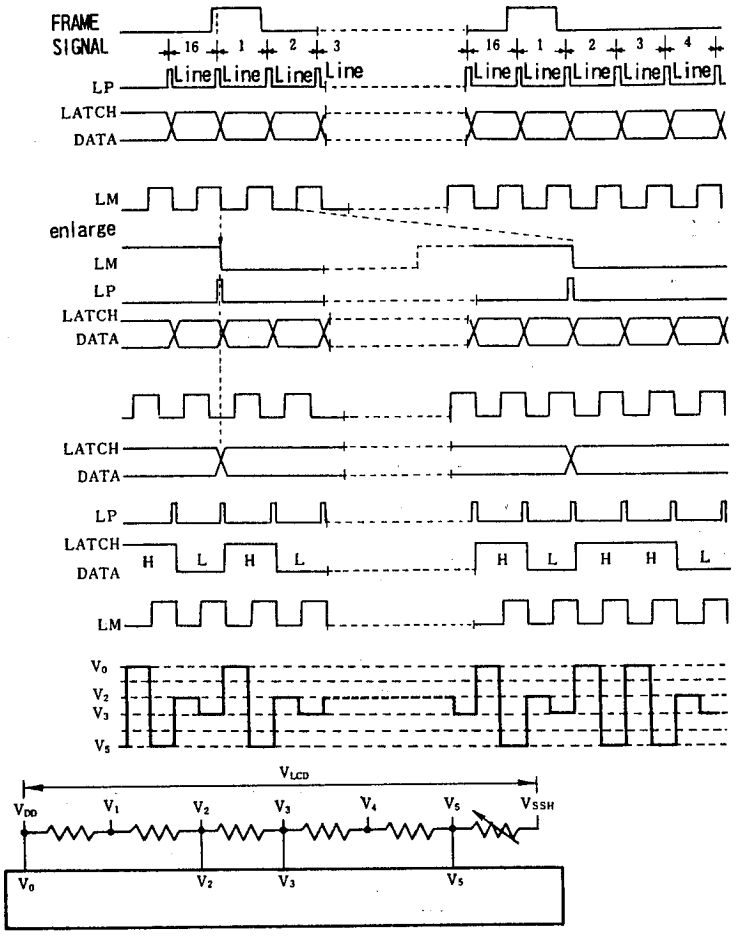
・AC Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation Delay Time | $T_{PLH(HL)}$ | | | | 250 | ns |
| Maximum Operating Frequency | $f_{SCL}$ | Duty = 50 % | 3.3 | | | MHz |
| SCL Pulse Width | $T_{WS}$ | | 125 | | | ns |
| LP Pulse Width | $T_{WL}$ | | 125 | | | ns |
| Set up Time | $T_{SET}$ | | 50 | | | ns |
| SCL → LP Time | $T_{SL}$ | | 250 | | | ns |
| LP → SCL Time | $T_{LS}$ | | 0 | | | ns |
| Data Hold Time | $T_{HOLD}$ | | 50 | | | ns |
| SCL Rise, Fall Time | $T_{FS}$, $T_{RS}$ | | | | 50 | ns |
| LP Rise, Fall Time | $T_{FL}$, $T_{RL}$ | | | | 1 | μs |

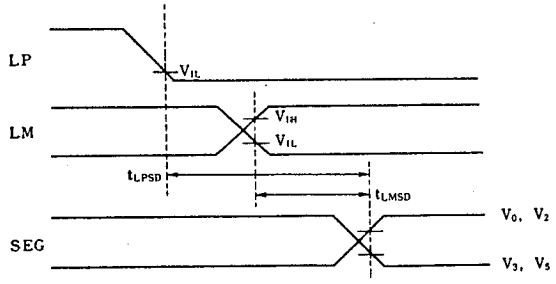
## ■ AC CHARACTERISTICS TIMING CHART



■ TIMING CHART 1/5 Bias, 1/16 Duty Ratio

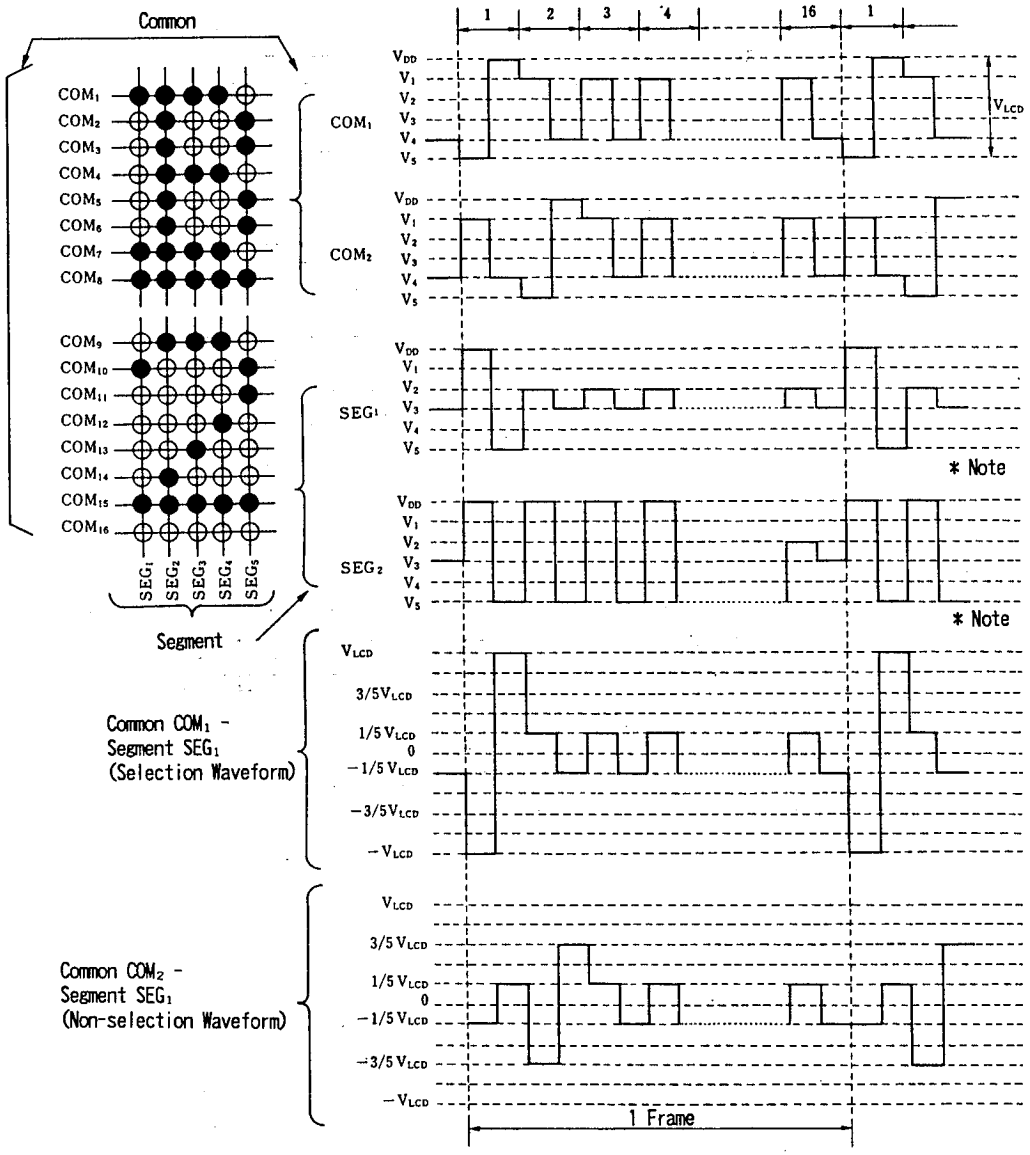



■ SEGMENT SIGNAL OUTPUT TIMING




| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| LP - SEG Output Delay Time | $T_{LPSD}$ | $C_L$ = 100pF | | | 4.5 | μs |
| LM - SEG Output Delay Time | $T_{LMSD}$ | $C_L$ = 100pF | | | 4.5 | |

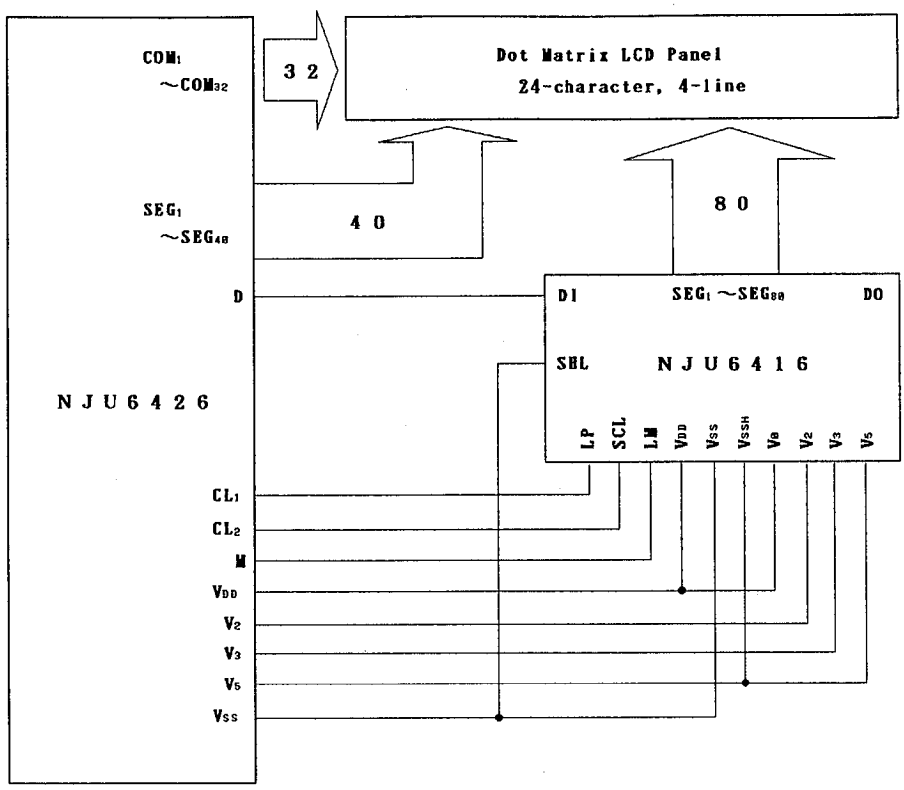
■ LCD DRIVING WAVEFORM EXAMPLE 1/5 Bias, 1/16 Duty Ratio




* Note : In case of $V_O$ terminal connected to the $V_{DD}$.

## ■ APPLICATION CIRCUIT

24-character 4-line Display Example (NJU6426 + NJU6416)



MEMO

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