M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP
M37210E4-XXXSP/FP, M37210E4SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37210M3-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP or a 64-pin plastic molded QFP. This single-chip microcomputer is useful for the channel selection system for TVs because it provides PWM function, OSD display function and so on. In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

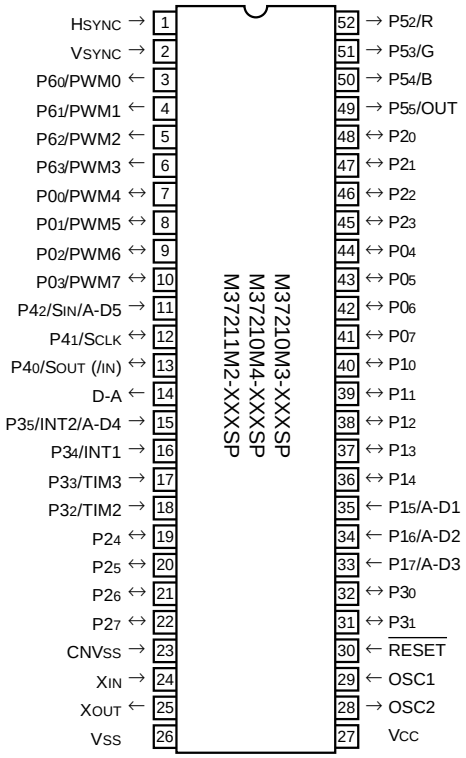
The features of the M37210E4-XXXSP/FP and the M37210E4SP/FP are similar to those of the M37210M4-XXXSP except that these chips have a built-in PROM which can be written electrically.

The differences between the M37210M3-XXXSP/FP, the M37210 M4-XXXSP, and the M37211M2-XXXSP are the ROM size, the RAM size, and the PWM outputs as shown below. Accordingly, the following descriptions will be for the M37210M3-XXXSP/FP unless otherwise noted.

Type name	ROM size	RAM size	6-bit PWM outputs
M37210M3-XXXSP/FP	12 K bytes	256 bytes	8
M37210M4-XXXSP	16 K bytes	320 bytes	8
M37211M2-XXXSP	8 K bytes	192 bytes	6

Note : After the reset, set the stack page selection bit which is set "1" to "0" because the internal RAM of the M37211M2-XXXSP is in only the zero page.

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

Note : The M37211M2-XXXSP does not have the PWM6 and the PWM7.

FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 12 K bytes (M37210M3-XXXSP/FP)
  16 K bytes (M37210M4-XXXSP)
  8 K bytes (M37211M2-XXXSP)
  RAM ..... 256 bytes (M37210M3-XXXSP/FP)
  320 bytes (M37210M4-XXXSP)
  192 bytes (M37211M2-XXXSP)
  ROM for display ..... 3 K bytes
  RAM for display ..... 72 bytes
- The minimum instruction execution time
  ..... 0.5µs (at 8MHz oscillation frequency)
- Power source voltage ..... 5V ± 10%
- Power dissipation 110mW
  (at 4MHz oscillation frequency, VCC = 5.5V, at CRT display)
- Subroutine nesting ..... 96 levels (Max.)
- Interrupts ..... 12 types, 12 vectors
- 8-bit timers 4
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4) 25
- Output ports (ports P5, P6) 8
- Output ports (ports P52, P56) 12
- 12 V withstand ports 4
- Serial I/O ..... 8-bit × 1 channel
- PWM output circuit ..... (14-bit × 1, 6-bit × 8) ... M37210M3
  M37210M4
  (14-bit × 1, 6-bit × 6) M37211M2
- A-D comparator (5-bit resolution) ..... 5 channels
- CRT display function
  Display characters ..... 18 characters × 2 lines
  (16 lines max.)
  Character kinds ..... 96 kinds
  Dot structure ..... 12 × 16 dots
  Character size ..... 3 kinds
  Character color kinds (It can be specified by the character)
  max. 7 kinds (R, G, B)
  Raster color (max. 7 kinds)
  Display layout
  Horizontal ..... 64 levels
  Vertical ..... 128 levels
  Bordering (horizontal and vertical)

APPLICATION

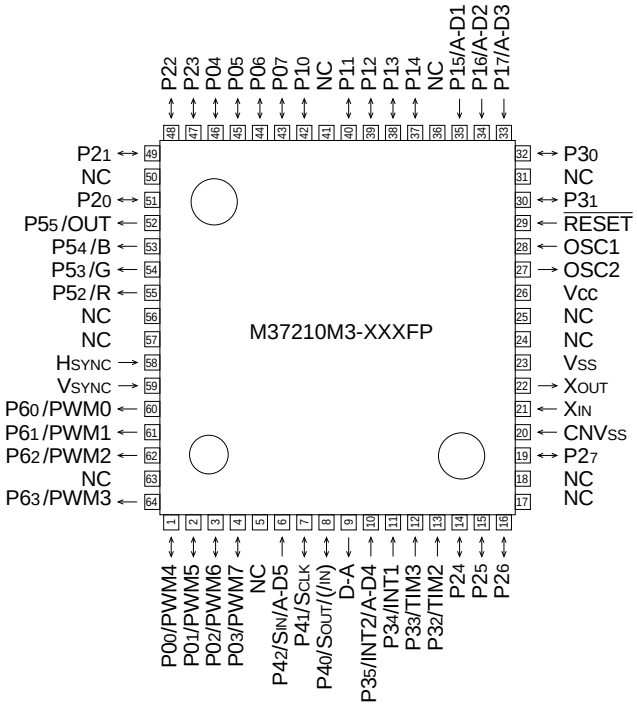
TV

MITSUBISHI ELECTRIC

M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP
M37210E4-XXXSP/FP, M37210E4SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

PIN CONFIGURATION (TOP VIEW)



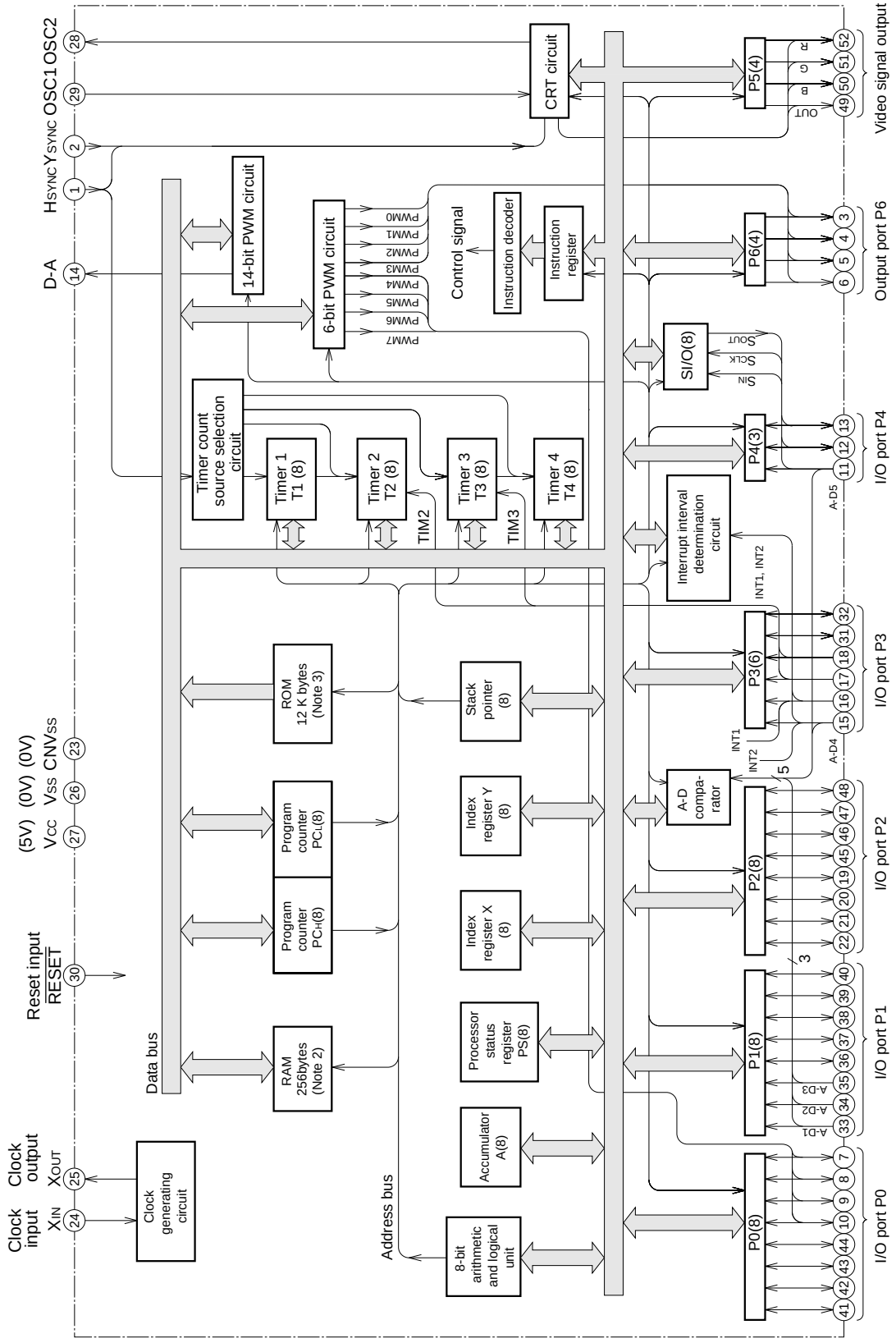
Outline 64P6N-A

NC : No connection

M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP
M37210E4-XXXSP/FP, M37210E4SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONAL BLOCK DIAGRAM of M37210M3-XXXSP



Notes 1 : The M37211M2-XXXSP does not have PWM outputs of pins 9 and 10.
2 : 320 bytes for M37210M4-XXXSP and 192 bytes for M37211M2-XXXSP
3 : 16 K bytes for M37210M4-XXXSP and 8 K bytes for M37211M2-XXXSP

M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP
M37210E4-XXXSP/FP, M37210E4SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.5μs (the minimum instruction execution time, at 8MHz oscillation frequency)
Clock frequency			8MHz
Memory size	M37210M3-XXXSP/FP	ROM	12 K bytes
		RAM	256 bytes
	M37210M4-XXXSP	ROM	16 K bytes
		RAM	320 bytes
	M37211M2-XXXSP	ROM	8 K bytes
		RAM	192 bytes
Input/Output ports	P0	I/O	8-bit X 1 (can be used as N-channel open-drain output and PWM4-PWM7)(Note)
	$P1_0$ – $P1_4$	I/O	5-bit X 1 (CMOS 3-state output)
	$P1_5$ – $P1_7$	Input	3-bit X 1 (can be used as A-D input)
	P2	I/O	8-bit X 1 (CMOS 3-state output)
	$P3_0$, $P3_1$	I/O	2-bit X 1 (CMOS 3-state input/output)
	$P3_2$, $P3_5$	Input	4-bit X 1 (can be used as timer input pins, INT input pins and A-D input pins)
	$P4_0$, $P4_1$	I/O	2-bit X 1 (can be used as N-channel open-drain output and serial I/O function pins)
	$P4_2$	Input	1-bit X 1 (can be used as serial I/O and A-D input)
	P5	Output	4-bit X 1 (can be used as R, G, B, OUT pins)
	P6	Output	4-bit X 1 (can be used as N-channel open-drain output and PWM0-PWM3 output pins)
Serial I/O			8-bit X 1
Timers			8-bit timer X 4
Subroutine nesting			96 levels (max.)
Interrupt			Two external interrupts, four internal timer interrupts, one serial I/O interrupt, one CRT interrupt, one f(X_{IN})/4096 interrupt, one V_{SYNC} interrupt, BRK instruction
Clock generating circuit			Built-in circuit (externally connected a ceramic resonator or a quartz-crystal oscillator)
Power source voltage			5V ± 10%
Power dissipation	at CRT display ON		110mW (at 4MHz oscillation frequency, V_{CC} = 5.5V, Typ.)
	at CRT display OFF		55mW (at 4MHz oscillation frequency, V_{CC} = 5.5V, Typ.)
	at stop mode		1.65mW (Max.)
Operating temperature range			–10 to 70°C
Device structure			CMOS silicon gate process
Package	M37210M3-XXXSP, M37210M4-XXXSP, M37211M2-XXXSP		52-pin shrink plastic molded DIP
	M37210M3-XXXFP		64-pin plastic molded QFP
CRT display function	Number of character		18 characters X 2 lines : maximum 16 lines (by software)
	Character dot construction		12 X 16 dots
	Kinds of characters		96 kinds
	Character size		3 kinds
	Kinds of color		7 kinds max, (R, G, B) : can be specified by character unit
	Display position (horizontal, vertical)		64 levels (horizontal) X 128 levels (vertical)

Note : The M37211M2-XXXSP can be also used as PWM4 and PWM5.

PIN DESCRIPTION

Pin	Name	Input / Output	Functions
V_{CC}, V_{SS}	Power source voltage		Apply voltage of 5V ± 10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2μs or more (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
φ	Timing output	Output	This is the timing output pin.
$P0_0$ – $P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output. The output structure is N-channel open-drain output. When PWM4, PWM5, PWM6 and PWM7 are used, $P0_0$, $P0_1$, $P0_2$ and $P0_3$ are in common with PWM output pins of PWM4, PWM5, PWM6 and PWM7.
$P1_1$ – $P1_4$	I/O port P1	I/O	Ports $P1_0$, $P1_1$, $P1_2$, $P1_3$ and $P1_4$ are 5-bit I/O ports and have basically the same functions as port P0. The output structure is CMOS output.
$P1_5$ – $P1_7$	Input port P1	Input	Ports $P1_5$, $P1_6$ and $P1_7$ are 3-bit input ports and they are in common with input pins of A-D comparator (A-D1, A-D2 and A-D3).
$P2_0$ – $P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
$P3_0$, $P3_1$	I/O port P3	I/O	Ports $P3_0$ and $P3_1$ are 2-bit I/O ports and have basically the same functions as port P0. The output structure is CMOS output.
$P3_2$ – $P3_5$	Input port P3	Input	Ports $P3_2$, $P3_3$, $P3_4$ and $P3_5$ are 4-bit input ports and ports $P3_2$ and $P3_3$ are in common with external clock input pins of timers 2 and 3. Ports $P3_4$ and $P3_5$ are in common with external interrupt input pins INT1 and INT2. Port $P3_5$ is in common with an input pin of A-D comparator (A-D4).
$P4_0$, $P4_1$	I/O port P4	I/O	Ports $P4_0$ and $P4_1$ are 2-bit I/O ports and have basically the same functions as port P0. When serial I/O is used, ports $P4_0$ and $P4_1$ are in common with S_{OUT} pin and S_{CLK} pin, respectively.
$P4_2$	Input port P4	Input	Port $P4_2$ is an 1-bit Input port, and it is common with an input pin of A-D comparator (A-D5) and serial input pin (S_{IN}).
$P6_0$ – $P6_3$	Output port P6	Output	Port P6 is an 4-bit output port. The output structure is N-channel open-drain. This port is in common with 6-bit PWM output pins PWM0-PWM3.
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function.
H_{SYNC}	H_{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V_{SYNC}	V_{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display.
R, G, B, OUT	CRT output	Output	This is a 4-bit output pin for CRT display. The output structure is CMOS output. This is in common with port $P5_2$ – $P5_5$.
D-A	DA Output	Output	This is an output pin for 14-bit PWM.

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37210M3-XXXSP/FP uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 〈Software〉 User's Manual for details on the instruction set.

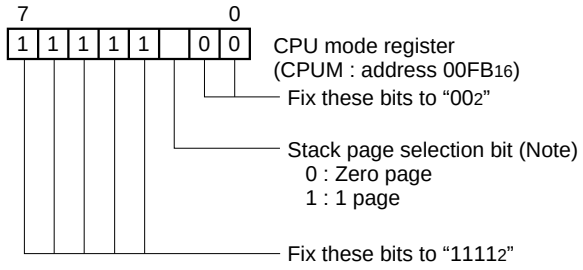
Machine-resident 740 family instructions are as follows :

The FST and SLW instruction cannot be used.

The MUL, DIV, WIT, and STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address $00FB_{16}$. The CPU mode register contains the stack page selection bit.



Note : Please beware of this bit when programming because it is set to "1" after the reset release.
Especially the internal RAM of the M37211M2-XXXSP is in the zero page, so be sure to set this bit to "0".

Fig. 1 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

ROM is used for sroring user programs as well as the interrupt vector area.

RAM for Display

RAM for display is used for specifing the character codes and colors to display.

ROM for Display

ROM for display is used for storing character data.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

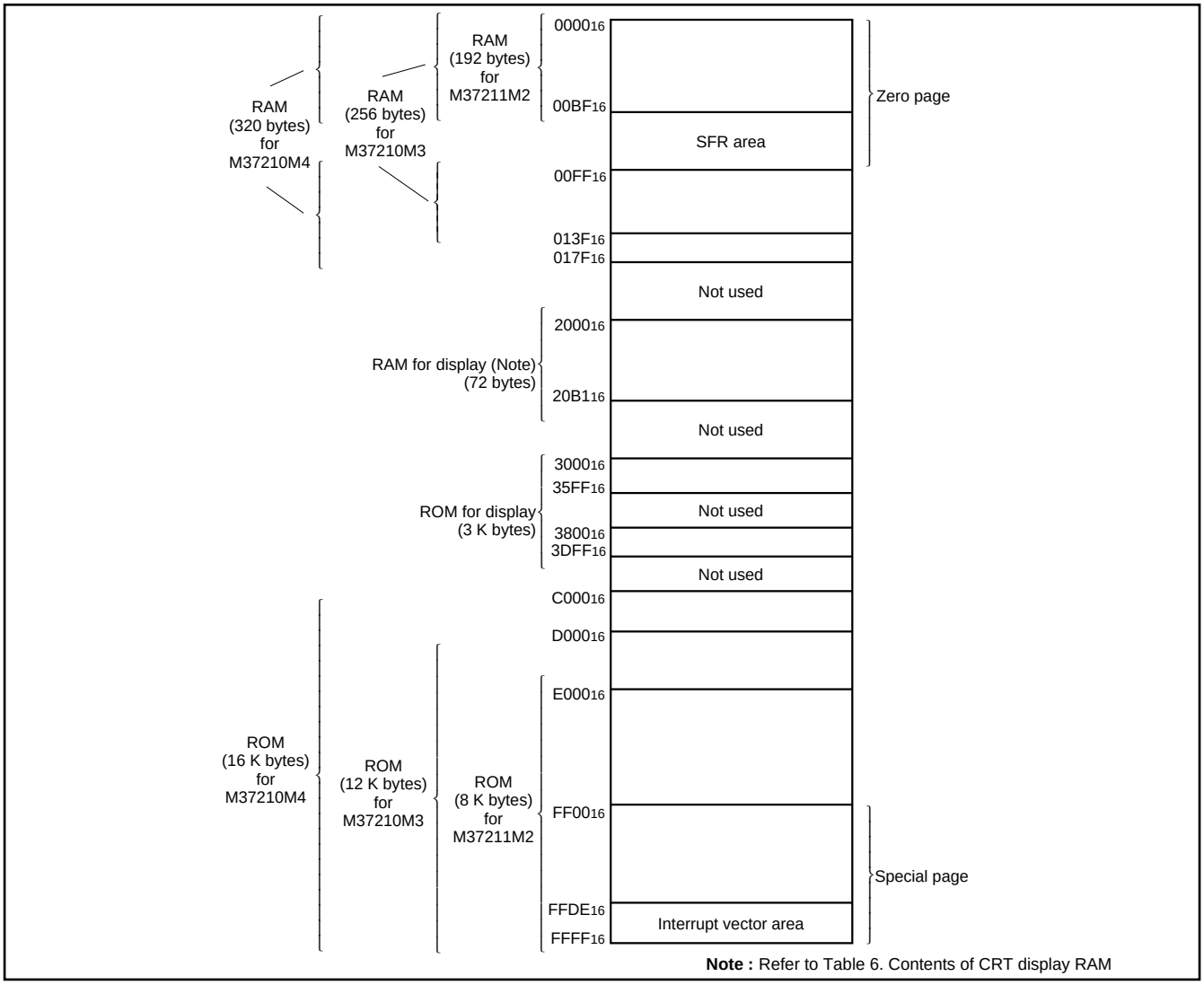


Fig. 2 Memory map

00C0$_{16}$	Port P0
00C1$_{16}$	Port P0 directional register
00C2$_{16}$	Port P1
00C3$_{16}$	Port P1 directional register
00C4$_{16}$	Port P2
00C5$_{16}$	Port P2 directional register
00C6$_{16}$	Port P3
00C7$_{16}$	Port P3 directional register
00C8$_{16}$	Port P4
00C9$_{16}$	Port P4 directional register
00CA$_{16}$	Port P5
00CB$_{16}$	Port P5 control register
00CC$_{16}$	Port P6
00CD$_{16}$	Port P6 directional register
00CE$_{16}$	14DA-H register
00CF$_{16}$	14DA-L register
00D0$_{16}$	PWM0 register
00D1$_{16}$	PWM1 register
00D2$_{16}$	PWM2 register
00D3$_{16}$	PWM3 register
00D4$_{16}$	PWM4 register
00D5$_{16}$	PWM output control register 1
00D6$_{16}$	PWM output control register 2
00D7$_{16}$	Interrupt Interval determination register
00D8$_{16}$	Interrupt Interval determination control register
00D9$_{16}$	
00DA$_{16}$	
00DB$_{16}$	
00DC$_{16}$	Serial I/O mode register
00DD$_{16}$	Serial I/O register
00DE$_{16}$	
00DF$_{16}$	

00E0$_{16}$	Horizontal position register
00E1$_{16}$	Vertical position register 1 (block 1)
00E2$_{16}$	Vertical position register 2 (block 2)
00E3$_{16}$	
00E4$_{16}$	Character size register
00E5$_{16}$	Border selection register
00E6$_{16}$	Color register 0
00E7$_{16}$	Color register 1
00E8$_{16}$	Color register 2
00E9$_{16}$	Color register 3
00EA$_{16}$	CRT control register
00EB$_{16}$	
00EC$_{16}$	CRT port control register
00ED$_{16}$	
00EE$_{16}$	A-D mode register
00EF$_{16}$	A-D control register
00F0$_{16}$	Timer 1
00F1$_{16}$	Timer 2
00F2$_{16}$	Timer 3
00F3$_{16}$	Timer 4
00F4$_{16}$	Timer 12 mode register
00F5$_{16}$	Timer 34 mode register
00F6$_{16}$	PWM5 register
00F7$_{16}$	PWM6 register (Note)
00F8$_{16}$	PWM7 register (Note)
00F9$_{16}$	
00FA$_{16}$	
00FB$_{16}$	CPU mode register
00FC$_{16}$	Interrupt request register 1
00FD$_{16}$	Interrupt request register 2
00FE$_{16}$	Interrupt control register1
00FF$_{16}$	Interrupt control register2

Note : The M37211M2-XXXSP dose not have this register

Fig. 3 Memory map of special function register (SFR)

INTERRUPTS

Interrupts can be caused by 12 different sources consisting of 3 external, 7 internal, 1 software, and reset.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is “1”, interrupt request bit is “1”, and the interrupt disable flag is “0”. The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector addresses and priority

Interrupt sources	Priority	Vector addresses	Remarks
Reset	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT_2 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
INT_1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	Active edge selectable
Timer 4 interrupt	5	$FFF5_{16}$, $FFF4_{16}$	
f(X_{IN})/4096 interrupt	6	$FFF3_{16}$, $FFF2_{16}$	
V_{SYNC} interrupt	7	$FFF1_{16}$, $FFF0_{16}$	Active edge selectable
Timer 3 interrupt	8	$FFEF_{16}$, $FFEE_{16}$	
Timer 2 interrupt	9	$FFED_{16}$, $FFEC_{16}$	
Timer 1 interrupt	10	$FFEB_{16}$, $FFEA_{16}$	
Serial I/O interrupt	11	$FFE9_{16}$, $FFE8_{16}$	
BRK instruction interrupt	12	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

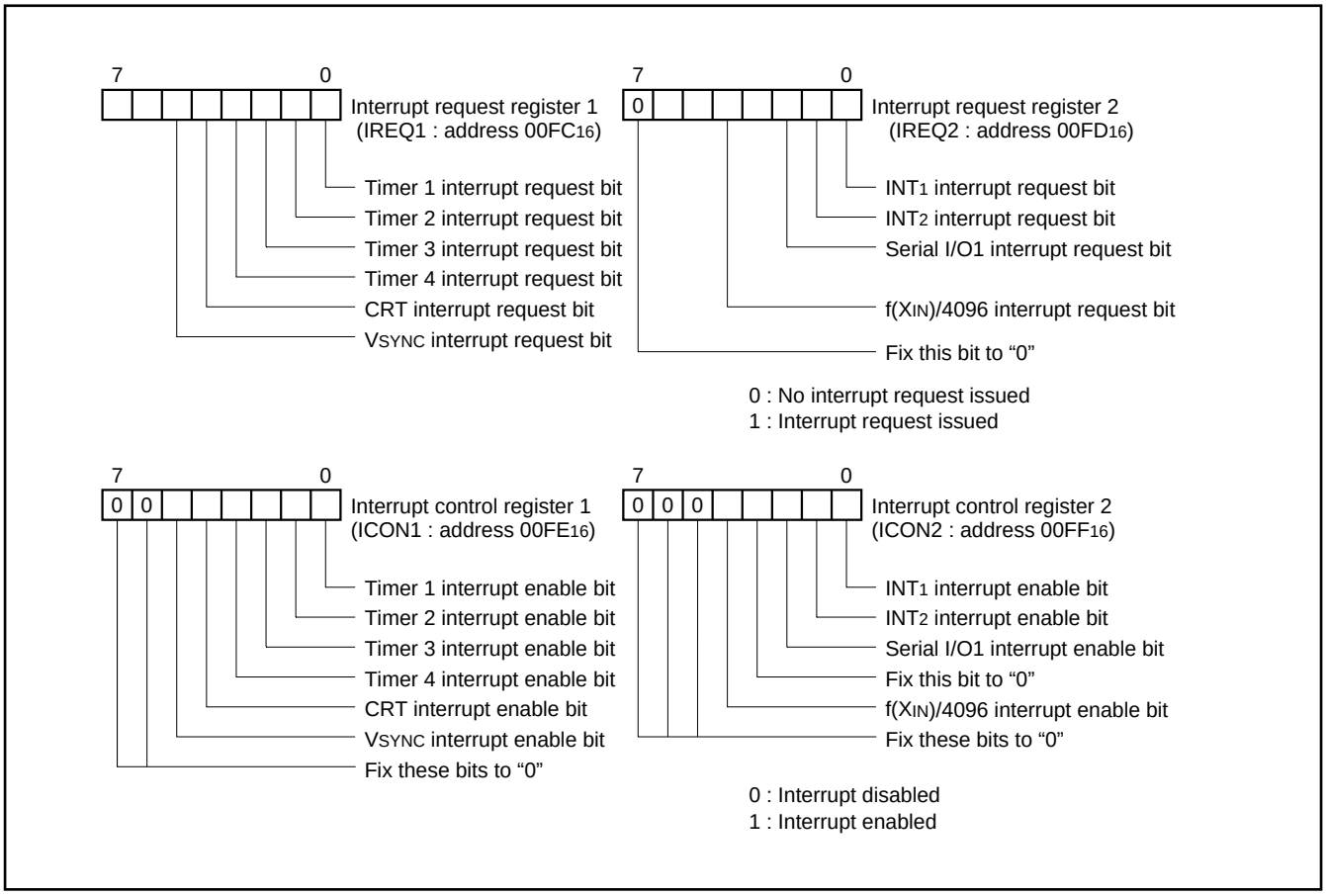


Fig. 4 Structure of interrupt-related registers

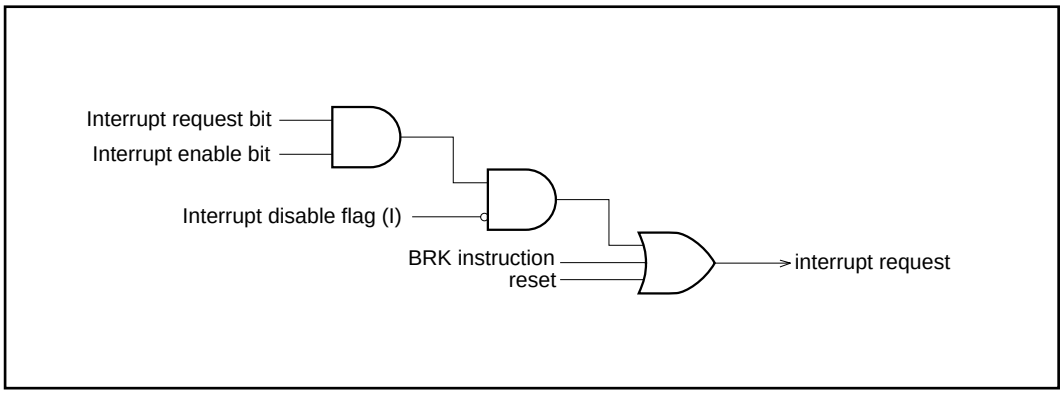


Fig. 5 Interrupt control

TIMERS

The M37210M3-XXXSP has 4 timers: timer 1, timer 2, timer 3 and timer 4. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 7.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. The value is set to a timer at the same time by writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$: timers 1 to 4).

The count value is decremented by 1. The timer interrupt request bit is set to "1" by an timer overflow at the next count pulse after the count value reaches "00_{16}."

(1) Timer 1

Timer 1 can select one of the following count sources:

- f(X_{IN})/16
- f(X_{IN})/4096

The count source of timer 1 is selected by setting bit 0 of the timer 12 mode register (address $00F4_{16}$).

Timer 1 interrupt request occurs at timer 1 overflow.

(2) Timer 2

Timer 2 can select one of the following count sources:

- f(X_{IN})/16
- Timer 1 overflow signal
- External clock from the $P3_2$/TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of the timer 12 mode register (address $00F4_{16}$). When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- f(X_{IN})/16
- External clock from the $P3_3$/TIM3 pin and the H_{SYNC} pin

The count source of timer 3 is selected by setting bits 5 and 0 of the timer 34 mode register (address $00F5_{16}$).

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- f(X_{IN})/16
- f(X_{IN})/2
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 4 and 1 of the timer 34 mode register 2 (address $00F5_{16}$). When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. The f(X_{IN})/16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow at these state, the internal clock is connected .

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. However, the f(X_{IN})16 is not selected as the timer 3 count source. So set bit 0 of the timer 34 mode register (address $00F5_{16}$) to "0" before the execution of the STP instruction (f(X_{IN})16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow at these state, the internal clock is connected .

Because of this, the program starts with stable clock.

The structure of timer-related registers is shown in Figure 6.

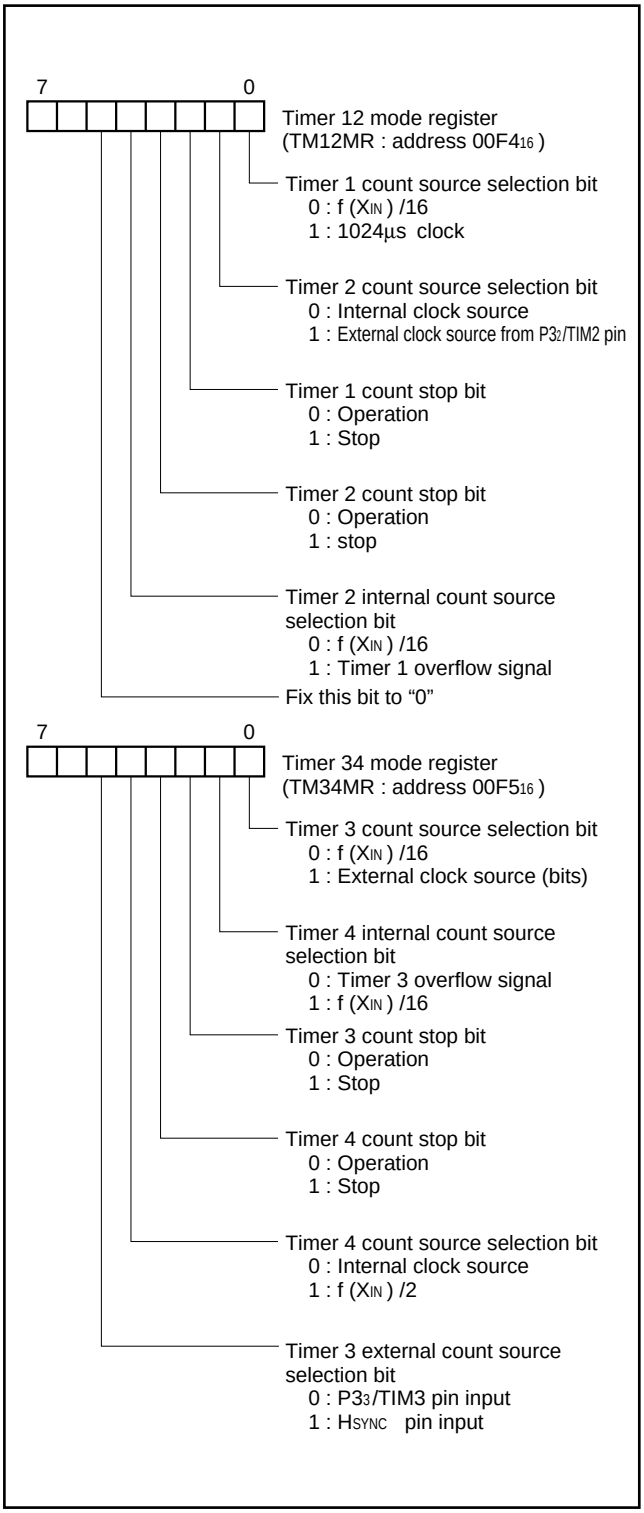
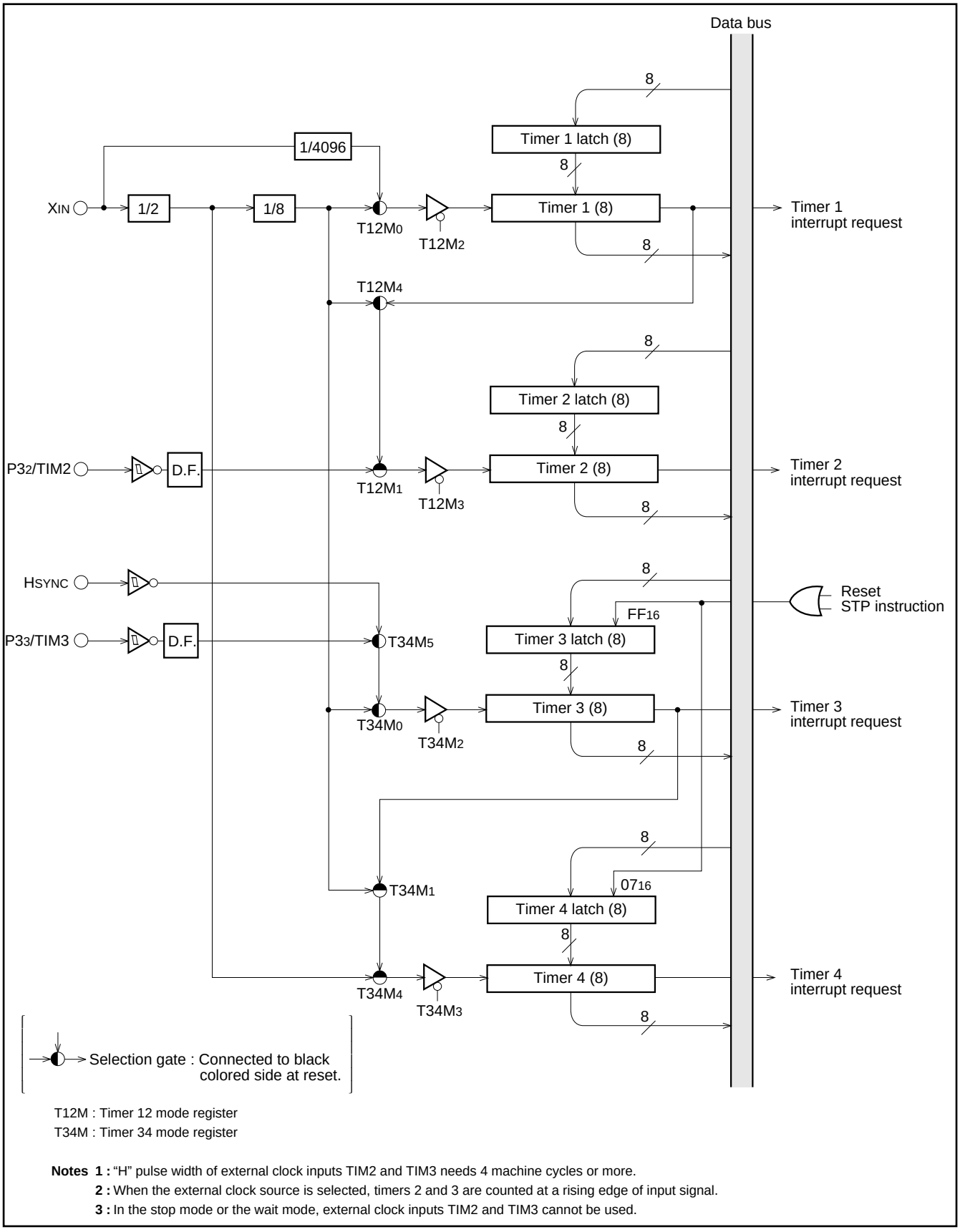


Fig. 6 Structure of timer-related registers



Notes 1 : "H" pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2 : When the external clock source is selected, timers 2 and 3 are counted at a rising edge of input signal.
3 : In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 7 Timer block diagram

SERIAL I/O

M37210M3-XXXSP has a serial I/O.

A block diagram of the serial I/O is shown in Figure 8.

Synchronous input/output clock (SCLK), and the serial I/O pins (SOUT, SIN) are used as port P4. The serial I/O mode registers (address 00DC16) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bit 3 decides whether parts of P4 will be used as a serial I/O or not. To use P42 as a serial input, set the directional register bit which corresponds to P42 to "0". For more information on the directional register, refer to the I/O pin section.

The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source ; external clock or internal clock.

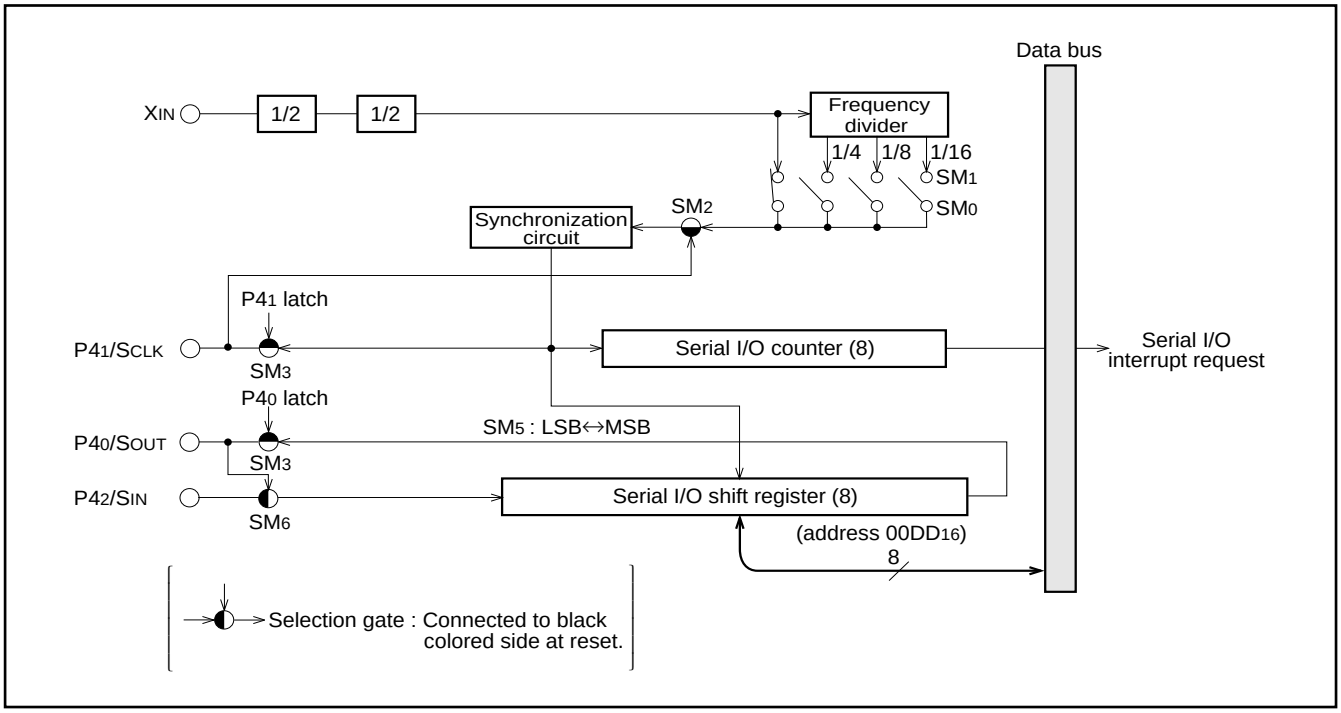


Fig. 8 Serial I/O block diagram

The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to SOUT. During the rising edge of this clock, data can be input from SIN and the data in the serial I/O register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O mode register.

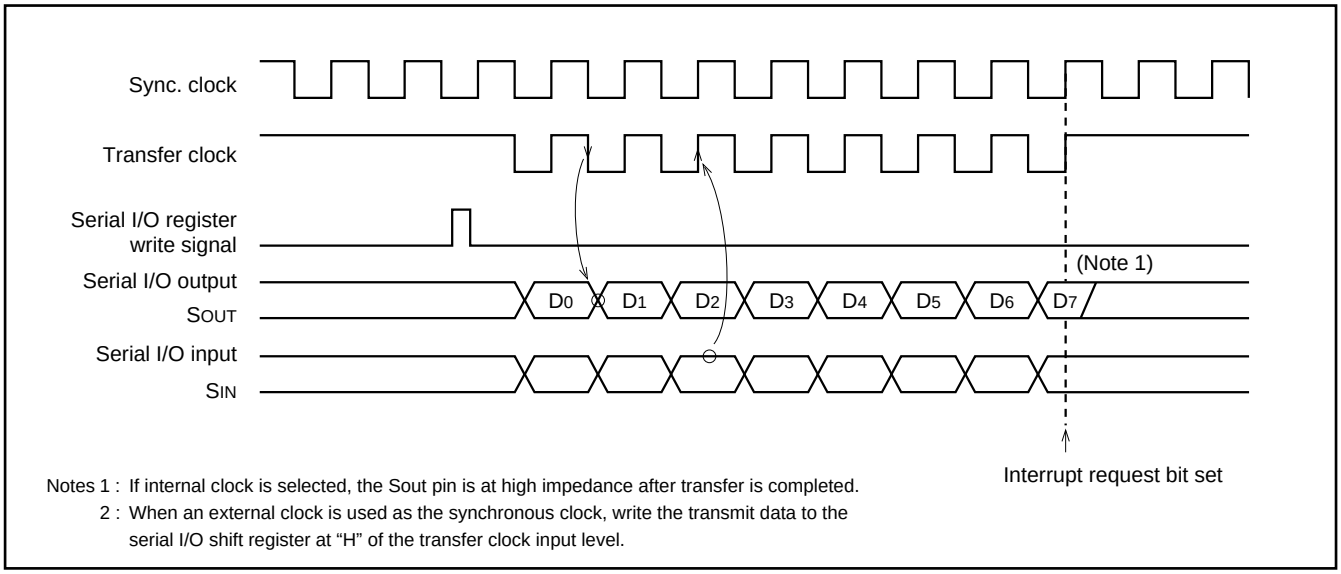
After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 1MHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions as SEB and CLB instructions.

2: When an external clock is used as the synchronizing clock, write transmit data to the serial I/O register at "H" of the transfer clock input level.



Notes 1 : If internal clock is selected, the Sout pin is at high impedance after transfer is completed.
2 : When an external clock is used as the synchronous clock, write the transmit data to the serial I/O shift register at "H" of the transfer clock input level.

Fig. 9 Serial I/O timing (for LSB first)

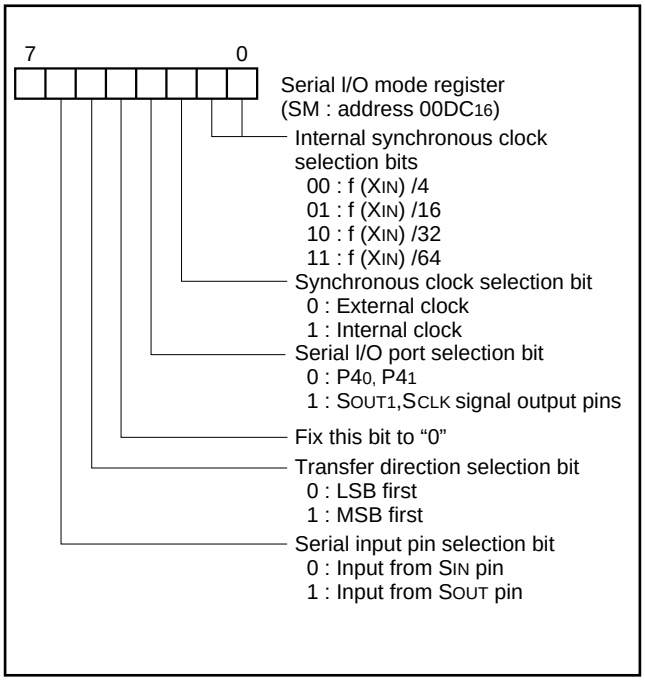


Fig. 10 Structure of serial I/O mode register

Serial I/O common transmission/reception mode.

Write 1 to bit 6 of serial I/O mode register, and signals SIN and SOUT switch internal to be able to serial data transmission/reception.

Figure 11 shows signals on serial I/O common transmission/reception mode.

Note : Receive the serial data after writing "FF16" to the serial I/O register.

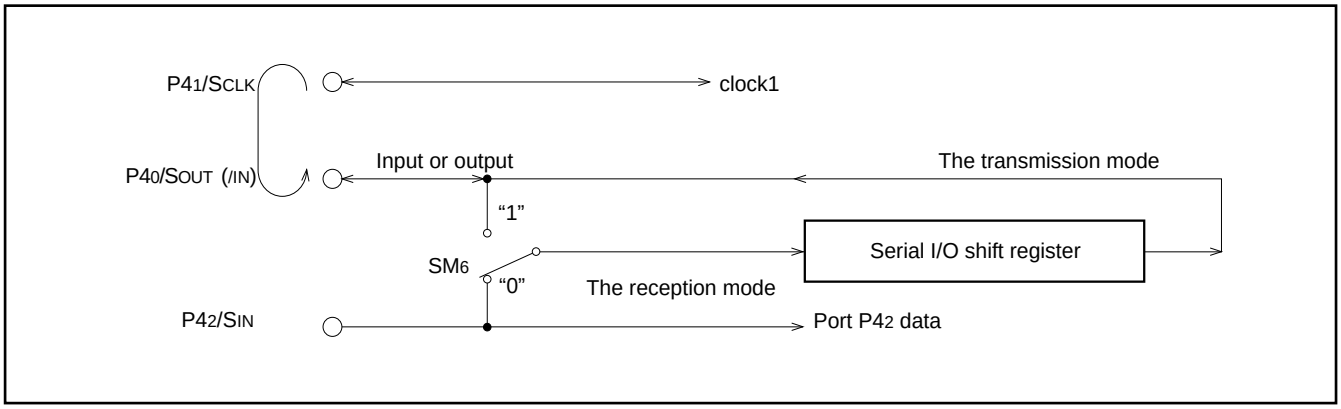


Fig. 11 Signals on serial I/O common transmission/reception mode

PWM OUTPUT CIRCUIT

(1) Introduction

The M37210M3-XXXSP/FP and M37210M4-XXXSP are equipped with one 14-bit PWM (DA) and eight 6-bit PWMs (PWM0-PWM7), and the M37211M2-XXXSP is equipped with six 6-bit PWMs (PWM0-PWM5). The 14-bit resolution gives DA the minimum resolution bit width of 500ns (for f(X_{IN}) = 4MHz) and a repeat period of 8192µs. PWM0-PWM7 have a 6-bit resolution with minimum resolution bit width of 16μs and repeat period of 1024µs.

Block diagram of the PWM is shown in Figure 16.

The PWM timing generator section applies individual control signals to DA and PWM0-7 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data Setting

The output pins PWM0-3 are in common with port P6 and PWM4-7 are in common with port $P0_0$-$P0_3$.

For PWM output, each PWM output selection bit (bit 1 to 7 of PWM output control register 1, bit 0, 1 of PWM output control register 2, should be set. When DA is used for output, first set the higher 8-bit of the DA-H register (address $00CE_{16}$), then the lower 6-bit of the DA-L register (address $00CF_{16}$).

When one of the PWM0-7 is used for output, set the 6-bit in the PWM0-7 register (address $00D0_{16}$ to $00D4_{16}$, $00F6_{16}$ to $00F8_{16}$), respectively.

(3) Transferring Data from Registers to PWM Circuit

The data written to the PWM registers. 8 bits of the DA-H register is transferred to 14-bit PWM circuit when writing to lower 6 bits of the DA-L register.

(4) Operation of the 6-bit PWMs

The timing diagram of the eight 6-bit PWMs (PWM0-7) is shown in Figure 13. One period (T) is composed of 64 (2^6) segments. There are six different pulse types configured from bits 0 to 5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 13 (a).

Six different pulses can be output from the PWM.

These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5 to 0 are selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 13 (b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. A length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM Operation

The output example of the 14-bit PWM is shown in Figure 14. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length D_H times τ is output every short area of t = 256 τ =128µs as determined by data D_H of the higher 8 bits.

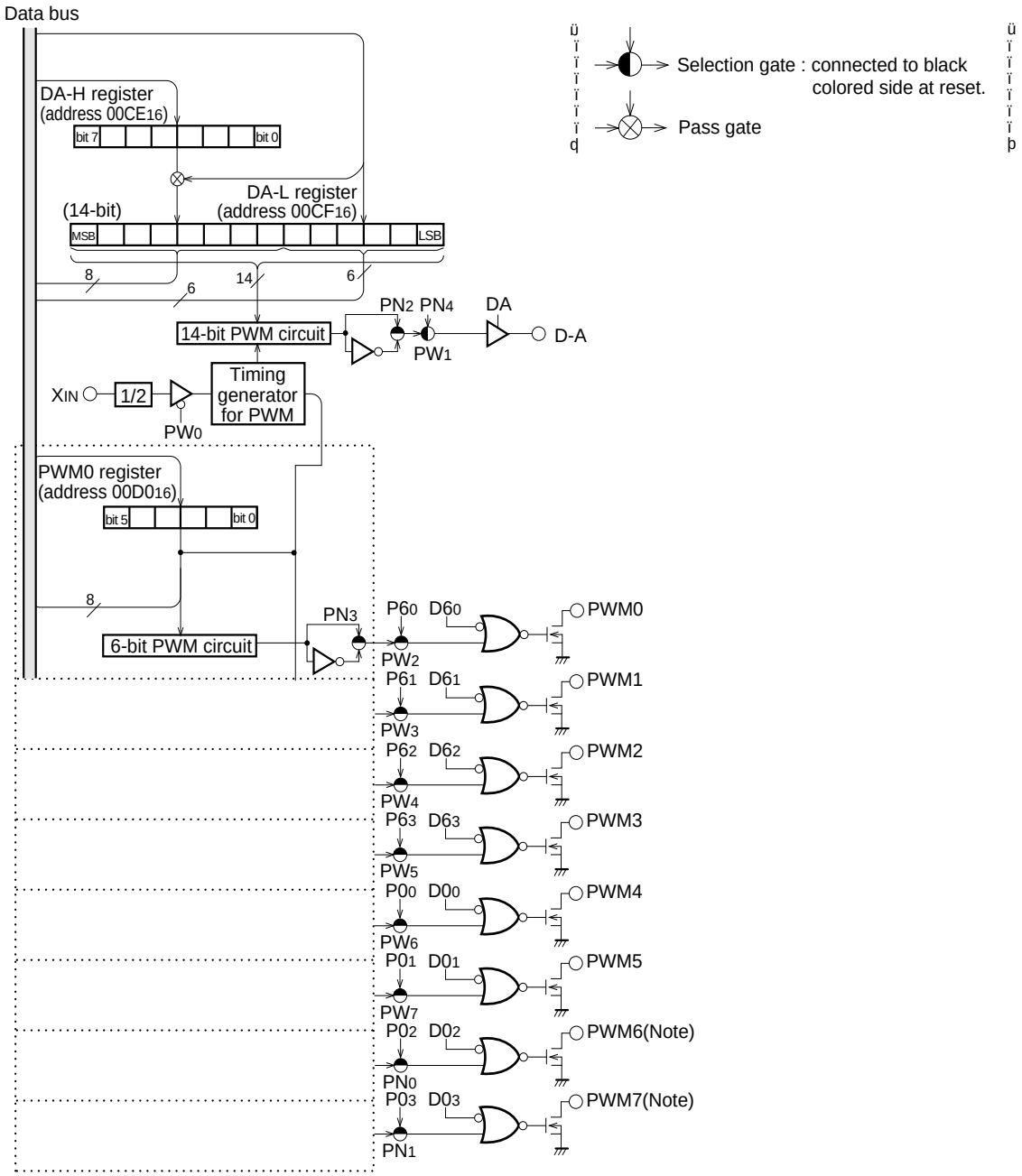
Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ. As a result, the short-area period t (= 128µs, approx. 7.8 kHz) becomes an approximately repetitive period.

(6) Output after Reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the low-order 6 bits of data and high-level area increase space

6 low-order bits of data	Area longer by τ than that of other t_m (m = 0 to 63)
0 0 0 0 0 0 (LSB)	Nothing
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ... 57, 59, 61, 63



Note : The M37211M2-XXXSP can not output the PWM.

Inside of ⋮⋮⋮ is as same contents with the others.

PW : PWM output control register 1
PN : PWM output control register 2
D0 : Port P0 direction register
P0 : Port P0
D6 : Port P6 directional register
P6 : Port P6

Fig. 12 PWM block diagram

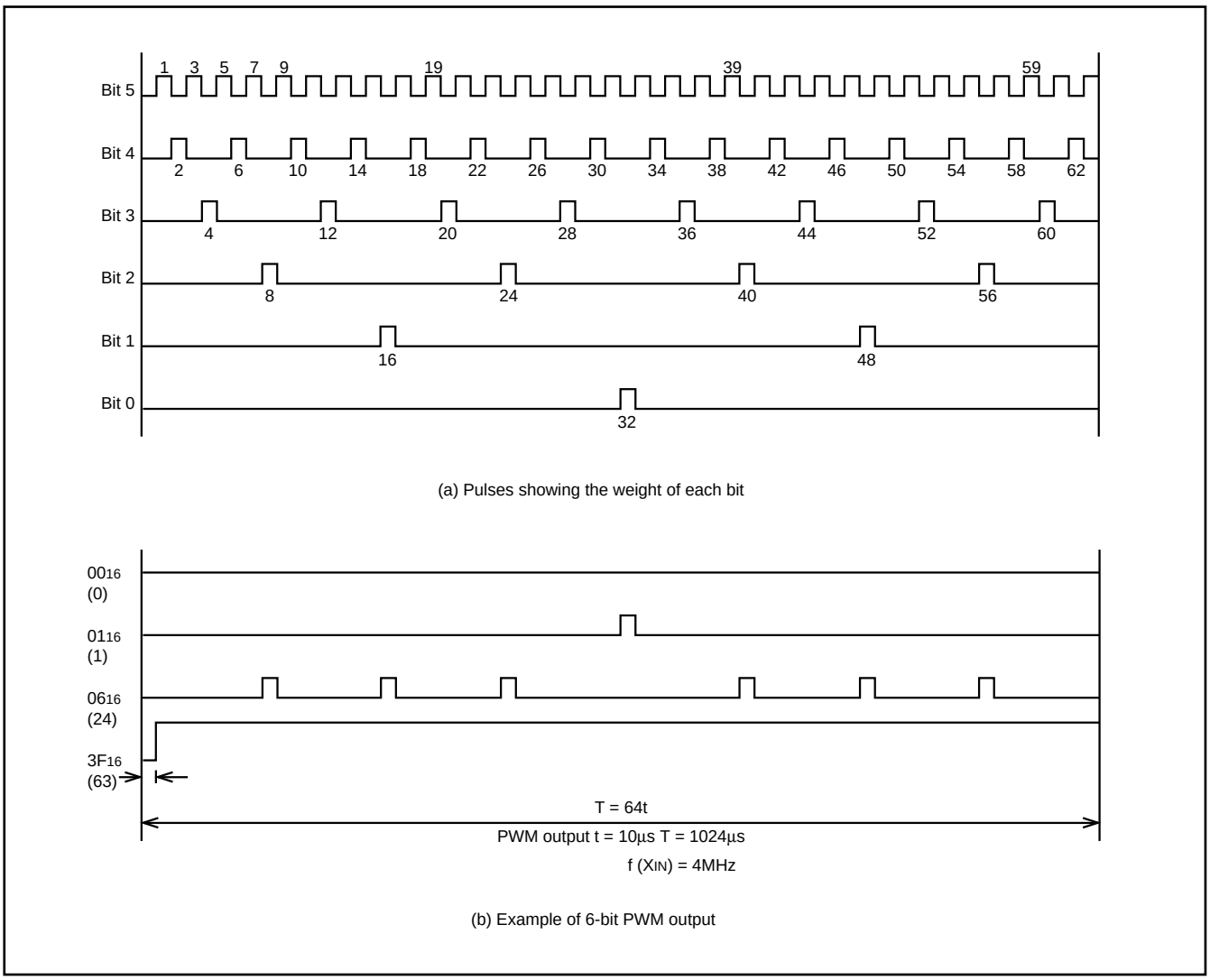


Fig. 13 6-bit PWM timing

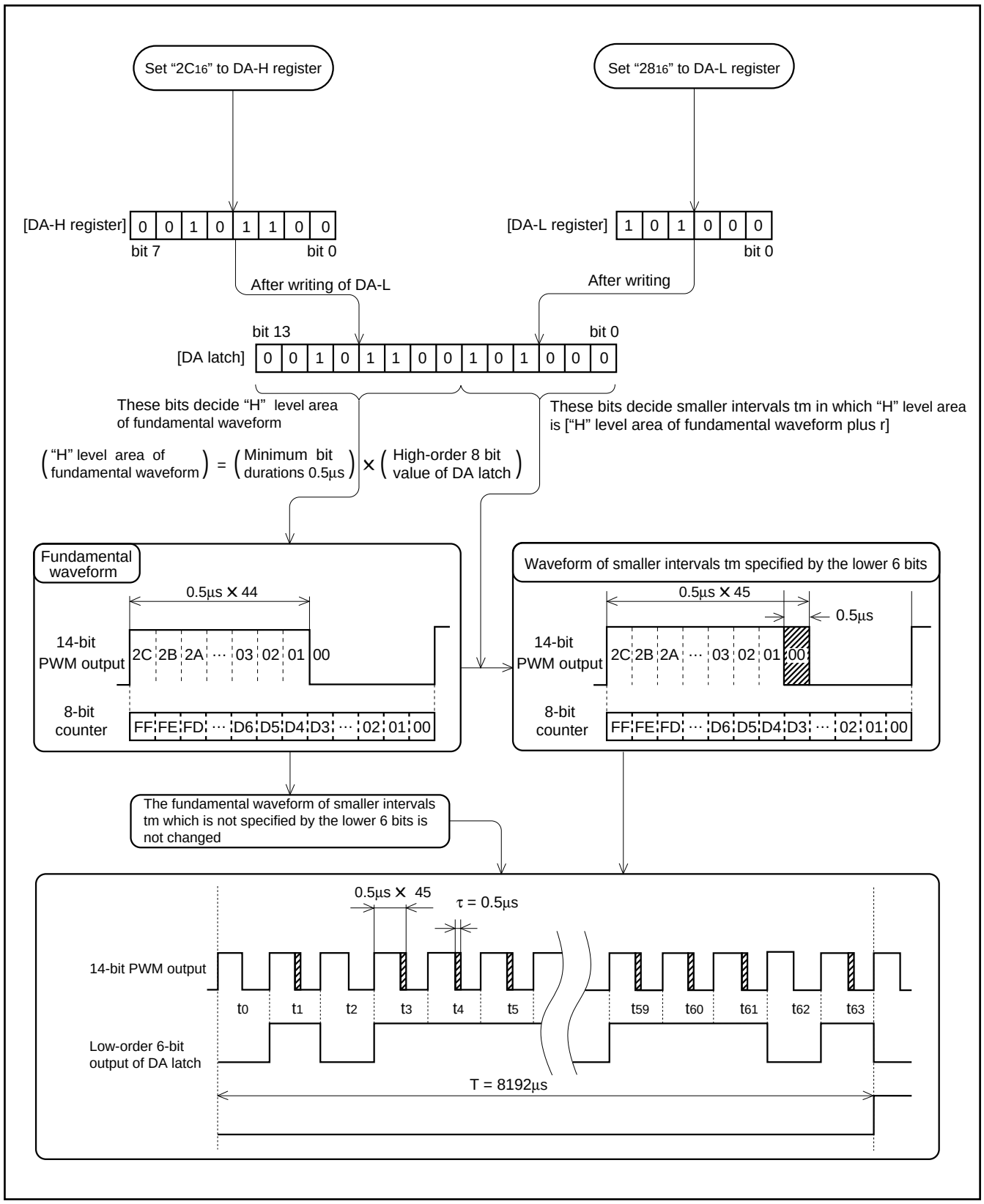


Fig. 14 14-bit PWM output example (f (XIN) = 4MHz)

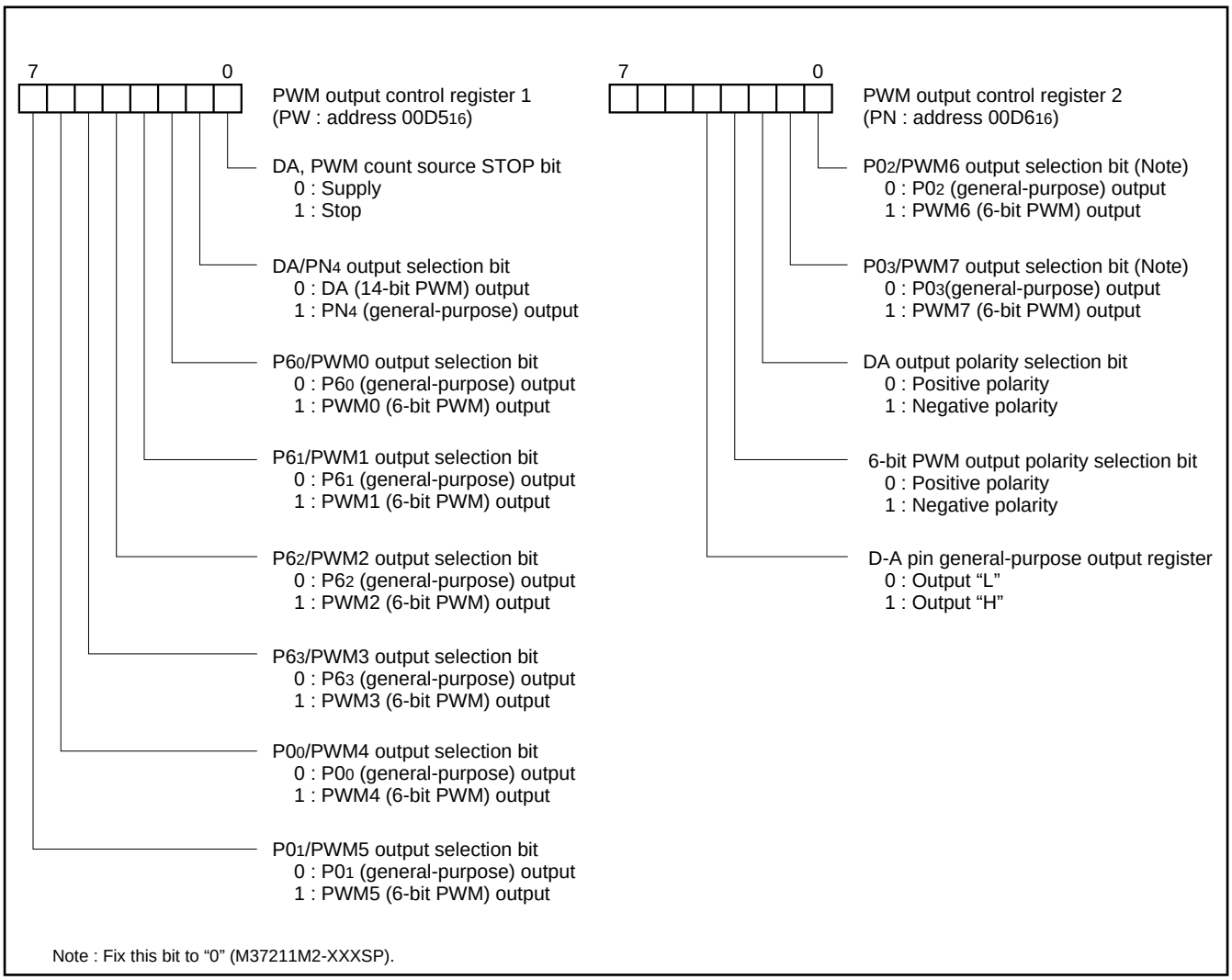


Fig.15 Structure of PWM output control registers 1 and 2

A-D COMPARATOR

Block diagram of A-D comparator is shown in Figure 18. A-D comparator consists of 5-bit D-A converter and comparator. The A-D control register can generate 1/64 Vcc-step internal analog voltage based on the settings of bits 0 to 4.

Table 3 gives the relation between the descriptions of A-D control register bits 0 to 4 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 5.

After selection of an analog input pin by bits 0-2 of A-D mode register (address 00EE16), the digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 16 machine cycle, the voltage comparison is completed.

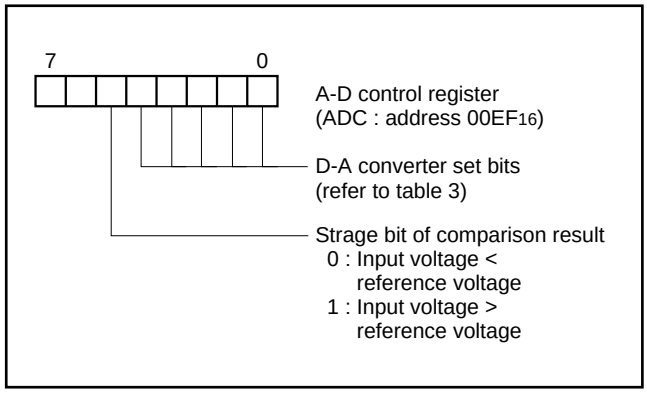


Fig. 16 Structure of A-D control register

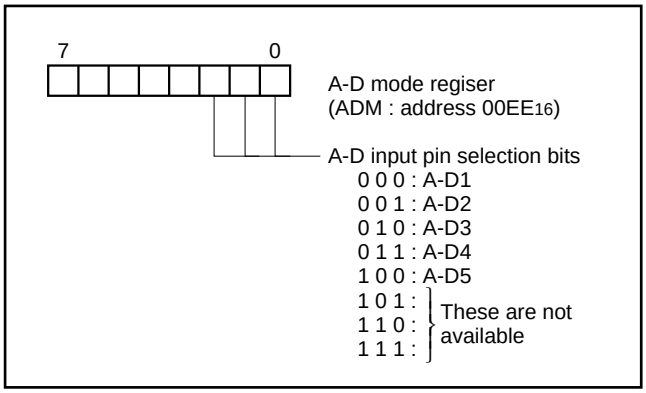


Fig. 17 Structure of A-D mode register

Table 3. Relationship between the contents of A-D control register and reference voltage

A-D control register					Reference voltage Vref
Bit4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	1/64 Vcc
0	0	0	0	1	3/64 Vcc
0	0	0	1	0	5/64 Vcc
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	0	1	27/64 Vcc
1	1	1	1	0	29/64 Vcc
1	1	1	1	1	31/64 Vcc

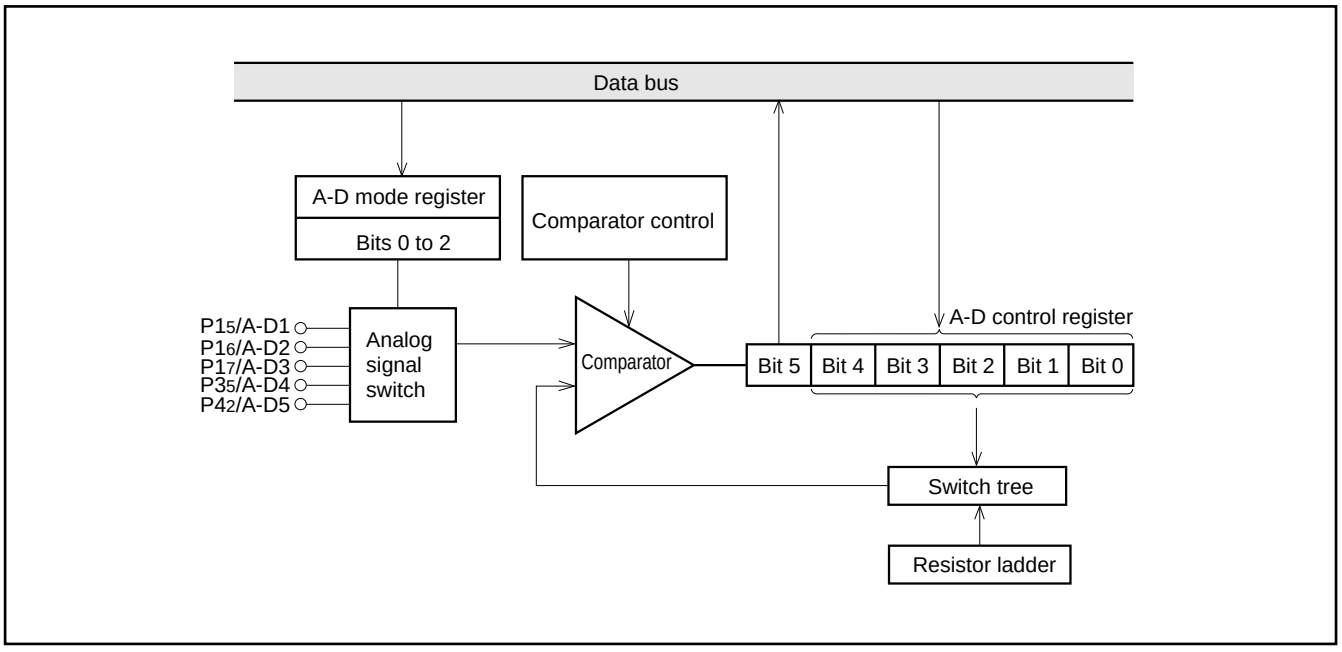


Fig. 18 A-D comparator block diagram

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37210M3-XXXSP. The M37210M3-XXXSP incorporates a 18 columns × 2 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 96 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 7 colors can be obtained by using each output signal (R, G and B).

Characters are displayed in a 12 × 16 dot configuration to obtain smooth character patterns (refer to Figure 19).

The following shows the procedure how to display characters on the CRT screen.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display character		18 characters × 2 lines
Character configuration		12 × 16 dots (refer to Figure 19)
Kinds of character		96
Character size		3 kinds
Color	Kinds of color	1 screen : 4 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 7 kinds)

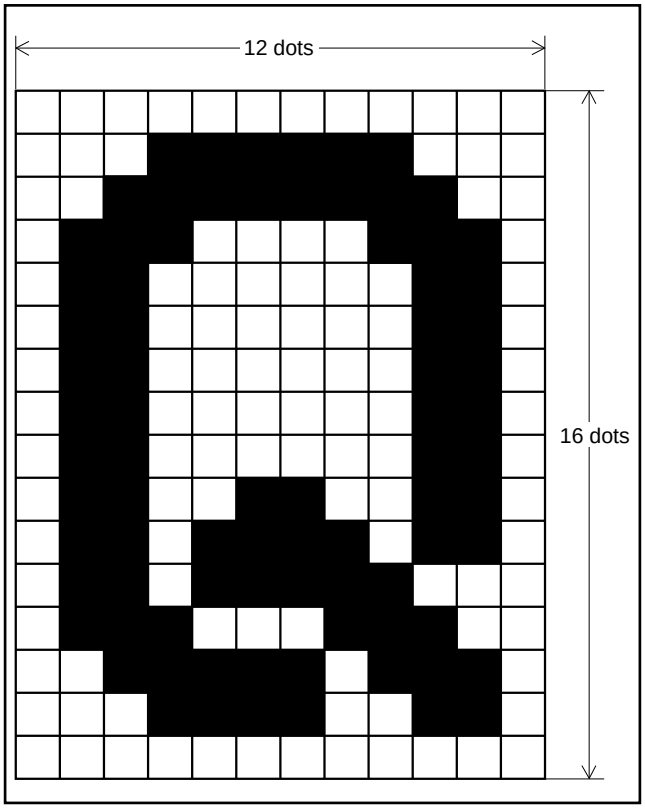


Fig. 19 CRT display character configuration

① Set the character to be displayed in display RAM.
② Set the display color by using the color register.
③ Specify the color register in which the display color is set by using the display RAM.
④ Specify the vertical position and character size by using the vertical position register and the character size register.
⑤ Specify the horizontal position by using the horizontal position register.
⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode.

This mode allows multiple lines (more than 3 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 21 shows a block diagram of the CRT display control circuit. Figure 20 shows the structure of the CRT display control register.

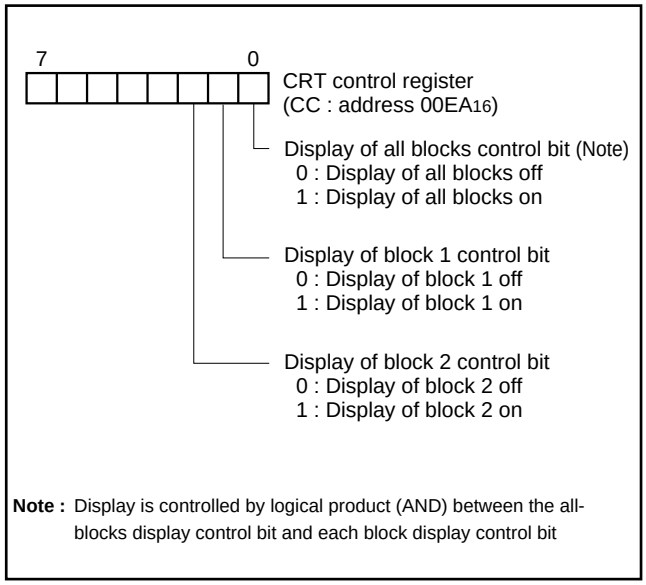


Fig. 20 Structure of CRT control register

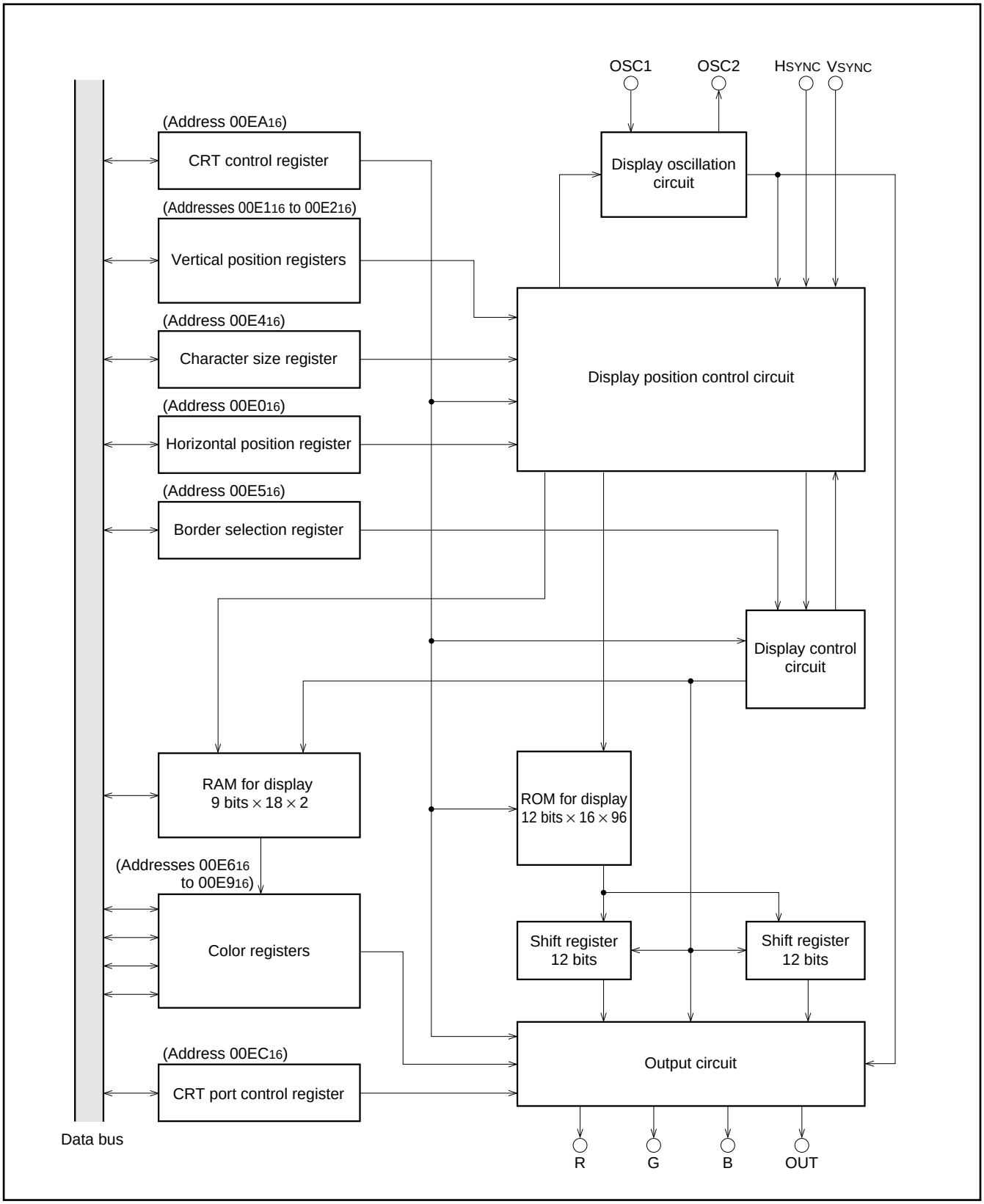


Fig. 21 Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block". There are two blocks, block 1 and block 2.
Up to 18 characters can be displayed in one block (refer to (4) Memory for Display).
The display position of each block in both horizontal and vertical directions can be set by software.
The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of 4Tc (Tc = oscillating cycle for display).
The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.
Block 2 is displayed after the display of block 1 perfectly (fig. 24(a)). Then if the display of block 2 starts during the display of block 1, only block 1 is displayed. As same, when multiline display, block 1 is displayed after the display of block 2 perfectly (fig. 24(b)).
The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ and $00E2_{15}$). Figure 22 shows the structure of the vertical position register.

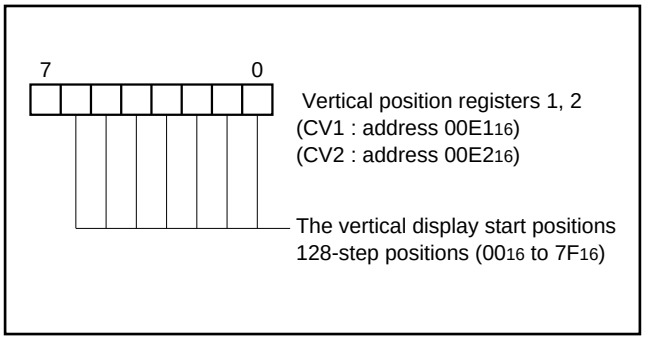


Fig. 22 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions (4Tc per step (Tc = oscillating cycle for display) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 23 shows the structure of the horizontal position register.

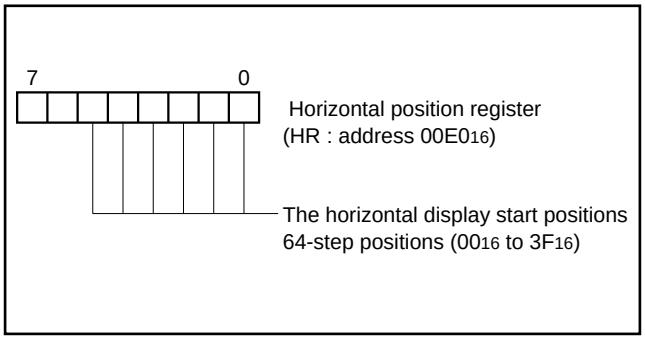
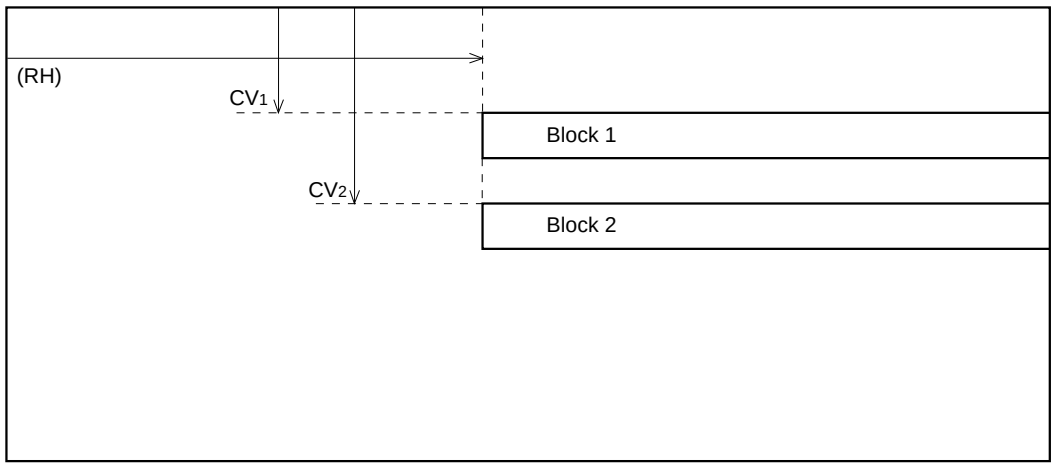
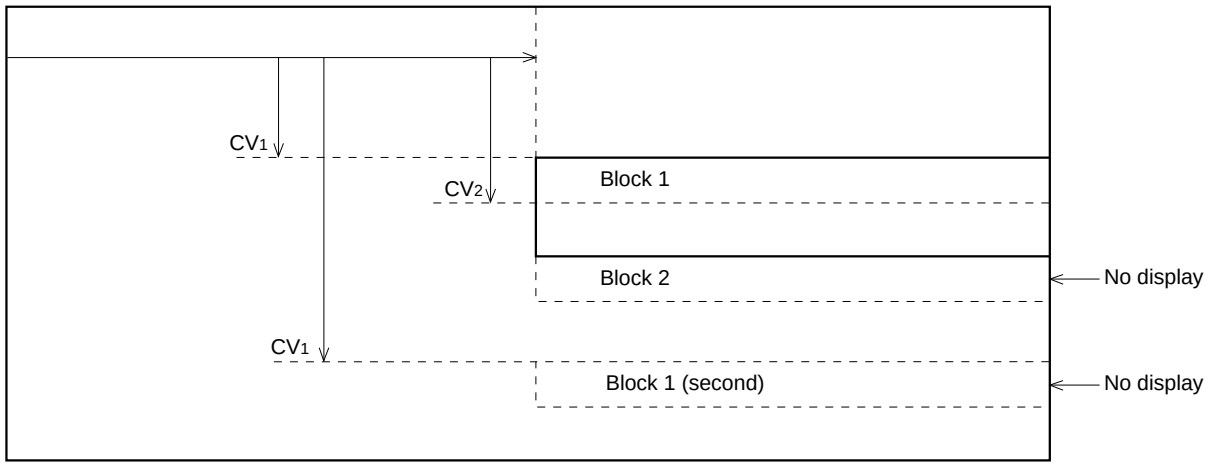


Fig. 23 Structure of horizontal position register



(a) Example when each block is separated



(b) Example when block 2 overlaps with block 1

Fig. 24 Display position

(3) Character Size

The size of characters to be displayed can be selected from three sizes for each block. Use the character size register (address $00E4_{16}$) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register ; the character size in block 2 can be specified by using bits 2 and 3. Figure 25 shows the structure of the character size register.

The character size can be selected from three sizes : small size, medium size and large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (= Tc) in the width (horizontal) direction.

The small size consists of [one scanning line] × [1 Tc] ; the medium size consists of [two scanning lines] × [2 Tc] ; and the large size consists of [three scanning lines] × [3 Tc].

Table 5 shows the relationship between the set values in the character size register and the character sizes.

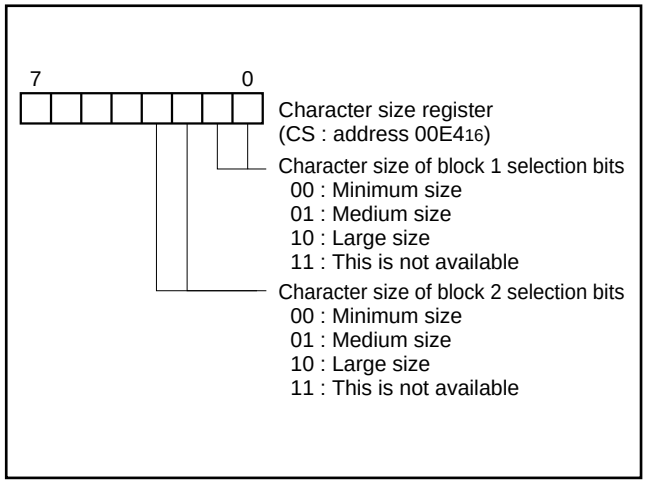


Fig. 25 Structure of character size register

Table 5. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction Tc : oscillating cycle for display	Height (vertical) direction scanning lines
CSn_1	CSn_0			
0	0	Minimum	1 Tc	1
0	1	Medium	2 Tc	2
1	0	Large	3 Tc	3
1	1	This is not available		

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 26).

(4) Memory for Display

There are two types of memory for display : ROM of CRT display (addresses 3000_{16} to $35FF_{16}$, 3800_{16} to $3DFF_{16}$) used to store character dot data (masked) and display RAM (addresses 2000_{16} to $20B1_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① **ROM for display (addresses 3000_{16} to $35FF_{16}$ and 3800_{16} to $3DFF_{16}$)**

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

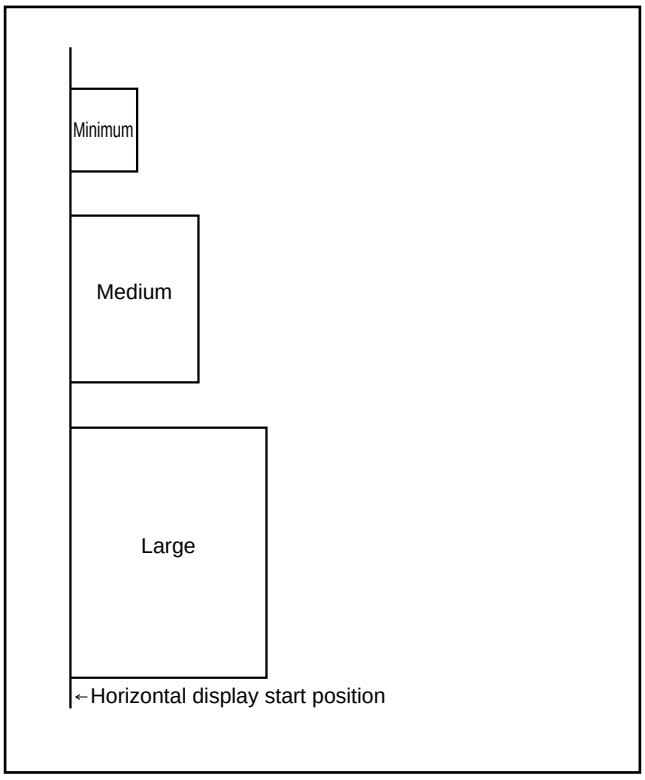


Fig. 26 Display start position of each character size (horizontal direction)

The CRT display ROM has a capacity of 3K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 96 kinds of characters.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000_{16} to $35FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3DFF_{16}$ (refer to Figure 27). Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3DFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

Table 6. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16} : 10_{16}	3030_{16} to $303F_{16}$: 3100_{16} to $310F_{16}$	3830_{16} to $383F_{16}$: 3900_{16} to $390F_{16}$
11_{16} : $4F_{16}$	3110_{16} to $311F_{16}$: $34F0_{16}$ to $34FF_{16}$	3910_{16} to $391F_{16}$: $3CF0_{16}$ to $3CFF_{16}$
50_{16} : $5D_{16}$	3500_{16} to $350F_{16}$: $35D0_{16}$ to $35DF_{16}$	$3D00_{16}$ to $3D0F_{16}$: $3DD0_{16}$ to $3DDF_{16}$
$5E_{16}$	$35E0_{16}$ to $35EF_{16}$	$3DE0_{16}$ to $3DEF_{16}$
$5F_{16}$	$35E0_{16}$ to $35FF_{16}$	$3DF0_{16}$ to $3DFF_{16}$

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.
Assume that data for one character is stored at addresses $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $5F_{16}$) and addresses $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to DF_{16}), then the character code for it is “XX16”.

In other words, character code for any given character is configured with two middle digits of the four-digit (hexnotated) addresses 3000_{16} to $35FF_{16}$ where data for that character is stored.
Table 6 lists the character codes.

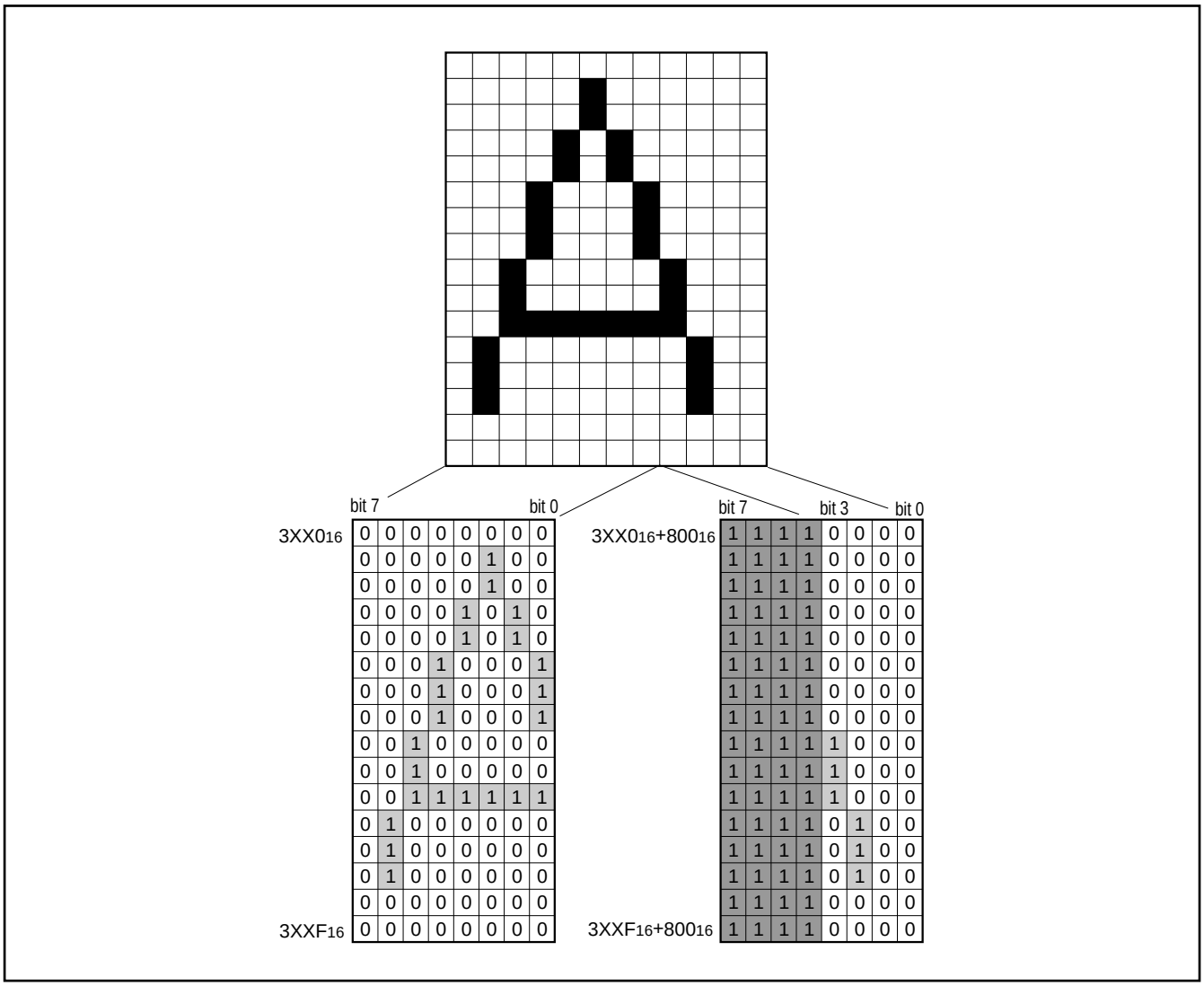


Fig. 27 Display character stored area

② RAM for display (address 2000_{16} to $20B1_{16}$)

The CRT display RAM is allocated at addresses 2000_{16} to $20B1_{16}$, and is divided into a display character code specifying part and display color specifying part for each block.

Table 7 shows the contents of the CRT display RAM.

When a character is to be displayed at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16}. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 27.

Table 7. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st character	2000_{16}	2080_{16}
	2nd character	2001_{16}	2081_{16}
	3rd character : 16th character	2002_{16} : $200F_{16}$	2082_{16} : $208F_{16}$
	17th character	2010_{16}	2090_{16}
	18th character	2011_{16}	2091_{16}
Not used		2012_{16} : $201F_{16}$	2092_{16} : $209F_{16}$
Block 2	1st character	2020_{16}	$20A0_{16}$
	2nd character	2021_{16}	$20A1_{16}$
	3rd character : 16th character	2022_{16} : $202F_{16}$	$20A2_{16}$: $20AF_{16}$
	17th character	2030_{16}	$20B0_{16}$
	18th character	2031_{16}	$20B1_{16}$
Not used		2032_{16} : $203F_{16}$	$20B2_{16}$: $20BF_{16}$

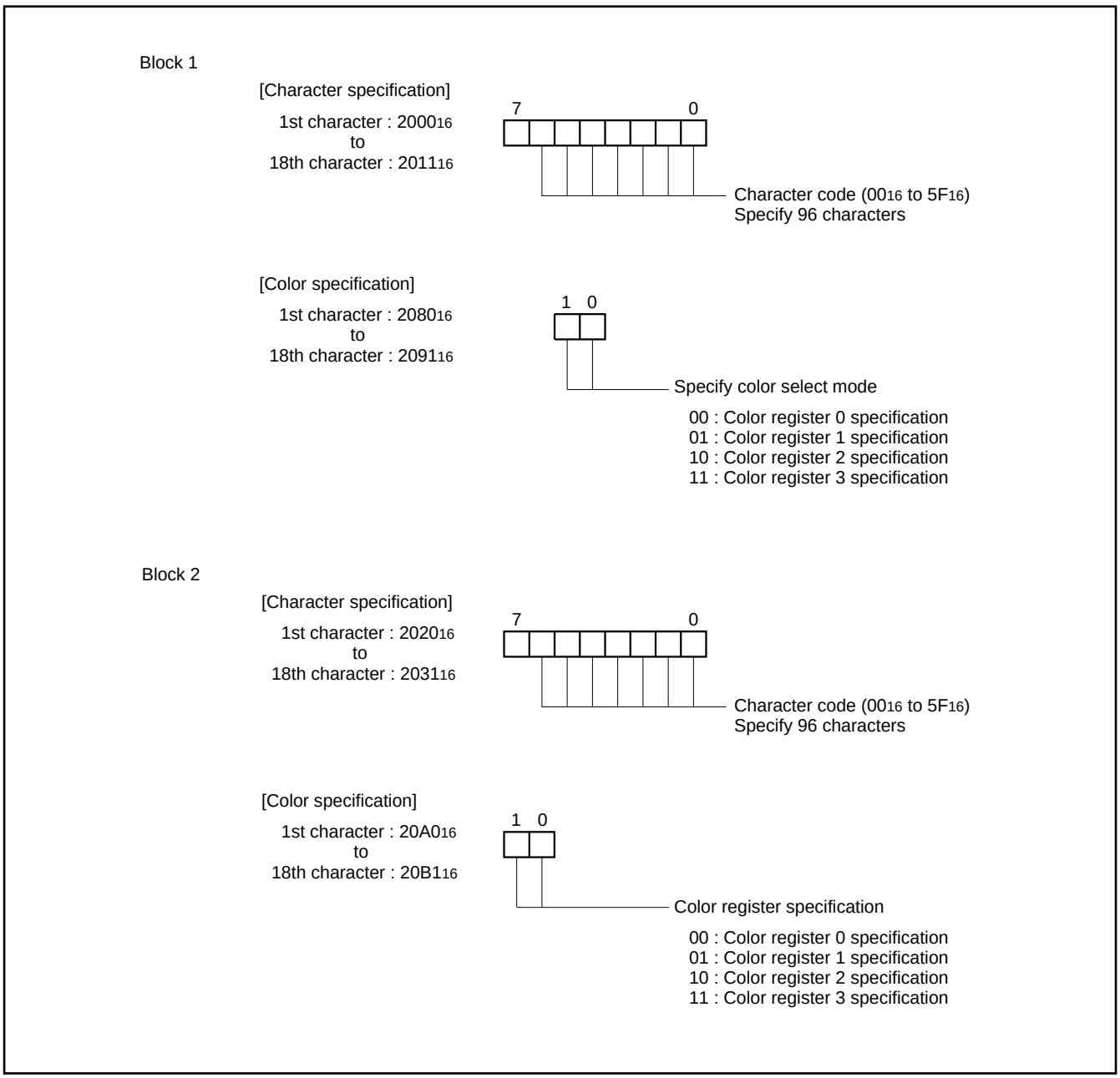


Fig. 28 Structure of the CRT display RAM

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3 : addresses $00E6_{16}$ to $00E9_{16}$) and then specifying that color register with the CRT display RAM.

There are three color outputs : R, G and B. By using a combination of these outputs, it is possible to set 2^3-1 (when no output) = 7 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G and B outputs are set by using bits 1 to 3 in the color register. Bit 5 is used to specify whether a character output or blank output. Figure 29 shows the structure of the color register.

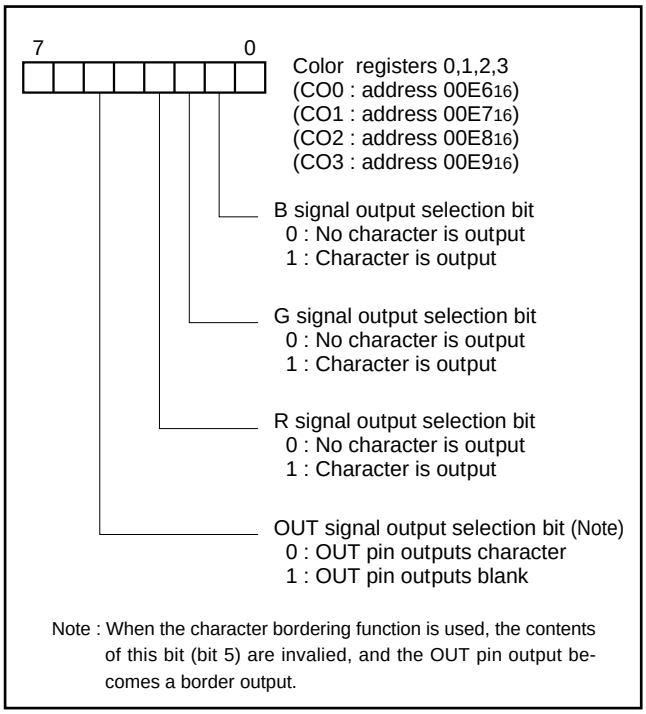


Fig. 29 Structure of color registers

(6) Multiline Display

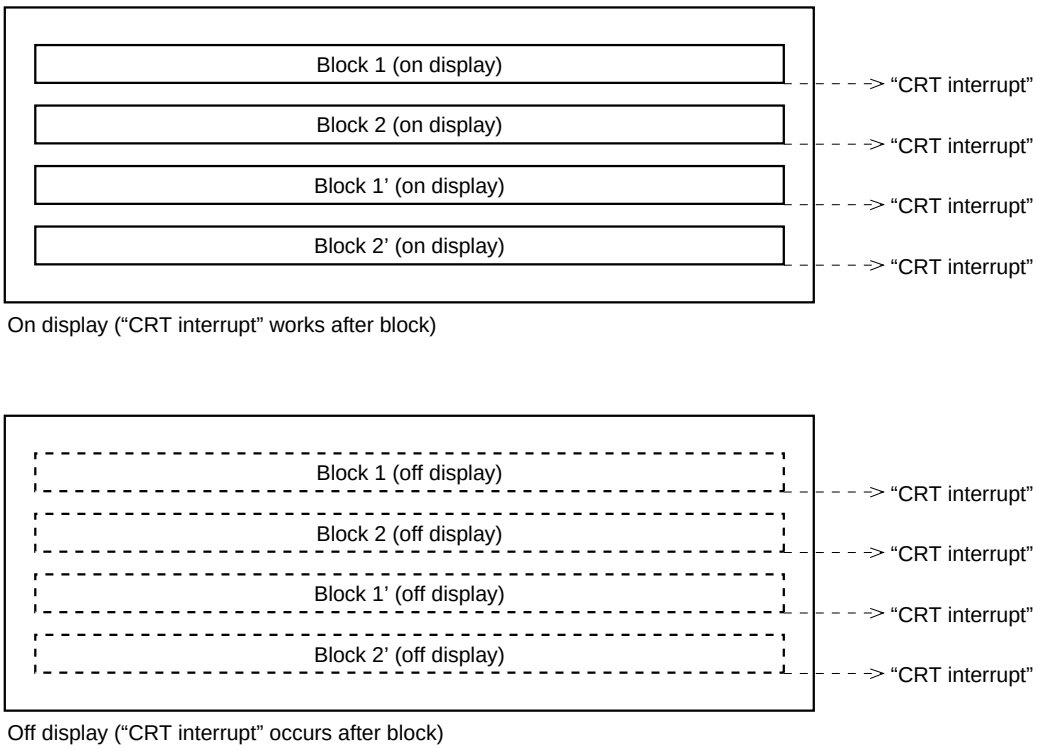
The M37210M3-XXXSP can normally display two lines on the CRT screen by displaying two blocks at different vertical positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated.

In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical position register) and when the range of that block is exceeded, an interrupt is applied.

Note : A CRT interrupt does occurs at the end of display regardless of display on or off. In other words, even if a block is set to off display with the display control bit of the CRT control register (address $00EA_{16}$), a CRT interrupt request occurs (refer to Figure 30).



(Note) : That is to say, "CRT interrupt" occurs even when it is off display by setting the display control flag of the CRT control register (address $00EA_{16}$).

Fig. 30 Timing of CRT interrupt

(7) Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT pin. In this case, bit 5 in the color register (contents output from the OUT pin) is nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the border select register (address $00E5_{16}$). Table 8 shows the relationship between the values set in the border select register and the character border function. Figure 32 shows the structure of the border select register.

Table 8. The relationship between the value set in the border selection register and the character border function

Border selection register MDn0	Functions	Example of output
0	Ordinary	R, G, B output OUT output
1	Border including character	R, G, B output OUT output

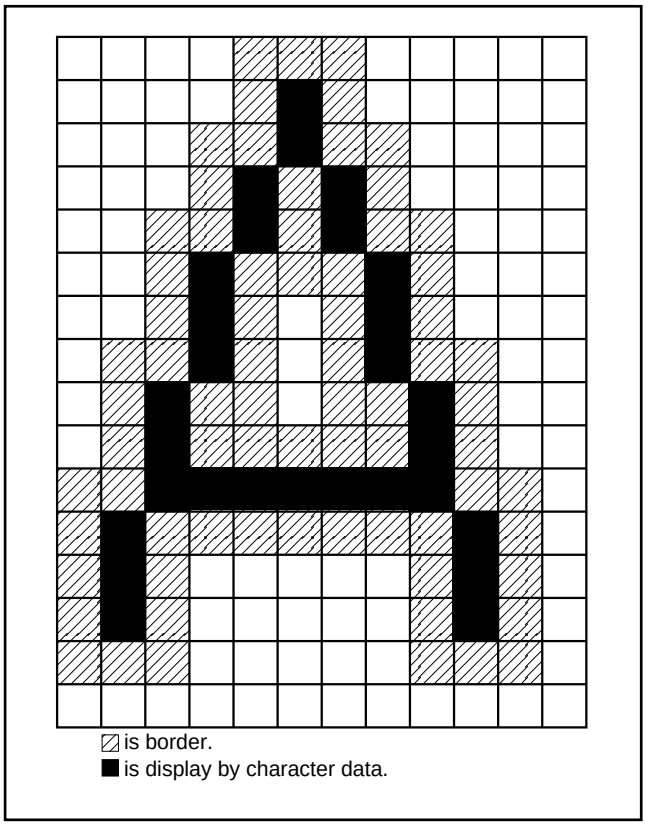


Fig. 31 Example of border

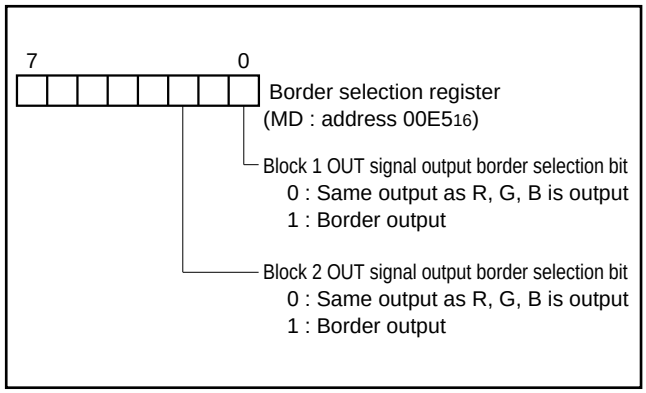


Fig. 32 Structure of border selection register

(8) CRT Output Pin Control

CRT output pins R, G, B and OUT are respectively shared with port $P5_2$, $P5_3$, $P5_4$ and $P5_5$. When the corresponding bits in the port P5 control register (address $00CB_{16}$) are cleared to "0", the pins are set for CRT output ; when the bits are set to "1", the pins function as port P5 (general- purpose output pins).

The polarities of CRT outputs (R, G, B and OUT, as well as HSYNC and VSYNC) can be specified by using the CRT port control register (address $00EC_{16}$).

Use bits 0 to 4 in the CRT port control register to set the output polarities of HSYNC, VSYNC, R/G/B and OUT. When these bits are cleared to "0", a positive polarity is selected ; when the bits are set to "1", a negative polarity is selected.

Bits 5 to 7 in the CRT port control register are used to specify pin by pin whether normal video signals or R-MUTE, G-MUTE, and B-MUTE signals are output from each pin (R, G, B). When set for R-MUTE, G-MUTE, and B-MUTE outputs, the whole background colors of the screen become red, green, and blue.

Figure 33 shows the structure of the CRT port control register.

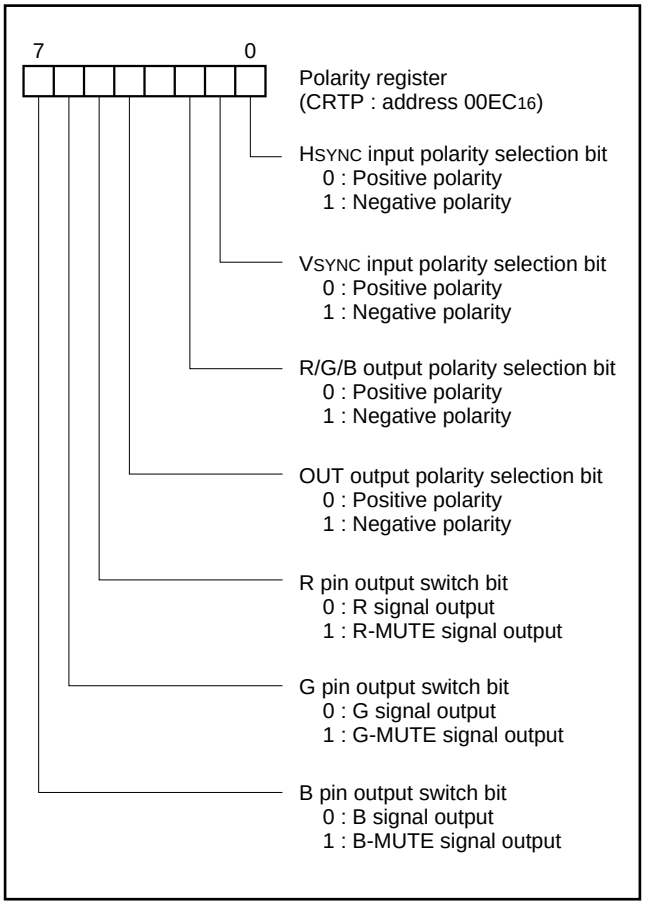


Fig. 33 Structure of CRT port control register

INTERRUPT INTERVAL DETERMINATION FUNCTION

The M37210M3-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter as shown in Figure 34.

Using this counter, it determines an interval or a pulse width on the INT1 or INT2 (refer to Figure 36).

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address $00D8_{16}$). When this bit is cleared to "0", the INT1 input is selected ; when the bit is set to "1", the INT2 input is selected.
2. When the INT1 input is to be determined, the polarity is selected by using bit 3 of the interrupt interval determination control register ; when the INT2 input is to be determined, the polarity is selected by using bit 4 of the interrupt interval determination control register.
   When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising transition) ; when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).
3. The reference clock is selected by using bit 1 of the interrupt interval determination control register. When the bit is cleared to "0", a 64μs clock is selected ; when the bit is set to "1", a 32µs clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary up counter starts counting up with the selected reference clock (64µs or 32µs).
5. Simultaneously with the next input pulse, the value of the 8-bit binary up counter is loaded into the determination register (address $00D7_{16}$) and the counter is immediately reset (00_{16}). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00_{16}".
6. When count value "FE_{16}" is reached, the 8-bit binary up counter stops counting. Then, simultaneously when the next reference clock is input, the counter sets value "FF_{16}" to the determination register.

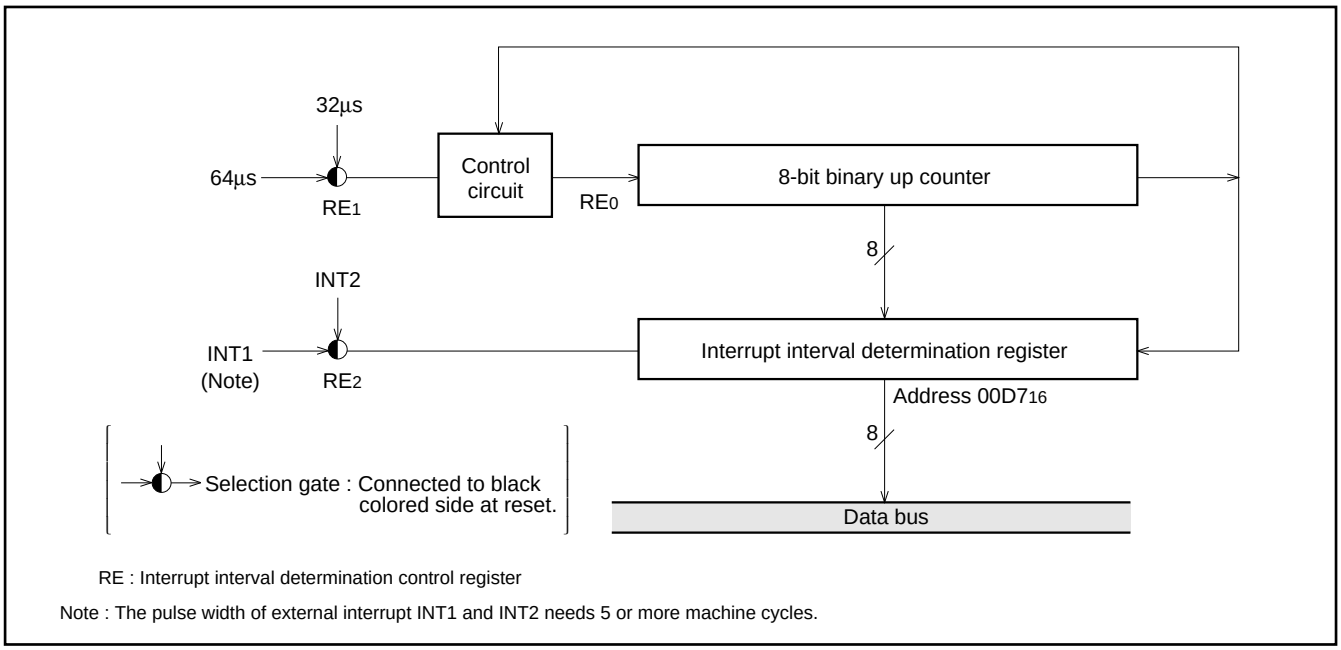


Fig. 34 Block diagram of interrupt interval determination circuit

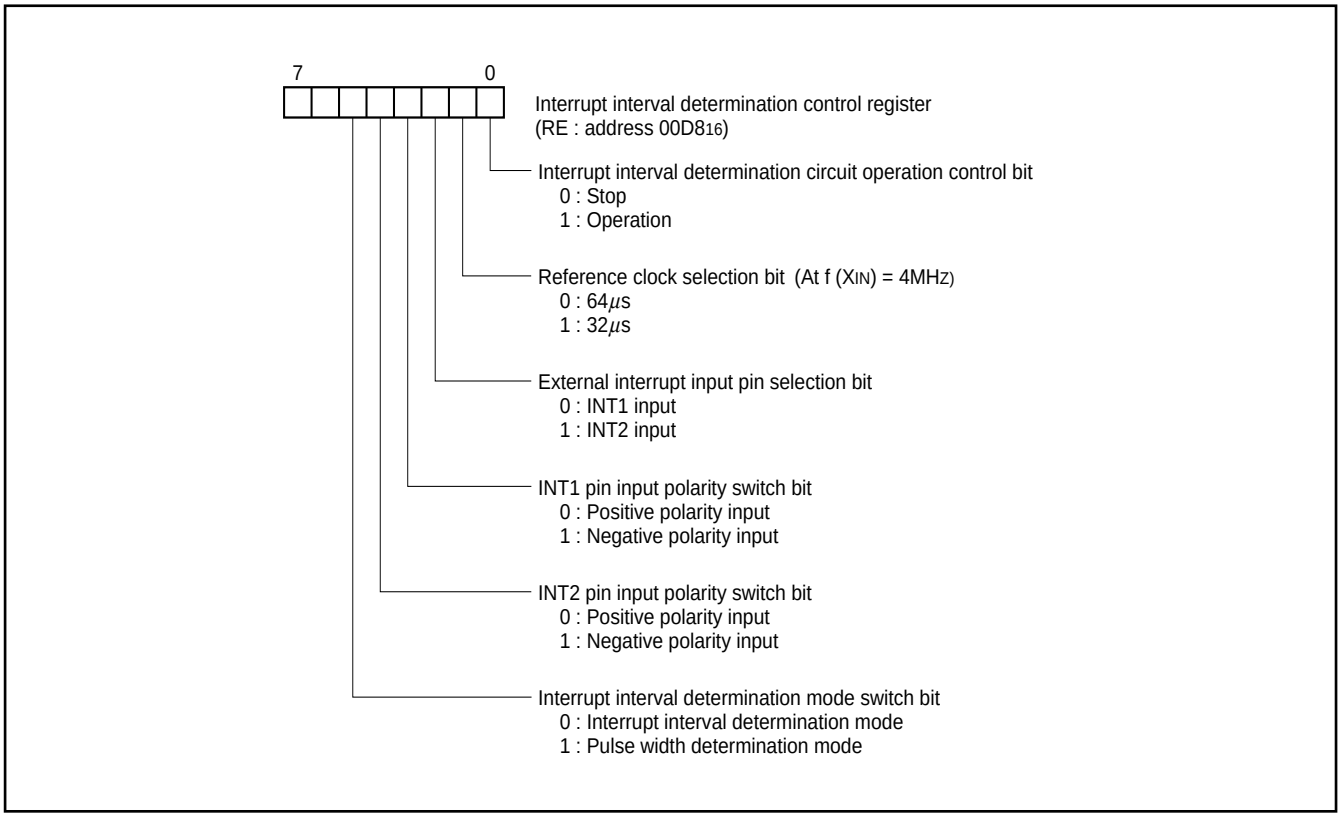


Fig. 35 Structure of interrupt space distinguish control register

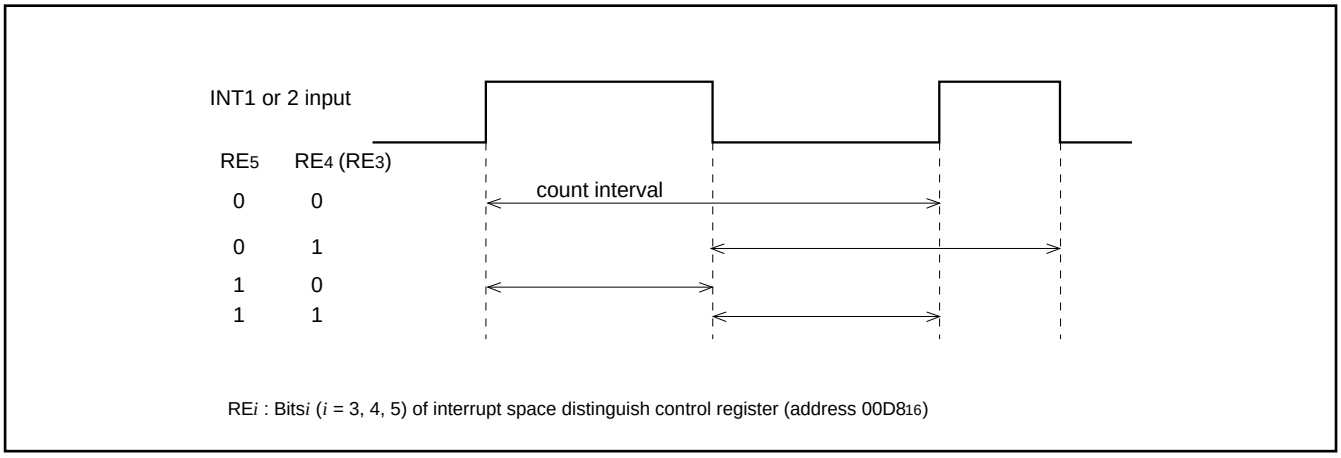


Fig. 36 Interrupt space distinguish control register setting value and the measuring interval

RESET CIRCUIT

The M37210M3-XXXSP is reset according to the sequence shown in Figure 39. It starts the program from the address formed by using the content of address FFFF16 as the high order address and the content of the address FFFE16 as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V ± 10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 37.

An example of the reset circuit is shown in Figure 38. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

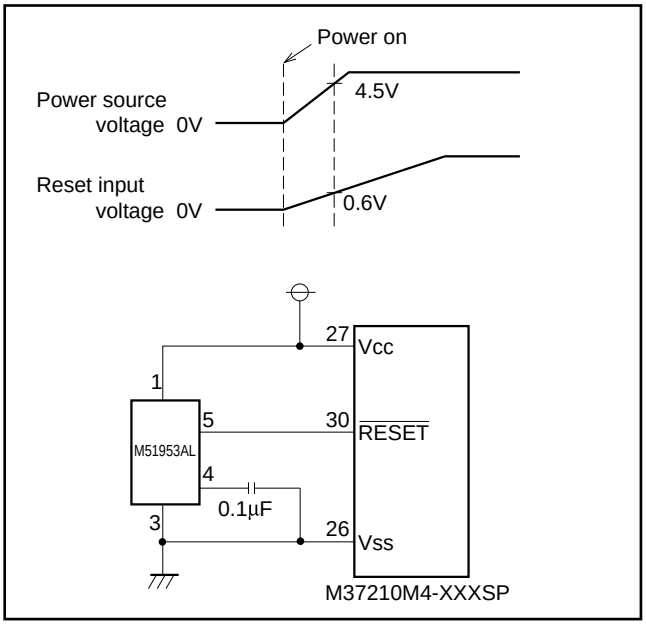
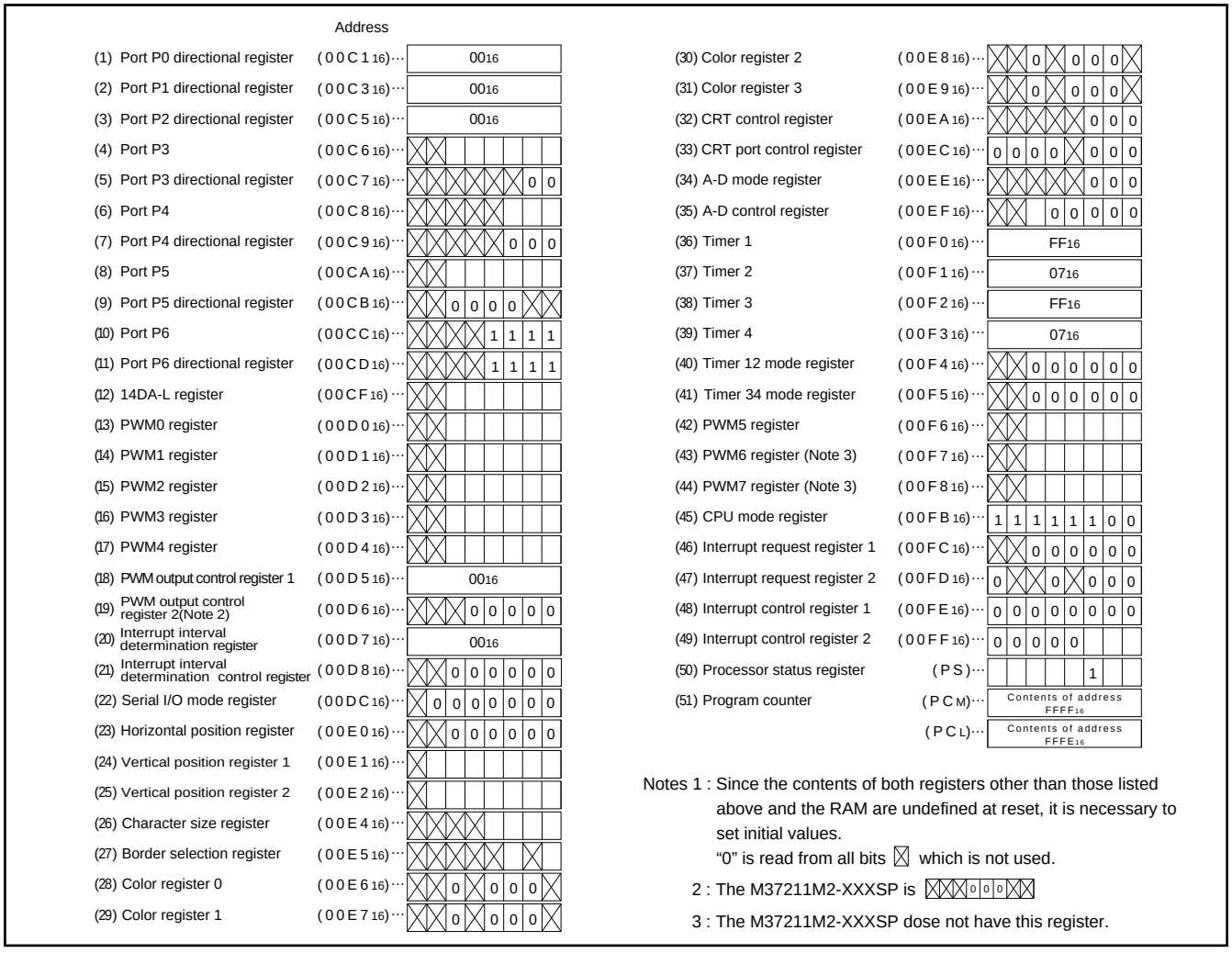
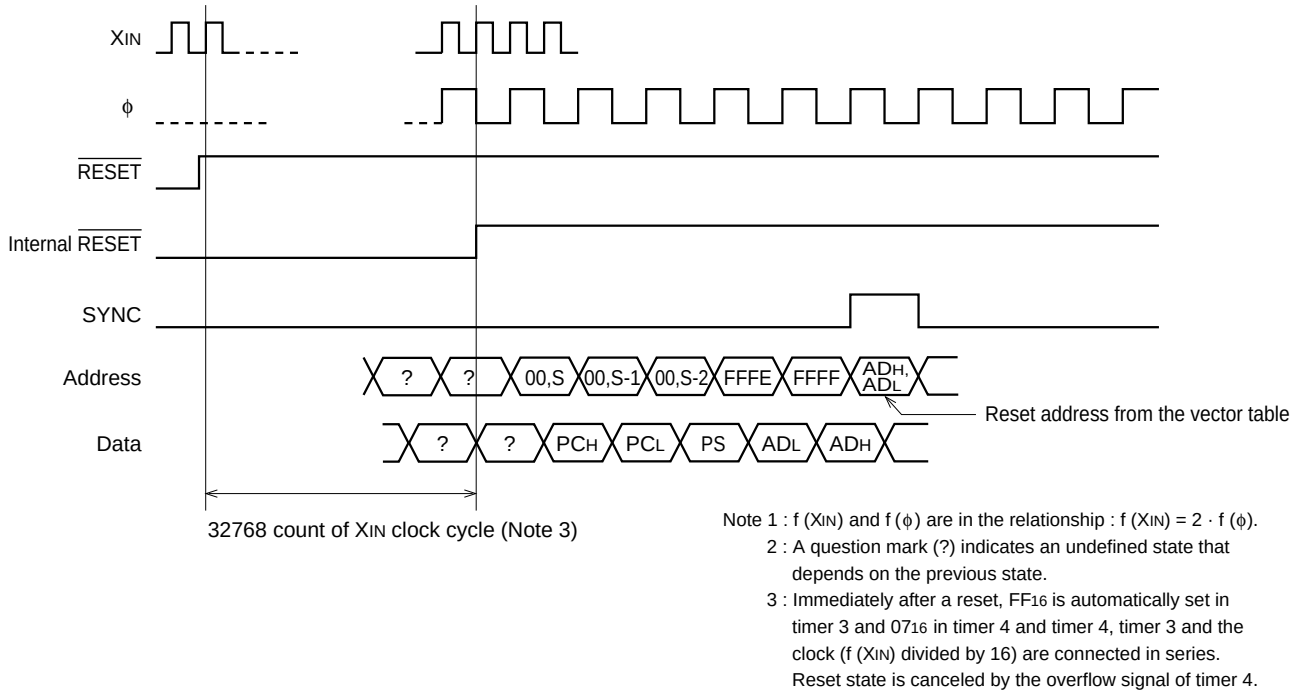


Fig. 38 Example of reset circuit



Notes 1 : Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values.
"0" is read from all bits ☒ which is not used.
2 : The M37211M2-XXXSP is ☒☒☒000☒☒
3 : The M37211M2-XXXSP dose not have this register.

Fig. 37 Internal state at reset



Note 1 : f (XIN) and f (φ) are in the relationship : f (XIN) = 2 · f (φ).
2 : A question mark (?) indicates an undefined state that depends on the previous state.
3 : Immediately after a reset, FF16 is automatically set in timer 3 and 0716 in timer 4 and timer 4, timer 3 and the clock (f (XIN) divided by 16) are connected in series. Reset state is canceled by the overflow signal of timer 4.

Fig. 39 Reset sequence

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open-drain output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a directional register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down.

Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Ports $P0_0$-$P0_3$ are in common with 6-bit PWM outputs PWM4-PWM7. For the M37211M2, ports $P0_0$ and $P0_1$ are in common with 6-bit PWM outputs PWM4 and PWM5.

(2) Port P1

Port P1 has basically the same function as port P0 except the output structure is CMOS output. But, pins $P1_5$-$P1_7$ are input ports and in common with analog input pins A-D1-A-D3.

(3) Port P2

Port P2 has basically the same function as port P1.

(4) Port P3

Port P3 are a 2-bit I/O port and a 4-bit input port with function similar to port P2, but the output structure of $P3_0$, $P3_1$ is CMOS output.

$P3_2$, $P3_3$ are in common with the external clock input pins of timer 2 and 3.

$P3_4$, $P3_5$ are in common with the external interrupt input pins INT1, INT2 and $P3_5$ with the analog input pin of A-D comparator A-D4.

(5) Port P4

Port P4 are a 2-bit I/O port and a 1-bit input port with function similar to port P2, but the output structure is N-channel open-drain output.

When a serial I/O function is selected, $P4_0$-$P4_2$ are in common with pins S_{OUT}, S_{CLK} and S_{IN}.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, OUT pins

This is an 4-bit output pin for CRT display and in common with $P5_2$-$P5_5$.

(9) Port P6

Port P6 is an 4-bit output port with function similar to port P0, but the output structure is N-channel opendrain output.

This port is in common with 6-bit PWM output pin PWM0-PWM3.

(10) D-A pin

This is a 14-bit PWM output pin.

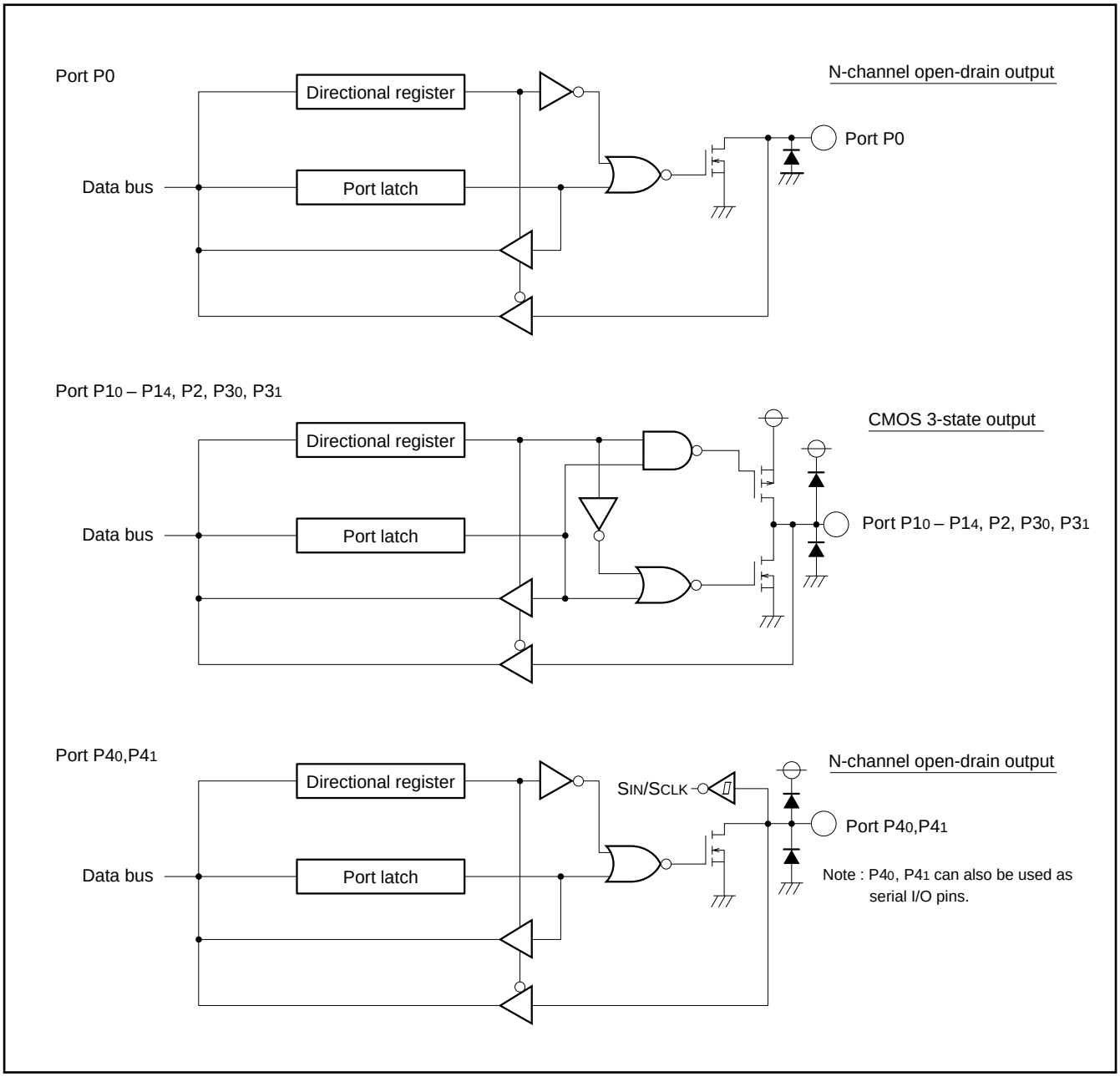


Fig. 40 I/O pin block diagram (1)

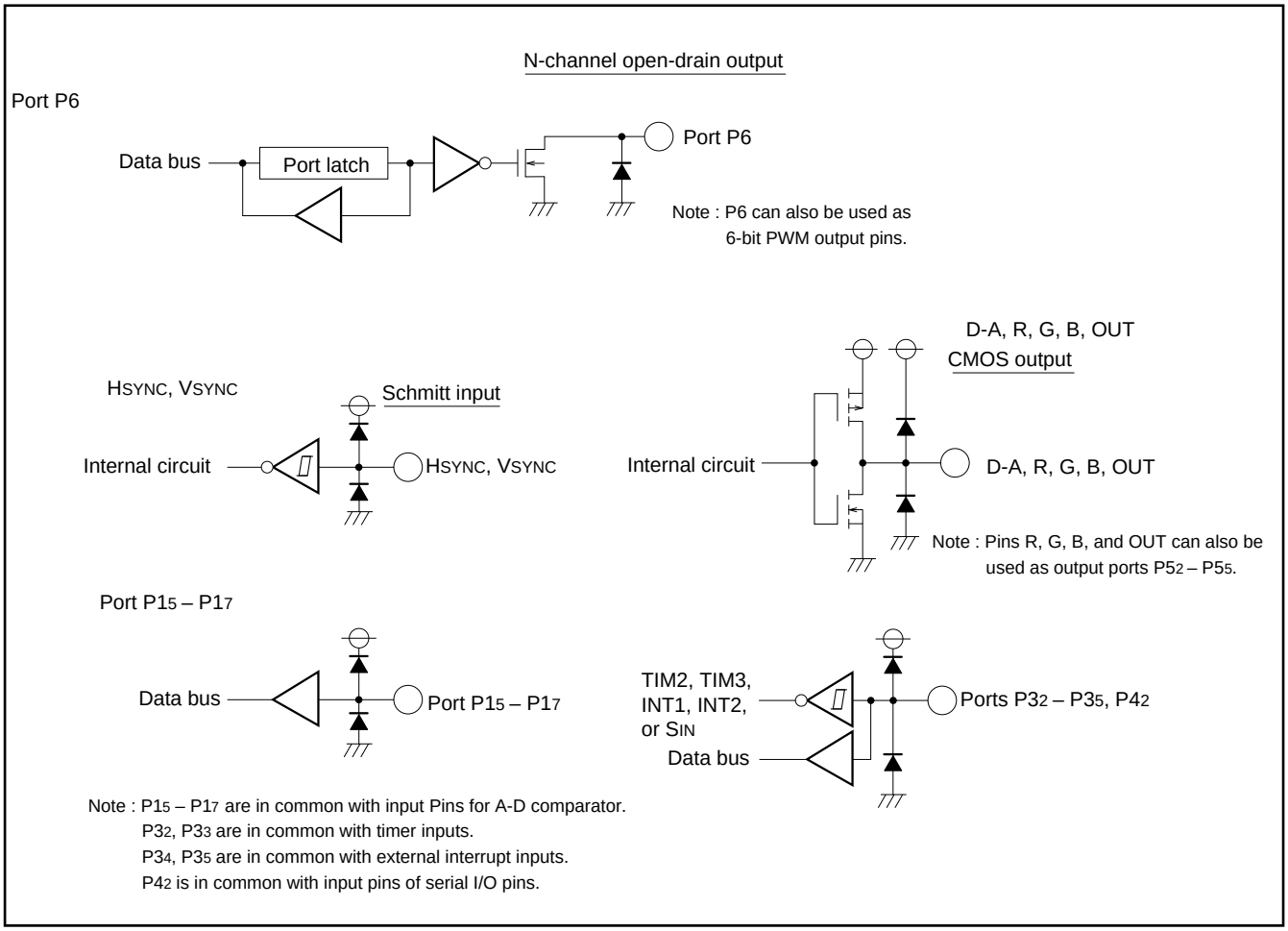


Fig. 41 I/O pin block diagram (2)

CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 44.

When the STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timers 3 and 4 are connected in hardware and "FF_{16}" is set in the timer 3, "07_{16}" is set in the timer 4. Select f(X_{IN})/16 as the timer 3 count source (set bit 0 of the timer 34 mode register to "0" before the execution of the STP instruction). And besides, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction.

The oscillator is restarted when an external interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic resonator or a quartz-crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted (Note). Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait state, set the interrupt enable bit to "1" before executing the STP or the WIT instruction.

Note : In the wait mode, the following interrupts are invalid.

(1) V_{SYNC} interrupt
(2) CRT interrupt
(3) Timer 2 interrupt using $P3_2$/TIM2 pin input as count source
(4) Timer 3 interrupt using $P3_3$/TIM3 pin input as count source
(5) Timer 4 interrupt using f(X_{IN})/2 as count source

The circuit example using a ceramic resonator (or a quartz crystal oscillator) is shown in Figure 42.

Use the circuit constants in accordance with the resonator manufacture's recommended values.

The example of external clock usage is shown in Figure 43 X_{IN} is the input, and X_{OUT} is open.

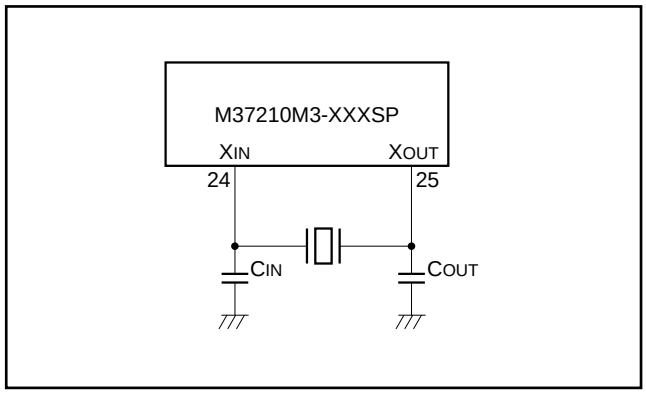


Fig. 42 Ceramic resonator circuit example

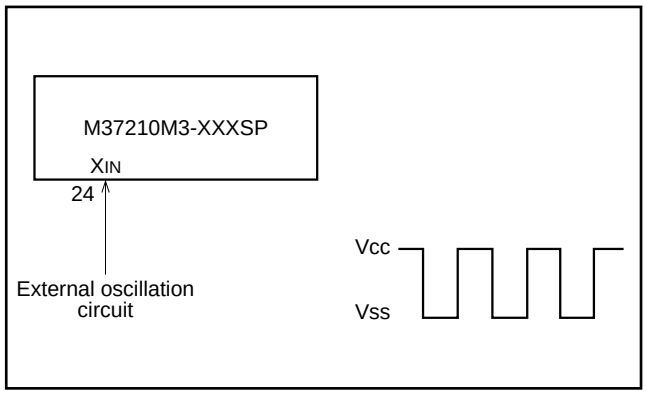


Fig. 43 External clock input circuit example

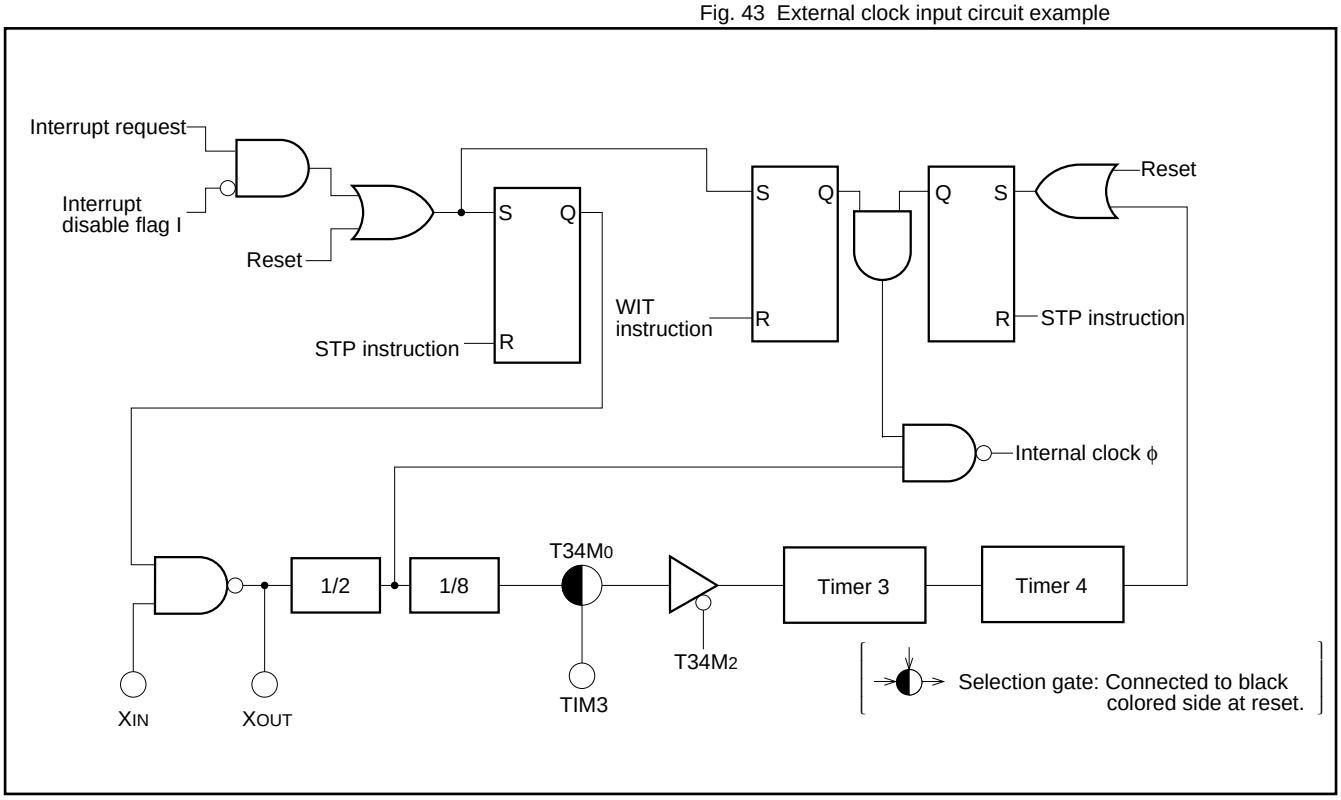


Fig. 44 Clock generating circuit block diagram

PROGRAMMING NOTES

(1) The divide ratio of the timer is 1/ (n + 1).
(2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (indecimal operation mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(4) An NOP instruction is needed immediately after the execution of a PLP instruction.
(5) In order to avoid noise and latch-up, connect a bypass capacitor (≈ 0.1μF) directly between the V_{CC} pin and V_{SS} pin using a thick wire.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production.
(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (28-pin DIP type 27256, three identical copies)

PROM Programming Method

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37210E4SP	PCA4754
M37210E4FP	PCA4756

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 45 is recommended to verify programming.

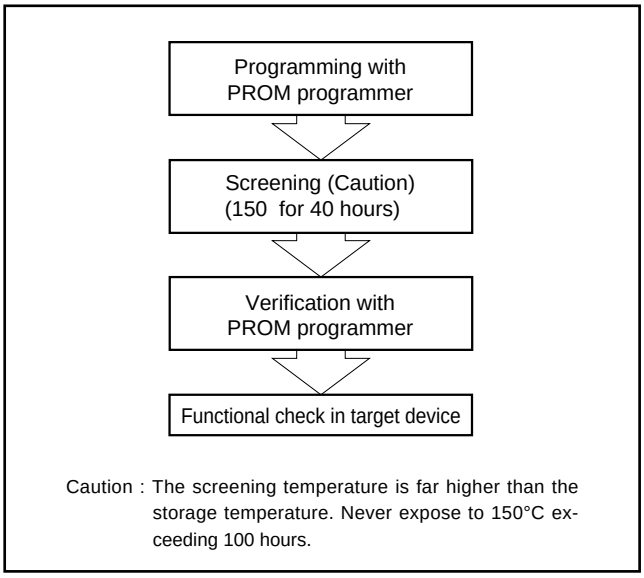


Fig. 45 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	– 0.3 to 6	V
V_I	Input voltage CNV$_{SS}$		– 0.3 to 6	V
V_I	Input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, $P4_0$ – $P4_2$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, OSC1, X_{IN}		– 0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P1_0$ – $P1_4$, $P2_0$ – $P2_7$, $P3_0$, $P3_1$, $P4_0$, $P4_1$, R, G, B, OUT, D-A, X_{OUT}, OSC2		– 0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P6_0$ – $P6_3$, $P0_0$ – $P0_7$		– 0.3 to 13	V
I_{OH}	"H" average output current R, G, B, OUT, $P1_0$ – $P1_4$, $P2_0$ – $P2_3$, $P3_0$, $P3_1$, D-A		0 to 1 (Note 1)	mA
I_{OL1}	"L" average output current R, G, B, OUT, $P1_0$ – $P1_4$, $P2_0$ – $P2_3$, $P3_0$, $P3_1$, $P4_0$, $P4_1$ D-A		0 to 2 (Note 2)	mA
I_{OL2}	"L" average output current $P6_0$ – $P6_3$, $P0_0$ – $P0_7$		0 to 1 (Note 2)	mA
I_{OL3}	"L" average output current $P2_4$ – $P2_7$		0 to 10 (Note 3)	mA
Pd	Power dissipation	Ta = 25°C	550	mW
Topr	Operating temperature		– 10 to 70	°C
Tstg	Storage temperature		– 40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = –10 to 70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage (Note 4) During the CPU and the CRT operation	4.5	5.0	5.5	V
V_{SS}	Power source voltage	0	0	0	V
V_{IH}	"H" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, $P4_0$ – $P4_2$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1, TIM2, TIM3, INT1, INT2, S_{IN}, S_{CLK}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, $P4_0$ – $P4_2$	0		0.4V_{CC}	V
V_{IL}	"L" input voltage TIM2, TIM3, INT1, INT2, S_{IN}, S_{CLK}, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1	0		0.2V_{CC}	V
I_{OH}	"H" average output current (Note 1) R, G, B, OUT, $P1_0$ – $P1_4$, $P2_0$ – $P2_7$, $P3_0$, $P3_1$, D-A			1	mA
I_{OL1}	"L" average output current (Note 2) R, G, B, OUT, $P1_0$ – $P1_4$, $P2_0$ – $P2_3$, $P3_0$, $P3_1$, $P4_0$, $P4_1$, D-A			2	mA
I_{OL2}	"L" average output current (Note 2) $P6_0$ – $P6_3$, $P0_0$ – $P0_7$			1	mA
I_{OL3}	"L" average output current (Note 3) $P2_4$ – $P2_7$			10	mA
f_{CPU}	Oscillation frequency (for CPU operation)(Note 5)	3.6	4.0	8.1	MHz
f_{CRT}	Oscillation frequency (for CRT display)	4.0	5.0	6.0	MHz
fhs	Input frequency TIM2, TIM3, INT1, INT2			100	kHz
fhs	Input frequency S_{CLK}			1	MHz

Notes 1 : The total current that flows out of the IC should be 20mA (max.).
2 : The total of I_{OL1} and I_{OL2} should be 30mA (max.).
3 : The total of I_{OL} of port $P2_4$-$P2_7$ should be 20mA (max.).
4 : Connect 0.022µF or more capacitor externally between the V_{CC} – V_{SS} power source pins so as to reduce power source noise.
Also connect 0.068µF or more capacitor externally between the V_{CC} – CNV$_{SS}$ pins.
5 : Use a quartz-crystal oscillator or a ceramic resonator for CPU oscillation circuit.

ELECTRIC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = – 10 to 70°C, f (X_{IN}) = 4MHz unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
I_{CC}	Power source current	V_{CC} = 5.5V, f (X_{IN}) = 4MHz	CRT	OFF	–	10	20	mA
				ON	–	20	40	
		V_{CC} = 5.5V, f (X_{IN}) = 8MHz	CRT	OFF	–	20	40	mA
				ON	–	30	60	
		At stop mode			–	–	300	µA
V_{OH}	"H" output voltage $P1_0$ – $P1_4$, $P2_0$ – $P2_7$, $P3_0$, $P3_1$, R, G, B, OUT, D-A	V_{CC} = 4.5V, I_{OH} = – 0.5mA			2.4			V
V_{OL}	"L" output voltage $P1_0$ – $P1_4$, $P2_0$ – $P2_3$, $P3_0$, $P3_1$, $P4_0$, $P4_1$, R, G, B, OUT, D-A	V_{CC} = 4.5V, I_{OL} = 0.5mA					0.4	V
	"L" output voltage $P6_0$ – $P6_3$, $P0_0$ – $P0_7$	V_{CC} = 4.5V, I_{OL} = 0.5mA					0.4	
	"L" output voltage $P2_4$ – $P2_7$	V_{CC} = 4.5V, I_{OL} = 10.0mA					3.0	
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 5.0V				0.5	0.7	V
	Hysteresis (Note) H_{SYNC}, V_{SYNC}, TIM2, TIM3, INT1, INT2, S_{IN}, S_{CLK}	V_{CC} = 5.0V				0.5	1.3	
I_{IZH}	"H" input leak current $\overline{RESET}$, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, $P4_0$ – $P4_2$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5V, V_I = 5.5V					5	µA
I_{IZL}	"L" input leak current $\overline{RESET}$, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, $P4_0$ – $P4_2$, $P6_0$ – $P6_3$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5V, V_I = 0V					5	µA
I_{OZH}	"H" input leak current $P6_0$ – $P6_3$, $P0_0$ – $P0_7$	V_{CC} = 5.5V, V_O = 12V					10	µA

Note : $P3_2$ – $P3_5$, have the hysteresis when these pins are used as interrupt input pins or timer input pins.
$P4_0$ – $P4_2$ have the hysteresis when these pins are used as serial I/O ports.

M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP
M37210E4-XXXSP/FP, M37210E4SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

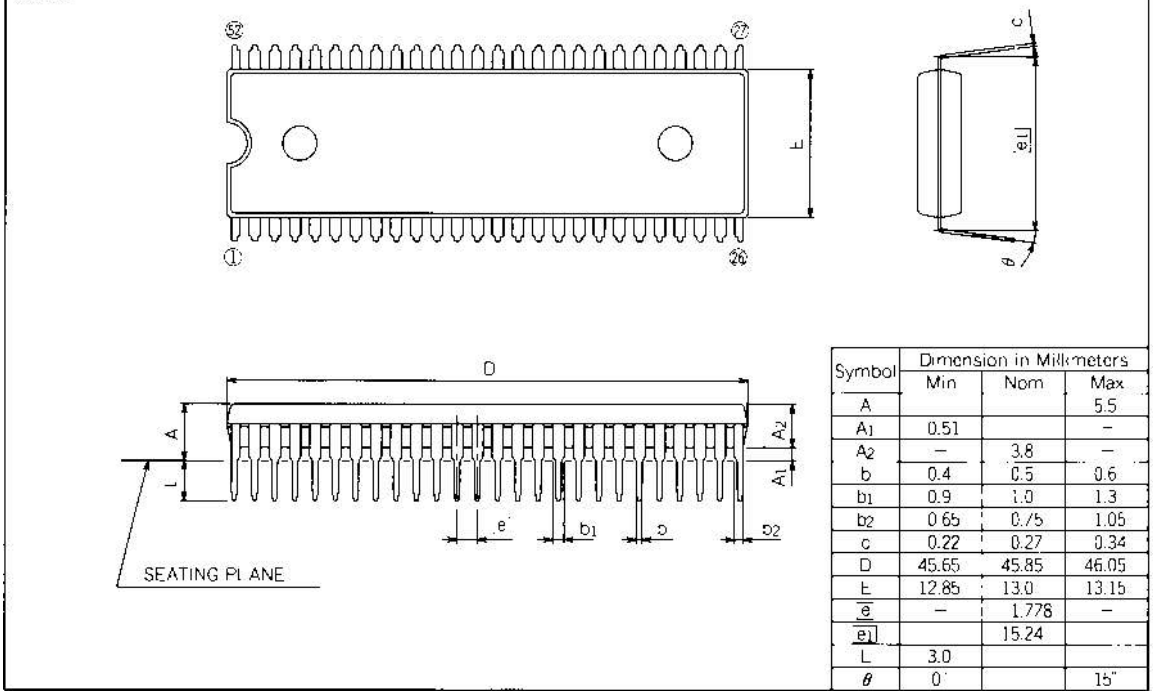
PACKAGE OUTLINE

52P4B

Plastic 52pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP52-P-600-1.78		5.1	Alloy 42/Cu Alloy

Scale :



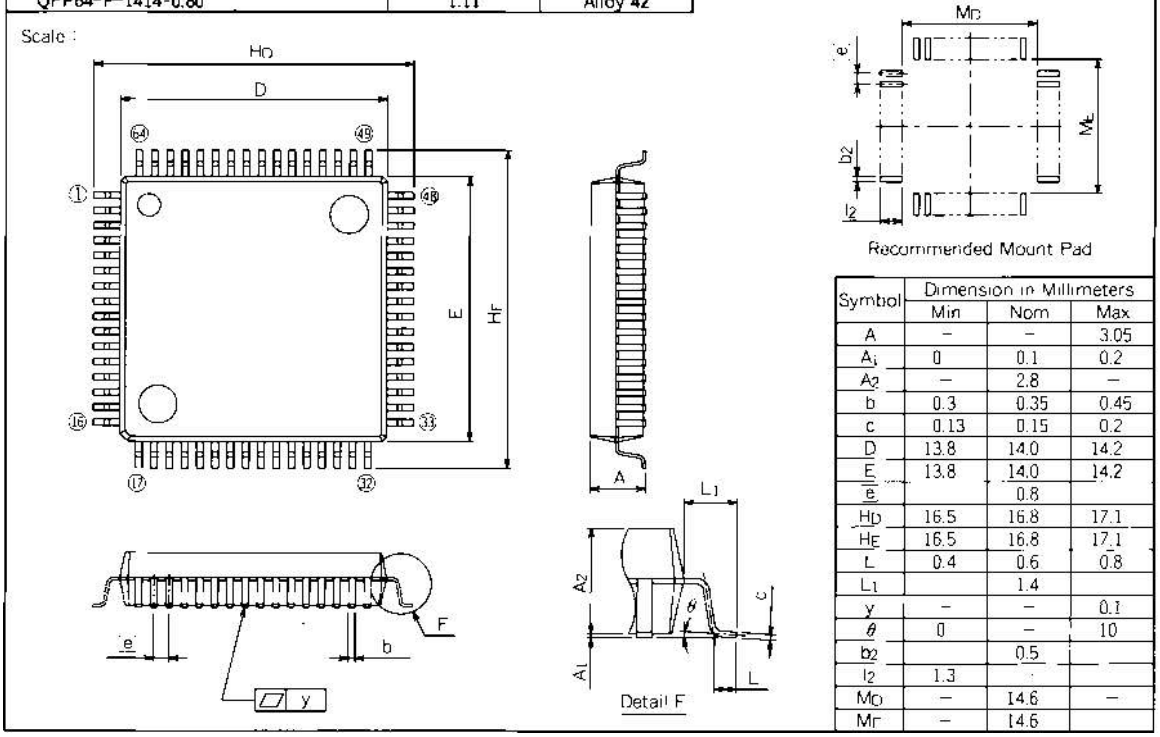
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A			5.5
A_1	0.51		–
A_2	–	3.8	–
b	0.4	0.5	0.6
b_1	0.9	1.0	1.3
b_2	0.65	0.75	1.05
c	0.22	0.27	0.34
D	45.65	45.85	46.05
E	12.85	13.0	13.15
e	–	1.778	–
e1		15.24	
L	3.0		
θ	0°		15°

64P6N-A

Plastic 64pin 14×14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP64-P-1414-0.80		1.11	Alloy 42

Scale :



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e		0.8	
H_D	16.5	16.8	17.1
H_E	16.5	16.8	17.1
L	0.4	0.6	0.8
L_1		1.4	
y	–	–	0.1
θ	0°	–	10°
b_2		0.5	
l_2	1.3		
M_D	–	14.6	–
M_E	–	14.6	

MITSUBISHI ELECTRIC

GZZ–SH06–09B < 25C0 >

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor sighature

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37210M3-XXXSP/FP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

✵ 1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

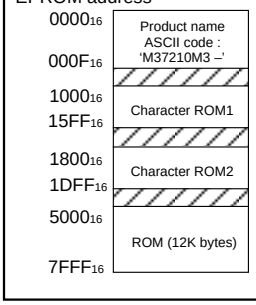
Microcomputer name : ☐ M37210M3-XXXSP ☐ M37210M3-XXXFP

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27256**

EPROM address



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the product name of "M37210M3–" to addresses 0000$_{16}$ to 000F$_{16}$.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37210M3-XXXSP; 64P6N for M37210M3-XXXFP) and attach to the mask ROM confirmation form.

✵ 3. Comments

GZZ–SH06–09B < 25C0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37210M3-XXXSP/FP
MITSUBISHI ELECTRIC

Writing the product name and character ROM data onto EPROMs

Addresses 0000_{16} to $000F_{16}$ store the product name, and addresses 1000_{16} to $15FF_{16}$ and addresses 1800_{16} to $1DFF_{16}$ store the character pattern.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code
   ASCII codes 'M37210M3-' are listed on the right.
   The addresses and data are in hexadecimal notation.

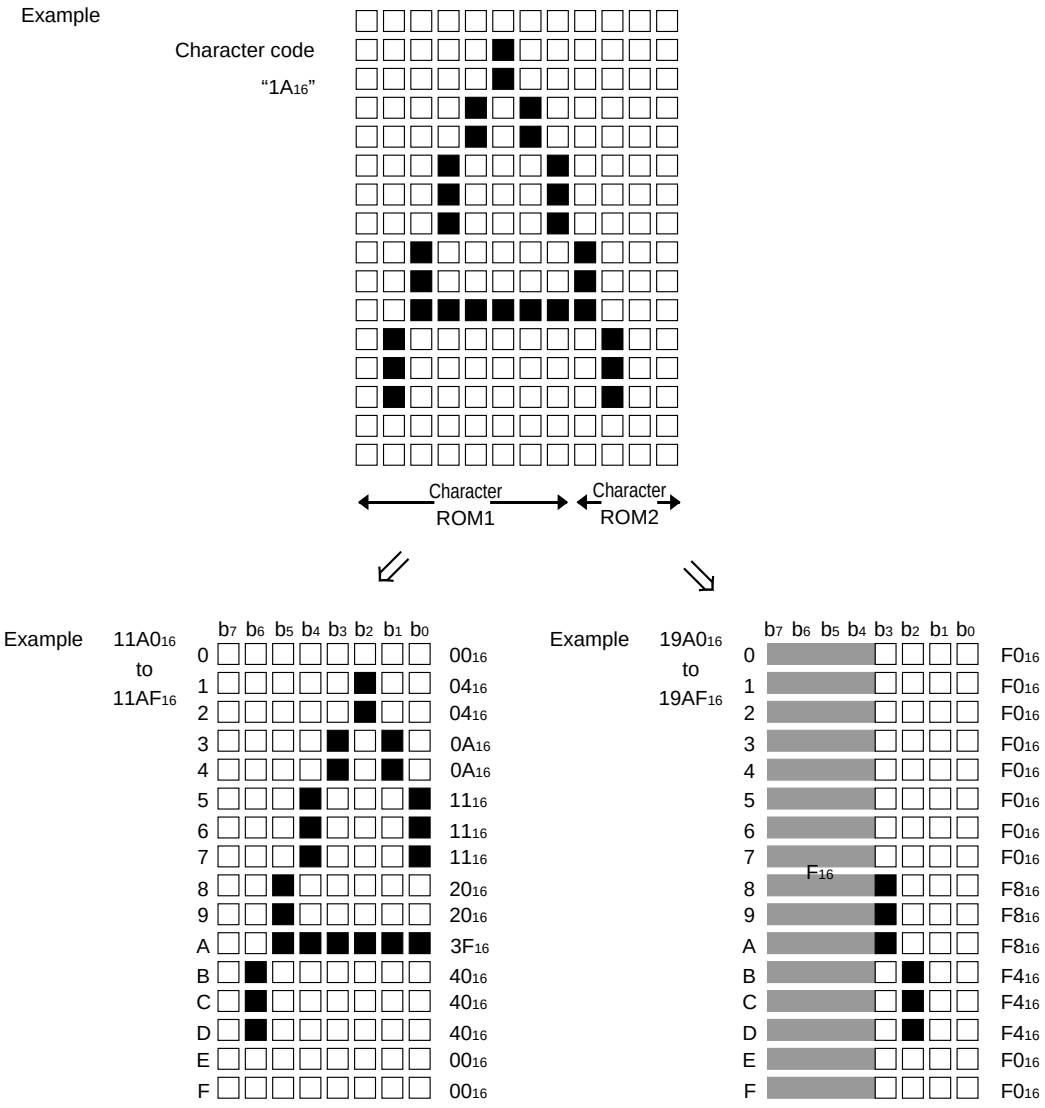
Address		Address	
0000_{16}	'M' = 4 D $_{16}$	0008_{16}	'–' = 2 D $_{16}$
0001_{16}	'3' = 3 3 $_{16}$	0009_{16}	F F $_{16}$
0002_{16}	'7' = 3 7 $_{16}$	$000A_{16}$	F F $_{16}$
0003_{16}	'2' = 3 2 $_{16}$	$000B_{16}$	F F $_{16}$
0004_{16}	'1' = 3 1 $_{16}$	$000C_{16}$	F F $_{16}$
0005_{16}	'0' = 3 0 $_{16}$	$000D_{16}$	F F $_{16}$
0006_{16}	'M' = 4 D $_{16}$	$000E_{16}$	F F $_{16}$
0007_{16}	'3' = 3 3 $_{16}$	$000F_{16}$	F F $_{16}$

2. Inputting the character ROM
   Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data, see the next page and on.

GZZ–SH06–09B < 25C0>

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37210M3-XXXSP/FP
MITSUBISHI ELECTRIC

The structure of character ROM (divided of 12×16 dots font)



M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP
M37210E4-XXXSP/FP, M37210E4SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

GZZ–SH06–10B < 25B0 >

Mask ROM number	

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37210M4-XXXSP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor sighature

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

✵ 1. Confirmation

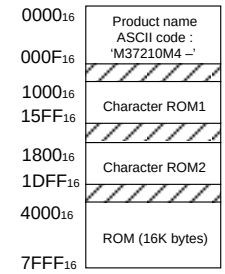
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27256**

EPROM address



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the product name of "M37210M4–" to addresses 0000$_{16}$ to 000F$_{16}$.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37210M4-XXXSP) and attach to the mask ROM confirmation form.

✵ 3. Comments

MITSUBISHI ELECTRIC

GZZ–SH06–10B < 25B0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37210M4-XXXSP
MITSUBISHI ELECTRIC

Writing the product name and character ROM data onto EPROMs

Addresses 0000_{16} to $000F_{16}$ store the product name, and addresses 1000_{16} to $15FF_{16}$ and addresses 1800_{16} to $1DFF_{16}$ store the character pattern.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code
   ASCII codes 'M37210M4-' are listed on the right.
   The addresses and data are in hexadecimal notation.

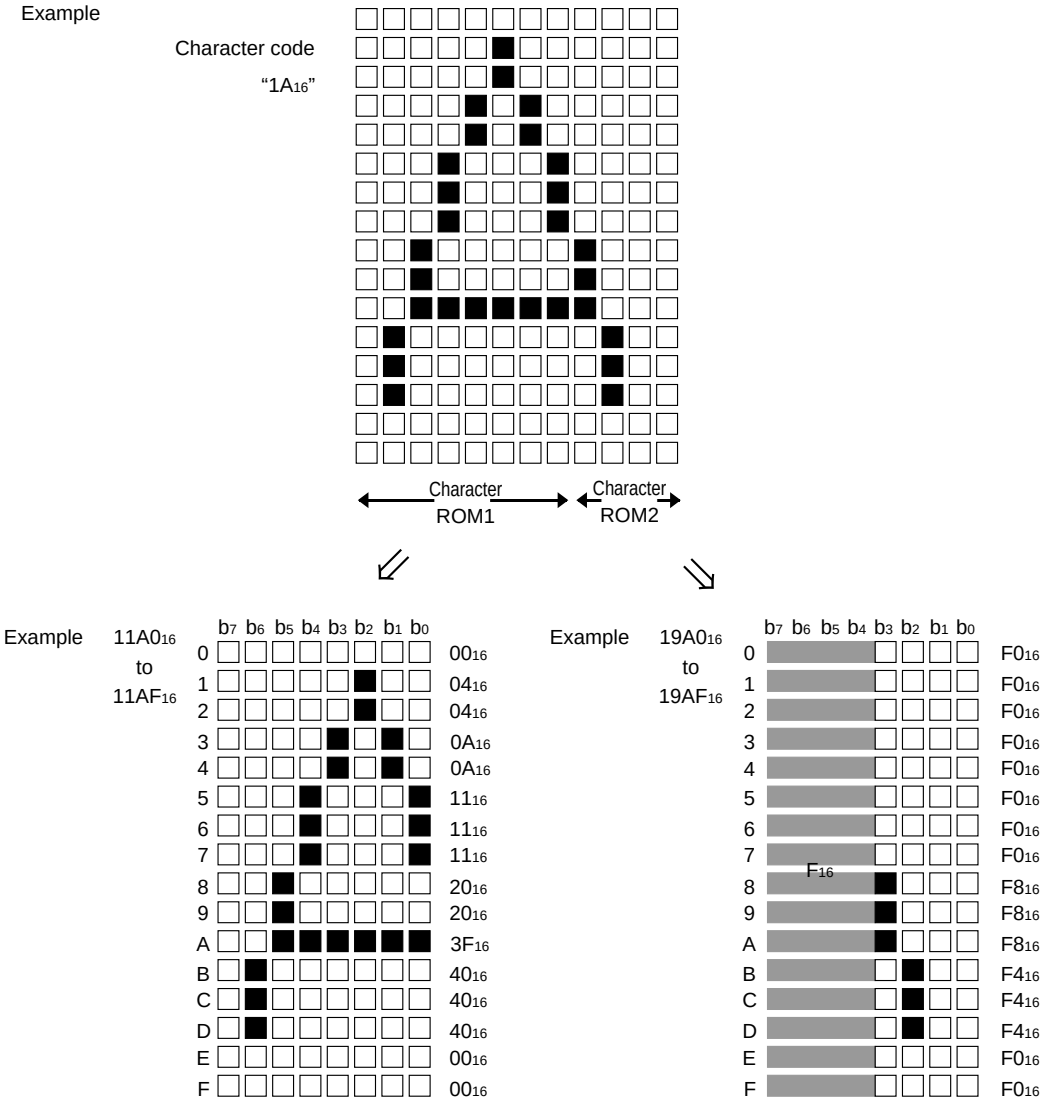
Address		Address	
0000_{16}	'M' = 4D $_{16}$	0008_{16}	'–' = 2D $_{16}$
0001_{16}	'3' = 33 $_{16}$	0009_{16}	FF $_{16}$
0002_{16}	'7' = 37 $_{16}$	$000A_{16}$	FF $_{16}$
0003_{16}	'2' = 32 $_{16}$	$000B_{16}$	FF $_{16}$
0004_{16}	'1' = 31 $_{16}$	$000C_{16}$	FF $_{16}$
0005_{16}	'0' = 30 $_{16}$	$000D_{16}$	FF $_{16}$
0006_{16}	'M' = 4D $_{16}$	$000E_{16}$	FF $_{16}$
0007_{16}	'4' = 34 $_{16}$	$000F_{16}$	FF $_{16}$

2. Inputting the character ROM
   Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data, see the next page and on.

GZZ–SH06–10B < 25B0 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37210M4-XXXSP
MITSUBISHI ELECTRIC

The structure of character ROM (divided of 12×16 dots font)



GZZ–SH06–11B < 25B1 >

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor sighature

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37211M2-XXXSP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked ✵.

✵	Customer	Company name	TEL ( )	Issuance signature	Submitted by	Supervisor
		Date issued	Date :			

✵ 1. Confirmation

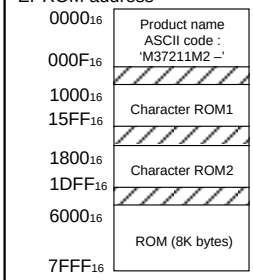
Specify the name of the product being ordered and the type of EPROMs submitted.
Three EPROMs are required for each pattern.
If at least two of the three sets of EPROMs submitted contain identical data, we will produce masks based on this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differs from this data. Thus, extreme care must be taken to verify the data in the submitted EPROMs.

Checksum code for entire EPROM | | | | | (hexadecimal notation)

EPROM type (indicate the type used)

☐ **27256**

EPROM address



(1) Set "FF$_{16}$" in the shaded area.
(2) Write the ASCII codes that indicates the product name of "M37211M2–" to addresses 0000$_{16}$ to 000F$_{16}$.

✵ 2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M37211M2-XXXSP) and attach to the mask ROM confirmation form.

✵ 3. Note

(1) Set the stack page selection bit to "0", because this bit is set to "1" after reset but the internal RAM is located at 0 page only.
(2) Both P0$_2$ pin (9th pin) and P0$_3$ pin (10th pin) are not used as PWM output pins.

✵ 4. Comments

GZZ–SH06–11B< 25B1 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37211M2-XXXSP
MITSUBISHI ELECTRIC

Writing the product name and character ROM data onto EPROMs

Addresses 0000_{16} to $000F_{16}$ store the product name, and addresses 1000_{16} to $15FF_{16}$ and addresses 1800_{16} to $1DFF_{16}$ store the character pattern.
If the name of the product contained in the EPROMs does not match the name on the mask ROM confirmation form, the ROM processing is disabled. Write the data correctly.

1. Inputting the name of the product with the ASCII code
   ASCII codes 'M37211M2-' are listed on the right.
   The addresses and data are in hexadecimal notation.

Address		Address	
0000_{16}	'M' = 4D $_{16}$	0008_{16}	'–' = 2D $_{16}$
0001_{16}	'3' = 33 $_{16}$	0009_{16}	FF $_{16}$
0002_{16}	'7' = 37 $_{16}$	$000A_{16}$	FF $_{16}$
0003_{16}	'2' = 32 $_{16}$	$000B_{16}$	FF $_{16}$
0004_{16}	'1' = 31 $_{16}$	$000C_{16}$	FF $_{16}$
0005_{16}	'1' = 31 $_{16}$	$000D_{16}$	FF $_{16}$
0006_{16}	'M' = 4D $_{16}$	$000E_{16}$	FF $_{16}$
0007_{16}	'2' = 32 $_{16}$	$000F_{16}$	FF $_{16}$

2. Inputting the character ROM
   Input the character ROM data by dividing it into character ROM1 and character ROM2. For the character ROM data, see the next page and on.

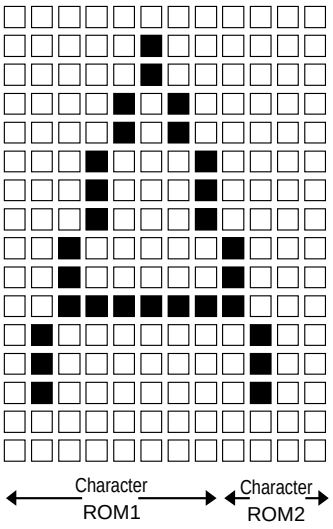
GZZ–SH06–11B < 25B1 >

740 FAMILY MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37211M2-XXXSP
MITSUBISHI ELECTRIC

The structure of character ROM (divided of 12 ×16 dots font)

Example

Character code "1A16"



Example 11A016 to 11AF16

	b7 b6 b5 b4 b3 b2 b1 b0	
0	□□□□□□□□	0016
1	□□□□□□■□	0416
2	□□□□□□■□	0416
3	□□□□■□■□	0A16
4	□□□□■□■□	0A16
5	□□□■□□□■	1116
6	□□□■□□□■	1116
7	□□□■□□□■	1116
8	□□■□□□□□	2016
9	□□■□□□□□	2016
A	□□■■■■■■	3F16
B	□■□□□□□□	4016
C	□■□□□□□□	4016
D	□■□□□□□□	4016
E	□□□□□□□□	0016
F	□□□□□□□□	0016

Example 19A016 to 19AF16

	b7 b6 b5 b4 b3 b2 b1 b0	
0	■■■■□□□□	F016
1	■■■■□□□□	F016
2	■■■■□□□□	F016
3	■■■■□□□□	F016
4	■■■■□□□□	F016
5	■■■■□□□□	F016
6	■■■■□□□□	F016
7	■■■■□□□□	F016
8	■■■■□□□□	F816
9	■■■■□□□□	F816
A	■■■■□□□□	F816
B	■■■□□□□□	F416
C	■■■□□□□□	F416
D	■■■□□□□□	F416
E	■■■■□□□□	F016
F	■■■■□□□□	F016

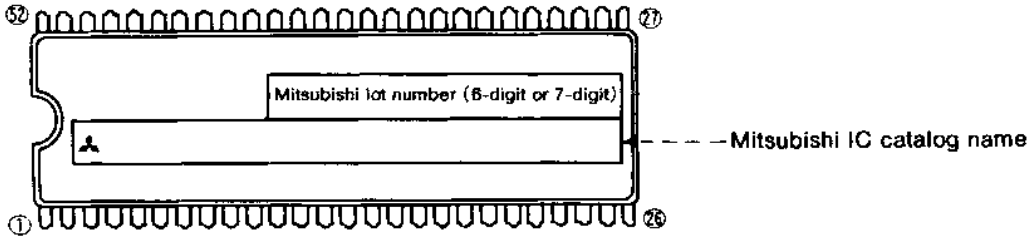
F16

52P4B (52-PIN SHRINK DIP) MARK SPECIFICATION FORM

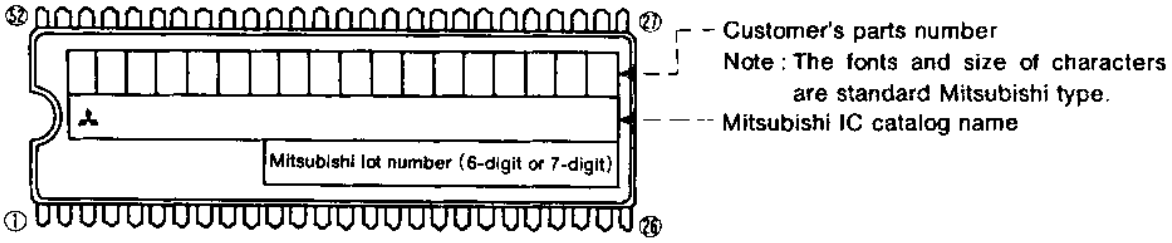
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

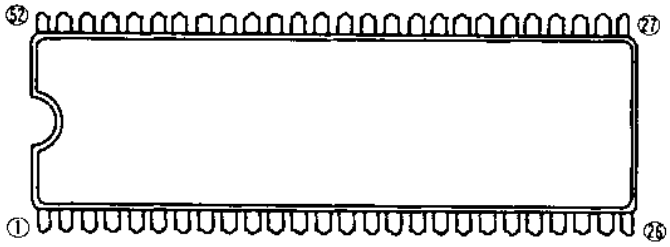


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 18 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.
4 : If the Mitsubishi logo ⅄ is not required, check the box on the right. ⅄Mitsubishi logo is not required ☐

C. Special Mark Required



Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the upper figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.
Special logo required ☐

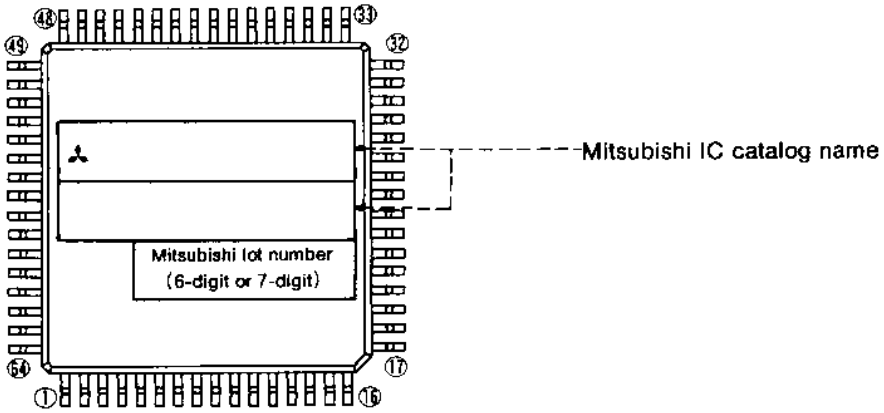
The standard Mitsubishi font is used for all characters except for a logo.

64P6N-A (64-PIN QFP) MARK SPECIFICATION FORM

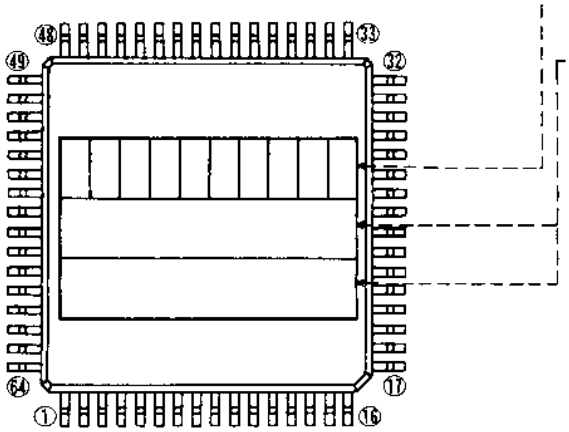
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

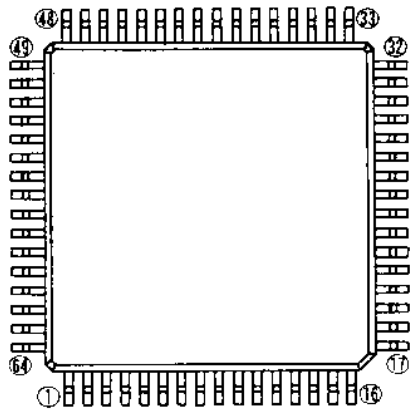


B. Customer's Parts Number + Mitsubishi Catalog Name



Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type. (The character size became smaller than A (standard Mitsubishi mark) type)

C. Special Mark Required



Note : The fonts and size of characters are standard Mitsubishi type.

Note3 : Customer's parts number can be up to 10 characters :
Only 0~9, A~Z, +, −, /, (,), &, ©, . (period), and , (comma) are usable.

4 : If the Mitsubishi logo ⅄ is not required, check the box below.

⅄ Mitsubishi logo is not required ☐

5 : Arrangement of Mitsubishi IC catalog name and Mitsubishi lot number is dependent on number of Mitsubishi IC catalog name and that Mitsubishi logo ⅄ is required or not.

Note1 : If the special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible. Mitsubishi lot number (6-digit or 7-digit) and mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the special mark, check the box below. Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special logo required ☐

The standard Mitsubishi font is used for all characters except for a logo.

MITSUBISHI DATA BOOK
SINGLE-CHIP 8-BIT MICROCOMPUTERS Vol.3

Sep. First Edition 1996 H-DF319-B

Editioned by
Committee of editing of Mitsubishi Semiconductor Data Book

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REVISION DESCRIPTION LIST	M37210M3-XXXSP/FP, M37210M4-XXXSP, M37211M2-XXXSP, M37210E4-XXXSP/FP, M37210E4SP/FP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	9708
2.0	Information about copyright note, revision number, release date added (last page).	971130