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- On-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- Versatile pin function selections allow more possibilities for using on-chip peripheral functions.

3. Applications

- Industrial control
- Medical systems
- Protocol converter
- Communications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2387FBD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash (kB)	SRAM (kB)					Ether net	USB device + 4 kB FIFO	SD/ MMC	GP DMA	Channels			Temp range
		Local bus	Ethernet buffers	GP/ USB	RTC	Total					CAN	ADC	DAC	
LPC2387FBD100	512	64	16	16	2	98	RMII	yes	yes	yes	2	6	1	–40 °C to +85 °C

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
P0[26]/AD0[3]/ AOUT/RXD3	6[3]	I/O	**P0[26] —** General purpose digital input/output pin.
		I	**AD0[3] —** A/D converter 0, input 3.
		O	**AOUT —** D/A converter output.
		I	**RXD3 —** Receiver input for UART3.
P0[27]/SDA0	25[4]	I/O	**P0[27] —** General purpose digital input/output pin.
		I/O	**SDA0 —** I^{2}C0 data input/output. Open-drain output (for I^{2}C-bus compliance).
P0[28]/SCL0	24[4]	I/O	**P0[28] —** General purpose digital input/output pin.
		I/O	**SCL0 —** I^{2}C0 clock input/output. Open-drain output (for I^{2}C-bus compliance).
P0[29]/USB_D+	29[5]	I/O	**P0[29] —** General purpose digital input/output pin.
		I/O	**USB_D+ —** USB bidirectional D+ line.
P0[30]/USB_D−	30[5]	I/O	**P0[30] —** General purpose digital input/output pin.
		I/O	**USB_D− —** USB bidirectional D− line.
P1[0] to P1[31]		I/O	**Port 1:** Port 1 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect block. Pins 2, 3, 5, 6, 7, 11, 12, and 13 of this port are not available.
P1[0]/ ENET_TXD0	95[1]	I/O	**P1[0] —** General purpose digital input/output pin.
		O	**ENET_TXD0 —** Ethernet transmit data 0.
P1[1]/ ENET_TXD1	94[1]	I/O	**P1[1] —** General purpose digital input/output pin.
		O	**ENET_TXD1 —** Ethernet transmit data 1.
P1[4]/ ENET_TX_EN	93[1]	I/O	**P1[4] —** General purpose digital input/output pin.
		O	**ENET_TX_EN —** Ethernet transmit data enable.
P1[8]/ ENET_CRS	92[1]	I/O	**P1[8] —** General purpose digital input/output pin.
		I	**ENET_CRS —** Ethernet carrier sense.
P1[9]/ ENET_RXD0	91[1]	I/O	**P1[9] —** General purpose digital input/output pin.
		I	**ENET_RXD0 —** Ethernet receive data.
P1[10]/ ENET_RXD1	90[1]	I/O	**P1[10] —** General purpose digital input/output pin.
		I	**ENET_RXD1 —** Ethernet receive data.
P1[14]/ ENET_RX_ER	89[1]	I/O	**P1[14] —** General purpose digital input/output pin.
		I	**ENET_RX_ER —** Ethernet receive error.
P1[15]/ ENET_REF_CLK	88[1]	I/O	**P1[15] —** General purpose digital input/output pin.
		I	**ENET_REF_CLK/ENET_RX_CLK —** Ethernet receiver clock.
P1[16]/ ENET_MDC	87[1]	I/O	**P1[16] —** General purpose digital input/output pin.
		O	**ENET_MDC —** Ethernet MIIM clock.
P1[17]/ ENET_MDIO	86[1]	I/O	**P1[17] —** General purpose digital input/output pin.
		I/O	**ENET_MDIO —** Ethernet MI data input and output.
P1[18]/ USB_UP_LED/ PWM1[1]/ CAP1[0]	32[1]	I/O	**P1[18] —** General purpose digital input/output pin.
		O	**USB_UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
		O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
RTCK	100[1]	I/O	**RTCK —** JTAG interface control signal. **Note:** LOW on this pin while $\overline{RESET}$ is LOW enables ETM pins (P2[9:0]) to operate as Trace port after reset.
$\overline{RSTOUT}$	14	O	**$\overline{RSTOUT}$ —** This is a 1.8 V pin. LOW on this pin indicates LPC2387 being in Reset state. **Note:** This pin is available in LPC2387FBD100 devices only (LQFP package).
$\overline{RESET}$	17[7]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	22[8]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	23[8]	O	Output from the oscillator amplifier.
RTCX1	16[8]	I	Input to the RTC oscillator circuit.
RTCX2	18[8]	O	Output from the RTC oscillator circuit.
V_{SS}	15, 31, 41, 55, 72, 97, 83[9]	I	**ground:** 0 V reference.
V_{SSA}	11[10]	I	**analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(3V3)}$	28, 54, 71, 96[11]	I	**3.3 V supply voltage:** This is the power supply voltage for the I/O ports.
$V_{DD(DCDC)(3V3)}$	13, 42, 84[12]	I	**3.3 V DC-to-DC converter supply voltage:** This is the supply voltage for the on-chip DC-to-DC converter only.
V_{DDA}	10[13]	I	**analog 3.3 V pad supply voltage:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC.
VREF	12[13]	I	**ADC reference:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC and DAC.
VBAT	19[13]	I	**RTC pin power supply:** 3.3 V on this pin supplies the power to the RTC peripheral.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis.

[2] 5 V tolerant pad providing digital I/O functions (with TTL levels and hysteresis) and analog input. When configured as a DAC input, digital section of the pad is disabled.

[3] 5 V tolerant pad providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[4] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines.

[5] Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[6] 5 V tolerant pad with 5 ns glitch filter providing digital I/O functions with TTL levels and hysteresis

[7] 5 V tolerant pad with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis

[8] Pad provides special analog functionality.

[9] Pad provides special analog functionality.

[10] Pad provides special analog functionality.

[11] Pad provides special analog functionality.

[12] Pad provides special analog functionality.

[13] Pad provides special analog functionality.

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- Single DMA and burst DMA request signals. Each peripheral connected to the GPDMA can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the GPDMA.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority. Each DMA channel has a specific hardware priority. DMA channel 0 has the highest priority and channel 1 has the lowest priority. If requests from two channels become active at the same time the channel with the highest priority is serviced first.
- AHB slave DMA programming interface. The GPDMA is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB master for transferring data. This interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data. Usually the burst size is set to half the size of the FIFO in the peripheral.
- Internal four-word FIFO per channel.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Interrupt masking. The DMA error and DMA terminal count interrupt requests can be masked.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

LPC2387 uses accelerated GPIO functions:

- GPIO registers are relocated to the ARM local bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.

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7.16 SSP serial I/O controller

The LPC2387 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.16.1 Features

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

7.17 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) allows access to external SD memory cards. The SD card interface conforms to the *SD Multimedia Card Specification Version 2.11*.

7.17.1 Features

- The MCI provides all functions specific to the SD/MMC memory card. These include the clock generation unit, power management control, and command and data transfer.
- Conforms to *Multimedia Card Specification v2.11*.
- Conforms to *Secure Digital Memory Card Physical Layer Specification, v0.96.*
- Can be used as a multimedia card bus or a secure digital memory card bus host. The SD/MMC can be connected to several multimedia cards or a single secure digital memory card.
- DMA supported through the GPDMA controller.

7.18 I^{2}C-bus serial I/O controllers

The LPC2387 contains three I^{2}C-bus controllers.

The I^{2}C-bus is bidirectional, for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^{2}C-bus implemented in LPC2387 supports bit rates up to 400 kbit/s (Fast I^{2}C-bus).

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- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the RTC clock, the Internal RC oscillator (IRC), or the APB peripheral clock. This gives a wide range of potential timing choices of Watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring, for increased reliability.

7.23 RTC and battery RAM

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in Power-down mode. On the LPC2387, the RTC can be clocked by a separate 32.768 kHz oscillator, or by a programmable prescale divider based on the APB clock. Also, the RTC is powered by its own power supply pin, VBAT, which can be connected to a battery or to the same 3.3 V supply used by the rest of the device.

The VBAT pin supplies power only to the RTC and the Battery RAM. These two functions require a minimum of power to operate, which can be supplied by an external battery.

7.23.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator or programmable prescaler from APB clock.
- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers, and selected fractional second values.
- 2 kB data SRAM powered by VBAT.
- RTC and Battery RAM power supply is isolated from the rest of the chip.

7.24 Clocking and power control

7.24.1 Crystal oscillators

The LPC2387 includes three independent oscillators. These are the Main Oscillator, the Internal RC oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Any of the three clock sources can be chosen by software to drive the PLL and ultimately the CPU.

Following reset, the LPC2387 will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

7.24.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4 MHz. The IRC is trimmed to 1 % accuracy.

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7.25.6 Memory mapping control

The memory mapping control alters the mapping of the interrupt vectors that appear at the beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the Boot ROM or the SRAM. This allows code running in different memory spaces to have control of the interrupts.

7.26 Emulation and debugging

The LPC2387 supports emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on P2[0] to P2[9]. This means that all communication, timer, and interface peripherals residing on other pins are available during the development and debugging phase as they are when the application is run in the embedded system itself.

7.26.1 EmbeddedICE

The EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. The EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM7TDMI-S core present on the target system.

The ARM core has a Debug Communication Channel (DCC) function built-in. The DCC allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The DCC is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The DCC allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The DCC data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

7.26.2 Embedded trace

Since the LPC2387 has significant amounts of on-chip memories, it is not possible to determine how the processor core is operating simply by observing the external pins. The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to a trace port. A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external Trace Port Analyzer captures the trace information under software debugger control. The trace port can broadcast the Instruction trace information. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers.

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Table 5. Static characteristics *...continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V		-	-	±10	μA
V_{BUS}	bus supply voltage			-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[11]	36	-	44.1	Ω
R_{pu}	pull-up resistance	SoftConnect = ON		1.1	-	1.9	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[3] Including voltage on outputs in 3-state mode.

[4] $V_{DD(3V3)}$ supply voltages must be present.

[5] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[6] Accounts for 100 mV voltage drop in all supply lines.

[7] Only allowed for a short time period.

[8] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[9] On pin VBAT.

[10] To V_{SS}.

[11] Includes external resistors of 18 Ω ± 1 % on D+ and D−.

Table 6. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB

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10. Dynamic characteristics

Table 7. Dynamic characteristics of USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to $V_{DD(3V3)}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 7		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 7		−2	-	+5	ns
t_{JR1}	receiver jitter to next transition			−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 7	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 7	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 8. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications; $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		1	-	24	MHz
$T_{cy(clk)}$	clock cycle time		42	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
I²C-bus pins (P0[27] and P0[28])						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns
SSP interface						
$t_{su(SPI_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 8	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2387_1.00	20071106	Product data sheet		LPC2387_0.01
	Data sheet status updated to Product data sheet.			
LPC2387_0.01	20071016	Preliminary data sheet	-	-

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