International
IOR Rectifier

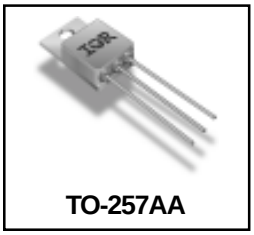
PD - 94028

HEXFET® POWER MOSFET THRU-HOLE (TO-257AA)

IRF5Y5305CM 55V, P-CHANNEL

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRF5Y5305CM	-55V	0.065Ω	-18A*



TO-257AA

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

Features:

- Low $R_{DS(on)}$
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I_D @ V_{GS} = -10V, T_C = 25°C	Continuous Drain Current	-18*	A
I_D @ V_{GS} = -10V, T_C = 100°C	Continuous Drain Current	-15	
I_{DM}	Pulsed Drain Current ①	-72	
P_D @ T_C = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	160	mJ
I_{AR}	Avalanche Current ①	-16	A
E_{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.0	V/ns
T_J	Operating Junction	-55 to 150	°C
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063in./1.6mm from case for 10sec)	
	Weight	4.3 (Typical)	g

* Current is limited by package

For footnotes refer to the last page

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-55	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.053	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.065	Ω	V_{GS} = 10V, I_D = -15A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	8.0	—	—	S (℧)	V_{DS} = -25V, I_{DS} = -16A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	µA	V_{DS} = -55V ,V_{GS}=0V
		—	—	-250		V_{DS} = -44V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	70	nC	V_{GS} =-10V, I_D = -16A
Q_{gs}	Gate-to-Source Charge	—	—	17		V_{DS} = -44V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	30		
$t_{d(on)}$	Turn-On Delay Time	—	—	26	ns	V_{DD} = -28V, I_D = -16A, R_G = 7.5Ω
t_r	Rise Time	—	—	125		
$t_{d(off)}$	Turn-Off Delay Time	—	—	56		
t_f	Fall Time	—	—	74		
$L_S + L_D$	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	1290	—	pF	V_{GS} = 0V, V_{DS} = -25V
C_{oss}	Output Capacitance	—	495	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	203	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-18*	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-72		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	T_j = 25°C, I_S = -15A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	100	ns	T_j = 25°C, I_F = -16A, di/dt ≥ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	250	nC	V_{DD} ≤ -30V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	1.67	°C/W	

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

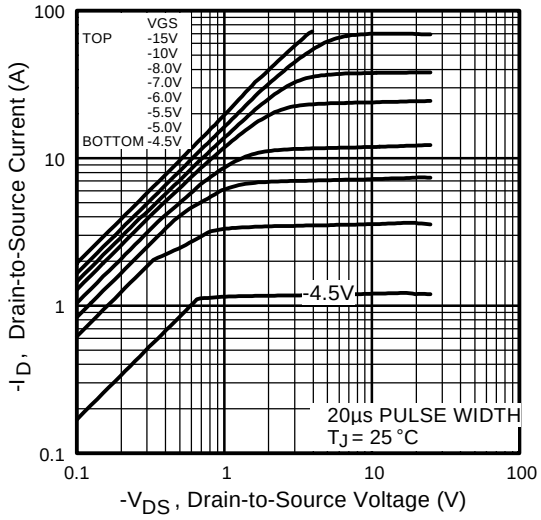


Fig 1. Typical Output Characteristics

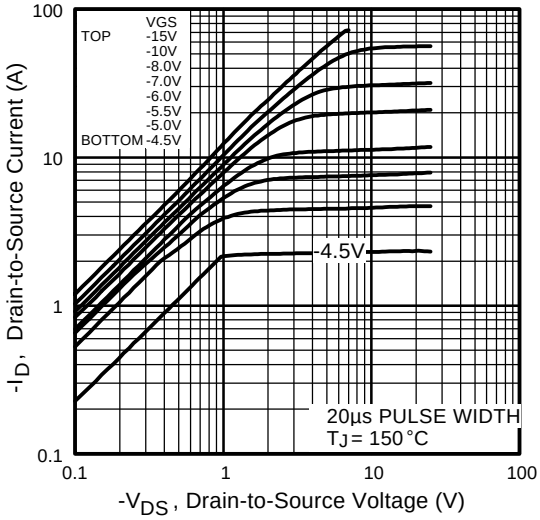


Fig 2. Typical Output Characteristics

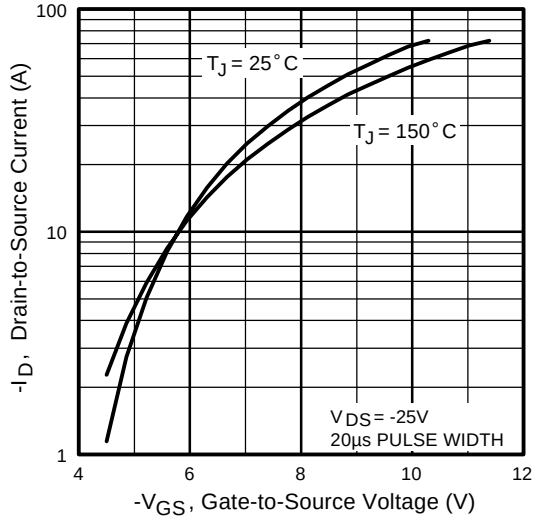


Fig 3. Typical Transfer Characteristics

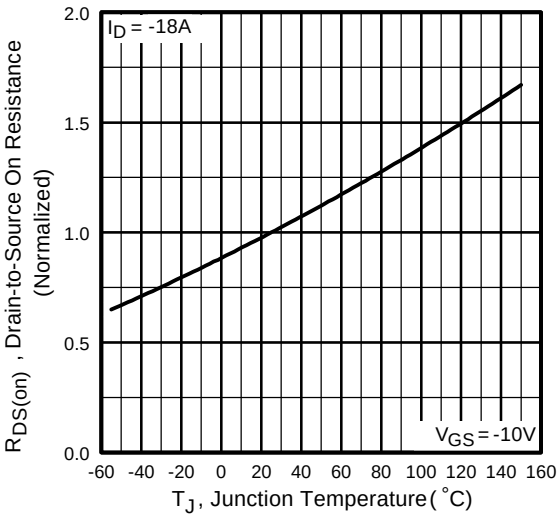


Fig 4. Normalized On-Resistance Vs. Temperature

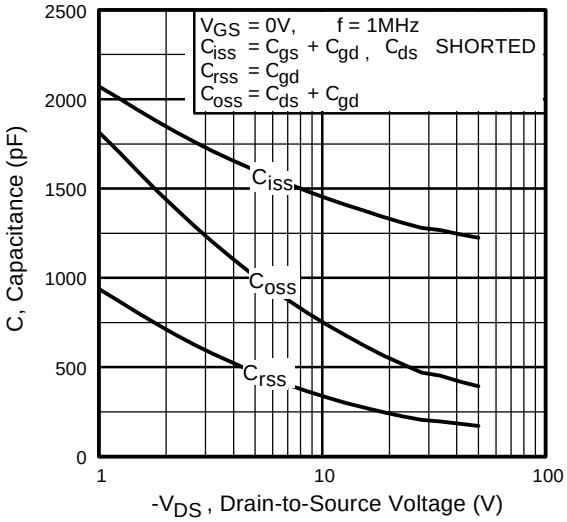


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

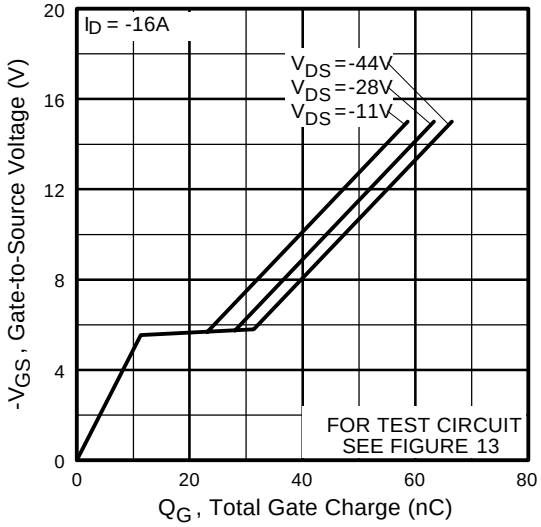


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

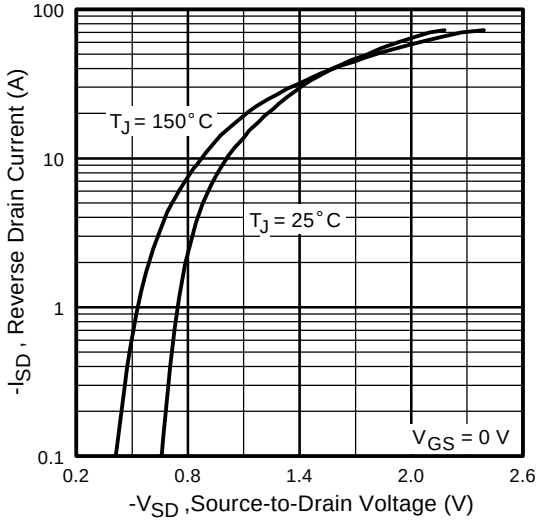


Fig 7. Typical Source-Drain Diode Forward Voltage

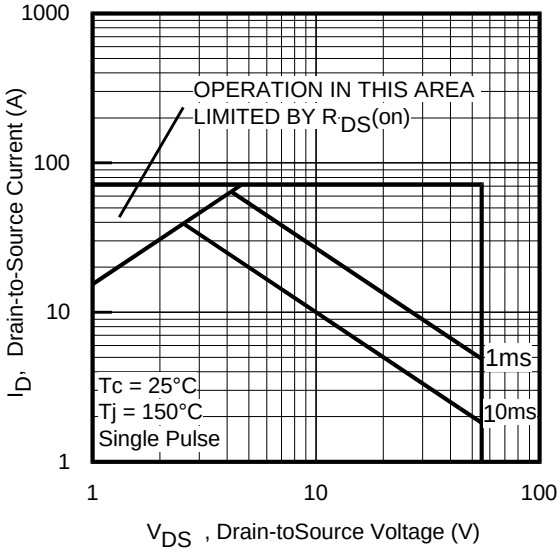


Fig 8. Maximum Safe Operating Area

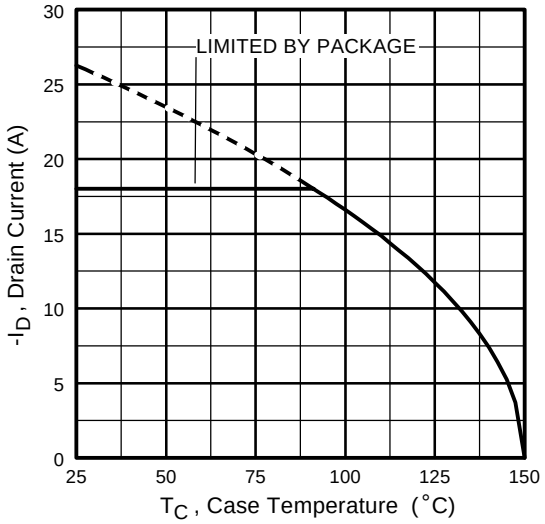


Fig 9. Maximum Drain Current Vs. Case Temperature

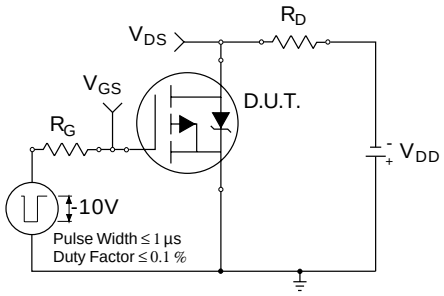


Fig 10a. Switching Time Test Circuit

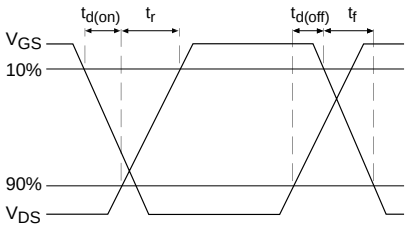


Fig 10b. Switching Time Waveforms

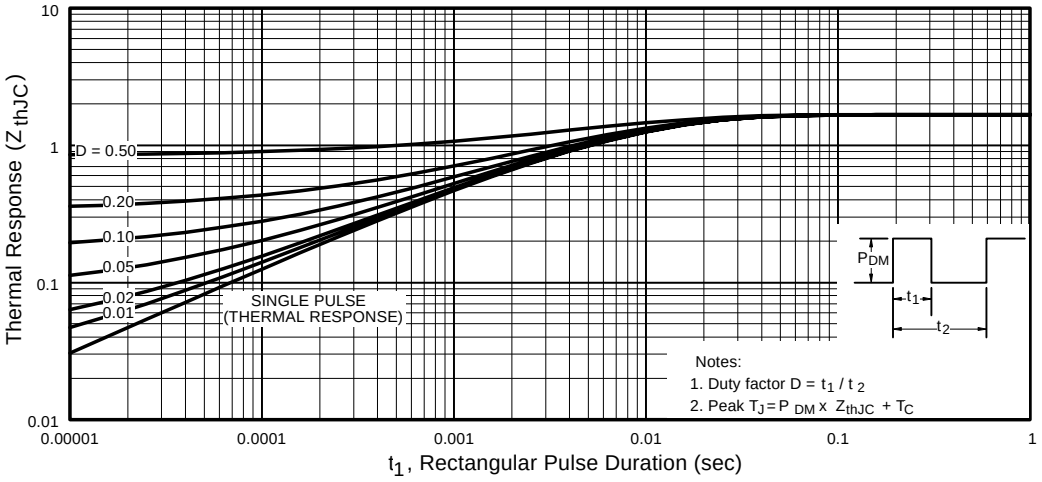


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

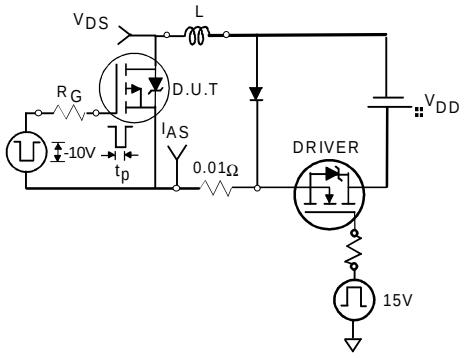


Fig 12a. Unclamped Inductive Test Circuit

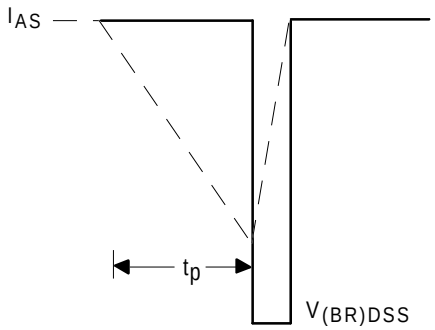


Fig 12b. Unclamped Inductive Waveforms

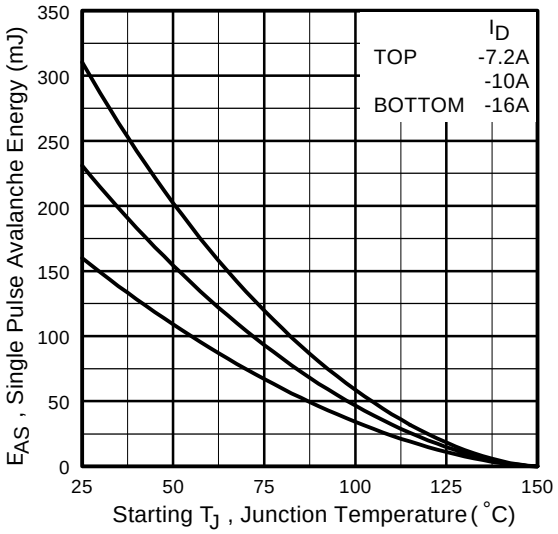


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

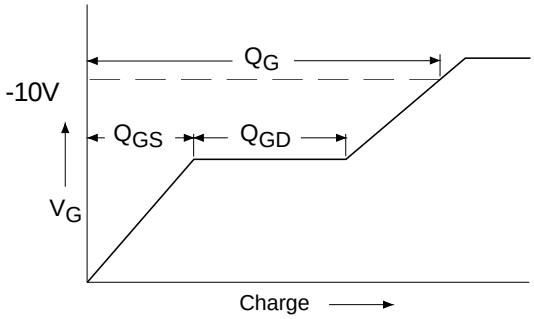


Fig 13a. Basic Gate Charge Waveform

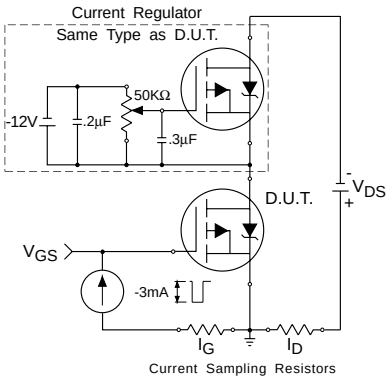
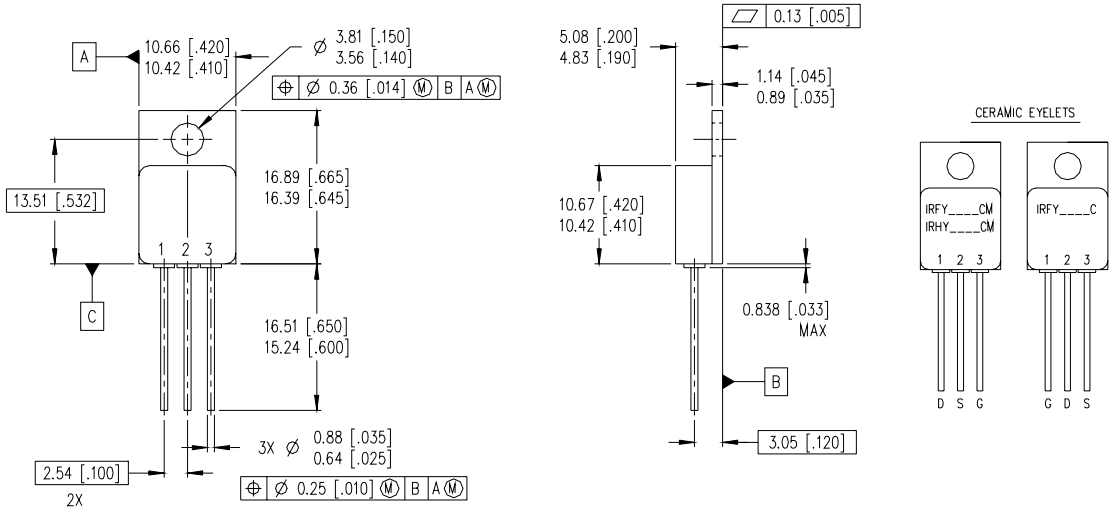


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = -25 V, Starting T_J = 25°C, L= 1.3mH Peak I_{AS} = -16A, R_G= 25Ω
③ I_{SD} ≤ -16A, di/dt ≤ -213 A/µs, V_{DD} ≤ -55V, T_J ≤ 150°C
④ Pulse width ≤ 400 µs; Duty Cycle ≤ 2%

Case Outline and Dimensions — TO-257AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

LEGEND
D – DRAIN
S – SOURCE
G – GATE

International
IOR Rectifier

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Data and specifications subject to change without notice. 11/00