Low Power EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 15dB EMI reduction
- Generates a 1x, 2x and 4x low EMI spread spectrum clock of the input frequency
  - 1x: P2811A/B
  - 2x: P2812A/B
  - 4x: P2814A/B
- Optimized for input frequency range from 10MHz to 40MHz
- Internal loop filter minimizes external components and board space
- Selectable spread options:
  - Down Spread and Center Spread
- 8 frequency deviation selections:
  - ±0.625% to -3.5%
- Low inherent Cycle-to-Cycle Jitter
- 3.3V Operating Voltage
- CMOS/TTL compatible inputs and outputs.
- Pin-out compatible with Cypress CY25811, CY25812 and CY25814
- Available in 8-pin SOIC Package

Product Description

The P28XX devices are versatile spread spectrum frequency modulators designed specifically for a wide range of input clock frequencies from 10MHz to 40MHz. Refer to *Input/output Frequency Range Selection* Table. The P28XX can generate an EMI reduced clock from crystal, ceramic resonator, or system clock. The P28XX-A and the P28XX-B offer various combinations of spread options and percentage deviations. Refer to *Frequency Deviation and Spread Selection* Table. These combinations include Down and Center Spread, and percentage deviation range from ±0.625% to -3.5%.

The P28XX reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of downstream clock and data dependent signals. The P28XX allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The P28XX modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

The P28XX uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

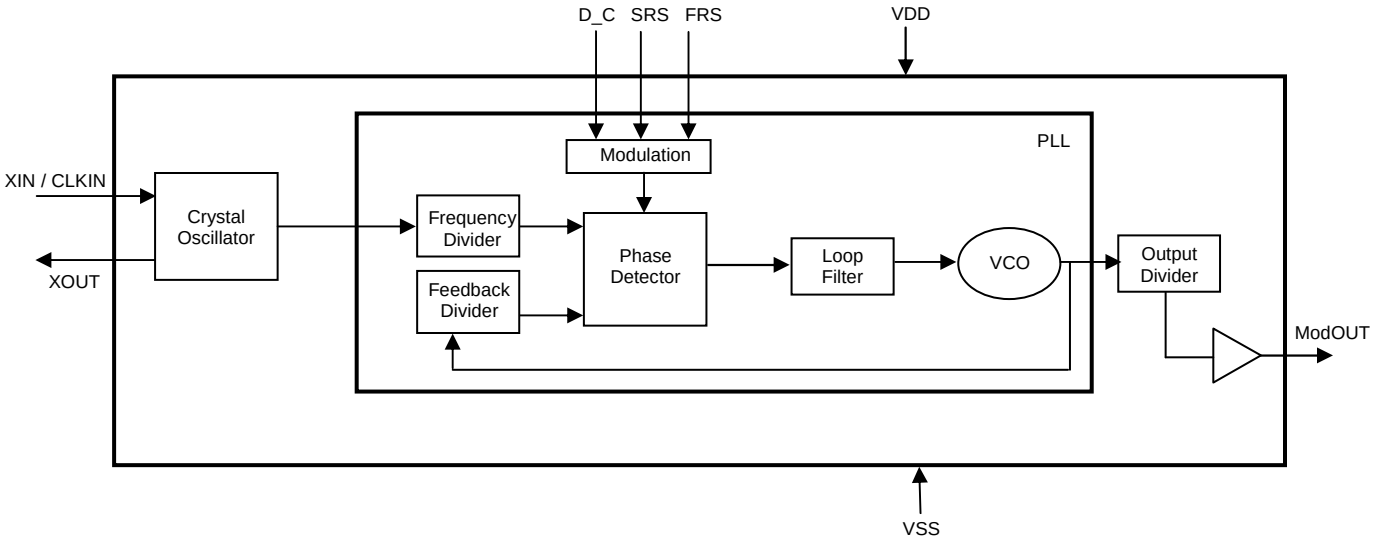
Applications

The P28XX is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high-speed digital applications such as PC peripheral devices, consumer electronics, and embedded controller systems.

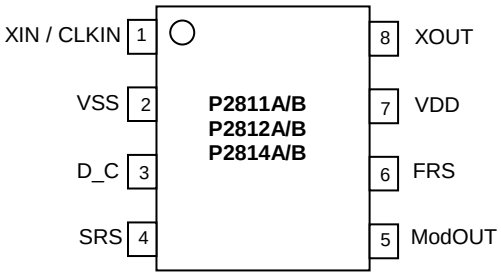
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Publication Order Number:
P2811/D

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN / CLKIN	I	Crystal connection or external Clock input.
2	VSS	P	Ground to entire chip.
3	D_C	I	Digital logic input used to select Down (LOW) or Center (HIGH) spread options. (Refer to *Frequency Deviation and Spread Selection* Table*).* This pin has an internal pull-up resistor.
4	SRS	I	Spread range select. Digital logic input used to select frequency deviation (Refer to *Frequency Deviation and Spread Selection* Table*).* This pin has an internal pull-up resistor.
5	ModOUT	O	Spread spectrum clock output.
6	FRS	I	Frequency range select. Digital logic input used to select Input frequency range (Refer to *Input/Output Frequency Range Selection* Table). This pin has an internal pull-up resistor.
7	VDD	P	Power supply for the entire chip.
8	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.

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Input/Output Frequency Range Selection Table

FRS (pin 6)	Part Number						Modulation Rate
	P2811 (1x)		P2812 (2x)		P2814 (4x)		
	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	Input (MHz)	Output (MHz)	
0	10-20	10-20	10-20	20-40	10-20	40-80	Input Frequency / 448
1	20-40	20-40	20-40	40-80	20-40	80-160	Input Frequency / 896

Output Frequency Deviation and Spread Selection Table

Part Number	D_C (pin 3)	SRS (pin 4)	Frequency Deviation[1] (%)			
			FS=0		FS=1	
			10/20/40 (MHz)	20/40/80 (MHz)	20/40/80 (MHz)	40/80/160 (MHz)
P28XXA	0	0	-3	-2.5	-2.7	-2.6
	0	1	-3.7	-3.4	-3.8	-3.6
	1	0	±1.5	±1.2	±1.5	±1.3
	1	1	±1.8	±1.6	±1.9	±1.8
P28XXB	0	0	-1.7	-1.0	-1.5	-1.4
	0	1	-2.0	-1.5	-2.0	-1.9
	1	0	±0.75	±0.6	±0.8	±0.7
	1	1	±1.0	±0.75	±1.0	±0.9

Note: 1. Frequency Deviation given in the table is for the Output Frequency Range covering P2811x / 12x / 14x.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage(As per JEDEC STD 22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Symbol	Parameter	Min	Max	Unit
VDD	Supply Voltage	3.0	3.6	V
T_A	Operating temperature	-40	+85	℃
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	VSS – 0.3		0.8	V
V_{IH}	Input high voltage	2		V_{DD} + 0.3	V
I_{IL}	Input low current (Inputs D_C, SRS and FRS are pulled high internally)			-50	µA
I_{IH}	Input high current			50	µA
I_{XOL}	XOUT Output low current (V_{XOL}@ 0.4V, V_{DD} = 3.3V)			3	mA
I_{XOH}	XOUT Output high current (V_{XOH}@ 2.5V, V_{DD} = 3.3V)			3	mA
V_{OL}	Output low voltage (V_{DD} = 3.3V, I_{OL} = 15mA)			0.4	V
V_{OH}	Output high voltage (V_{DD} = 3.3V, I_{OH} = -15mA)	2.5			V
I_{CC}	Dynamic supply current (Unloaded Output)	8		24	mA
I_{DD}	Static supply current , Standby mode (CLKIN pulled to GND)			4.5	mA
VDD	Operating voltage	3.0	3.3	3.6	V
t_{ON}	Power up time (first locked clock cycle after power up)			500	µS
Z_{OUT}	Clock out impedance		26		Ω

AC Electrical Characteristics

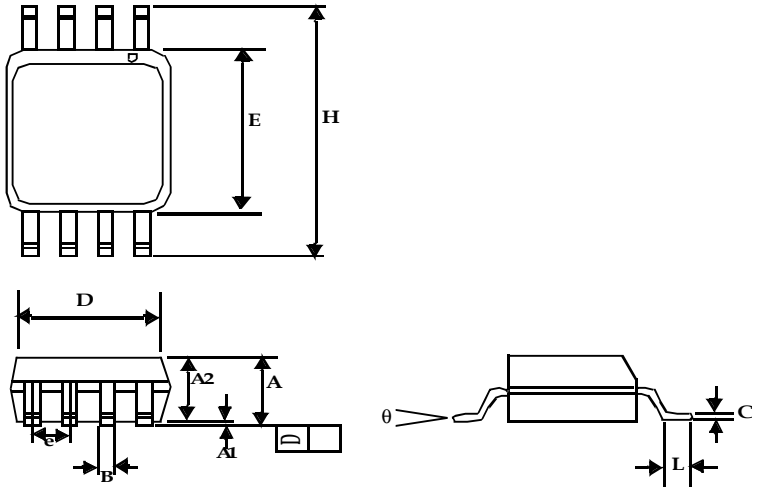
Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency for P2811/12/13/14 A/B	10		40	MHz
f_{OUT}	Output frequency for P2811A/B	10		40	MHz
	Output frequency for P2812A/B	20		80	MHz
	Output frequency for P2814A/B	40		160	MHz
t_{LH}[1]	Output rise time (measured at 0.8V to 2.0V)	0.4	0.5	0.7	nS
t_{HL}[1]	Output fall time (measured at 2.0V to 0.8V)	0.5	0.6	0.8	nS
t_{JC}	Cycle-to-Cycle Jitter (Unloaded Output)		±250		pS
t_D	Output duty cycle	45	50	55	%

Note: 1. t_{LH} and t_{HL} are measured into a capacitive load of 15pF

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Package Information

8-Pin SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Note: Controlling dimensions are millimeters.
SOIC: 0.074 grams unit weight.

Ordering Code

Part Number	Marking	Package Type	Temperature
P2811BF-08SR	ABU	8-Pin SOIC, Tape & Reel, Pb free	0℃ to +70℃
I2811BF-08SR	ABV	8-Pin SOIC, Tape & Reel, Pb free	-40℃ to +85℃
P2814BG-08SR	ACD	8-Pin SOIC, Tape & Reel, Pb free	0℃ to +70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

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